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OPTIMIZED TEST PCBS FOR SAW / FBAR RF FILTERS

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Abstract — **The characterization of the precise performance of packaged SAW RF filters is an extremely difficult task, due to their high complexity and high performance. If printed circuit boards (PCBs) for testing the filters are not carefully designed, they presumably show parasitic effects influencing the measurement results of the overall system consisting of PCB and filter. Actually, commonly used application environments exhibit different electromagnetic properties, and so the characterization may not be valid.**

This paper presents a new approach to design physically different PCBs in such a way that SAW RF components exhibit identical performance. The new approach is based on the concept of using optimized test environments, i.e., test environments with minimal reflections, minimal cross-talk, and minimal losses, in order to obtain the pure filter characteristics. The applicability and advantages of the new approach are exemplified.

I. INTRODUCTION

In the last decade surface acoustic wave (SAW) and film bulk acoustic resonator (FBAR) radio frequency (RF) filters have proven to be key components in the RF sections of mobile communication equipment. Keeping up with the miniaturization of mobile devices, the size of the packages has decreased from a typical form factor of 5.0 mm x 5.0 mm to 1.4 mm x 2.0 mm. Furthermore, center frequencies have shifted from 1 GHz to above 2 GHz due to additional frequency bands. At the same time further functionality has been added to the pure filtering function, e. g., impedance transformation or balun functionality to handle balanced signals. Besides, the permanent pressure for quality enhancements in the field of wireless communication has driven manifold improvements of the filter performance regarding matching, close-in, and far-off selectivity, and pass band attenuation [1, 2].

Due to these requirements, the accurate determination of the electrical characteristics of SAW RF filters is becoming a critical prerequisite for their efficient design. It is well known that the measurement environment can significantly influence the measured electrical characteristics. This paper will focus in particular on the PCB on which the component is soldered for operation. The decreased package size and enlarged complexity do not only provide new challenges for the package design, they also effect the test PCB design, as the distance between signal pads decreases, and additional shielding measures have to be taken.

In this contribution, new approaches for test PCBs will be proposed. These designs have been optimized towards minimal reflections, minimal feed-through or cross-talk, as well as minimal losses. This is a prerequisite for test PCBs, which are used to check the agreement of the performance of a SAW RF filter with its specifications.

In most application environments the electrical properties of the filter in the application deviate at least slightly from the measured characteristics on the test PCB, as the PCB layout differs considerably from the test PCB.

Furthermore, the paper will give a new design proposal for the landing area on the application PCB, offering the same optimized electrical properties as the landing area on the previously described test PCB in spite of the different layer stacks.

Sec. II starts with an example comprising a couple of SAW filter setups pointing out the potential impact of PCBs on the electrical filter characteristics. Sec. III shows measures to avoid these effects leading to new designs for parts of test PCBs and for a new landing area for the PCB in the application environment. Sec. IV summarizes the results and Sec. V concludes the paper.

II. CHARACTERIZATION OF RELEVANT EFFECTS BY MEASUREMENT AND SIMULATION

In order to examine the measurement setup and to discover parasitic effects, a reliable and accurate simulation technique had to be established. A combination of commercial field simulators for PCB and package simulation and proprietary tools for SAW chip simulation has proven best for this purpose [3-5]. Fig. 1 shows the simulation results achieved using such a simulation method in comparison to measurement data of a SAW RF filter mounted on different setups. The agreement can be stated as excellent. Therefore, it can be concluded that all electrical properties of the simulated component have been taken into account sufficiently. Consequently, in Secs. III and IV this procedure will be used to proof the performance of our designs for parts of test PCBs.

The typical measurement setup, shown in Fig. 2, is composed of the following parts. At the connection interface for the measurement equipment, the test setups consist of the connectors and the transition to the microstrip line (MSL). For the PCB, a multilayer FR4 material is used. The landing area comprises the metal structure onto which the filter is soldered.

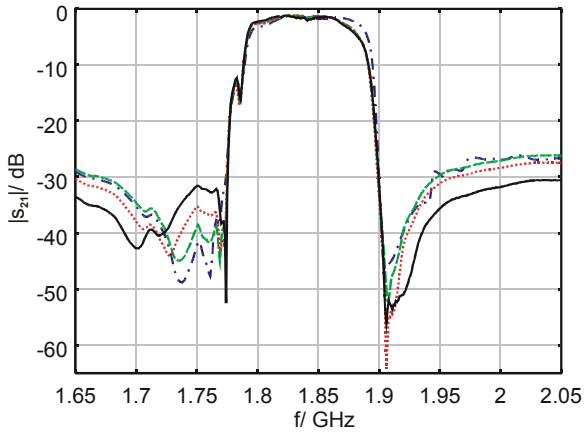

Fig. 1: Measured scattering parameters of identical filters on three different PCBs ((1) green-dashed, (2) red-dotted, (3) black-solid) and simulated values (blue-dash-dotted) of the same filter on the PCB used for measurement (1).

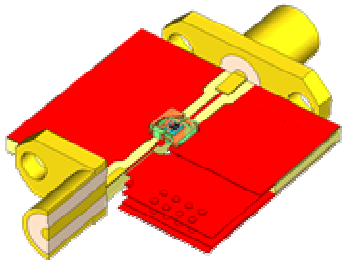

Fig. 2: Typical measurement setup with mounted SAW RF filter.

Parasitic effects inside the dielectric layers and in the signal and ground paths of the PCB depend on the different PCB designs. The different effects influence the measurement result for the SAW RF filter in the test setups, as shown in Fig. 1. For example, the close-in and far-off selectivity levels change significantly, and also the matching characteristics alter.

III. Design of an Optimized Quasi-Application PCB

A. Requirements for Neutral Environment

For a convincing filter test, a PCB design is needed that gives results independent of the test or application environment. To this end, a number of measures are taken.

Firstly, the measurement system impedance is well matched at the external ports of the test setup. Moreover, reflections along the complete signal path as well as parasitic feed-through or cross-talk between the ports are minimized. Thus, the filter performance should be accessible as original as possible.

B. PCB Substrate Material and Layer Stack

The substrate material used is FR4 and was chosen to conform with the mobile phone PCB. It is a cheap material in comparison to RF materials, but it is also known to have pretty poor RF properties and to considerably suffer from large fabrication spreads.

The basic material parameters of FR4 are its permittivity, $\varepsilon_r = 4.5 \pm 0.3$ and its dielectric loss, $\tan\delta \approx 0.02$.

Tolerances in PCB circuits of ±5% and more have been reported in all dimensions, e.g., line width, slot width, substrate thickness, and metalization thickness, as well as material parameters, e.g., the substrate permittivity. Also the alignment of layers, and the positioning of vias are influenced by these tolerances.

Our original test PCBs consist of three dielectric layers allowing four metalized layers, as shown in Fig. 3. The thicknesses of the outer dielectric layers are given in Table I. The center layer serves as carrier. Its thickness is not critical. In the following, the four metalized layers are referred to as top side, upper ground, lower ground, and bottom side metal layer.

Table I
Dimensions and properties of 50 Ω microstrip line used for the test PCB (a) and the quasi-application PCB (b).

PCB design	(a)	(b)	unit
Substrate height h_1 of outer layer	200	60	µm
Substrate height h_2 of center layer	-	135	µm
line width w	340	100	µm
metal thickness t	35	17	µm
height of solder resist s	0	0	µm
relative permittivity ε_r	4.5	4.5	
Line impedance Z	50	50	Ω

C. Proposal for a Neutral Test PCB

During a project we precisely investigated the effects of the transitions from SMA connectors to MSLs, and the landing areas for the devices under test (DUTs).

The dimensions of the structures of the test PCB are summarized in column (a) of Table I. Although the dimensions have been carefully designed to meet the required line impedance of 50 Ω, fabrication tolerances result in large spreads of the line impedance and the need for prior verification.

A first step in our optimization procedure was aiming at keeping the tolerances in layer thickness of the outer dielectric layers low in order to have characteristic impedance of the MSL as close to 50 Ω as possible. This led to a change in the fabrication technology of the PCB. In contrast to the old PCB, the new design exhibits 5 dielectric layers and 4 metal layers. The center dielectric layer consists of two layers of soft resin filled fiberglas material (prepreg) and one of prehardened material (core), according to Fig. 3.

For the outer dielectric layers copperplated cores are used. During the lamination process, the height of the outer layers remains constant, and tolerances only occur in the center layer.

Next, the transition from the SMA connector to the MSL has been optimized for minimal reflections. A SMA connector with a thin center connector is used, which allows direct soldering to the MSL without contact pad. Careful positioning of vias led to a shortened and optimized ground path in the

transition. Regarding Fig. 4, an improvement of around 20 dB compared to earlier designs has been obtained in the relevant frequency range from 1 to 2 GHz. In the inset of Fig. 4 the layout of the transition is shown. Note that the inner ground layers are continuous, i.e., not partially removed in the area of the solder pads of the connector.

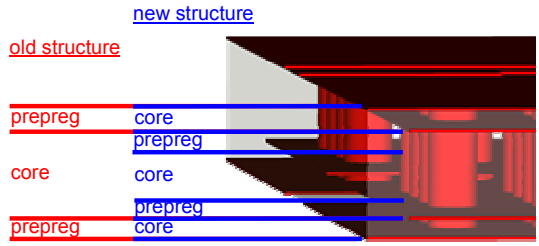

Fig. 3: Old and new layer stack of test PCBs.

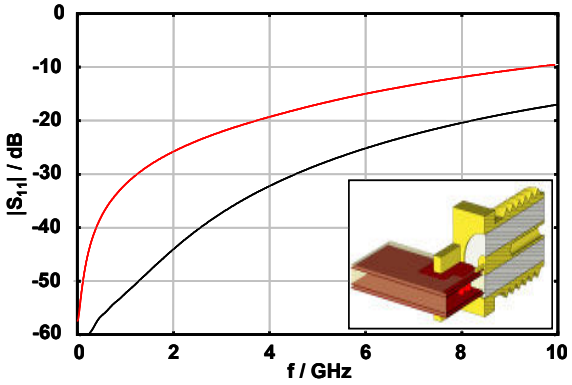

Fig. 4: Simulation results for old (red) and new (black) transitions from SMA connector to MSL; perspective drawing of the transition.

As the landing areas have to be laid out according to the required footprints of the packages and to the modes of operation of the SAW components, a variety of different landing areas has to be handled. In general, good connection for ground pads on the PCB surface to the inner ground layer and good shielding of signal pads implies the use of many vias between the top and the inner ground metalizations, as shown in Fig. 5. Again, the inner ground metalization is continuous in order to avoid field coupling into the other dielectric layers.

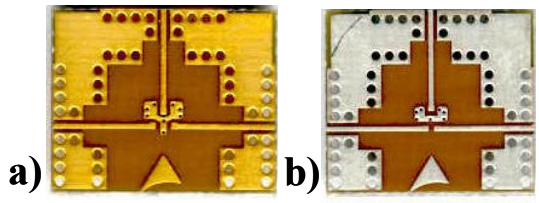

Fig. 5: Top view of test PCBs providing a neutral environment to SAW filters with unbalanced input and balanced output, (a) in 1.6 mm x 2.0 mm 6-pin, and (b) in 1.4 mm x 2.0 mm 5-pin packages.

Another important point in test PCBs is the suppression of unsymmetric parasitic crosstalk in PCBs for 3-port filters, with e.g. unbalanced input and balanced output. Therefore the routing of the lines and the positioning of the transitions should lead to a symmetric design. Parallel arrangement of MSLs should be also avoided. Then, crosstalk from the unsymmetric port does only influence the common mode and does not modify the differential mode of the symmetric port and vice versa. The described properties are realized in the new PCB designs, shown in Fig. 5.

The next development step was to transfer the obtained electrical properties of the test PCB to a quasi-application PCB. Due to the modified layer stack in the application, the landing area had to be redesigned as described below. The specifications of the layer stacks of a quasi-application PCB are listed in column (b) of Table I. It should be noted that the height of the top dielectric layer of 60 µm is similar to that of the phone PCBs and, thus, the application environment.

The reduction of the layer height requires several changes in the layout of the landing area. Firstly, in order to achieve a characteristic impedance of the MSLs of 50 Ω, the line width has to be reduced from 340 µm to 100 µm.

Secondly, a strong field discontinuity in the signal path is generated by the step discontinuity from the microstrip line to the soldering pad. As a size reduction of the soldering pad is not possible due to the predetermined solder pad size of the SAW component and the placing tolerances, an attempt has been made to reduce the effect of the discontinuity at the soldering pads by cutting out the areas in the upper inner ground layer below the soldering pads. Thus, the second inner metal layer is used as the actual ground plane below the soldering pad.

The designs of the landing areas for an optimized quasi-application PCB is given in Fig. 6. As an example, a well-known ceramic 3 mm x 3 mm package has been chosen.

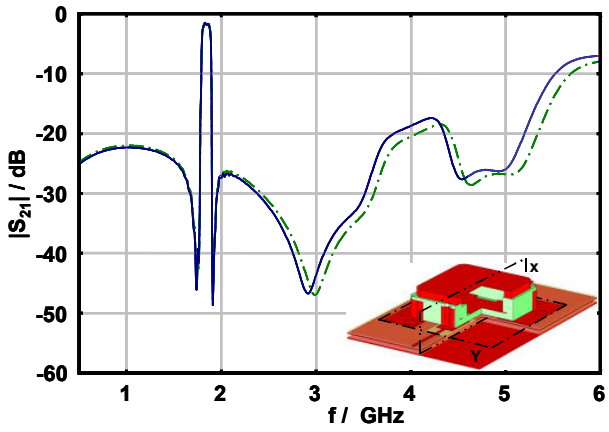

Fig. 6: Comparison of simulated scattering parameters of identical filters on optimized test PCB (green, dash-dotted) and new quasi-application PCB (blue, solid).

In order to avoid field fringing and to guarantee optimal properties of the PCB, both size and position of the cut-out area have to be chosen carefully as indicated below.

The size of the cut-out area has to be realized in a way ensuring that the main part of the electromagnetic field below the soldering pad goes to the second ground layer, field components towards the edges of the cut-out in the upper ground layer have to be avoided [6]. An undersized cut-out area will lead to almost unchanged field fringing as without cut-out.

Special focus has to be put on the front edge of the cut-out towards the microstrip line. Its position must be chosen close to the soldering pad. Otherwise, an additional MSL with high characteristic impedance will be unintentionally created by cutting away the original ground plane of the microstrip line, altering the properties of the SAW component.

Another important point during optimization is the provision for an undisturbed current path. Hereto, a sufficient number of vias has to be positioned in the ground structures on top of the PCB in the vicinity of the MSLs.

It should be noted that during the layout process, general design guidelines, as given in [7], have to be taken into account. To avoid field propagation by parallel plate modes between the inner ground layers of the PCB, a sufficient number of ground vias is necessary. A technique using vias for this purpose is given in [8]. Under certain circumstances, this effect can lead to parasitic coupling, PCB resonances, or radiation on the outside of the PCB.

IV. Results

For validation purposes, the same filter as already used in Sec. II, has been simulated on the neutral test and on the quasi-application PCB structure using techniques explained in [3-5]. In Fig. 6 simulation results of this filter on the previous test PCB and on the new quasi-application PCB are given. The plotted curves indicate a good agreement of electrical characteristics with respect to close-in and far-off selectivity. Differences resulting from parasitic effects in the PCBs, as explained in Sec. II (Fig. 1), do not occur in Fig. 6. Thus, the concept of a landing area design for application PCBs, having the same optimized electrical characteristics as on an optimized test PCB, has been proven.

V. Conclusion

The paper shows that optimized test PCBs for testing SAW RF components and optimized application PCBs for operating SAW RF components allow to yield the same performance of the components. It has been shown that this is possible despite the considerable physical differences regarding the layer stacks of the two PCBs, for instance. In order to prove the concept, a quasi-application PCB representing the final phone PCB has been designed and evaluated. This work should encourage the designers of mobile equipment to implement this technique in their application PCBs. Thus, the specified filter characteristics are guaranteed in the application. A proposal for an efficient landing area design for the application PCB and, thus, for a phone PCB has been given and discussed in detail.

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