A Novel Frequency Divider Configuration for Micro- and Millimeter-Wave Signals

P. Nüchter and W. Menzel

Abstract—**A novel frequency divider configuration is presented that is based on the well-known regenerative frequency divider. In addition to a multiplier in the feedback loop—as originally suggested—an auxiliary frequency divider is included in the loop. The maximum operating frequency of the novel configuration can be close to twice the maximum input frequency of the auxiliary divider.**

I. Introduction

FREQUENCY dividers are useful devices for frequency synthesis and measurement, e.g., phase-locked loops (PLL's) and frequency counters or digitizing oscilloscopes.

While many different principles of frequency division are known, integrated prescalers are commercially available mostly as "digital" dividers. The maximum operating frequency of these digital dividers is continuously approaching the mm-wave frequency range [1], [2].

In this work analog divider principles and digital components are combined to form a novel frequency divider configuration.

II. Novel Frequency Divider Configuration

Fig. 1 shows the novel configuration of the frequency divider. The input and a feedback signal are mixed and the resulting IF signal is used as input for an auxiliary frequency divider. The output signal of this auxiliary divider, which is also the resulting output signal, is multiplied and used as feedback signal. Due to the mixing process, the operating range of this configuration is above the maximum frequency of the auxiliary divider.

This structure is similar to the MILLER-divider [3], but here a frequency divider is included in the loop.

Many integrated dividers[1] use regenerative circuits [3], [4] or dynamic flip-flops [2], [5] as a first stage, followed by static divide by two stages. Due to the high internal gain and limiting behavior of the input stages, they often exhibit a self-oscillating behavior in the absence of an input signal.

Such a behavior is important for this configuration, because in order to ensure proper startup conditions, a persistent feedback signal is mandatory.[2]

Since the input signal must synchronize the system, the name "Self-Synchronized Frequency Divider" is proposed.

Manuscript received February 13, 1996.

The authors are with the University of Ulm, Microwave Techniques, D-89069 Ulm, Germany.

Publisher Item Identifier S 1051-8207(96)05321-4.

[1] Temic U6028BS-FP or NEC UPG506, for example.

[2] A multiplying phase-locked loop could be used as well.

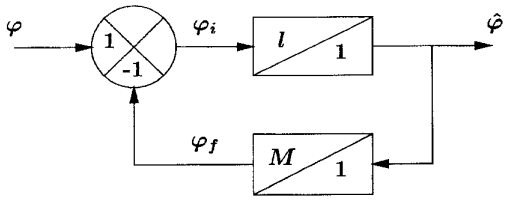

Fig. 1. Novel configuration.

III. Theory

A. Pull-In Process

In the absence of an input signal, there will be no IF signal and the self oscillating divider will output a signal at its free-running frequency $\hat{f} = \hat{f}_f$. With an input signal of adequate power, the auxiliary divider will lock onto the IF signal $f_i = f - M \cdot \hat{f}_f$ and produce the output frequency $\hat{f} = f/l - M/l \cdot \hat{f}_f$. Iterating infinitely yields the output frequency

$$\hat{f} = \frac{f}{l+M}; \quad \frac{M}{l} < 1. \tag{1}$$

Therefore, successful pull-in requires $M/l < 1$.

B. Stability Conditions

Under proper operating conditions,[3] the input and output signal of a divider $s(t) \sim \cos[\omega t + \varphi(t)]$ and $\hat{s}(t) \sim \cos[(\omega/n)t + \hat{\varphi}(t)]$ are related according to

$$\hat{\varphi}(t) \approx \frac{\varphi(t-\tau)}{n} + \vartheta + \Delta\vartheta(t) \tag{2}$$

where τ and ϑ model the phase delay and phase shift of the divider and passive filter networks [6] and $\Delta\vartheta(t)$ represents the residual phase noise [7].

In order to describe the behavior of the configuration of Fig. 1, the input power is assumed to be sufficient to generate an IF signal in the operating range of the auxiliary divider. Since frequency dividers are essentially limiting devices, amplitudes are not considered.

The auxiliary divider and the multiplier of Fig. 1 can be described according to (2), e.g.,

$$\varphi_f(t) = M \cdot \hat{\varphi}(t - \tau_M) + \vartheta_M + \Delta\vartheta_M(t). \tag{3}$$

[3] For example, the input signal is in the operating window of the divider.

The resulting phase-transfer-characteristic in the Laplace domain is

$$\hat{\varphi}(s) = H(s) \cdot \varphi(s) + \frac{\vartheta}{s} + \Delta\vartheta(s) \tag{4}$$

with

$$H(s) = \frac{e^{-\tau_l s}}{l + Me^{-(\tau_l+\tau_M)s}} \approx \frac{e^{-\tau s}}{l+M}; \quad \tau = \frac{l\tau_l - M\tau_M}{l+M} \tag{5}$$

$$\vartheta = (l\vartheta_l - \vartheta_M + l \cdot k2\pi) \cdot H(0) \tag{6}$$

$$\Delta\vartheta(s) = [l\Delta\vartheta_l(s) \cdot e^{\tau_l s} - \Delta\vartheta_M] \cdot H(s). \tag{7}$$

In the time domain, the result is

$$\hat{\varphi}(t) \approx \frac{\varphi(t-\tau)}{l+M} + \vartheta + \Delta\vartheta(t). \tag{8}$$

A straightforward stability analysis [6] shows that the steady state is stable for $M/l \leq 1$.

C. Bandwidth

If the operating window of the auxiliary divider is limited by the range $f_{i_{\min}} \leq f \leq f_{i_{\max}}$ and an ideal multiplier with pure sinusoidal output is used, the new configuration has the bandwidth

$$\left(1 + \frac{M}{l}\right) f_{i_{\min}} \leq f \leq \left(1 + \frac{M}{l}\right) f_{i_{\max}} < 2f_{i_{\max}}. \tag{9}$$

A real multiplier usually produces not only the desired harmonic $M\hat{f}$, but also some sub- and superharmonics $M^-\hat{f}$ and $M^+\hat{f}$ with $M^- < M < M^+$. The auxiliary divider fails to operate if more than one signal with similar power is applied. Therefore the limits of (9) may be narrowed by

$$f > \frac{M+l}{M - M^- + l} f_{i_{\max}} \tag{10}$$

$$f < \frac{M+l}{l - (M^+ - M)} f_{i_{\min}} \tag{11}$$

respectively, whichever is more restrictive. These additional constraints are less severe, if the division ratio l is chosen as small as possible.

D. Remarks

- The special case $l = 1$ corresponds to the MILLER-divider with multiplier [3]. Albeit, this circuit not only has startup-problems, but appears to be unstable for $M > 1$.
- If a self-oscillating divider is utilized, the multiplier can be replaced by a filter,[4] which selects the desired harmonic of the "digital" output signal of the divider. In such a case the useful range of M is limited to about three.

[4] As will be shown in the example, the operating window of the auxiliary divider acts like a filter.

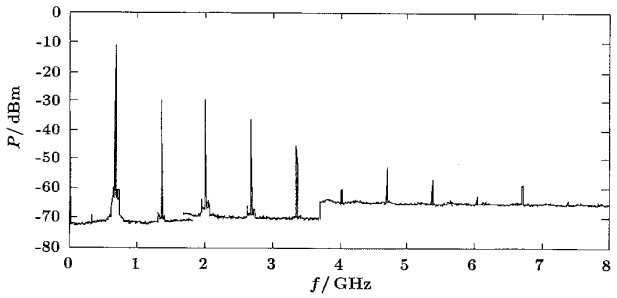

Fig. 2. Self-oscillating output spectrum.

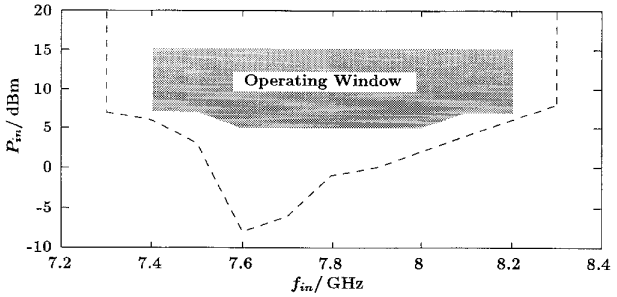

Fig. 3. Input sensitivity of experimental novel divider.

- If the multiplier is realized as phase-locked loop, some modifications of the theory must be taken into account, i.e., the phase-transfer-function of the PLL must be used, the resulting phase-transfer-characteristic will differ from (5), and the stability condition is no longer valid. In fact, the configuration will be stable in a much wider range because of the integrating properties of a PLL.[5]

IV. Example

A first test was made with readily available components.[6] The experimental setup consisted of a self-oscillating dynamic frequency divider with $l = 8$ and an operating window of 3–6 GHz, a standard mixer, and a simple 20-dB gain-block in the feedback path. All components were housed separately and connected with coaxial cables.

Fig. 2 shows the output spectrum of the setup without input signal. Instead of an extra multiplier, the third harmonic of the auxiliary dividers output signal is chosen as feedback,[7] such that the overall division ratio is $M + l = 3 + 8 = 11$. Since the second harmonic is in the same order of magnitude, (10) applies with $M = 3$ and $M^- = 2$ and the lower frequency limits is 7.3 GHz.

The divider works as expected, and the measured input sensitivity is shown in Fig. 3.

As a dynamic test, a FM-modulated carrier at 7.7 GHz with modulation index $\eta = 2.405$ was used as input signal. Fig. 4 shows the corresponding output spectrum. The output

[5] If a first-order PLL with negligible delay is used, the configuration is stable for arbitrary M/l.

[6] Temic U6028BS-FP, Miteq TBR 0226LW2, HP MGA-86 576.

[7] The fourth harmonic is too weak to be significant.

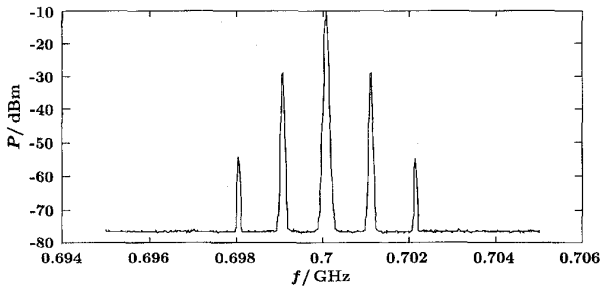

Fig. 4. Output spectrum of divided FM signal.

modulation index is $\hat{\eta} = 2.405/11 = 0.219$, and the sidebands appear at -19 and -45 dBc, as expected.

V. Outlook

In the above example, the relative gain in maximum operating frequency was only 3/8.

A more impressive increase in maximum operating frequency could be obtained with a divide-by-four circuit and the third harmonic as feedback signal. With this, the operating window of the commercially available NEC UPG503 could be translated from 3.5–9 GHz to 12.6–15.7 GHz, for example.

With ongoing progress in GaAs technology, integrated dividers for the 60 GHz-band are conceivable—an ultra-high-speed divider for 36–48 GHz [2] and the output signal directly as feedback should yield an operating range of 54–72 GHz!

VI. Conclusion

A novel frequency divider configuration is presented that makes use of an auxiliary divider. It is shown that the maximum operating frequency of the new configuration can be nearly twice the maximum frequency of the auxiliary divider. The conditions for successful pull-in and stability are derived. An example with off-the-shelf components is presented.

Since "digital" dividers are approaching 50 GHz, this configuration provides the possibility to build integrated mm-wave frequency dividers.

References

[1] A. Felder, R. Stengl, J. Hauenschild *et al.*, "Static frequency dividers for high operating speed (25 GHz, 170 mW) and low power consumption (16 GHz, 8 mW) in selective epitaxial Si bipolar technology," *Electron. Lett.*, vol. 29, no. 12, pp. 1072–1074, 1993.

[2] M. Tokumitsu, M. Hirano, K. Murata *et al.*, "A 0.1 μm GaAs MESFET technology for ultra-high-speed digital and analog IC's," in *IEEE Int. Microwave Symp. Dig.*, 1994, pp. 1629–1632.

[3] R. L. Miller, "Fractional-frequency generators utilizing regenerative modulation," *Proc. IRE,* pp. 446–457, July 1939.

[4] R. H. Derksen and H.-M. Rein, "7.3-GHz dynamic frequency dividers monolithically integrated in a standard bipolar technology," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 537–541, Mar. 1988.

[5] K. Fujita, H. Itoh, and R. Yamamoto, "A 15.6 GHz commercially based 1/8 GaAs dynamic prescaler," in *IEEE GaAs Symp.*, 1989, pp. 113–116.

[6] G. Immovilli and G. Mantovani, "Analysis of the miller frequency divider by two in view of applications to wideband FM signals," *Alta Frequenza,* vol. XLII, no. 11, pp. 583–593, Nov. 1973.

[7] V. F. Kroupa, "Noise properties of PLL systems," *IEEE Trans. Commun.*, vol. COM-30, no. 10, pp. 2244–2252, Oct. 1982.