Pulse Modulation Techniques for Switched-Mode Transmitter

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Abstract

Nowadays more and more communication devices incorporate multiple transceivers operating in different frequency bands. To reduce form factor and power consumption of such devices, a fully digital, multi-standard, multiband transmitter is highly demanded. In modern communication systems, the peak-to-average ratio of the transmitted signals is often more than 10 dB. This means that the power amplifier has to operate in significant back-off from its compression point, where the classical amplifier architectures suffer from very low efficiency. The class-S power amplifier may provide a potential solution to such a transmitter because it incorporates an amplifier which is operating in the switch mode where 100% efficiency can be theoretically approached. A nonlinear switch mode power amplifier can be linearized if driven by a pulse encoder and followed by a bandpass filter. The efficiency and available power of a class-S power amplifier are highly dependent on the employed pulse encoding technique.

Within the framework of this thesis, the main characteristics of pulse modulators and their limitations while driving different classes of switch-mode power amplifiers are discussed. The definitions of the pulse encoder parameters are given and the performance of several pulse encoder architectures was compared for the case when they are driven by a real communication signal.

For class-S power amplifier demonstrators, at three different operating frequencies (450 MHz, 900 MHz and 2.1-2.2 GHz), the corresponding bandpass delta-sigma modulators (DSMs) have been developed. For the latter two cases, the switching speed of power transistors was not high enough and common DSM architectures were not applicable. For example, for the 2.1-2.2 GHz class-S demonstrator the maximum required sampling frequency of the DSM was limited to 5 GHz. Thus, a design procedure for a 5 GS/s 2.1-2.2 GHz center frequency DSM has been established. The developed bandpass DSM enabled the implementation of the complete class-S power amplifier at 2.1-2.2 GHz carrier frequencies.

In the successive steps of the study, a new fully digital pulse encoder architecture has been developed. The results of comparison of this pulse encoding technique with the state-of-the-art have been presented. Finally, the performance of the proposed digital polar modulator was demonstrated by driving a real class-F power amplifier at 2.1 GHz.
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<tr>
<td>ACLR</td>
<td>Adjacent Channel Leakage Ratio</td>
</tr>
<tr>
<td>ADPLL</td>
<td>All-Digital Phase-Locked Loop</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
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<tr>
<td>BP</td>
<td>bandpass</td>
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<tr>
<td>BPG</td>
<td>Bit-Pattern Generator</td>
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<tr>
<td>BW</td>
<td>Bandwidth</td>
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<tr>
<td>CCDF</td>
<td>Complementary Cumulative Distribution Function</td>
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<tr>
<td>CDMA</td>
<td>Code Division Multiple Access</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
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<td>CORDIC</td>
<td>COordinate Rotation Digital Computer</td>
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<tr>
<td>CSCD</td>
<td>Current-Switched Class-D</td>
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<td>CT</td>
<td>Continuous Time</td>
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<td>CW</td>
<td>Continuous Wave</td>
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<td>DAC</td>
<td>Digital-to-Analog Converter</td>
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<td>DPM</td>
<td>Digital Polar Modulation</td>
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<td>DSM</td>
<td>Delta-Sigma Modulation</td>
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<td>EER</td>
<td>Envelope Elimination and Restoration</td>
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<td>ENOB</td>
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<td>FET</td>
<td>Field Effect Transistor</td>
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<td>FFT</td>
<td>Fast Fourier Transform</td>
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<td>FoM</td>
<td>Figure of Merit</td>
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<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<td>GMSK</td>
<td>Gaussian Minimum Shift Keying</td>
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<td>GPRS</td>
<td>General Packet Radio Service</td>
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<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>HRZ</td>
<td>Half-delayed return-to-zero</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Laterally Diffused Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>LP DSM</td>
<td>Lowpass DSM</td>
</tr>
<tr>
<td>MPG</td>
<td>Multi-phase generator</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-return-to-zero</td>
</tr>
<tr>
<td>NTF</td>
<td>Noise Transfer Function</td>
</tr>
<tr>
<td>OFDM</td>
<td>Orthogonal Frequency-Division Multiplexing</td>
</tr>
<tr>
<td>OSR</td>
<td>Oversampling Ratio</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power-added efficiency</td>
</tr>
<tr>
<td>PAPR</td>
<td>Peak-to-Average Power Ratio</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PDF</td>
<td>Probability Density Function</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Modulation</td>
</tr>
<tr>
<td>PPM</td>
<td>Pulse-Position Modulation</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RFPA</td>
<td>Radio Frequency Power Amplifier</td>
</tr>
<tr>
<td>RZ</td>
<td>Return-to-zero</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious Free Dynamic Range</td>
</tr>
<tr>
<td>SMA</td>
<td>Surface-Mount Assembly</td>
</tr>
<tr>
<td>SMPA</td>
<td>Switch-Mode PA</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-Noise and Distortion Ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>STF</td>
<td>Signal Transfer Function</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal Mobile Telecommunications System</td>
</tr>
<tr>
<td>VSA</td>
<td>Vector Signal Analyzer</td>
</tr>
<tr>
<td>VSCD</td>
<td>Voltage-Switched Class-D</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband CDMA</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
</tr>
</tbody>
</table>
1.1 Motivation

In modern wireless communication systems, the power consumption of a power amplifier (PA) dominates the power budget of a radio transceiver. Improving PA efficiency will result in extending battery life in handheld devices. On the other hand, in the base station equipment, a decrease in the power consumption reduces the energy costs and CO$_2$ emission. Therefore, an improvement in the PA efficiency is very important from the economic and environment points of view.

One of the main goals in the development of wireless communication systems is increasing of the data transmission rate. This can be achieved by using higher channel bandwidth and/or by improving a spectral efficiency of a signal by means of modulation. A PA architecture, its available power and efficiency are dependent on how the input signal is modulated. This determines back-off conditions of PA operation or, in other words, how far the PA has to operate from its compression point.

To see how the PA requirements have been changing, we consider the evolution of the available throughput defined in cellular phone standards. In 2$^{nd}$ generation mobile communication systems, such as GSM, a constant envelope signal modulated using Gaussian minimum shift keying (GMSK) has to be transmitted. To gain more throughput, the GSM standard has been extended by general packet radio service (GPRS) which initially used GMSK modulation as well. In this case, a PA operates in the non-linear mode, where it achieves maximum efficiency. GPRS allows a maximum transmission data rate of 70.4 kbit/s occupying a 200 kHz bandwidth. To improve data transmission rates within the GSM standard, enhanced GPRS (EGPRS or EDGE) has been implemented. By using the 8 phase-shift keying modulation (8PSK) the number of bits transmitted per one symbol increased three times compared to GPRS. The maximum data rate achieved by using EDGE is 247.4 kbit/s for 200 kHz channel. In this case, the envelope of a transmitted signal is not constant anymore. Signals with non-constant envelope require a linear PA operating in
back-off. Quantitatively, an operation in back-off can be estimated by the peak-to-average power ratio (PAPR) of a signal. The PAPR for the EDGE signal is 3.6 dB. Targeting for higher data rates resulted in development of the 3rd generation (3G) mobile communication system that introduces data rates up to tens of Mbit/s for downlink. In 3G systems, the WCDMA access technique, including QPSK, 4QAM, 16QAM for data modulation, has been introduced to increase the data rate that can be transmitted over a given bandwidth. The development of the LTE standard, which represents the 4th generation (4G) communication system, resulted in further increase in the data rate up to 100 Mbit/s. The user data are modulated with conventional modulation schemes (QPSK, 16QAM, 64QAM). Then, by means of highly spectral efficient orthogonal frequency-division multiplexing (OFDM), data symbols are mapped onto a set of sub-carriers. The PAPR of the resulting signal increases as the number of sub-carriers increases [1]. Thus, one of the drawbacks of an OFDM signal is that it has a high PAPR. This aspect means that a linear PA has to operate with significant back-off from the compression point to prevent the signal peaks from experiencing distortion due to the PA non-linearity. Fig. 1.1 shows the complementary cumulative distribution function (CCDF) for different modulated signals. The CCDF curve shows the percentage of time when the signal is above some value in dB from the average signal power. The maximum value above the average signal power represents the corresponding PAPR value for a given signal. As can be seen from Table 1-1, along with increasing of the throughput, the PAPR of the transmitted signals is also increasing and shows values of higher than 10 dB.

![Fig. 1.1. CCDF for signals defined by different communication standards.](image-url)
Table 1-1. Comparison of the signals [2-4]

<table>
<thead>
<tr>
<th>Standard</th>
<th>PAPR</th>
<th>Modulation</th>
<th>BW</th>
<th>Max. Data rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPRS</td>
<td>0 dB</td>
<td>GMSK</td>
<td>200 kHz</td>
<td>70.4 kbit/s</td>
</tr>
<tr>
<td>EDGE</td>
<td>3.6 dB</td>
<td>8PSK</td>
<td>200 kHz</td>
<td>247.4 kbit/s</td>
</tr>
<tr>
<td>WCDMA</td>
<td>10.5 dB</td>
<td>16QAM</td>
<td>5 MHz</td>
<td>14.4 Mbit/s</td>
</tr>
<tr>
<td>LTE</td>
<td>12.5 dB</td>
<td>64QAM</td>
<td>20 MHz</td>
<td>108 Mbit/s</td>
</tr>
</tbody>
</table>

Transmitted signals in 3G and 4G systems have high PAPR values which makes conventional linear PAs operating in deep back-off to amplify signals without distortion. Class-A and class-AB PAs, operating in deep back-off from their compression point, suffer from a significant efficiency drop. Fig. 1.2 shows the simulated output power and power-added efficiency (PAE) curves for a class-AB PA based on LDMOS transistors. It can be seen that in saturation, the PA achieves a maximum PAE of 70%. However, looking at 6 dB back-off, the efficiency is 13%, whereas at 10 dB back-off it is 5.3% only.

On the other hand, switch mode power amplifiers (SMPA) are very attractive because of their theoretically high efficiency of 100%. An ideal switch doesn’t dissipate any power because either current or voltage across it is zero. There are some realizations of SMPA at GHz frequencies achieving reasonable power levels with excellent efficiency values [5-7]. Unfortunately, highly efficient SMPAs cannot directly process modern communication.
signals because the latter requires a linear amplification. However, an SMPA driven by a pulse encoded signal and followed by a bandpass filter can act as a linear amplifier [8]. Such a system is called class-S amplifier and is widely used in audio applications. Because of demonstrated linear operation and high efficiency, a class-S PA gradually replaced bulky class-A or class-AB linear audio amplifiers. This PA concept is very attractive to be implemented at GHz carrier frequencies where many communication standards are defined. However, pulse encoded signals may contain very short pulses that cannot fully switch the available power transistors because of their low transit frequency $f_T$. In other words, the power transistor’s bandwidth sets the limitation of the minimum pulse width of the encoder. Thus, the class-S PA can be a candidate to fulfill the requirement of simultaneous efficiency and linearity at high frequencies in case an appropriate pulse modulation technique can be used with relaxed switching requirements to the PA.

Usually, a class-S amplifier is referred to a class-D SMPA driven by a pulse-width modulated signal. Because of the invention of different pulse modulation techniques, which enable the linearization of any SMPA class, the definition of a class-S PA can be correspondingly extended.

A class-S PA (Fig. 1.3) is a linear PA system based on an SMPA, driven by a pulse encoder (pulse modulator) and followed by an output filter network. The pulse encoder converts an input signal (RF or baseband) into a pulse train which is suitable to drive the input of an SMPA. The output filter network reconstructs the amplified original narrow-band input RF signal and delivers it to the antenna.

![Fig. 1.3. Class-S PA system.](image)

The choice of the SMPA architecture in a class-S system and the requirements to the reconstruction filter are determined by the pulse modulation technique. Depending on the pulse encoder architecture, the class-S PA can be used either as replacement of an existing PA in the analog front-end [9] or as a complete transmitter [10]. In the former case, the pulse
encoder is supposed to be a direct conversion one having the input at the carrier frequency (Fig. 1.4); in the latter case the pulse encoder has to perform the frequency upconversion from the baseband to a pulse modulated signal at the carrier frequency (Fig. 1.5).

![Fig. 1.4. Analog transmitter incorporating a class-S PA based on the direct conversion pulse encoder.](image1)

![Fig. 1.5. Class-S transmitter based on the frequency upconverting pulse encoder.](image2)

The Class-S PA concept can be a potential approach to fully digital multistandard multiband transmitters. Such kind of devices became recently highly demanded since more and more devices incorporate several transceivers for different frequency bands to operate at different communication standards (e.g. Bluetooth, LTE, WLAN). All of these transceivers consume power and occupy area. Substituting all transmitters by a single efficient one would extend operation time of the handheld device and reduce its cost. The same is valid for the base station equipment, where the radio part consumes more than 80% of the energy [11].

### 1.2 History and state-of-the-art

The very first idea to use an SMPA for the linear amplification belongs to B. Bedford [12] and dates to 1931. He proposed to encode the input signal by means of pulse-width modulation (PWM). The pulse modulated signal drives an electrical valve, which has been
used as a switch. Then the output filter recovers the original input signal. Because of many components needed for implementation of PWM, at that time, this approach has been rarely used. In 1966 H. R. Camenzind [13] recovered the attention to the class-S PA by proposing an integrated realization of the amplifier. He also proposed several methods how to generate the PWM sequence. The application of the method was found in audio and servo amplifiers. However, the PWM approach wasn’t suitable for RF power amplifiers because of the very narrow pulses which cannot switch a transistor completely into ON- or OFF-state. In 1968, P. Besslich proposed the so-called RF-PWM which relaxed switching conditions on SMPA [14]. The SMPA implementation driven by RF-PWM was successfully demonstrated by Raab in 1973 [15]. With increasing speed in integrated circuits, only in the 1990-s engineers came back to this approach; thus, highly efficient class-S amplifiers have been gradually replacing bulky audio class-A and class-AB amplifiers. Also in context of audio amplifier, in 1997, A. Tripathi proposed to use a bandpass DSM [16] instead of PWM for the signal encoding. PA efficiency values up to 80% for audio signals with a PAPR of more than 10 dB encouraged scientists to explore the class-S amplifier at RF frequencies as well. The first trial at 800 MHz carrier frequency belongs to Jayaraman [9], which presented simulation results of the GaAs SMPA driven by a bandpass DSM pulse train.

In 2002, S. Stapleton presented an idea how to linearize the class-S PA [17] by generation of a correction signal from the PA output and feeding it back to the pulse encoder input. This enables sufficient linearity improvement in order to satisfy requirements of existing telecommunication standards. Later on, this idea transformed into the so-called class-M PA which was produced by a company PWRF [18]. In 2008 this scheme was improved by using a pulse-position modulation (PPM) based on a noise shaping [19]. In case of PPM, the output pulse train contains only pulses with a pulse width of $T_c/2$ which allows using an SMPA of either class-E or class-F configuration. Also, the PPM encoder demonstrated better coding efficiency in comparison to the bandpass DSM. The PPM encoder is based on the noise shaping scheme and a pulse generator, which produce the pulses of $T_c/2$ width. The realization of the complete amplifier driven by the PPM encoder has been presented in [20].

There are also approaches that not only substitute the transmitter output stage by the class-S PA but a complete transmitter, generating the SMPA driving signal from the baseband signals either from amplitude and phase or from in-phase (I) and quadrature (Q) signals. In this thesis, such kind of circuits are referred to frequency upconverting pulse encoders.
In 2003, Y. Wang proposed several improvements [21] to the envelope elimination and restoration (EER) transmitter architecture [22]. Firstly, by using a bandpass DSM instead of a PWM for encoding of the envelope signal used for the dynamic supply of the radio frequency power amplifier (RFPA) (Fig. 1.6). Secondly, by generating a digitally modulated RF carrier from amplitude and phase to drive an SMPA (Fig. 1.7), which significantly reduces AM-PM distortion compared to the architecture using an envelope modulation of the PA power supply. Another improvement was proposed in [23], where a class-E configuration has been used as an SMPA. This architecture has been investigated, modified and improved in various designs of pulse encoders [24-29] in order to generate the modulated RF carrier in the digital domain.

![Fig. 1.6. Improved Kahn transmitter architecture [21].](image1)

A fully digital transmitter architecture based on the separate processing of I and Q signals was proposed in [10]. The IQ signals are encoded by means of PWM and then upconverted by two multiplexers as shown in Fig. 1.8. A similar concept has been used in [30]. But, instead of PWM, lowpass DSMs encode I and Q signals.

![Fig. 1.7. Polar transmitter architecture with a constant supply in SMPA [21].](image2)
In the last decade, many activities in the area of class-S PA have been seen at radio frequencies. and summarize class-S PA realizations based on III-V and CMOS power devices, respectively. There are implementations that are based on PWM, RF-PWM, bandpass DSM, and on relatively new concepts as well. Many different realizations of a class-S PA can be explained by looking for an optimal encoder, since the operation at RF frequencies presents more stringent requirements to a pulse encoder from the SMPA side. First of all, the switching losses rise with frequency. To keep the switching losses low, the pulse train generated by a pulse encoder must contain as few as possible switching events. On the other hand, in case of lossless signal encoding, the power at the carrier in the pulse train is lower compared to the input signal. The “quality” of pulse encoding is characterized by coding efficiency and will be reviewed in Chapter 2. This parameter is one of the main parameters which is used for comparison of the different pulse encoding schemes. The pulse width statistic has to be analyzed as well, because very short pulses cannot completely switch the transistor ON and OFF which leads to additional power losses. All of these aspects will be discussed in detail in the next chapters.
<table>
<thead>
<tr>
<th>Encoder</th>
<th>Encoder realization</th>
<th>SMPA class</th>
<th>SMPA Tech.</th>
<th>Filter</th>
<th>$f_C$/ GHz</th>
<th>Test signal</th>
<th>Continuous wave</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BW/MHz</td>
<td>PAPR / dB</td>
<td>Pch/ dBm</td>
</tr>
<tr>
<td>Noise shaped PPM</td>
<td>IC</td>
<td>E</td>
<td>GaN</td>
<td>yes</td>
<td>0.9</td>
<td>1.23</td>
<td>-</td>
<td>43.1</td>
</tr>
<tr>
<td>*BP DSM</td>
<td>IC</td>
<td>D^1</td>
<td>GaN</td>
<td>yes</td>
<td>0.9</td>
<td>3.84</td>
<td>10.3</td>
<td>26</td>
</tr>
<tr>
<td>PWM</td>
<td>IC</td>
<td>D^1</td>
<td>GaN</td>
<td>yes</td>
<td>0.9</td>
<td>3.84</td>
<td>5.4</td>
<td>17</td>
</tr>
<tr>
<td>Dig. IQ (BP DSM)</td>
<td>FPGA</td>
<td>E</td>
<td>GaN</td>
<td>no</td>
<td>1</td>
<td>1.23</td>
<td>-</td>
<td>29.1</td>
</tr>
<tr>
<td>*Dig. Polar (EDSM)</td>
<td>BPG</td>
<td>F^1</td>
<td>GaN</td>
<td>no</td>
<td>2.14</td>
<td>3.84</td>
<td>9.5</td>
<td>30.2</td>
</tr>
<tr>
<td>Dig. IQ (BP DSM)</td>
<td>FPGA</td>
<td>F^1</td>
<td>GaN</td>
<td>no</td>
<td>2.45</td>
<td>1.23</td>
<td>-</td>
<td>29.3</td>
</tr>
<tr>
<td>Polar (EDSM)</td>
<td>BPG</td>
<td>E</td>
<td>GaAs</td>
<td>yes</td>
<td>2.47</td>
<td>3-tone</td>
<td>4.7</td>
<td>-</td>
</tr>
<tr>
<td>Dig. Polar</td>
<td>IC</td>
<td>H</td>
<td>GaN</td>
<td>yes</td>
<td>0.4</td>
<td>3.84</td>
<td>7.5</td>
<td>28.4</td>
</tr>
</tbody>
</table>

*contributions of this work
Table 1-3. State-of-the-art of CMOS based Class-S PAs at RF carrier frequency $f_C$.

<table>
<thead>
<tr>
<th>Encoder</th>
<th>Encoder realization</th>
<th>SMPA class</th>
<th>SMPA Tech.</th>
<th>Filter</th>
<th>$f_C$ / GHz</th>
<th>Test signal</th>
<th>Continuous wave</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dig. IQ (PWM)</td>
<td>BPG</td>
<td>D</td>
<td>0.18 um CMOS</td>
<td>no</td>
<td>0.65</td>
<td>-</td>
<td>-</td>
<td>19.4</td>
</tr>
<tr>
<td>Dig. BP DSM</td>
<td>IC</td>
<td>D</td>
<td>0.18 um CMOS</td>
<td>yes</td>
<td>0.8</td>
<td>1.23</td>
<td>5.5</td>
<td>15</td>
</tr>
<tr>
<td>Dig. BP DSM</td>
<td>BPG</td>
<td>D</td>
<td>0.13 um CMOS</td>
<td>yes</td>
<td>0.8</td>
<td>1.25</td>
<td>5.5</td>
<td>-</td>
</tr>
<tr>
<td>Polar (EDSM)</td>
<td>BPG</td>
<td>D</td>
<td>0.13 um CMOS</td>
<td>yes</td>
<td>0.8</td>
<td>0.27</td>
<td>3.5</td>
<td>-</td>
</tr>
<tr>
<td>Dig. Polar (ADPLL)</td>
<td>FPGA/IC</td>
<td>D</td>
<td>90 nm CMOS</td>
<td>yes</td>
<td>1.7</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>RF-PWM</td>
<td>IC</td>
<td>E</td>
<td>65 nm CMOS</td>
<td>yes</td>
<td>2.2</td>
<td>0.19</td>
<td>4</td>
<td>26.7</td>
</tr>
<tr>
<td>Polar (EDSM)</td>
<td>BPG/IC</td>
<td>D</td>
<td>90 nm CMOS</td>
<td>yes</td>
<td>2.4</td>
<td>1</td>
<td>3</td>
<td>14</td>
</tr>
</tbody>
</table>

*PAE
1.3 Research contribution

The work described in this thesis was partially done within a large research project [41] dedicated to the investigation of the class-S power amplifiers at 450MHz [42], 900MHz [32] and 2.1-2.2 GHz carrier frequencies. The delta-sigma modulation was chosen as a pulse encoder in the class-S architecture; therefore, bandpass DSM at the corresponding carrier frequencies were developed [43-46].

At the beginning of the project, available power transistors could efficiently process digital signals up to 2.2 GS/s. Therefore, the first bandpass DSM design at 450 MHz [46] was straightforward and was based on the well described architecture with sampling frequency of 4 times higher than the input frequency (so called $f_s/4$-architecture). Thus, the bandpass DSM sampling frequency can be chosen between 1.8 and 2.2 GS/s. More attention was paid to the interface between the bandpass DSM and the GaN-based PA, because GaN transistors require an input signal with a swing of more than 4.5 V single-ended in order to switch completely into ON/OFF states. Since an SMPA employs a class-D architecture, which requires two transistors operating in push-pull configuration, the needed differential swing at the input has to be more than 9 V. For this purpose a SiGe driver with 10 Vpp output swing at 2 GS/s has been designed [47].

At the second step, a bandpass DSM for the 900 MHz carrier frequency had to be implemented. In case of a $f_s/4$-architecture, the bandpass DSM sampling frequency of 3.6 GS/s would be in contradiction with the maximum data rate of 2.2 GS/s of the power transistor. In this case, the maximum data rate of the transistor sets the upper limit for the bandpass DSM sampling frequency. A 2.2 GS/s 900 MHz bandpass DSM [43] was developed and used in a class-S demonstrator [32].

The realization of a class-S PA module at $f_c = 2.1-2.2$ GHz with the available GaN transistor posed a big challenge. An exploration of the bandpass DSM performance at 2.1-2.2 GHz center frequencies resulted in a bandpass DSM implementation based on the $f_s/4$-architecture with a sampling frequency of 9 GS/s [44]. Another investigated approach was to use the output of the 900 MHz bandpass DSM at the first image frequency. By setting the sampling frequency of this bandpass DSM at 3.1 GHz, one can obtain the mirrored modulated
signal centered at the 2.2 GHz carrier frequency [48]. This, of course, essentially reduces the output data rate of the bandpass DSM but it still did not allow using the available GaN transistors. Another drawback of this approach is that the output power of a class-S PA is significantly reduced because of low coding efficiency.

Finally, the solution for the 2.1-2.2 GHz class-S demonstrator resulted from synergy between technology and system design. A GaN power transistor with rise/fall times of 55/65ps was developed and characterized [49]. This extends the DSM sampling frequency to up to 5 GHz. At the system level, a design procedure for a non-$f_s/4$ center frequency bandpass DSM in GHz frequency range has been established. Based on the developed design procedure, a 5 GS/s 2.1-2.2 GHz bandpass DSM [45], [50] has been developed which relaxes switching conditions for the power device.

Further research work in investigating the pulse encoders was conducted, since the available output power of the class-S amplifier driven by bandpass DSM modulator is limited by relatively low coding efficiency for signals with high PAPR. The primary goal was to develop a fully digital pulse encoder with possibly improved coding efficiency having the input at the baseband and targeting to increase the SMPA output power while driven by a real communication signal. This research work resulted in a fully digital polar pulse encoder architecture [29].

1.4 Organization of the thesis

Chapter 2 contains a brief overview of existing switch-mode power amplifier architectures and principal operating differences. The advantages and disadvantages of different SMPA types will be compared. Sources of losses will be presented and estimated for all architectures.

In Chapter 3, the requirements of the pulse encoder as a part of class-S PA are defined. The pulse encoder parameters, which affect the performance of a complete class-S PA are considered. Chapter 3 also provides an overview of the state-of-the-art modulation techniques that are used to encode a signal with non-constant envelope into a bi-level signal. Direct conversion pulse encoders and pulse encoders with upconversion function are analyzed and compared.
Chapter 4 describes the complete design procedure for \( f_{S}/4 \) and non-\( f_{S}/4 \) center frequency RF bandpass DSMs starting from the system design and up to circuit design, the estimation of non-idealities, and determining a relation between the system and circuit parameters.

In Chapter 5, the measurement setup and measurement results for the designed bandpass DSMs at 900 MHz and 2.1-2.2 GHz center frequencies are presented.

A fully digital polar modulation technique is presented in Chapter 6. The characteristics, which affect the overall SMPA performance, are shown. Also, the key parameters of the proposed pulse encoder architecture are compared with existing pulse modulation techniques, described in Chapter 3. A performance estimation of the digital polar modulation by driving a 2.1 GHz Class-F power amplifier completes this chapter.

Finally, Chapter 7 summarizes the presented work and includes considerations for future research.
Chapter 2. Switch mode power amplifier architectures

As was mentioned in the introduction, an SMPA driven by a signal source encoder and followed by a reconstruction filter can act as a linear amplifier; and such a system is called class-S PA. SMPAs are very attractive because they can theoretically achieve 100% efficiency. Previously, only a class-D PA could be used as an SMPA in a class-S system because of the ability to process non-periodic pulse trains (e.g. DSM, PWM). The rest of the SMPA classes require a periodic driving signal. Recently, the development of advanced modulation methods [21], [30], [19] could extend the choice of the SMPA architecture to the SMPA classes that require 50% duty cycle signal at the input for a most efficient operation (e.g class-E, class-F PAs). In this chapter a brief overview of the basic SMPA types is given and advantages and disadvantages are discussed.

2.1 Losses in a switch

The ideal operation of a switch assumes zero transition times and no parasitic effects associated with a switch and can be described as follows. When a switch is in the ON-state, a high current is flowing without any voltage drop across the switch (resistance of the switch is zero). In the opposite case, in the OFF-state a high voltage can be applied to the switch and no current flows through it (resistance of the switch is infinity). This leads to 100% efficient operation, because voltage and current waveforms are non-overlapping. In electronic circuits, transistors can be used as switches. However, the real transistor has non-ideal parameters that affect the performance of the switch based amplifier. For the operation in a switch mode, the transistor can be represented by an ideal switch connected in series with the resistance $R_{ON}$ and a parallel output capacitance $C_{OUT}$ as it is shown in Fig. 2.1. This simple model is sufficient to compare the losses in different SMPA architectures. Switching and conductive losses are relevant in almost all SMPA classes of operation.
2.1.1 Conductive losses

The conductive losses are caused by non-zero on-impedance $R_{ON}$ of a switch and occur during the time period when a power device is in the ON-state, i.e. when the current through the switch is a non-zero value. The conductive power loss is an inherent loss in all SMPA configurations and can be expressed as

$$P_{cond.loss} \approx I_{sw,rms}^2 R_{ON},$$

where $I_{sw,rms}$ is the root mean square current through the switch. The conducting losses can be decreased by choosing a large transistor, but this leads to increasing the output capacitance and switching losses correspondingly. Also, large transistors will have high input capacitance and in order to drive it, significant power could be dissipated. Another way to reduce conductive losses is to decrease $I_{sw,rms}$ through the switch. The switch current waveform is determined by the SMPA class of operation. On the other hand, in case of non-periodic drive signal, it depends on the ratio of the time period $t_{ON}$, when the switch is in the ON-state, to the total time of operation, i.e $t_{ON}+t_{OFF}$. Decreasing the $t_{ON}/(t_{ON}+t_{OFF})$ decreases $I_{RMS}$ and, consequently, conductive losses. Although, the $R_{ON}$ is defined by the chosen power transistor, the $t_{ON}$ time is dependent on the pulse modulation technique and applied input signal.

2.1.2 Switching losses

Depending on the SMPA class of operation, its performance may be degraded by switching losses. The most dominant source of the switching power losses in the SMPA is caused by the output capacitance $C_{OUT}$ of the switch and described by
\[ P_{sw,loss} = f_{AVG} C_{OUT} V_{OUT}^2, \]  

where \( f_{AVG} \) is the average frequency of the pulse train, \( V_{OUT} \) is the amplitude of the output square-wave signal, which is equal to \( V_{DD} \) in case of a FET-transistor or \( V_{DC} - V_{CE,sat} \) in case of a bipolar transistor (assuming \( R_{ON} = 0 \)). The switching losses are highly undesirable, since they increase with increasing the frequency of operation, making it difficult to achieve high efficiency values at higher frequencies. Though, \( V_{OUT} \) and \( C_{OUT} \) are defined by the chosen SMPA configuration, the average frequency of the pulse train \( f_{AVG} \) is determined by the encoder architecture, if class-S operation is considered.

On the other hand, there are switching losses associated with the driving of the switch, which are related to charging and discharging of the input capacitance. This kind of losses is described similar to the switching losses associated with output capacitance

\[ P_{dr,loss} = f_{AVG} C_{IN} V_{IN}^2, \]  

where \( f_{AVG} \) is the average frequency of the pulse train, \( V_{IN} \) is the amplitude of the driving square-wave signal. Usually, a transistor which acts as a switch is relatively big in order to produce high output power. In this case the input of the transistor introduces a substantial load capacitance to the driving stage. This will cause additional power consumption in a driver, and thus further degradation of the efficiency. In equations (2.2) and (2.3), it is assumed for simplicity that the capacitances are linear and do not depend on the voltage across it.

2.2 Classes of Switch-Mode Power Amplifiers

2.2.1 Periodically driven class-D PA

The class-D RF resonant power amplifier was proposed in 1959 by Baxandall and has been widely used in various applications including radio transmitters. It is based on two active devices operated as switches. There are two types of class-D PAs voltage-switched class-D (VSCD) PA and current switched class-D (CSCD or class-D\(^{-1}\)) PA [51]. Both types have been recently implemented at RF frequencies [5], [52], [53], [54] driven by a 50\% duty cycle square-wave.
2.2.1.1 Voltage switched class-D PA

Fig. 2.2 shows one of the possible realizations of the voltage switched class-D PA. It is a quasi-complementary structure based on two npn bipolar transistors, which are driven in anti-phase by a square-wave signal. In ideal case, 100% efficiency is achieved, because output voltage and output current waveforms of transistors are not overlapping. When the ideal switch is on, it has 0 V across it and can support any current. When it is off there is no current flowing through it. For the ideal switch, lossless driving conditions, an intrinsic $R_{ON} = 0$ and negligible transistor output capacitance are assumed.

The voltage signal at node S in Fig. 2.2 is switched between supply and ground depending on which transistor $Q_1$ or $Q_2$ is open. This yields that the voltage waveform at node S is square. In order to transmit this signal by an antenna, the series LC filter is placed between node S and the load, which allows only the first harmonic to pass to the load. The circuit operates theoretically with 100% efficiency if the input frequency is equal to the resonant frequency of the series LC tank. The output power delivered to the load is

$$P_{out} = \frac{2V^2_{DC}}{\pi^2 R_L}. \quad (2.4)$$

The class-D amplifier has to be driven with a square-wave signal. Delivering of such a signal to the input of the PA is associated with additional power consumption in a corresponding driver.

For a voltage switched class-D PA, the collector current of both transistors is a sinewave for the first half of the period and zero for another half of the period (Fig. 2.3).
Because this PA type has two transistors acting as switches, the switching losses can be determined by

\[
\begin{align*}
P_{\text{switch, loss}} &= 2C_{\text{OUT}}V_{\text{OUT}}^2f_{\text{AVG}} \\
\end{align*}
\]  

(2.7)

Increasing of the average input frequency sets the limitation of using a VSCD PA at GHz input frequencies.
2.2.1.2 Current-switched class-D PA

Fig. 2.4 shows a simplified schematic of the current-switched class-D PA and Fig. 2.5 presents corresponding waveforms. Two transistors are supplied by current sources. Both of the transistor emitters are connected to ground and driven in anti-phase by a square-wave signal. A parallel resonant circuit connected between collectors of the transistors acts as a bandpass filter. If the quality factor of the resonant circuit is high enough, then the voltage signal across the load is a sinewave. During a half period, one transistor is closed, and the current from the sources flows through the open transistor. In the next half period, the current flows through another transistor.

![Simplified circuit of the current switched class-D PA.](image)

**Fig. 2.4. Simplified circuit of the current switched class-D PA.**

![Ideal waveforms.](image)

**Fig. 2.5. CSCD ideal waveforms.**
The collector voltage of the transistor in the OFF-state is sinusoidal, and zero when the transistor is conducting current (Fig. 2.5). The collector voltage waveform $v_1$ can be expanded into a Fourier series as

$$v_1 = \frac{V_m}{\pi} + \frac{V_m}{2} \sin \omega t - \frac{2V_m}{\pi} \sum_{n=1}^{\infty} \frac{1}{4n^2 - 1} \cos(2n\omega t)$$

The DC supply voltage is equal to the first term of expression (2.8)

$$V_{DC} = \frac{V_m}{\pi}$$

By using (2.9), the output power delivered to the load can be expressed as

$$P_{out} = \frac{V_m^2}{2R_L} = \frac{\pi^2V_{DC}^2}{2R_L}$$

The conductive losses for the CSCD PA are expected to be higher than for the VSCD PA, because all the current from the supply flows through a switch. The conductive losses for one transistor can be found as

$$P_{cond.loss}^{CS} = 2I_{DC}^2R_{ON}$$

The efficiency of the current-switched class-D amplifier can be determined as

$$\eta = \frac{1}{1 + \frac{\pi^2 R_{ON}}{2R_L}}$$

The periodically driven Class-D PA can be used in a class-S configuration if driven by a pulse encoder that delivers pulses of width which is close or equal to half of the carrier period $T_c$ and followed by a bandpass filter. The CSCD configuration is more advantageous at high frequencies compared to the VSCD because the parasitic output capacitance in CSCD can be absorbed into the resonant circuit. This eliminates the output capacitance discharge loss and enables better performance of the CSCD PA at a given frequency. For the same reason, the class-D PA implementations at carrier frequencies above 2 GHz delivering more than 5 W output power are current-switched PAs [54], [55].
2.2.2 Non-periodically driven class-D PA

Previously considered VSCD (Fig. 2.2) and CSCD (Fig. 2.4) configurations can be linearized by encoding of the input signal. The drive signals are usually PWM or DSM encoded pulse trains, which are non-periodic signals. The output filter network has to provide corresponding in-band and out-of-band terminations. The in-band termination should represent the optimum impedance. The out-of-band termination has to be an open circuit for VSCD PA and short circuit for CSCD. Since the driving signal frequency is not periodic anymore, an LC tank represents non-constant reactance to the PA which causes phase shifts of the output current. This leads to negative voltages across the switch in case of the CSCD architecture. To prevent negative currents flowing through the switch, series diodes should be connected in the drain or collector of a CSCD amplifier as it is shown in Fig. 2.6.

![Fig. 2.6. Current switched class-D PA with series diodes in collectors to prevent the negative voltage drop across the switches.](image)

The waveforms of the CSCD amplifier in Fig. 2.6 driven by PWM pulse sequence are shown in Fig. 2.7.
Assuming a non-zero $R_{ON}$, the available output power of the CSCD PA driven by a non-periodic pulse train can be expressed as

$$P_{out} = \frac{4}{\eta_C} \frac{1}{1 + \frac{4}{\eta_C} \frac{R_{ON}}{R_L}} \frac{V_{DC}^2}{R_L}$$  \hspace{1cm} (2.13)$$

and the efficiency as

$$\eta = \frac{1}{1 + \frac{4}{\eta_C} \frac{R_{ON}}{R_L}}$$  \hspace{1cm} (2.14)$$

where $\eta_C$ is the coding efficiency that can be determined for any driving pulse train as relation between the in-band power after filtering the pulse train by an ideal filter to the total power in the pulse train [56]. The coding efficiency $\eta_C$ is dependent on the method how the driving pulse train is encoded and will be discussed in Chapter 3.

In case of the non-periodic drive signal, a VSCD PA based on FET transistors can withstand negative currents. Alternatively, if a VSCD PA is based on bipolar transistors, the negative current cannot flow through the transistors and charges the intrinsic output capacitance of the device. This can cause large voltage spikes which can damage the transistors [57]. In order to prevent negative currents flowing through the switch, anti-parallel diodes should be connected to the switches as it is shown in Fig. 2.8. Then the negative portions of the currents $i_1$ and $i_2$ result in currents $i_3$ and $i_4$ correspondingly, which flow through the diodes. However, at GHz input frequencies, anti-parallel diodes substantially degrade the efficiency because of their capacitance. Therefore in some realizations, a VSCD PA is implemented without diodes and still shows reliable operation [58].
The waveforms of the VSCD amplifier in Fig. 2.8 driven by PWM pulse sequence are shown in Fig. 2.9.

The output power assuming non-zero $R_{on}$ can be expressed as follows [59]:

$$P_{out} = \frac{1}{4} \frac{\eta_c}{1 + cf \sqrt{\eta_c} \frac{R_{on}}{R_L}} \frac{V_{dc}^2}{R_L}$$  \hspace{1cm} (2.15)
where $cf$ is the crest factor that is defined as ratio between the maximum signal value and its rms value. The PA efficiency can be determined as [59]

$$\eta = \frac{1}{1 + cf \sqrt{\eta_c}} \frac{R_{ON}}{R_L}$$ (2.16)

With respect to the class-S PA system, a class-D PA (CSCD or VSCD) is the only SMPA that can be driven by non-periodic pulse trains such as PWM or DSM. The output capacitance in the non-periodically driven CSCD PA cannot be absorbed by the output load network because of diodes connected in series. On the other hand, in VSCD PA, anti-parallel diodes can be omitted [58] enabling better PA efficiency. Also, the reconstruction filter in CSCD PA is more complex because it has to transform a differential signal to an unbalanced one whereas in VSCD PA the filter is a two port network. Thus, for processing of non-periodic driving pulses, the VSCD PA is the most promising architecture.

### 2.2.3 Class-E PA

A class-E power amplifier (Fig. 2.10) was invented by Sokals in 1975 [60]. Because of simplicity and high efficiency, it is a very popular one among other PA classes. In a class-E power amplifier, the output capacitance of the transistor is incorporated into the load network. This eliminates the switching losses which becomes a significant advantage at higher frequencies. The class-E PA has a simple load network, which is designed to avoid an overlapping of the voltage and current waveforms. The current and voltage waveforms are depicted in Fig. 2.11 and correspond to a zero-voltage switching (ZVS) class-E power amplifier. At the turn-OFF, when the current goes to zero, a voltage is delayed by using shunt capacitor $C_p$, eliminating switching losses at this time instant. At the turn-ON time, the load network controls the voltage waveform to have a zero slope. This allows avoiding a corresponding current spike and, thus, diminishes conductive losses.
CHAPTER 2. SWITCH MODE POWER AMPLIFIER ARCHITECTURES

The output power of the ZVS class-E PA can be expressed as [61]

$$ P_{\text{out}} = \frac{8}{\pi^2 + 4} \frac{V_{\text{dc}}^2}{R_L} $$  \hspace{1cm} (2.17)

In presence of non-zero switch resistance, the classical class-E approach does not fulfill zero-voltage condition at the turn-ON instant. In this case, the efficiency can be found as [61]

$$ \eta = \frac{1}{1 + \frac{\pi^2 + 28}{2(\pi^2 + 4)} \frac{R_{\text{ON}}}{R_L}} $$  \hspace{1cm} (2.18)

A classical class-E PA, shown in Fig. 2.10, must be driven by a periodic signal with a 50% duty cycle to operate at maximum efficiency. A simulation of an ideal class-E PA ($R_{\text{ON}} = 0, R_{\text{OFF}} = \infty$, transistor $C_{\text{OUT}} = 0$) versus different duty cycle values of the input signal is shown in Fig. 2.12. It can be seen, that in case of rectangular drive, the duty cycle
has to be near or equal to 50% to keep the efficiency close to the maximum. The same is valid for an encoded pulse train in case of the class-S configuration. Pulse widths of the encoded pulse train must be close or equal to half of the carrier period. Pulse encoding techniques satisfying this criterion have been proposed in [21], [24], [29], [30], [62]. For some of these encoding techniques, aperiodic zero-crossings in a class-E PA can generate large voltage transients across the transistor [31], such that a diode is required in order to protect the device.

On the other hand, it is also possible to achieve 100% efficiency for an ideal class-E PA driven by a periodic square-wave with different duty cycles. The RF pulse-width modulation (PWM) technique can be applicable, if the load network can be changed dynamically depending on the driving pulses. A design procedure of the class-E PA, driven by a signal with different duty cycles, is presented in [63] and relates to the PA with an RF-choke. Since an RF-choke lowers the operating frequency of the PA, in [64], the design equations for a finite DC-feed were proposed, however, only for the case if the driving signal is a 50% duty cycle square-wave. In [65], a class-E topology and design equations were proposed to achieve an efficient operation of a class-E amplifier driven by an RF PWM signal.

![Simulated efficiency of an ideal class-E PA vs. duty cycle.](image)

Fig. 2.12. Simulated efficiency of an ideal class-E PA vs. duty cycle.

Thus, the classical class-E PA can be used in a class-S configuration if driven by a pulse encoder that delivers pulses which are close or equal to half of the carrier period $T_c$ (Fig. 2.12). Or, on the other hand, a class-E PA, having a load network varied along with the pulse width, can be driven by an RF-PWM signal [65]. However, in the latter case the
transmitter signals cannot have a PAPR of higher then 6.5 dB. Along with all advantages listed above, the class-E PA has some drawbacks. The ZVS operation in the class-E concept is limited up to a certain frequency where it is possible to absorb the output transistor capacitance into a load network. The output power capability of the class-E PA is approximately 1.6 times smaller compared to the class-D or class-F SMPAs due to the voltage and current waveforms at the collector of a power transistor [51].

2.2.4 Class-F PA

The class-F power amplifier principle is based on the termination of harmonics by the output circuit in a special way in order to minimize overlapping of the switch voltage and current, that yields an increase of the switch efficiency. In this section, only the inverse class-F ($F^{-1}$) PA is reviewed since it shows superior performance compared to a class-F PA [66]. In a class-$F^{-1}$ PA, the current through a switch is a square-wave and the voltage across the switch is a half-sinewave. Proper termination at harmonics forms corresponding voltage and current waveforms. The output circuit in a class-$F^{-1}$ PA represents a short circuit at all odd harmonics and an open circuit at all even harmonics. The class-$F^{-1}$ output network at few GHz frequencies usually employs a quarter wavelength transmission line (Fig. 2.13) because it has reasonable size to be realized on a printed circuit board (PCB). In Fig. 2.13, the series resonant circuit introduces an open circuit at harmonic frequencies. The quarter-wavelength transmission line at all odd harmonics transforms an open circuit to short circuit. At even harmonics, the switch sees an open circuit. Corresponding current and voltage waveform are shown in Fig. 2.14.

![Fig. 2.13. Class-$F^{-1}$ power amplifier circuit.](image)
The collector voltage waveform $v_1$ can be expanded into a Fourier series as

$$v_1 = \frac{V_m}{\pi} + \frac{V_m}{2} \sin \omega t - \frac{2V_m}{\pi} \sum_{n=1}^{\infty} \frac{1}{4n^2 - 1} \cos (2n\omega t)$$  \hspace{1cm} (2.19)

The DC supply voltage is equal to the first term of expression (2.19).

$$V_{DC} = \frac{V_m}{\pi}$$  \hspace{1cm} (2.20)

The amplitude of the output voltage $v_1$ is equal to the second term of expression (2.19).

$$V_{out} = \frac{V_m}{2}$$  \hspace{1cm} (2.21)

By combining (2.20) and (2.21), the output power of the class-F\(^1\) PA with properly terminated odd and even harmonics can be expressed as

$$P_{out} = \frac{V_{out}^2}{2R_L} = \frac{\pi^2 V_{DC}^2}{8R_L}$$  \hspace{1cm} (2.22)

Theoretically, the class-F\(^1\) PA with a quarter-wavelength transmission line can operate at 100% collector efficiency. The collector efficiency in case of non-zero ON-resistance can be expressed as [57]

$$\eta = \frac{1}{1 + \frac{\pi^2 R_{ON}}{4R_L}}$$  \hspace{1cm} (2.23)

The class-F\(^1\) PA can be used in a class-S configuration if driven by a pulse encoder that delivers pulses which are close or equal to half of the carrier period $T_C$. An ideal class-F\(^1\) PA shows much worse efficiency when the driving pulses differ from $T_C/2$ width compared with...
to the class-E (Fig. 2.12) [34]. However, for a real class-F\(^{1}\), this is not the case as it will be demonstrated in Chapter 6. Moreover, the class-F\(^{1}\) PA can achieve higher output power than a class-E PA. In contrast to a class-E PA, a class-F\(^{1}\) PA is subject to switching losses. Compared to a class-D PA, a class-F\(^{1}\) PA requires a simpler driving network because it consists of only one transistor. The output circuit of a class-F\(^{1}\) PA acts as a reconstruction filter which is not as complex as the reconstruction filter in a CSCD PA.

### 2.3 Conclusion

In this chapter, basic SMPA configurations that can be used in a class-S PA have been reviewed. Table 2-1 compares the operation conditions for these SMPA classes.

For a replacement of a PA in the analog transmitter by a class-S implementation, the direct conversion pulse encoding techniques can be employed. In case of non-periodic pulse trains (e.g. PWM, DSM) in a class-S PA system only VSCD or CSCD PA can be used. At such driving conditions, both SMPA architectures suffer from losses associated with finite switch impedance and non-zero output capacitance. For a CSCD based class-S PA, the reconstruction filter is more complex because it has not only to provide proper termination but also transform a differential signal to an unbalanced one. In VSCD PA case, the filter is a two port network. Although, in the VSCD PA a more complex driver circuitry is required, the anti-parallel diodes can be omitted [58] enabling a better PA efficiency as in the CSCD case. Thus, for processing of non-periodic driving pulses, the VSCD PA seems to be the more promising solution.

Periodically driven SMPA classes can be used in a class-S configuration if driven by a pulse encoder that delivers pulses which are close or equal to half of the carrier period \(T_c\). Most of the frequency upconverting pulse encoders satisfy that conditions [10], [24], [30]. Thus, in conjunction with an upconverting pulse encoder, a periodically driven SMPA forms a class-S based fully digital transmitter (Fig. 1.5). In this regard, class-E and class-D\(^{1}\) PAs are very attractive structures because they do not suffer from the switching losses at a given driving signal. However, a class-D\(^{1}\) PA requires two transistors and additionally a balun circuit which consume substantial space on the printed circuit board (PCB). Also driving circuit is more complex as in the case of a class-E or a class-F\(^{1}\). The Class-E PA should
Table 2-1. Comparison of class-S PAs based on basic SMPA classes.

<table>
<thead>
<tr>
<th>SMPA class</th>
<th>D</th>
<th>D(^1)</th>
<th>E</th>
<th>F(^1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driving signal duty cycle</td>
<td>non-periodic</td>
<td>(non-)periodic</td>
<td>periodic</td>
<td>periodic</td>
</tr>
<tr>
<td>Driving circuit</td>
<td>+</td>
<td>++</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>Power capability</td>
<td>++</td>
<td>++</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Zero voltage switching</td>
<td>-</td>
<td>(-)+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>+</td>
<td>(+)++</td>
<td>+++</td>
<td>++</td>
</tr>
<tr>
<td>Reconstruction filter</td>
<td>++++</td>
<td>+</td>
<td>+++</td>
<td>++</td>
</tr>
</tbody>
</table>

++++ denotes better performance and/or realization simplicity

provide better performance than the class-F\(^1\) PA in terms of bandwidth, ZVS operation and simplicity of the output network. On the other hand, an SMPA based on the class-F\(^1\) has higher output power capability and is able to more efficiently amplify pulses which are not equal to half of the carrier period \(T_c\). The ZVS operation in the class-E concept is limited up to a certain frequency which is around 2 GHz for modern GaN power transistors [67]. Therefore, a class-E PA still can be considered in a 2 GHz switched-mode transmitter driven by the upconverting pulse encoder. Thus, in order to determine the most suitable SMPA class for a fully digital transmitter, both PA classes, class-E and class-F\(^1\), should be investigated in realistic environment. Within the scope of this work, the class-F\(^1\) PA has been used for performance estimation of the proposed upconverting pulse encoder [29].

In the next chapter, different pulse encoder architectures that are suitable for linearization of the considered SMPAs will be presented.
Chapter 3. Pulse encoders for RF switch mode amplifiers

A pulse encoder in a class-S system is required to convert the input non-constant envelope signal to a bi-level signal, which is needed to drive an SMPA. There are numerous of different pulse modulation techniques that can perform the required operation. Some of them, which may be applicable to an SMPA at RF frequencies, are described and compared in this chapter. In most cases, encoders are based on or contain components incorporating pulse-width modulation (PWM) or delta-sigma modulation (DSM). Research activities in the last decade concentrated on RF pulse encoder architectures that can be classified into two groups according to a frequency conversion method:

- direct conversion pulse encoders
- upconverting pulse encoders

In direct conversion pulse encoders, the signal containing information appears at the output at the same carrier frequency as it was at the input. This group of pulse encoders can be realized as either a pulse-width or delta-sigma modulation. Each encoder type has its advantages and disadvantages that will be discussed in this chapter.

The pulse encoder architectures with a frequency upconversion function take an input at baseband frequency and convert it to a higher (carrier) frequency. This group of encoders can be further subdivided into IQ pulse encoders and polar pulse encoders.

Some metrics have to be defined in order to provide a comparison of the different encoding techniques. The next section explains the requirements and performance metrics of pulse encoders.

3.1 Pulse encoder requirements

Since a communication signal with a high PAPR has to be linearly amplified and transmitted by a class-S PA, the usual transmitter requirements to different distortion types have to be applied to an encoder as well. Usually, for such signals, a communication standard
specifies an acceptable adjacent channel leakage ratio (ACLR) and an error vector magnitude (EVM).

The ACLR is the measure of out-of-band distortion caused by intermodulation products of the band-limited signal to neighboring channels. According to Fig. 3.1, an ACLR in the adjacent channel at the \( \pm f_1 \) frequency offset from the center frequency \( f_c \) can be found as

\[
ACLR_{\pm f_1} = 10 \log \frac{P_{CH1}}{P_{CH0}}
\]

where \( P_{CH1} \) is the power in the left or right adjacent channels CH1L or CH1R (Fig. 3.1), respectively, integrated over the bandwidth \( f_{BW} \) and \( P_{CH0} \) is the power in the main channel. Similarly, the ACLR in the alternative channel at the \( \pm f_2 \) frequency offset can be found by substitution of the power \( P_{CH2} \) calculated in the left or right channels CH2L or CH2R in (3.1) instead of \( P_{CH1} \).

\[
ACLR_{\pm f_2} = 10 \log \frac{P_{CH2}}{P_{CH0}}
\]

In this thesis, a test signal is based on a CDMA signal corresponding to the Test Model1 which is defined in the communication standard [68]. This standard sets the ACLR values as specified in Table 3-1. In this case, the values of \( f_{BW} \), \( f_1 \), \( f_2 \) in Fig. 3.1 are equal to 3.84 MHz, 5 MHz and 10 MHz, respectively. According to the standard, the bandwidth of the adjacent channels is specified to be equal to the bandwidth of the main channel.
Table 3-1. ACLR requirements according to the UMTS standard.

<table>
<thead>
<tr>
<th></th>
<th>Uplink</th>
<th>Downlink</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ACLR_{15MHz}$, dBc</td>
<td>-33</td>
<td>-45</td>
</tr>
<tr>
<td>$ACLR_{10MHz}$, dBc</td>
<td>-43</td>
<td>-55</td>
</tr>
</tbody>
</table>

The EVM characterizes an in-channel distortion. In a transmitter, the EVM is a measure of modulation accuracy. Fig. 3.2 shows the location of an ideal symbol which has to be sent and the location of a measured symbol which represents the ideal symbol passed through a transmitter chain. The error vector is a difference between the reference vector pointing to the ideal symbol location and the measured vector. The EVM is defined as the square root of the ratio of the mean error vector power $P_{err}$ to the mean reference power $P_{ref}$ expressed in % [68]

$$EVM(\%) = \sqrt{\frac{P_{err}}{P_{ref}}} \times 100$$  \hspace{1cm} (3.2)

According to [68], the EVM for a composite CDMA signal modulated by QPSK and 16QAM should be lower than 12.5%.
CHAPTER 3. PULSE ENCODERS FOR RF SWITCH MODE AMPLIFIERS

3.2 Pulse encoder parameters

Besides the power transistor and reconstruction filter properties, the overall SMPA performance is highly dependent on the encoder characteristics such as

- coding efficiency
- average frequency of the pulse train
- on-state duration
- pulse statistic in the output pulse train
- encoder power dissipation

The first four parameters can be calculated on the system level and will be estimated in this chapter for different encoding techniques. The last parameter, the pulse encoder power dissipation, can be determined during the circuit design phase only.

3.2.1 Coding efficiency

The available output power of the class-S amplifier is dependent on the coding efficiency $\eta_c$ of a pulse encoder, where $\eta_c$ is defined as the ratio of the mean RF signal power in the pulse train to the total pulse train power [56] and described by

$$\eta_c = \frac{P_{\text{SIGNAL}}}{P_{\text{TOTAL}}},$$

where $P_{\text{SIGNAL}}$ is the signal power in the band of interest and $P_{\text{TOTAL}}$ is the total power in the output pulse train which in the ideal case corresponds to the power of the signal at the input of the encoder. For a bi-level zero-mean periodic signal with an arbitrary duty cycle $D$, the coding efficiency $\eta_c$ can be determined as [69]

$$\eta_c = \frac{8}{\pi^2} \sin^2(\pi D)$$

Equation (3.4) shows that the maximum coding efficiency is achieved for a square-wave signal with a duty cycle of 50% and is equal to $8/\pi^2 \approx 81\%$. This value is the maximum limit of the coding efficiency for any bi-level pulse modulation technique.
Superior encoding techniques assume that much power should be concentrated at the carrier frequency while the power in the harmonics is reduced. Thus, any improvement in coding efficiency results in reduction of the power transistor size [70].

Throughout this thesis, the coding efficiency for different pulse encoders is given for a full-scale input unless otherwise stated.

### 3.2.2 Average frequency

As was mentioned in Chapter 2, the performance of SMPA at GHz frequencies is highly degraded by switching losses. Therefore, SMPAs which can absorb the output capacitance in a load network are very attractive. As can be seen from (2.2), the switching losses are proportional not only to the value of the output capacitance but also to the average frequency of the driving pulse train as well. The average frequency \( f_{\text{AVG}} \) is dependent on the encoding principle. Usually, it is determined with respect to the carrier frequency and can be found as [56]:

\[
    f_{\text{AVG}} / f_c = \frac{n_t}{n_c},
\]

where \( n_t \) is the number of transitions in the pulse train; \( n_c \) is the number of transitions of the square-wave at the carrier frequency \( f_c \).

### 3.2.3 ON-state duration

The conductive losses in an SMPA are proportional to \( i_{\text{RMS}}^2 R_{\text{ON}} \). The \( R_{\text{ON}} \) is fixed by a chosen transistor. In case of a periodic driving signal, \( i_{\text{RMS}} \) is determined by the SMPA class of operation. If a non-periodic pulse train is applied to the input of SMPA, then \( i_{\text{RMS}} \) is defined by the total time when the switch is in the ON-state. The time period during which the switch is in the ON-state \( t_{\text{ON}} \) is dependent on a pulse encoding technique as well. Comparing the ratio \( t_{\text{ON}} / (t_{\text{ON}} + t_{\text{OFF}}) \) for different pulse encoders it is possible to roughly estimate the conductive losses they cause in an SMPA.
3.2.4 Pulse width statistic

Another very important characteristic of a pulse modulation technique is its pulse width statistic. By analyzing pulse widths in the pulse encoder output, an appropriate SMPA class can be determined. For example, ideally, for class-E and class-F SMPAs, all pulses in the encoded pulse train have to be equal to half of the carrier period. Otherwise, if pulse widths are not concentrated near half of the carrier period, a class-D PA has to be considered. In this chapter, a pulse width statistic will be presented for each considered pulse modulation technique.

3.3 Direct frequency conversion pulse encoders

In the analog transmitter, a class-S PA requires a direct frequency conversion pulse encoder. The direct conversion pulse encoder receives at its input an analog modulated signal at carrier frequency $f_c$, and converts it to the bi-level signal. The exploration of class-S amplifiers at radio frequencies has been started from two different direct conversion encoders, PWM and bandpass DSM, which have been inherited to RF from audio amplifier architectures. Early audio amplifiers incorporated PWM modulation as a driver of the class-D PA. During the last two decades, research in DSM-driven audio amplifiers made significant steps in terms of achievable SNDR values [16], [71].

3.3.1 Pulse width modulation direct conversion encoder

3.3.1.1 Conventional PWM

A PWM-encoded pulse train can be obtained by comparing an amplitude of the input signal $s_{in}$ with a triangular or sawtooth waveform. If the input signal $s_{in}$ is higher than the reference waveform $s_{tri}$, the PWM encoder generates a “1” pulse, otherwise a “0” pulse. The block diagram of the PWM is depicted in Fig. 3.3.
Fig. 3.3. Block diagram of the PWM encoder.

Fig. 3.4. PWM encoder waveforms.

The higher the triangle wave frequency the better accuracy of the output signal. However, with an increase of the ratio $f_{tri}/f_{in}$, the pulses become narrower which will require more bandwidth from the output stage. As an example, at the input of the PWM, a two-channel RF carrier modulated by a 5 MHz bandwidth WCDMA signal corresponding to a TestModel1 [68] and having a PAPR=9.9 dB is applied. In Fig. 3.5 (a) and (b), the pulse statistics for $f_{tri}/f_{in}=1.7$ and for $f_{tri}/f_{in}=3.2$ are shown, respectively. In the case if $f_{tri}/f_{in}=1.7$, it can be seen that the pulse distribution extends over a larger part of the carrier period $T_C$, and thus it relaxes the switching requirements of the SMPA. The average frequency of the PWM pulse train is equal to the value of $f_{tri}/f_{in}$. Thus, the lower the ratio $f_{tri}/f_{in}$, the lower the switching losses are in an SMPA. In the case if realizing $f_{tri}/f_{in}$ as an integer value, the harmonic content is much lower in the output spectrum, which relaxes selectivity requirements of the reconstruction filter.
Fig. 3.5. Pulse width statistics for (a) $f_{tri} / f_{in} = 1.7$; (b) $f_{tri} / f_{in} = 3.2$.

Fig. 3.6 shows the output spectrum of the PWM encoder while the exemplary WCDMA signal is applied. The strong reference tone at $f_{tri}$ and sideband harmonics (Fig. 3.6 (a)) may highly degrade the coding efficiency. Indeed, by using equation (3.3), the calculated coding efficiency for the resulted PWM pulse train is 3.6 % only. The ACLR is -55.5 dB for a 3.84 MHz adjacent channel at 5 MHz offset from the right channel.

Fig. 3.6. Simulated output spectrum of the conventional PWM encoder with $f_{tri} / f_{in} = 1.7$ driven by a WCDMA modulated carrier (a) from DC to $5f_{in}$; (b) at $f_{in}$ with a 60 MHz span.

There are some PWM realizations at hundreds of MHz input frequencies. A complete class-S PA based on the conventional PWM encoder at 900 MHz presented in [33]
demonstrated ACLR of -52 dB. The PA fulfills 3GPP specification [72] in terms of EVM and ACLR. However, the authors stated that because of the PWM’s poor coding efficiency, the output power of the complete class-S PA was 50 mW only. In contrast, the used SMPA driven by a 50% duty cycle square-wave demonstrates a peak output power of 5 W [32]. The realization of the classical PWM at 450 MHz and at 955 MHz in SiGe 0.25 um can be also found in [73] and [74], respectively.

Since the PWM is not a time-discrete pulse modulation technique, it does not suffer from quantization noise as in the case of a DSM. This may relax the selectivity requirements of the reconstruction filter in a class-S SMPA for PWM with a higher ratio of $f_{tri}/f_{in}$. On the other hand, the PWM has two main drawbacks. Firstly, the smaller the amplitude of the input signal the more often narrow pulses are generated. For a signal with high PAPR, the peak in PDF will be further shifted from the half period point to a shorter pulse width, as it is demonstrated in Fig. 3.5. Thus, for the PWM, a broadband operation of the power transistors is required. Secondly, the presence of the strong reference tone at $f_{tri}$ and sideband harmonics highly degrades the coding efficiency.

### 3.3.1.2 RF-PWM

In contrast to conventional PWM, in RF-PWM, only one (unipolar) or two (bipolar) pulses are transmitted during each period of the RF carrier signal (Fig. 3.7). The transmitted signal can be expressed as

$$s_{TX}(t) = A(t) \cdot \cos(\omega_c t + \varphi(t))$$  \hspace{1cm} (3.6)

The idea of the unipolar RF-PWM is based on comparing a pre-distorted envelope signal $A(t)$ with a phase modulated RF carrier signal $\cos(\omega_c t + \varphi(t))$. The signal $A(t)$ has to be pre-distorted in such a way that after bandpass filtering of the RF-PWM pulse train, one obtains a signal described by (3.6).

By means of straightforward comparison of the envelope signal $A(t)$ with the phase modulated RF carrier signal $\cos(\omega_c t + \varphi(t))$, the needed pre-distortion function can be found. The pulse width $\Phi(t)$ (Fig. 3.7(a)) of the output pulse train is related to the envelope $A(t)$ as follows
\[ \Phi(t) = 2 \arccos A(t) \] (3.7)

The demodulated envelope \( A_{\text{out}}(t) \) can be found by bandpass filtering at the carrier frequency \( \omega_c \), and expressed as

\[ A_{\text{out}}(t) = \frac{2}{\pi} \sin \left( \frac{\Phi(t)}{2} \right) \] (3.8)

Combining (3.7) and (3.8), the transfer function of the RF-PWM encoder and subsequent bandpass filter is obtained

\[ A_{\text{out}}(t) = \frac{2}{\pi} \sin \left( \arccos A(t) \right) \] (3.9)

Equation (3.9) represents a nonlinear operation of the RF-PWM modulator-demodulator chain. Thus, the envelope \( A(t) \) of the transmitted signal (3.6) has to be pre-distorted according to (3.9) in order to linearize the RF-PWM modulation-demodulation process.

![Waveforms in RF-PWM](image)

(a) \( \cos(\omega_c t + \phi(t)) \)  \( \Phi(t) \) \( A(t) \) \( s_{\text{out}} \)  
(b) \( |\cos(\omega_c t + \phi(t))| \)  \( A(t) \) \( s_{\text{out}} \)

**Fig. 3.7. Waveforms in RF-PWM (a) unipolar; (b) bipolar.**

The unipolar RF-PWM pulse encoder was simulated for the same exemplary signal with a high PAPR as the conventional PWM in section 3.3.1.1 at 2.12 GHz carrier frequency. The pulse width statistic is shown in Fig. 3.8. The group of pulse widths on the left side are zeros, and on the right side are ones. In order to be able to amplify 90% of all pulses without distortion, an SMPA has to process the pulses which are up to 20 times narrower than the carrier period. This sets very strict requirements to the power transistor in terms of bandwidth. The average frequency for RF-PWM is equal to the carrier which decreases switching losses in comparison to conventional PWM.
Remarkably, the coding efficiency of the simulated unipolar RF-PWM pulse train for
the given test signal is 24.2%. The simulated output spectrum in Fig. 3.9 (a) shows a DC
component and relatively high power at low frequencies in the pulse train. This means that a
DC-coupled driver has to be implemented for driving of an SMPA. On the other hand, by
employing the bipolar RF-PWM as illustrated in Fig. 3.7(b), the output pulse train is DC-free
and correspondingly an AC coupling can be used for driving of an SMPA. Moreover, the
power at lower frequencies is decreased and even harmonics are eliminated (Fig. 3.10). This
doubles the coding efficiency to 48.4 % for the given test signal. However, a more complex
amplifier architecture is required (e.g. as in [15]).
CHAPTER 3. PULSE ENCODERS FOR RF SWITCH MODE AMPLIFIERS

Fig. 3.10. Output spectrum of the bipolar RF-PWM encoder driven by a WCDMA modulated carrier.

The RF-PWM encoding technique was proposed by Besslich [14]. The first realization of class-D amplifier driven by RF-PWM was demonstrated by Raab in 1973 [15]. A push-pull Class-D PA driven by RF-PWM has been recently demonstrated at lower frequency 500 kHz while producing 187 W peak power [1]. This paper also showed measurement results of the amplifier by encoding the signals with high PAPR. For a signal with 10 dB PAPR the amplifier delivers 18.8 W with 79 % efficiency.

Implementation of the RF-PWM at 2 GHz is presented in [75]. The chip was realized in GaAs technology, demonstrated good accuracy (EVM < 1.5 %), and fits in the UMTS spectrum mask for uplink transmission. Unfortunately, the experimental results of the real PA driven by the proposed RF-PWM has not been presented.

An RF-PWM topology that eliminates the envelope pre-distortion and has a linear transfer function was proposed in [76] and [77].

From the above design examples, it can be concluded that the direct conversion pulse encoder by means of RF-PWM demonstrates good accuracy in terms of EVM, low out-of-channel distortion, and it relaxes the requirements of the reconstruction filter. The RF-PWM presents the best coding efficiency value among other bi-level encoding techniques. However, it requires a high-speed switching capability from the power transistor in order to operate efficiently at GHz carrier frequencies.
3.3.2 Bandpass DSM direct conversion encoder

3.3.2.1 Principle of operation

The bandpass DSM is another type of a direct-conversion pulse encoder which uses both level quantization and time sampling. The idea of the low pass DSM was proposed by Inose et al. in 1962 [78] whereas the bandpass DSM configuration was suggested only in 1987 [79]. The DSM circuit is widely used in audio amplifiers, ADCs, fractional-N PLLs and, with developing of semiconductor technologies, it tries to find its place in a software-defined radio [80],[81]. Since, a bandpass DSM has to sample the input signal at the GHz carrier frequency, only a continuous-time (CT) DSM realization is suitable to operate at this speed.

The general block diagram of CT DSM is depicted in Fig. 3.11 (a). In Fig. 3.11 (b), the quantizer is substituted by the linear model, where $Q(z)$ is a quantization noise, $X(s)$ is the input and $Y(z)$ is the output. Depending on the loop filter transfer function $H(s)$, the DSM usually implements either low-pass or band-pass characteristic.

By setting $X(s) = 0$, the noise transfer function (NTF) can be written as

$$\text{NTF}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1 + H(z)} \quad (3.10)$$

On the other hand, the signal transfer function (STF) can be found by setting $Q(z) = 0$ as

$$\text{STF}(s,z) = \frac{Y(z)}{X(s)} = \frac{H(z)}{1 + H(z)} \quad (3.11)$$
Considering the first order LP DSM, in Fig. 3.11 (a), $H(s)$ should represent an integration function and is equal to $f_s / s$. Then the $NTF(z)$ in (3.10) has a high pass response, whereas the $STF(s,z)$ in (3.11) is a lowpass if zero pulse width sampling is assumed. Thus, the quantization noise is shaped by the $NTF(z)$. The in-band noise is reduced, whereas, the out-of-band quantization noise is increased.

Finally, the system in Fig. 3.11 (b) with two inputs and one output can be represented by

$$Y(z) = STF(s,z)X(s) + NTF(z)Q(z)$$  \hspace{1cm} (3.12)

Fig. 3.12 shows the reduction of quantization noise in case of an oversampled quantizer noise-shaping compared to a Nyquist quantizer and compared to an oversampled quantizer.

![Fig. 3.12. Quantization noise for Nyquist quantizer, for oversampled quantizer and for noise-shaped DSM of different orders.](image)

In general, the in-band quantization noise power for all cases in Fig. 3.12 can be described by

$$P_{IBN} = \frac{\sigma_e^2}{f_s} \int_{-f_w}^{f_w} |NTF(f)|^2 df,$$  \hspace{1cm} (3.13)

where $\sigma_e^2$ is the quantization noise power of the Nyquist quantizer [82].

Knowing the in-band noise power and the power of the sinewave signal, a signal-to-noise ratio (SNR) can be determined, which is one of the main performance metrics of ADC
In case, a modulated signal is applied, the SNR can be used for rough estimation of the ACLR.

A bandpass DSM requires a bandpass loop filter. The most straightforward way is to find an appropriate DT low pass loop filter transfer function $H_{LP}(z)$ for a lowpass prototype according to required SNR. Then by applying $z \rightarrow -z^{-2}$ transformation, one obtains a bandpass loop filter transfer function $H_{BP}(z)$ (Fig. 3.13) [84].

![Fig. 3.13. $z \rightarrow z^{-2}$ transformation from low pass prototype (a) to the corresponding bandpass DSM (b).](image)

By using this transformation, the obtained bandpass DSM has the same characteristics as a lowpass prototype and the center frequency of the bandpass DSM will be shifted to $f_s/4$. Finally, a CT bandpass loop filter transfer function $H_{BP}(s)$ can be obtained from $H_{BP}(z)$ by using, for example, the impulse invariant transformation [85].

### 3.3.2.2 Bandpass DSM performance estimation

Simulations with the CDMA test signal are conducted on a 4th order CT bandpass DSM architecture proposed in [86] (Fig. 3.14). This structure is known as $f_s/4$-architecture because it is sampled at a clock frequency which is 4 times higher than the notch frequency. It consists of two resonators, a quantizer, and four feedback loops from the output of the quantizer to the resonator inputs. Each feedback loop comprises return-to-zero (RZ) or half-delayed return-to-zero (HRZ) DACs and corresponding scaling coefficients [86].
A simulation of the modulator in Fig. 3.14 has been performed using a finite quality factor in the resonators, without any delays in the feedback and with a jitter-free clock source. The simulated output spectrum of the bandpass DSM with the input WCDMA test signal is shown in Fig. 3.15 (a) and (b). From the spectrum, an ACLR at the neighbor channel was calculated and is equal to -63.5 dBc.

Fig. 3.15. Output spectrum of the bandpass DSM driven by a 2-channel WCDMA modulated carrier (a) from DC to \( f_s/2 \); (b) at \( f_s \) with a 120 MHz span.

Observing the pulse width statistic in Fig. 3.16, one can see that the minimum pulse width is equal to \( T_c/4 = T_s \), and the width of the rest of the pulses is a multiple of the minimum pulse width. This relaxes the requirements on the power transistor with respect to the bandwidth if compared with PWM-based techniques.
For the $f_s/4$ bandpass DSM architecture, the average frequency of the pulse train (section 3.2.2) is approximately equal to the carrier frequency. For a given two-channel WCDMA test signal with the PAPR of 9.9 dB, the coding efficiency is calculated to be 4.4%.

Compared to RF-PWM encoder, the bandpass DSM shows lower coding efficiency for signals with high PAPR. On the other hand, the bandpass DSM demonstrates a good design margin to fulfill the UMTS standard specification in terms of ACLR. Also, it demonstrates low in-band distortion and relaxed switching requirements to an SMPA.

### 3.4 Upconverting pulse encoders

An SMPA driven by an upconverting pulse encoder is an alternative transmitter architecture. It is of high importance to realize the upconverting pulse encoder in the digital domain because it enables a fully digital multi-standard multiband transmitter. In this case, the upconverting pulse encoder should receive at its input a digital baseband signal and convert it to a bi-level signal at the carrier frequency $f_c$. The output signal must be an appropriate pulse train for driving an SMPA. A modulated RF carrier, that has to be constructed by a class-S transmitter, can be represented in two ways. In the first case, both amplitude and phase of the carrier are changed as it is shown in (3.14).

$$s_{\text{tx}}(t) = A(t) \cdot \sin(\omega_c t + \phi(t))$$  \hspace{1cm} (3.14)
This implies the use of a polar type of pulse encoder, where amplitude and phase-modulated carrier are constructed separately. At the end, they must be combined before amplification and filtering. Another way is quadrature modulation and is described by (3.15).

\[ s_{\text{RX}}(t) = Q(t) \cdot \cos(\omega_c t) + I(t) \cdot \sin(\omega_c t) \]  

(3.15)

Here only signals \( I(t) \) and \( Q(t) \) are varied. \( I(t) \) and \( Q(t) \) represent the amplitudes of the RF carriers shifted by \( \pi / 2 \) with respect to each other.

An RF upconverting pulse encoders are based on these two approaches.

### 3.4.1 Upconverting quadrature pulse encoder

There are only few realizations of the quadrature pulse encoder that are dedicated for driving of a class-S PA ([25], [10], [30]). In this section the performance of a fully digital quadrature pulse encoder presented in [30] will be analyzed.

The architecture is shown in Fig. 3.17. It consists of two digital LP DSMs processing the digital baseband in-phase (I) and quadrature (Q) data. An upconversion function is performed by the output multiplexers. The first row of multiplexers performs convolution of the I(n) and Q(n) signals with square-waves at the carrier frequency shifted by \( \pi / 2 \) with respect to each other. The last multiplexer generates the 1-bit pulse train signal \( s_{\text{out}} \) at the carrier frequency \( f_C \) suitable for driving of an SMPA.

![Fig. 3.17. Fully digital quadrature pulse encoder from [30].](image-url)
The realization of a fully digital quadrature pulse encoder proposed in [30] was done by the authors with the help of an FPGA board and external multiplexers. The output frequency was chosen to be 2.4 GHz. The clock frequency of the LP DSMs is 300 MHz.

Simulations with a two-tone WCDMA test signal were conducted on this fully digital quadrature pulse encoder in the following configuration: \( f_C = 2.12 \text{ GHz} \)

\[ f_{DSM} = \{ f_C / 8; f_C / 4; f_C / 2; f_C \} \]. Both DSMs are based on a 3\(^{rd}\) order lowpass DSM architecture with coefficients described in [30]. The output spectra with \( f_{DSM} = f_C / 8 \) are shown in Fig. 3.18 (a) and zoomed around the carrier frequency in Fig. 3.18 (b). From the spectrum in Fig. 3.18 (a) it can be seen that a high selectivity filter would be required in the complete class-S PA in order to remove an upconverted quantization noise. The requirements to the reconstruction filter can be relaxed by increasing the DSM sampling frequency with respect to the carrier frequency. This is shown in Fig. 3.19 where the simulation with the same test signal was performed on the architecture with \( f_{DSM} = f_C / 4 \). The simulated spectrum is depicted in Fig. 3.19 (a) and the zoomed spectrum in a 60 MHz bandwidth around the carrier frequency is shown Fig. 3.19 (b)

![Fig. 3.18. Output spectrum of the fully digital quadrature pulse encoder from [30] at \( f_{DSM} = f_C / 8 \) driven by a 2-channel WCDMA modulated carrier (a) from DC to \( 2f_C \); (b) at \( f_c \) with a 60 MHz span.](image)
As was shown in Chapter 2, in order to maximize efficiency and power, an SMPA has to be driven by a periodic input signal with 50% duty cycle. Considering the pulse statistic of the discussed architecture, it can be noted that more than 90% of the output periods have a duty cycle of 50% if an architecture with $f_{DSM} = f_c / 8$ is considered (Fig. 3.20 (a)). This fact makes it possible to use the digital IQ upconverter not only for driving of a class-D PA but also class-E or class-F PAs to transmit non-constant envelope signals.

Fig. 3.19. Output spectrum of the fully digital quadrature pulse encoder from [30] at $f_{DSM} = f_c / 4$ driven by a 2-channel WCDMA modulated carrier (a) from DC to $2f_c$; (b) at $f_c$ with a 60 MHz span.

Fig. 3.20. Pulse width statistic (a) for a $f_{DSM}=f_c/8$ (b) probability of the pulse widths of $T_c/4$ and $T_c/2$ vs. sampling frequency in DSMs.
Fig. 3.20 (b) shows the pulse width probability for different DSM sampling frequencies. From the pulse statistic point of view, the lower the DSM sampling frequency with respect to the carrier frequency the more half period pulses are in the pulse train. Thus, by choosing the DSM sampling frequency, it is possible to find a compromise between the selectivity of a reconstruction filter and the pulse statistics. However, the coding efficiency of the discussed pulse encoder is low for a given test signal and it is independent from the DSM sampling frequency. Table 3-2 shows the simulated performance comparison of two fully digital pulse encoders with $f_{DSM} = f_c / 8$ and $f_{DSM} = f_c / 4$ [30]. The pulse encoder with $f_{DSM} = f_c / 4$ shows better performance in terms of ACLR because the DSMs are clocked at a higher sampling frequency. On the other hand, its power consumption will be higher compared to the encoder with $f_{DSM} = f_c / 8$.

Table 3-2. Performance comparison of the fully digital pulse encoders from [30].

<table>
<thead>
<tr>
<th>$f_{DSM}$</th>
<th>CEff,%</th>
<th>$f_{AVG}$ / $f_c$</th>
<th>$t_{ON}$,%</th>
<th>ACLR, dB</th>
<th>$p(T_c/2)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{DSM} = f_c / 8$</td>
<td>2.8</td>
<td>1</td>
<td>0.5</td>
<td>-18.1</td>
<td>0.92</td>
</tr>
<tr>
<td>$f_{DSM} = f_c / 4$</td>
<td>2.8</td>
<td>1</td>
<td>0.5</td>
<td>-26.2</td>
<td>0.85</td>
</tr>
</tbody>
</table>

In [25], another fully digital quadrature pulse encoder architecture was proposed and implemented. I and Q signals are encoded by means of the digital PWM and upconverted to the carrier in the digital domain. Then, the upconverted I and Q signals are supposed to drive two corresponding SMPAs. The drawback of such an approach is that the signal combining happens after the SMPAs which may lead to a significant efficiency drop. The fully digital upconverting pulse encoder in [25] is dedicated for WLAN standard where ACLR requirements are in the range from -28 dBc to 20 dBc [87] which is not as stringent as in mobile communications. The pulse encoder demonstrates good measured EVM values. Unfortunately, the authors didn’t provide enough information for including this fully digital upconverting pulse encoder into a comparison.
3.4.2 Upconverting polar pulse encoder

Polar modulation is another approach to generate an upconverted 1-bit driving signal in the digital domain from the baseband signal. The research in the area of polar pulse encoders for an SMPA began in 2003 by Y. Wang, who proposed to combine an amplitude signal with a phase-modulated carrier resulting in a digital RF modulated carrier (a pulse train) [21]. Fig. 3.21 shows a general block diagram of a polar pulse encoder. The envelope signal $A(t)$ is processed by a lowpass DSM and the phase-modulated carrier is quantized by a limiter. The delay element is needed to compensate for the propagation delay between the clock input and the output of the LP DSM. The combining of the envelope signal and the phase-modulated carrier is realized by means of an AND-gate [24].

![General block diagram of a polar pulse encoder.](image)

To estimate the performance of the polar pulse encoder, the same 2-channel WCDMA signal as in the previous cases has been applied to the input. A 2nd order lowpass DSM clocked by phase-modulated square-wave was used in simulation. The delay is set to zero because of the ideal DSM model. The simulated output spectrum of the polar pulse encoder is shown in Fig. 3.22 (a) and (b).
The coding efficiency is calculated to be 17.5%. The switching requirements are highly relaxed because the output signal $s_{out}$ will switch only if the output of the LP DSM is high. The simulated average frequency is only $0.29 f_c$ which will result in decreasing of switching losses (section 2.1.2) in context of a class-S system. The ACLR is simulated to be -39.8 dBc, which is not enough to fulfill the specification requirements given in section 3.1. However, the ACLR could be improved to some extent by using a multibit envelope encoder as proposed in [88].

3.5 Conclusion

The pulse encoder is a very important part of the class-S PA, because its properties have a direct impact on the switching requirements to the SMPA, on the utilization of the power device and on the reconstruction filter requirements. Table 3-3 summarizes the performance of different pulse encoder architectures driven by a two-channel 10 MHz WCDMA signal with 9.9 dB PAPR, as simulated in this chapter.

The direct frequency conversion RF-PWM pulse encoder shows the best coding efficiency among all considered pulse encoder architectures. However, in order to amplify 90% of all pulses without distortion, an RF-PWM driven SMPA has to process pulses which
are up to 20 times narrower than the carrier period. This makes the RF-PWM pulse encoder not applicable at GHz carrier frequencies. On the other hand, for a direct frequency

Table 3-3. Simulative performance comparison of pulse encoder architectures with a two-channel WCDMA signal at the input

<table>
<thead>
<tr>
<th>Encoder</th>
<th>CEff, %</th>
<th>$f_{\text{avg}} / f_c$</th>
<th>$t_{\text{on}}, %$</th>
<th>ACLR, dBc</th>
<th>EVM, %</th>
<th>Pulse width with max. probability</th>
<th>PA class</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>3.6</td>
<td>1.7</td>
<td>0.5</td>
<td>-55.5</td>
<td>&lt; 1.5</td>
<td>0.31 Tc</td>
<td>D</td>
</tr>
<tr>
<td>RF-PWM</td>
<td>24.2</td>
<td>1</td>
<td>0.09</td>
<td>-57.8</td>
<td>&lt; 1.5</td>
<td>0.08 Tc</td>
<td>D</td>
</tr>
<tr>
<td>bandpass DSM</td>
<td>4.4</td>
<td>1</td>
<td>0.5</td>
<td>-63.5</td>
<td>&lt; 1.5</td>
<td>0.25 Tc</td>
<td>D</td>
</tr>
<tr>
<td>Polar</td>
<td>17.5</td>
<td>0.29</td>
<td>0.1</td>
<td>-39.8</td>
<td>&lt; 1.5</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
<tr>
<td>Dig. IQ*</td>
<td>2.8</td>
<td>1</td>
<td>0.5</td>
<td>-26</td>
<td>5.8</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
</tbody>
</table>

$* f_{\text{DSM}} = f_c / 4$

conversion bandpass DSM-based SMPA, the minimum pulse length at the input of an amplifier is just one clock period, which is a substantially less demanding constraint on the $f_T$ of the PA. Therefore, a bandpass DSM is the obvious choice as a direct conversion encoder in a class-S PA at GHz frequencies. However, already at 2.2 GHz, the standard $f_s / 4$ -architecture would generate pulses with a minimum pulse width of 113 ps. If in such configuration the state-of-the-art GaN power transistors with 65/55 ps rise/fall times [49] are used, then an SMPA will not be able to switch completely in the on/off states during all occurrences of the minimum pulse width. Thus, a bandpass DSM architecture with reduced sampling frequency is required.

One of the main advantages of the polar pulse encoder is a generation of the output pulse train which contains only pulses with a pulse width of $T_c / 2$. This extends the choice of SMPA to class-E or class-F configurations in the class-S system. Also the coding efficiency of the polar pulse encoder is much better compared to the fully digital IQ upconverter. However, known realizations [24], [88] of the polar pulse encoders are not fully digital.

A fully digital polar pulse encoder would allow a multi-standard multiband transmitter and is another research topic in this thesis which is discussed in Chapter 6.
Chapter 4. RF Bandpass Delta-Sigma Modulator Design

Within the scope of this work, several bandpass DSMs at 450 MHz, 900 MHz and 2.1-2.2 GHz center frequency have been designed. The maximum data rate of the transistor used in class-S PA sets the upper limit for the bandpass DSM sampling frequency. At the beginning of the work, this limit was 2.2 GS/s which allowed a straightforward implementation of a bandpass DSM at $f_c = 450$ MHz center frequency [46] based on the $f_s/4$ -architecture. At $f_c = 900$ MHz center frequency, the bandpass DSM sampling frequency had to be set to this limit at 2.2 GHz [43]. The design was based on the non-$f_s/4$ -architecture with numerical optimization of the feedback coefficients. The developed bandpass DSMs at 450 and 900 MHz were successfully assembled into a corresponding class-S PAs [32], [42].

The realization of a class-S PA module at $f_c = 2.1$-2.2 GHz with the available GaN transistor posed a big challenge. An exploration of the bandpass DSM performance at 2.1-2.2 GHz center frequencies resulted in a bandpass DSM implementation based on the $f_s/4$ -architecture with a sampling frequency of 9 GS/s [44]. Another investigated approach was to use the output of the 900 MHz bandpass DSM at the first image frequency. By setting the sampling frequency of this bandpass DSM at 3.1 GHz, one can obtain the mirrored modulated signal centered at the 2.2 GHz carrier frequency [48]. This, of course, essentially reduces the output data rate of the bandpass DSM but it still did not allow to use the available GaN transistors. Another drawback of this approach is that the output power of a class-S PA is significantly reduced because of low coding efficiency.

Finally, the solution for the 2.1-2.2 GHz class-S PA was enabled by technology. A GaN power transistor with rise/fall times of 55/65ps was developed and characterized [49]. This allowed extending the limit for the sampling frequency for a bandpass DSM up to 5 GHz. Consequently, a non-$f_s/4$ center frequency 5 GS/s 2.1-2.2 GHz bandpass DSM [45], [50] has been developed on the established DSM design procedure. This design is discussed in detail in this chapter.
4.1 System design

In this thesis, a design procedure of a continuous time non-$f_s/4$ center frequency bandpass DSM for decreasing of the sampling frequency is proposed. In general, it can be described as follows:

1. Find an $f_s/4$ NTF($z$) by using standard filter design technique.
2. Determine system parameters of a variable center frequency DT prototype by using the NTF($z$) found at the previous step.
3. Find a loop filter transfer function $H(z)$ for the determined DT prototype.
4. Perform a transformation of a loop filter transfer function $H(z)$ in $z$-domain to the $s$-domain $H(s)$.
5. Map $H(s)$ to an appropriate circuit-level architecture.

Modeling a circuit on transistor level would lead to a long-time transient simulation compared to the system model. System level design benefits by simulation time but does not provide sufficient simulation accuracy to predict the signal quality parameters. On the other hand, a transistor level simulation takes into account realistic effects. Only the synergy of both approaches can lead to the most efficient design flow. The overall design procedure followed in this thesis is schematically shown in Fig. 4.1.

![Fig. 4.1. Block diagram of a CT bandpass DSM design procedure.](image)

The NTF for the $f_s/4$-bandpass DSM has been synthesized with help of Schreier’s Matlab toolbox [90] having an out-of-band gain of 1.6 for a single bit 4th order DSM:

$$NTF_{f_s/4}(z) = \frac{z^4 + 2z^2 + 1}{z^4 + 1.114z^2 + 0.386}$$  (4.1)

The DSM in Fig. 4.2 realizes a variable center frequency 4th order DT bandpass modulator based on two tunable resonators adjusted to the same center frequency.
CHAPTER 4. RF BANDPASS DELTA-SIGMA MODULATOR DESIGN

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Fig. 4.2. DT prototype of a variable center frequency bandpass DSM.

A tunable resonator $H_R(z)$ is expressed as

$$H_R(z) = -\frac{az + 1}{z^2 + 2az + 1},$$

(4.2)

where $a$ is the tuning parameter between -1 and 1, resulting in the resonance frequency changing from DC to $f_s/2$ [91].

The NTF of the architecture in Fig. 4.2 can be derived as

$$NTF(z) = \frac{(z^2 + 2az + 1)^2}{(z^2 + 2az + 1)^2 + c_1c_2(az + 1)^2 - c_2(az + 1)(z^2 + 2az + 1)}$$

(4.3)

Since the out-of-band gain at DC and $f_s/2$ is independent of the tuning parameter $a$, it is possible to calculate the parameters $c_1$ and $c_2$ by setting $a = 0$ in (4.3) [91]. Comparing the NTF in (4.3) at $a = 0$ to (4.1) and solving for $c_1$ and $c_2$ yields to $c_1 = 0.307$ and $c_2 = 0.886$.

For the required 5 GS/s and 2.1-2.2 GHz bandpass DSM, in the DT prototype in Fig. 4.2, the parameter $a$ has to be varied from 0.875 to 0.93. The center frequency of the WCDMA downlink bandpass DSM is equal to 2.14 GHz which corresponds to $a = 0.899$ in the DT model.

The loop filter transfer function $H_{LF}(z)$ of the DT prototype at $a = 0.899$ can be described as

$$H_{LF}(z) = \frac{0.784z^3 + 2.061z^2 + 1.871z + 0.614}{z^4 + 3.54z^3 + 5.133z^2 + 3.54z + 1}$$

(4.4)

The DT prototype in Fig. 4.2 with $c_1 = 0.307$, $c_2 = 0.886$ and $a = 0.899$ has been simulated. Fig. 4.3(a) shows a corresponding simulated SNDR as a function of the input signal amplitude $V_{in}$ related to a full-scale sinewave amplitude $V_{max}$. In Fig. 4.3(b), the output spectrum of the simulated DT prototype at half-scale input signal is shown.
Fig. 4.3. DT prototype simulation at $a = 0.899$: (a) SNDR as a function of the input signal level; (b) output spectrum at a half-scale input signal.

Fig. 4.4 demonstrates the variable center frequency operation of the DT prototype in Fig. 4.2 by controlling only the one parameter $a$ in a DT resonator. The coefficients $[c_1 \ c_2]$ are fixed for all simulations and equal to [0.307 0.886].

Fig. 4.4. Simulated spectrums of the DT prototype over parameter $a$. 
4.2 DT-CT conversion

At the next step, the corresponding CT architecture and its parameters have to be found based on the DT prototype loop filter transfer function. To determine an equivalent CT DSM, the impulse response of the CT and DT DSM loops at the sampling points have to be the same [92].

First, let us consider the mapping of a DT resonator to the CT domain. Setting \( a \) to zero in the resonator transfer function (4.2) corresponds to a resonator with a center frequency at \( f_s/4 \). Performing the impulse invariant transformation to a feedback path marked in Fig. 4.2, the corresponding transfer function in the CT domain can be found

\[
H_R(s) = L\left\{ Z^{-1}\left[ \frac{-z^{-2}}{1 + z^{-2}} \right] \right\} = \frac{\pi / 4(s - \pi / 2)}{s^2 + (\pi / 2)^2},
\]

where \( T_s \) is the sampling period, \( n \) is the sampling index.

On the other hand, in the CT domain, a non-ideal resonator is described by the transfer function:

\[
H_R(s) = \frac{As}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2},
\]

where \( \omega_0 \) is the center frequency, \( Q \) is the quality factor of the resonator and \( A \) is a constant gain factor described by

\[
A = G\frac{\omega_0}{Q},
\]

where \( G \) is the resonator gain.

For high enough resonator quality factor, the denominators of equations (4.5) and (4.6) are equal, however it is still not possible to equalize the nominators because of the constant term in (4.5). In [85], by introducing two feedback paths with different pulse types (RZ and HRZ in this case) instead of one NRZ, it is possible to perform the equivalent DT-CT mapping for resonators. The equivalent CT resonator is shown in Fig. 4.5.
The most commonly used DACs incorporate feedback pulses of three types: non-return-to-zero (NRZ), return-to-zero (RZ) and half-delayed return-to-zero (HRZ) (Fig. 4.6). Equations (4.8)-(4.10) describe corresponding transfer functions of the DACs.

\begin{align*}
D_{NRZ}(s) &= \frac{1-e^{-sT_s}}{s} \\
D_{RZ}(s) &= \frac{1-e^{-sT_s/2}}{s} \\
D_{HRZ}(s) &= e^{-sT_s/2}\frac{1-e^{-sT_s/2}}{s}
\end{align*}

(4.8) (4.9) (4.10)

In order to find coefficient values in Fig. 4.5, a pulse invariant transform has to be performed for the block diagram in Fig. 4.5 and for the inner loop marked in Fig. 4.2 which contains the multiplication factor \( c_2 \) and a variable frequency resonator \( H_R(z) \). The corresponding equation can be written as

\[ L^{-1}\left\{ H_R(s)\left[ k_{2R}D_{RZ}(s) + k_{2H}D_{HRZ}(s) \right] \right\}_{t=nT_s} = Z^{-1}\{ H_R(z) \}. \]

(4.11)

Solving equation (4.11) for \( H_R(z) \), one obtains the following expression
\[ H_R(z) = \frac{-a}{z^2 + 2az + 1} \left( k_{2H} b_{H1} + k_{2R} b_{R1} \right) + \frac{-1}{z^2 + 2az + 1} \left( k_{2H} b_{H0} + k_{2R} b_{R0} \right), \tag{4.12} \]

where the \( k_{2H} \) and \( k_{2R} \) are unknown. Equalizing the numerator of (4.12) to the numerator of (4.2), the coefficients \( k_{2H} \) and \( k_{2R} \) can be found. This shows that a DT variable frequency resonator described by (4.2) can be explicitly represented by a CT resonator tuned to the same frequency and by two feedback paths with different pulse types.

Fig. 4.7 shows a CT \( f_s/4 \) bandpass DSM architecture. In a similar way, by respectively mapping feedback loops containing both resonators in Fig. 4.2 and in Fig. 4.7 and omitting the feedback paths to the 2\(^{nd}\) summing point, it is possible to determine the coefficients \( k_{4H} \) and \( k_{4R} \).

Thus, the DT prototype in Fig. 4.2 can be mapped onto the \( f_s/4 \)-architecture in Fig. 4.7.

### 4.3 Compensation for excess loop delay

Because of the circuit level realization, an excess delay (ELD) between the output of the quantizer and DAC output results in one sample delay \( T_s \). This ELD has also to be accounted for in the DT loop filter transfer function (4.4) by increasing its numerator order by one. In this case, a new loop filter transfer function cannot be mapped to the architecture in Fig. 4.7. In other words, four feedback coefficients provide not enough degrees of freedom to
equalize the loop filter functions in the presence of one sample ELD. To compensate this additional sample delay, another feedback path has to be added. The fifth feedback path has been realized by an NRZ DAC, which is connected from the delayed output of the comparator directly to the comparator input [93]. Thus, the DT prototype (Fig. 4.2) including one sample delay can be explicitly mapped on the CT model in Fig. 4.8.

![Fig. 4.8. CT variable frequency bandpass DSM architecture compensating one sample excess loop delay](image)

Performing pulse invariant transformation for all feedback paths and solving corresponding equations, the parameters of the CT model in Fig. 4.8 at $f_S=1$ can be found. The signal path parameters and feedback coefficients can be determined as $[b_2, b_3, b_4] = [14.061, 0.886, 1]$ and $[k_{4r}, k_{4h}, k_{2r}, k_{2h}, k_n] = [16.322, -2.260, 8.970, -4.731, 0.786]$, respectively. The quality factor of both resonators is set to 150. The model in Fig. 4.8 is simply scalable by changing the center frequency $\omega_0$ in the resonator transfer function and the sampling frequency $f_S$. Thus, scaling of the center frequency does not require any recalculation of the model parameters.

Fig. 4.9(a) compares the simulated SNDR curve of the obtained CT model with a corresponding DT prototype as a function of input signal amplitude $V_{in}$ related to the full-scale sinewave amplitude $V_{max}$. The output spectrum of the simulated DT prototype at half-scale input signal is shown in Fig. 4.3(b).
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Fig. 4.9. CT DSM simulation at $f_c=2.14$ GHz: (a) SNDR (BW=10 MHz) as a function of the input signal level with $Q=150$ and $Q=70$ in both resonators; (b) output spectrum at half-scale input signal.

The model in Fig. 4.8 can demonstrate the variable center frequency operation by setting the center frequency in resonators and 8 parameters [$b_1, b_2, b_3$] in the signal and [$k_{r1}, k_{r2}, k_{s1}, k_{s2}$] in the feedback paths. Simulated output spectrums and corresponding model parameters of the CT model obtained from the DT prototypes (Fig. 4.2) with $a = [-0.6, 0.2, 0.9]$ are shown in Fig. 4.10.

Fig. 4.10. Simulated spectrums of the CT prototypes derived from the DT prototype (Fig. 4.2) at $f_c=5$ GHz with $a=[-0.6, 0.2, 0.9]$. 
Since the variation of the design parameters given in Fig. 4.10 for different center frequencies is very high, a robust design realizing the variable center frequency function is not achievable. Therefore, only a set of parameters which corresponds to the center frequency of 2.14 GHz has been chosen for the circuit-level CT bandpass DSM realization.

### 4.4 System to circuit mapping

An equivalent circuit-level model of a non-\(f_s/4\) center frequency LC bandpass DSM is shown in Fig. 4.11. Before starting with the system to circuit mapping procedure, resonator parameters in this model have to be determined. The transfer function of a real LC-resonator can be described in the CT-domain as

\[
H_r(s) = \frac{Gm}{C} \frac{s}{s^2 + Xs + \omega_0^2},
\]

where \(Gm\) is the transconductance of a resonator, \(C\) is the tank capacitance, and \(X=\omega_0/Q\) where \(\omega_0\) is the center frequency, \(Q\) is the quality factor of a resonator. The initial values of \(Gm\), \(Q\) and \(C\) have to be determined from the circuit design of a resonator. Then, based on the system model in Fig. 4.8, the parameters of the equivalent circuit-level model from Fig. 4.11 can be found.

**Fig. 4.11. Circuit-equivalent model of a non-\(f_s/4\) center frequency LC bandpass DSM.**

The full-scale sinewave amplitude is determined by the maximum amplitude of the resonator input signal \(V_{max}\). Therefore, knowing the resonator’s transconductance \(Gm_1\), the sum of the feedback transconductances at the 1\(^{st}\) summing point can be found from [92]:

\[
Gm_1 = \frac{s / C}{s^2 + Xs + \omega_0^2},
\]

\[
Gm_2 = \frac{s / C}{s^2 + Xs + \omega_0^2},
\]

\[
Gm_3 = \frac{s / C}{s^2 + Xs + \omega_0^2},
\]

\[
Gm_4 = \frac{s / C}{s^2 + Xs + \omega_0^2},
\]

\[
Gm_5 = \frac{s / C}{s^2 + Xs + \omega_0^2},
\]
\[ 2Gm_1 V_{\text{max}} = (Gm_{4r} + Gm_{4h}) \Delta, \quad (4.14) \]

where \( \Delta \) is a quantization step.

The ratio of the transconductances \( Gm_{4r} \) and \( Gm_{4h} \) is the same as the ratio of the corresponding coefficients \( k_{4r} \) and \( k_{4h} \) in the system-level model. Thus, these transconductances can be found as

\[ Gm_{4r} = \frac{Gm_4}{1 + \frac{k_{4h}}{k_{4r}}} \quad (4.15) \]
\[ Gm_{4h} = \frac{Gm_4}{1 + \frac{k_{4r}}{k_{4h}}} \quad (4.16) \]

The transconductance \( Gm_2 \) can be found by equalizing the expressions for a feedback loop comprising both resonators:

\[ Gm_2 = k_4 A^2 C^2 / Gm_4. \quad (4.17) \]

From an expression for the feedback loop comprising the resonator that precedes the quantizer, the transconductances \( Gm_{2r} \) and \( Gm_{2h} \) can be determined:

\[ Gm_{2x} = k_{2x} AC, \quad (4.18) \]

where \( Gm_{2x} = [Gm_{2r}, Gm_{2h}] \), \( k_{2x} = [k_{2r}, k_{2h}] \).

The transconductances \( Gm_3 \) and \( Gm_n \) can be found from the components \( b_4 \) and \( k_n \), respectively, in the model in Fig. 4.8 by dividing them by \( R \).

After scaling the voltage swings at the input of \( Gm_2 \) and \( Gm_3 \), the final set of the circuit parameters with \( C = 1.17 \) pF, \( T_s = 200 \) ps and \( \omega_b = 1.344 \times 10^8 \) rad/s is obtained. The corresponding signal path parameters and feedback coefficients can be found as

\[ [Gm_1, Gm_2, Gm_3] = [2.8e-3, 8.9e-3, 2e-3] \quad \text{and} \quad [Gm_{4r}, Gm_{4h}, Gm_{2r}, Gm_{2h}, Gm_n] = [4.8e-3, 0.4e-3, 11.2e-3, 5.3e-3, 0.7e-3], \]

respectively. The simulated SNDR curve and spectrum for the circuit-equivalent model (Fig. 4.11) are the same compared to the system-level model (Fig. 4.8) and shown in Fig. 4.9.
4.5 Circuit design

All components of the bandpass DSM are realized fully differentially. The supply voltage for the bandpass DSM is chosen to be 3 V in order to keep the power consumption as low as possible. The bandpass DSM is designed and fabricated in a 0.25 um SiGe BiCMOS process (f_T=180 GHz) of IHP.

4.5.1 Resonator

The first stage in an LC bandpass DSM is a resonator, and thus the dynamic range of this resonator determines the dynamic range of the complete modulator. The minimum detectable input voltage is determined by the input-referred noise of the resonator, and the maximum input signal is limited by its linearity.

The complete resonator structure (Fig. 4.12) consists of two gm-cells and one LC tank, including varactors to control the resonant frequency of the LC tank. By tuning the voltage at the Vt node, it is possible to cover the needed frequency range of 2.11-2.17 GHz. To achieve better linearity, the main gm-cell Gm of the resonator was designed as a multi-tanh structure (Fig. 4.13) [94]. The linearity of the gm-cell can be controlled to some extent by unbalancing the differential pairs and by emitter degeneration. Since the supply voltage is 3 V, it is possible to effectively use only one diode in the emitter. Consequently, only the tail currents and the emitter area ratio between the left and the right side transistors were optimized.

![Fig. 4.12. Resonator block diagram including Q-enhancement gm-cell GmQ.](image-url)
For the main Gm-cell the emitter area $A_E$ of the unit transistor is $0.21 \times 0.84 \text{ um}^2$. The tail currents can be changed in the range from 0.8 mA to 1.5 mA. The simulated input-referred noise of the resonator yields to $18 \text{nV/}\sqrt{\text{Hz}}$, while the input amplitude corresponding to the 1 dB compression point is $120 \text{ mV}$. The calculation of the maximum achievable dynamic range leads to $66.5 \text{ dB}$ in $10 \text{ MHz}$ bandwidth.

The LC tank includes a symmetrical octagonal inductor and varactors to cover the WCDMA base station transmitter frequency range (2.11-2.17 GHz). The octagonal geometry has been chosen for the inductor because it introduces better quality factor compared to the square one [51]. The following approach was used to find the optimum octagonal inductor geometry in a given area:

1. The developed parameterized cell generates octagonal inductor geometry depending on parameters such as number of windings, spacing between windings, winding width, inner radius.

2. Create simulation test benches for different octagonal inductor geometries with corresponding electromagnetic simulator settings (start frequency, stop frequency, number of simulation points, technology metal stack)

3. Run a batch simulation on all created inductor geometries which results in a file with a list of the simulated datasets for each inductor structure.

4. Running a test bench that reads out the obtained datasets from the previous step and performs an S-Parameter simulation on all geometry structures to extract the corresponding inductance and quality factor values.

The mentioned procedure was implemented in Agilent ADS environment. Momentum was used as an electromagnetic simulator.
The resulting octagonal inductor geometry has an inductance of 4.7 nH at 2.1 GHz. Occupying an area of 220 x 220 µm², the optimized coil has a quality factor of only 12 at 2.1 GHz. Since a low quality factor of the tank highly degrades the SNR and could cause idle tones, it is necessary to compensate for the losses in the inductor. For this reason an additional gm-cell GmQ is connected in a positive feedback configuration as a quality factor enhancement [95]. It is based on the multi-tanh structure which is four times larger than the main Gm-cell and is capable to supply about 4 times the current of the main Gm-cell. A 1-to-4 capacitive divider is used at the input of the GmQ-cell to keep the resonator stable. The main Gm-cell has a control voltage for adjusting the Gm value. Fig. 4.14(a) shows the adjustable transconductance range as well as the Gm dependency on process variation. Another control voltage is implemented to control the tail current in the GmQ-cell which allows adjusting the quality factor of the resonance circuit. As can be seen from Fig. 4.14(b), the quality factor is highly sensitive to the technological process variations. Since an increase in Q-factor causes an increase in the resonator gain, the quality factor has to be kept as low as 70 for linear operation of the subsequent stage.

![Fig. 4.14. Process variation dependency of (a) transconductance; (b) Q-factor.](image)

On the system level, the resonator in Fig. 4.13 is described by (4.6). To complete the system level model, two parameters have to be extracted from the circuit: the gain factor $A$ and the quality factor $Q$. The latter can be found from simulation as a ratio between the resonance frequency and the 3-dB bandwidth. Assuming an operation at resonance and high quality factor, the constant gain factor equals to $A = \frac{Gm}{C}$, where $C$ is the tank capacitance.
When simulating bandpass DSM with the enhanced Q-factor of 70 (Fig. 4.14(b)), an SNDR degradation compared to the infinite Q case is then limited to around 8 dB.

4.5.2 Comparator and pulse forming circuits

The comparator used in the bandpass DSM consists of a preamplifier, master and slave NRZ latches. The schematic is shown in Fig. 4.15. An emitter follower provides an isolation of the preamplifier from switching in the master latch. Transistors in the emitter followers have an emitter area 4 times higher than the minimum size transistor. The transistors are biased for peak $f_T$ operation. The output swing is around 360 mV which is enough to completely switch the DACs. In the simulation, the comparator shows a sensitivity value of 1 mV at 15 GHz clock frequency.

![Comparator schematic](image)

In Fig. 4.16, the schematic used for the generation of the RZ pulses is shown. The cross-coupled latch transistors in the NRZ latch are replaced with the diode-connected transistors in the RZ latches [95]. The bias currents and transistor sizes have been chosen

![RZ latch schematic](image)
identical to the NRZ latch. The circuit in Fig. 4.16 can also generate HRZ pulses. By clocking
the latch in anti-phase, the RZ pulse is delayed by half of the clock period forming the HRZ
pulse at the output.

### 4.5.3 Feedback DAC

The current steering DAC is a differential pair (Fig. 4.17) based on the minimum size
bipolar transistors. The tail current can be controlled off-chip in order to set a wide range of
gm values up to 20 mS. A differential swing of 360 mVpp is enough to completely switch the
current between the outputs. The circuit in Fig. 4.17 can implement either negative or positive
value of a feedback coefficient, depending on how the output is connected to a summing
point. Fig. 4.18 shows the switching behavior of the DAC circuit when it is driven by RZ or
NRZ latch.

![Fig. 4.17. DAC schematic.](image)

![Fig. 4.18. Output current of the DAC driven by RZ latch (a) and NRZ latch (b).](image)
4.5.4 Clock and output buffers

A clock buffer converts a sinewave coming from the generator to the rectangular clock signal. The schematic of the clock buffer is shown in Fig. 4.19. The input biasing stage is chosen to provide a 50 Ohm input impedance at both inputs. The circuit comprises two cascaded differential pairs separated by an emitter follower to decrease rise/fall time of the output clock signal. The rise/fall time of the differential clock signal delivered by clock buffer is 14.6 ps. One clock buffer is used to provide the clock signal for all latches in the modulator. Input and output signals of the clock buffer, output being loaded by eight latches, are shown in Fig. 4.20.

A bandpass DSM has to deliver a 0.8 Vpp differential voltage swing to a subsequent SMPA stage. An output buffer has to be used to provide the required voltage swing. The schematic of the output buffer is shown in Fig. 4.21. As a clock buffer, the circuit consists of
two cascaded differential pairs. In order to decrease the power consumption of the output buffer, the collector resistors in the last stage are set to 120 Ohm compromising for the output impedance matching. At such condition, the bias current of 12.2 mA required to achieve the 0.8 Vpp differential voltage swing at 2x50 Ohm differential load. The simulated differential output signal is shown in Fig. 4.22.

---

**Fig. 4.21. Output buffer schematic.**

---

**Fig. 4.22. Modulator output signal at 2x50 Ohm differential load.**
4.5.5 Bandpass DSM circuit simulations

A complete circuit diagram of the 5 GS/s 2.1-2.2 GHz bandpass DSM is shown in Fig. 4.23. The blocks employ the schematics presented in the previous section.

For calculating SNDR with a standard deviation of ~1 dB, the number of simulated samples has to be 64·OSR [96]. Thus, for a 5 GS/s bandpass DSM and a 10 MHz input signal, the number of sampling periods used in the simulation is $2^{14}$. The architecture in Fig. 4.23 with the coefficients from section 4.4 has been simulated with transistor-level models. Fig. 4.24(a) shows the simulated SNDR as a function of input signal amplitude $V_{in}$ related to the full-scale sinewave amplitude $V_{\text{max}}$. In Fig. 4.24(b), the output spectrum of the simulated DT prototype at the input signal amplitude corresponding to the quarter of the full-scale is shown.
In the transistor-level DSM model (Fig. 4.23), the dynamic range is reduced compared to the circuit-equivalent model (Fig. 4.11) due to not enough linearity in the second resonator. To decrease the voltage swing at the input of the second resonator, adjusting $G_m$’s in the signal path and tuning of the feedback coefficients has been performed. The corresponding signal path parameters and feedback coefficients are determined as $[G_m, G_{m_2}, G_m] = [1.8e-3, 7.7e-3, 2.9e-3]$ and $[G_{m_1}, G_{m_3}, G_{m_2}, G_{m_4}, G_m] = [3.4e-3, 4e-3, 0.22e-3, 14e-3, 1.5e-3]$.

An obtained SNDR curve is shown in Fig. 4.25(a). Fig. 4.25(b) shows the simulated output spectrum at the input signal amplitude corresponding to half of the DSM full scale.
4.6 Estimation of non-idealities

The architecture from Fig. 4.23 with the circuit-level model parameters from the section 4.5.5 have been simulated against circuit non-idealities such as excess loop delay and jitter.

4.6.1 Excess loop delay

Excess loop delay (ELD) is an important parameter which degrades the performance of the CT bandpass DSM. In addition to the decision time of the quantizer, it is determined by the propagation delay between the quantizer output and the output of the DAC. The excess loop delay for the developed modulators has been estimated between nodes A and B as shown in Fig. 4.26. The $f_s/4$ bandpass DSM (Fig. 4.7) is immune to exactly one sample delay in the feedback path. However, it is very sensitive to delay that exceeds one sample [97]. In the variable center frequency CT modulator (Fig. 4.8), one sample delay was compensated by introducing an additional feedback path. The remaining part of the ELD is caused by the propagation time through the latches that is referred to as relative ELD.

The $f_s/4$-architecture incorporates RZ and HRZ pulses in the feedback, thus the relative ELD should be estimated in the paths AB₁ and AB₂. For the non-$f_s/4$ center

![Fig. 4.26. Estimation of excess loop delay.](image_url)
frequency modulator, the NRZ path was added and the relative ELD is estimated for all three paths AB<sub>1</sub>, AB<sub>2</sub> and AB<sub>3</sub>.

Circuit level simulations reveal that the difference between all three paths is below 0.5 ps which is less than 1% of the sampling period for a 9 GHz clock and a single delay component can be used to estimate the delay influence on the modulator performance. The simulated relative ELD is equal to 13 ps that correspond to 11.7% of the sampling period in the $f_s/4$ modulator clocked by 9 GHz frequency. This value would degrade the SNDR of the $f_s/4$ modulator up to 8 dB [97].

The impact of the ELD on the non-$f_s/4$ center frequency modulator performance was estimated by simulation of the transistor-level model. At first, the relative ELD was completely compensated by delaying the comparator clock relative to the clock signal of the feedback latches [98]. Then, the delay elements were inserted in front of all DACs. By changing the delay value and calculating the corresponding SNDR value in a 10 MHz bandwidth, the ELD impact on the modulator performance (Fig. 4.27) was obtained. In contrast to the $f_s/4$-architecture [97], a non-$f_s/4$ center frequency modulator can withstand delays up to 20% of the sampling period, having a slight degradation in performance.

![Fig. 4.27. Effect of the relative loop delay on SNDR in the 5 GS/s 2.2 GHz bandpass DSM.](image)

In the designed 5 GS/s non-$f_s/4$ center frequency CT bandpass DSM, the simulated relative ELD is 13 ps which correspond to 6.5% of the sampling period $T_s$. This value causes an SNDR degradation of only 1.6 dB. Thus, in the developed 5 GS/s 2.1-2.2 GHz DSM, the additional ELD has not been compensated.
CHAPTER 4. RF BANDPASS DELTA-SIGMA MODULATOR DESIGN

4.6.2 Jitter

In contrast to DT modulators, CT modulators are very sensitive to clock jitter [99]. Therefore, a jitter influence on the SNDR should be estimated as well. For this purpose, a set of clock signals with different jitter values based on the normal distribution have been generated. For testing of the prototype, a clock generator with 0.72 ps rms jitter at 5 GHz was available; thus, the value was included in the simulation as well. Fig. 4.28 plots the simulation results. The SNDR values were calculated for 16384 samples at Pin = -16 dBm in 10 MHz bandwidth. The SNDR curve as a function of the input signal is shown in Fig. 4.29 (a). If the jitter free source is used, the modulator achieves 64.8 dB SNDR. If the jittered source introduces the same amount of jitter as the real clock generator (0.72 ps), the bandpass DSM SNDR drops significantly to 48.8 dB (Fig. 4.29 (b)).

![Jitter vs SNDR](image1.png)

**Fig. 4.28.** Simulated SNDR dependence on the different clock jitter values [45].

![Output Spectrum](image2.png)

**Fig. 4.29.** Simulated output spectrum of the bandpass DSM with a clock source having a jitter of 0.72 ps: (a) SNDR as a function of the input signal level with Q=70 in both resonators; (b) output spectrum.
4.6.3 Metastability

The risk of a metastable output exists when the signal at the input of the comparator is small. This makes the comparator to take a long time to settle to a corresponding output level. If the comparator drives the DACs directly and the output level is not settled, this may result in incomplete switching and thus a reduction of the SNDR. One way to reduce metastability in the comparator is to use a preamplifier. On the other hand, cascading of latches reduces the metastability problem as well. In the designed bandpass DSMs, a comparator consists of master and slave latches as described in 4.5.2. Moreover, to form RZ and NRZ pulses two additional latches are used and to form HRZ pulses even three (Fig. 4.26). Thus, the signal in both bandpass DSM architectures passes through at least four latches before driving any DAC circuit. Therefore, the risk of metastability in the $f_s/4$-architecture and in the non-$f_s/4$ center frequency architecture due to its configuration is very low.

4.7 Conclusion

A design procedure of the non-$f_s/4$ center frequency LC CT bandpass DSM has been presented. It shows that the realization of the non-$f_s/4$ center frequency CT bandpass DSM is more complex than for its DT counterpart. The non-$f_s/4$ center frequency CT bandpass DSM requires up to 9 design parameters (the resonator center frequency and transconductance values) for realization of the given NTF, whereas in the variable center frequency DT DSM only one parameter has to be controlled.

The proposed design procedure implements further improvements:

- Avoiding additional transfer function conversion step for a DT prototype to implement variable center frequency operation as it is proposed in [89]. Instead, a simple variable frequency DT prototype with only one controlling parameter is used to implement CT bandpass DSM.
- When converting from a normalized sample frequency model to the real circuit model, no scaling of the feedback coefficients is needed. The obtained system level coefficients’ ratios can be directly used in the schematic.
Chapter 5. Bandpass DSM Implementations

At the beginning of this chapter, a measurement setup used for characterizing the bandpass DSMs at different input excitations will be presented. Then, the performance of the explorative bandpass DSM implementations dedicated for a 2.1-2.2 GHz input frequency range, which have not been used in the final demonstrator, are shortly presented and summarized. Finally, the implementation results of the 5 GS/s 2.1-2.2 GHz bandpass DSM that was used in the final class-S module are shown.

All bandpass DSM realizations are fabricated in a 0.25 um SiGe BiCMOS process ($f_T=180$ GHz) of IHP.

5.1 Measurement setup

Two measurement setups are used for all designed bandpass DSMs. The bandpass DSMs have been measured by applying different input signals to determine performance characteristics. For measuring SNDR and dynamic range a measurement setup in Fig. 5.1 controlled by a Matlab script is used. A 40 µs output signal with 25 ps resolution is captured by a real-time oscilloscope, when a sinewave is applied at the input. The Matlab script processes the downloaded data to find the modulator parameters such as average switching frequency, ON-state duration and pulse width statistic. Also, it performs an FFT to obtain the output spectrum and to estimate the SNDR in a given bandwidth. The SNDR measurement is repeated for a set of input amplitudes in order to determine the modulators’ dynamic range.

The measurement setup consists of

- a signal source to generate a sinewave input signal
- a signal source to generate the sinewave clock signal
- Two hybrid couplers to provide the differential input and clock signals
- a programmable DC supply for controlling of the feedback coefficients, the gain and quality factor of the resonators
- a real-time 40 GS/s 15 GHz oscilloscope to capture the output pulse train for further processing in Matlab
- a PC that controls the measurement equipment and performs the automated measurements and data processing by means of Matlab

All designed DSMs were bonded on a Rogers PCB with 0.5 mm thickness. SMA connectors are used for high frequency signals at the input, clock and output. One of such PCBs is shown in Fig. 5.12. For measuring the DSM parameters such as EVM and ACLR, the measurement setup in Fig. 5.2 is used.

Fig. 5.1. Measurement setup for a sinewave input.

Fig. 5.2. Measurement setup for applying and analyzing a communication signal.
This measurement setup consists of

- a vector signal generator (Agilent E4438C) to generate the modulated input signal
- a signal source to generate the sinewave clock signal
- Two hybrid couplers to provide differential input and clock signals
- a programmable DC supply
- a vector signal analyzer (Agilent 89600S) for EVM and ACLR measurements
- a PC that controls measurement equipment

5.2 Explorative DSM implementations

5.2.1 9 GS/s 2.1-2.2GHz bandpass DSM

Before the speed limitation of a power transistor in a class-S PA was extended [49], the bandpass DSM based on the $f_s/4$-architecture was developed and characterized at the required carrier frequencies in 2.1-2.2 GHz range. A very high output data rate of up to 9 GS/s makes it impossible to use this bandpass DSM implementation in a class-S PA module with existing power transistors. On the other hand, this implementation reveals the DSM capability to process real communication signals in terms of EVM and ACLR parameters. Fig. 5.3 shows the microphotograph of the bandpass DSM.

Fig. 5.3. Chip photo of the 9 GS/s 2.1-2.2 GHz bandpass DSM [44].
The modulator consumes 90 mA current from -3 V supply voltage. The chip was mounted on the Rogers RO4003 printed circuit board with a thickness of 0.51 mm. The SNDR has been measured in a 10 MHz bandwidth for a sinewave input at 2.1 and 2.2 GHz (Fig. 5.4 (a)). The output spectrum observed by means of a spectrum analyzer is shown in Fig. 5.4(b).

![Graphs showing SNDR and output spectrum](image)

**Fig. 5.4. 9 GS/s 2.1-2.2 GHz bandpass DSM measurements:** (a) SNDR in 10 MHz bandwidth; (b) output spectrum at 2.2 GHz input.

The performance summary is given in Table 5-1. The communication standard [68] requires to keep the EVM lower than 12.5 % when the base station is transmitting a composite signal that includes 16QAM modulation. The measured EVM of less than 2.3 % over the tuning range provides a solid margin for a complete class-S PA. The measured ACLR value of -42 dBc at 5 MHz is close to the required by the standard (-45 dBc at 5 MHz).

Further details on this implementation can be found in [44].
Table 5-1. 9 GS/s 2.1-2.2 GHz bandpass DSM performance summary.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.25 um SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Notch frequency range</td>
<td>2.05..2.22 GHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>9 GHz</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>-3 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>270 mW</td>
</tr>
<tr>
<td>Output swing, diff</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Chip area</td>
<td>1.4 mm²</td>
</tr>
<tr>
<td>DR</td>
<td>45 dB</td>
</tr>
<tr>
<td>SNDRmax BW = 10 MHz</td>
<td>42 dB @ 2.1 GHz</td>
</tr>
<tr>
<td></td>
<td>43 dB @ 2.2 GHz</td>
</tr>
<tr>
<td>EVM (QAM16)</td>
<td>2.3% @ 2.1 GHz</td>
</tr>
<tr>
<td></td>
<td>1.7% @ 2.2 GHz</td>
</tr>
</tbody>
</table>

5.2.2 900 MHz bandpass DSM

A 2.2 GS/s 900 MHz bandpass DSM [43] was developed to solve the speed limitation problem in the first generation of GaN transistors. Since there was no design procedure established for a non-\(f_s/4\) center frequency modulator, the system design of the 2.2 GS/s 900 MHz bandpass DSM has been done numerically and resulted in an architecture with three feedback paths which is depicted in Fig. 5.5. The schematics of the building blocks are based on the schematics presented in section 4.5.

Fig. 5.5. 900 MHz bandpass DSM architecture.
The chip microphotograph of the 900 MHz bandpass DSM is shown in Fig. 5.6. The 2.2 GS/s 900 MHz bandpass DSM was successfully incorporated in a 900Hz class-S demonstrator [32]

Fig. 5.6. Chip photo of the 900 MHz bandpass DSM (1x1.4 mm²) [43], [48].

The measured SNDR, coding efficiency and output spectrum of the 2.2 GS/s 900 MHz center frequency bandpass DSM is shown in Fig. 5.7

Fig. 5.7. 2.2 GS/s 900 MHz bandpass DSM measurements: (a) SNDR in 10 MHz bandwidth and coding efficiency; (b) output spectrum.

Another way to reduce the sampling frequency, which could be useful for a 2.2 GHz class-S PA, is to use the images of the output signal spectrum [100]. The first image of the signal appears at $f_{\text{OUT}}^1 = f_S - f_{RF}$, where $f_{RF}$ is an input frequency, and $f_S$ is the sampling frequency. The required signal at 2.2 GHz can be considered as the first image of the input
CHAPTER 5. BANDPASS DSM IMPLEMENTATIONS

signal. Since the input frequency range of the developed 900 MHz modulator is fixed in vicinity of 900 MHz due to LC resonators, then only the sampling frequency can be changed resulting in \( f_s = f_{RF} + f^1_{OUT} = 3.1 \) GHz. The image based class-S PA is shown in Fig. 5.8. The center frequency of the bandpass reconstruction filter must be set to 2.2 GHz. On the receiver side it has to be taken into account that the spectrum at the 1\(^{st}\) image frequency has to be mirrored to obtain the original transmitted signal.

\[
\begin{align*}
 f_{CLK} &= 3.1\text{GHz} \\
 f_{IN} &= 900\text{MHz} \\
 f_{RF} &= 900\text{MHz} \\
 f^1_{OUT} &= 2.2\text{GHz} \\
 f_{OUT} &= 2.2\text{GHz}
\end{align*}
\]

Fig. 5.8. Class-S PA architecture with the output at the 1\(^{st}\) image frequency.

Taking the output at the image frequency can highly relax the switching conditions to a power transistor. Compared to a bandpass DSM from section 5.2.1 based on the \( f_s/4 \)-architecture, the data rate at the image-based modulator output is reduced from 9 GS/s to 3.1 GS/s. However, very low coding efficiency at the image frequency even for a sinewave input makes this approach impractical for a class-S PA application.

The 900 MHz bandpass DSM (Fig. 5.6) has been characterized at the 2.2 GHz output frequency while clocked at 3.1 GHz. Fig. 5.9 the measured SNDR, coding efficiency and

\[
\begin{align*}
 &\text{SNDR} \quad \eta_C \\
 &\text{PSD, dBm/Hz} \quad 1\text{st image}
\end{align*}
\]

Fig. 5.9. 3.1 GS/s 900 MHz bandpass DSM measurements with the first image at 2.2 GHz: (a) SNDR in 10 MHz bandwidth at 2.2 GHz image frequency and coding efficiency; (b) output spectrum.
output spectrum of the 3.1 GS/s 900 MHz center frequency bandpass DSM at the 2.2 GHz output frequency.

The performance of the developed 900 MHz center frequency bandpass DSM at the 900 MHz output frequency and at the 2.2 GHz image frequency is compared in Table 5-2.

Further details on this implementation can be found in [43], [48].

Table 5-2. Performance summary of a 900 MHz input bandpass DSM

<table>
<thead>
<tr>
<th></th>
<th>OUT $f_o$, GHz</th>
<th>0.89-0.93</th>
<th>2.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s$, GHz</td>
<td>2.2</td>
<td>3.1</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage, V</td>
<td>-2.8</td>
<td>-3.1</td>
<td></td>
</tr>
<tr>
<td>$P_{DC}$, mW</td>
<td>380</td>
<td>435</td>
<td></td>
</tr>
<tr>
<td>Output swing, diff</td>
<td>0.8 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chip area</td>
<td>1.4 mm$^2$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sinewave signal input</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$SNR_{MAX}$ in 10 MHz, dB</td>
<td>43.8</td>
</tr>
<tr>
<td>$\eta_c$ @ $SNDR_{MAX}$, %</td>
<td>36.5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WCDMA signal input</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth, MHz</td>
<td>1.23</td>
</tr>
<tr>
<td>PAPR, dB</td>
<td>9.5</td>
</tr>
<tr>
<td>EVM, %</td>
<td>2.2</td>
</tr>
</tbody>
</table>
5.3 5 GS/s 2.1-2.2GHz bandpass DSM

Based on the established design procedure described in Chapter 4, a 5 GS/s 2.1-2.2 GHz bandpass DSM has been developed. The final circuit diagram was shown in Fig. 4.23. Schematics of the designed blocks were introduced in Chapter 4.

The modulator was fabricated in a 0.25 um SiGe BiCMOS process ($f_T=180$ GHz) with three thin and two thick metal layers. It consists of two LC resonators that can be tuned within the required frequency range. The circuit dissipates 330 mW from a -3 V supply voltage. A power distribution chart among different blocks is shown in Fig. 5.10.

![Fig. 5.10. Power distribution chart of a 5 GS/s 2.1-2.2 GHz bandpass DSM.](image)

The most power is dissipated by latches which is 37% of the total power dissipation. The power consumption of the DSM can be further reduced because the latches were not optimized for power dissipation at the given sampling frequency of 5 GS/s and have been reused from the 9 GS/s 2.1-2.2 GHz bandpass DSM design.

The microphotograph of the bandpass DSM is shown in Fig. 5.11. The chip occupies 1.32 mm$^2$ area and was mounted on the Rogers RO4003 50x50 mm$^2$ printed circuit board (PCB) with a thickness of 0.51 mm (Fig. 5.12). The output stage of the bandpass DSM delivers more than 0.8 Vpp differential voltage swing into a 50 Ohm load at each output. Such a voltage swing is required for the driver circuit of a GaN-based switch mode amplifier.
CHAPTER 5. BANDPASS DSM IMPLEMENTATIONS

Fig. 5.11. Chip photo of a 5 GS/s 2.1-2.2 GHz bandpass DSM (1.1 x 1.2 mm²) [45].

Fig. 5.12. 5 GS/s 2.1-2.2 GHz bandpass DSM mounted on a 50x50 mm² PCB.

For a sine wave input, the modulator performance was estimated by a two-tone test and SNDR measurements in a 10 MHz bandwidth. The modulator notch frequency was tuned to the input frequency. Fig. 5.13 shows the bandpass DSM output spectrum around 2.22 GHz for a two-tone intermodulation test. The two tones have amplitude of -30 dBm each and spaced by 2 MHz. Corresponding SFDR is 46.2 dB.

For the SNDR estimation, 40 µs of the output signal has been saved and used for FFT calculations.
CHAPTER 5. BANDPASS DSM IMPLEMENTATIONS

Fig. 5.13. Intermodulation test with two signals of -30 dBm each at 2.220 GHz and 2.222 GHz, respectively [45].

At the power level applied in simulation which correspond to -7.6 dB referred to the full-scale, the measured SNDR is equal to 43.1 dB. The corresponding output spectrum is shown in Fig. 5.14. For measuring the bandpass DSM dynamic performance, the input amplitude was changed and the corresponding SNDR values were measured. Fig. 5.15 compares the measured SNDR curve with the simulated one at 2.2 GHz input frequency. The simulation with the 0.72 ps jittered clock source has been performed.

At the measured SNDR value would drop to 48.8 dB in the 10 MHz bandwidth as shown in Fig. 5.15. A simulation of the parasitic extracted layout with the jittered clock source revealed an SNDR of 45.3 dB, which is very close to the measured result. The remaining difference between the

Fig. 5.14. Measured output spectrum of the 5 GS/s bandpass DSM; SNDR=43.1 dB (BW=10 MHz).

Accounting for the 0.72 ps jittered clock source used during the measurements, the expected SNDR value would drop to 48.8 dB in the 10 MHz bandwidth as shown in Fig. 5.15. A simulation of the parasitic extracted layout with the jittered clock source revealed an SNDR of 45.3 dB, which is very close to the measured result. The remaining difference between the
simulation and measurements of 2.2 dB is attributed to PCB imperfections and technology mismatches during the fabrication process.

![Graph showing SNDR vs Input Power with simulated and measured data.](image)

Fig. 5.15. Simulated and measured SNDR for 2.2 GHz sine wave input signal in 10 MHz bandwidth. Full-scale power level corresponds to -8.4 dBm.

The coding efficiency curve and corresponding bandpass DSM output power for the different input power levels are shown in Fig. 5.16. For the coding efficiency estimation, the total power in the output pulse train was calculated from the spectrum in the range from 0 to 2f_S.

![Graph showing Coding efficiency vs Input Power with measured data.](image)

Fig. 5.16. Measured output power and coding efficiency for 2.2 GHz sine wave input signal.
Fig. 5.17 shows the measured average output frequency $f_{AVG}$, which is normalized to the input frequency $f_{IN}$. For small input signals, $f_{AVG}/f_{IN}$ is equal to 0.75, however, for a real communication signal, the DSM should operate in the range where the $f_{AVG}/f_{IN}$ ratio is equal to 0.8-0.9. This is 10-20% better when compared to an $f_s/4$-architecture, for which the ratio $f_{AVG}/f_{IN}$ is approximately 1 for all input levels [101].

![Fig. 5.17. Measured average frequency of the modulator output.](image)

In order to test how the bandpass DSM can process real signals, a WCDMA signal has been applied as shown in Fig. 5.2, and the EVM and ACLR values were measured by the vector signal analyzer. The signal was generated according to the Test Model 5 [68]. This model is used to perform EVM measurements for base station transmitters. The used model configuration consists of 8 high-speed physical channels and 30 dedicated physical channels. Data in the high speed channels are modulated by 16QAM.

This configuration allows measuring the bandpass DSM under the most stringent conditions, since the peak-to-average ratio is maximal for such a signal and is equal to 11.5 dB. The WCDMA signal was generated by software and uploaded to a signal generator. Fig. 5.18 shows the bandpass DSM output spectrum including the first image at 2.8 GHz. The bandpass DSM notch is adjusted to 2.2 GHz frequency.
CHAPTER 5. BANDPASS DSM IMPLEMENTATIONS

Fig. 5.18. Measured 5 GS/s 2.1-2.2 GHz bandpass DSM output spectrum when WCDMA signal is applied to the input [45].

For EVM measurements, the bandpass DSM output signal was captured and analyzed using the vector signal analyzer. Fig. 5.19 shows the bandpass DSM measured output spectrum in 18 MHz bandwidth and the corresponding constellation diagram, when the WCDMA test signal is applied to the input.

Fig. 5.19. Measured bandpass DSM output spectrum of the WCDMA signal modulated by QAM16 and corresponding constellation diagram; Pin = -16 dBm; measured EVM$_{\text{rms}}$ = 1.8% [45].

The communication standard [68] requires to keep the EVM not higher than 12.5% when the base station is transmitting a composite signal that includes 16QAM modulation. The measured EVM of less than 2.1% over the tuning range provides a solid margin for a complete SMPA. The bandpass DSM shows ACLR values of -42.4 dBc at 5 MHz and
-44.4 dBc at 10 MHz offsets, whereas the standard [68] requires -45 dBc at 5 MHz offset and -50 dBc at 10 MHz offset. The ACLR could potentially be improved by means of integrating a low-jitter frequency synthesizer and/or by improving linearity of the resonator in expense of additional power.

Table 5-3 summarizes the measured characteristics of the developed bandpass DSM.

Table 5-3. 5 GS/s 2.1-2.2 GHz bandpass DSM performance summary.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.25 µm SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{OUT}$ range, GHz</td>
<td>2.1-2.2</td>
</tr>
<tr>
<td>$f_s$, GHz</td>
<td>5</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>-3 V</td>
</tr>
<tr>
<td>$P_{DC}$, mW</td>
<td>330 mW</td>
</tr>
<tr>
<td>Output swing, diff</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Chip area</td>
<td>1.1 x 1.2 mm²</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sinewave signal</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$\eta_e @ SNDR_{MAX}$, %</td>
<td>51.5</td>
</tr>
<tr>
<td>SFDR, dB</td>
<td>46.2</td>
</tr>
<tr>
<td>$SNDR_{MAX}$ in 10 MHz, dB</td>
<td>47.1 @ 2.1 GHz</td>
</tr>
<tr>
<td></td>
<td>46.6 @ 2.2 GHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WCDMA signal</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM (WCDMA), %</td>
<td>2.1% @ 2.1 GHz</td>
</tr>
<tr>
<td></td>
<td>1.8% @ 2.2 GHz</td>
</tr>
<tr>
<td>ACLR ($f_c=2.2GHz$), dBc</td>
<td>-42.4 @ 5 MHz</td>
</tr>
<tr>
<td></td>
<td>-44.4 @ 10MHz</td>
</tr>
</tbody>
</table>

Table 5-4 introduces a comparison of this work with existing bandpass DSM realizations at a center frequency of more than 2 GHz. The figure of merit (FoM) is calculated as

$$\text{FoM} = 2^{\text{ENOB}} \times 2\text{BW} / P_{DC},$$  \hspace{0.5cm} (5.1)
where ENOB is the effective number of bits.

The best FoM results are demonstrated by modulators from [102] and [103]. In [103], six interleaved quantizers sampled at 6.1 GHz are used to relax speed requirements. However, after multiplexing, the output is sampled at 36.6 GS/s. In [102] the output is sampled at 40 Gb/s.

In both cases the minimum pulse width at the modulator output is very short, which requires power transistors with higher transit frequencies to keep power efficiency competitive [49].

Table 5-4. Performance comparison of bandpass DSMs with the center frequency above 2 GHz.

<table>
<thead>
<tr>
<th>Reference</th>
<th>[102]</th>
<th>[103]</th>
<th>[104]</th>
<th>[44]*</th>
<th>[45]*</th>
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</thead>
<tbody>
<tr>
<td>$f_{IF}$, GHz</td>
<td>2</td>
<td>2.4</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>$f_s$, GHz</td>
<td>40</td>
<td>6.1</td>
<td>7.5</td>
<td>9</td>
<td>5</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13µm SiGe</td>
<td>40nm CMOS</td>
<td>0.18µm SiGe</td>
<td>0.25µm SiGe</td>
<td>0.25µm SiGe</td>
</tr>
<tr>
<td>SNDR, dB</td>
<td>55</td>
<td>41</td>
<td>45.5</td>
<td>43</td>
<td>46.6</td>
</tr>
<tr>
<td>BW, MHz</td>
<td>60</td>
<td>80</td>
<td>20</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$P_{DC}$, mW</td>
<td>1600</td>
<td>52.8</td>
<td>1060</td>
<td>270</td>
<td>330</td>
</tr>
<tr>
<td>FoM, GHz/W</td>
<td>34.4</td>
<td>277</td>
<td>5.8</td>
<td>8.5</td>
<td>10.5</td>
</tr>
</tbody>
</table>

*This work
5.4 Conclusion

In this chapter, three silicon realizations of bandpass DSMs have been presented. The first design is a straightforward implementation at 2.1-2.2 GHz input frequencies based on the $f_s/4$-architecture. This bandpass DSM realization cannot be incorporated into a class-S PA system because of high sampling frequency, but it gives insight to how the DSM can process real communication signals at required center frequencies.

The second trial to obtain a pulse encoded signal at 2.1-2.2 GHz was based on the 900 MHz center frequency bandpass DSM design which was incorporated in a 900Hz class-S demonstrator [32]. This implementation has been used as a frequency converter in order to provide signal conditioning at 2.2 GHz by means of changing the clock frequency to 3.1 GHz. However, low coding efficiency makes this approach not applicable to a class-S PA.

In the meantime, a GaN switch developed by the project partners [49] extended the upper bit rate limit from 2.2 GS/s to 5 GS/s. At such condition, it was possible to design the third, a non-$f_s/4$ center frequency bandpass DSM clocked at 5 GHz and having an input at 2.1-2.2 GHz. This DSM has been successfully incorporated in a 2.1-2.2 GHz class-S PA system.

All modulators have been tested by applying a real communication signal and showed good margin in EVM values. However, to fulfill the specification in terms of ACLR, the SNDR would have to be improved. This could be achieved by means of integrating a low-jitter frequency synthesizer (e.g. [105]) and/or by improving linearity of the resonator in expense of additional power.
Chapter 6. Fully digital polar modulator for class-S amplifier

One of the main goals in the development of modern communication systems is to design reconfigurable transceivers which can transmit signals - if not all - but of several communication standards. Digital circuits are known to be highly reconfigurable. Therefore, developing a reconfigurable pulse encoder for a switch-mode power amplifier could be the next step towards a multi-standard transmitter.

As it has been previously discussed, high efficiency can be achieved if the driving signal of any SMPA class is a periodic square-wave signal. The development of such a modulation technique, which encodes the data in the pulse train such that all pulses have a width of a half period, is very attractive and has been investigated by many researchers [20, 24, 30]. Only the pulse modulation technique proposed in [30] presents a fully digital encoder; however it suffers from low coding efficiency. In this chapter, another fully digital encoder type is presented, which is based on the polar modulation (section 3.4.2). The performance of the proposed modulator is demonstrated on driving a class-F amplifier which was designed by project partners.

6.1 Operation principle

The digital polar modulator (DPM) architecture is depicted in Fig. 6.1. It consists of two lowpass DSMs: LP DSM_A and LP DSM_P, for processing of the amplitude and phase signals, respectively; a multi-phase generator (MPG) for generating a set of phase-shifted square-wave carrier signals; a multiplexer for constructing an approximated phase-modulated square-wave carrier signal; and an AND-gate for combining the multiplexer output and an output signal of the LP DSM_A. At the input, the DPM requires digital baseband amplitude and phase signals. These signals can be obtained from I and Q signals by means of the CORDIC algorithm preserving the use of the conventional baseband transceiver part.
CHAPTER 6. FULLY DIGITAL POLAR MODULATOR FOR CLASS-S AMPLIFIER

The target transmit signal after the power amplifier (PA) can be written as

\[ s_{\text{TX}}(t) = A(n) \cdot \sin(\omega_c t + \phi(n)), \tag{6.1} \]

where \( A(n) \) and \( \phi(n) \) are digital representation of the amplitude and phase of the carrier respectively, and \( \omega_c \) is the carrier frequency. The DPM constructs a signal in the digital domain, such that after amplification and bandpass filtering, \( s_{\text{TX}}(t) \) expressed by (6.1) is obtained.

A digital low pass delta-sigma modulator LP DSM\(_A\) converts the \( M \)-bit amplitude values \( A(n) \) to a 1-bit pulse train. The sampling frequency of the LP DSM\(_A\) \( f_{\text{DSMA}} \) is derived from the multiplexer output in the phase path in order to align the pulse edges at the input of the AND-gate. For the system simulation, a 2\(^{\text{nd}}\) order loop filter transfer function has been chosen for the LP DSM\(_A\). The corresponding LP DSM\(_A\) structure is depicted in Fig. 6.2.

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**Fig. 6.1. DPM pulse encoder architecture.**

**Fig. 6.2. 1-bit 2\(^{\text{nd}}\) order LP DSM\(_A\).**
In order to construct the phase-modulated square-wave carrier signal, the following approach is proposed [29]:

1. The LP DSM$_P$ receives the low frequency modulating phase signal $\varphi(n)$ and converts it to an $N$-bit wide select signal for the MUX.

2. The multi-phase generator (MPG) delivers to the MUX input $2^N$ square-wave signals having a common carrier frequency and exhibiting discrete phase shifts with respect to each other.

3. Under these conditions the phase-modulated square-wave carrier signal is approximated at the multiplexer output.

The generation of the phase-modulated square-wave is further described in detail. The input $M$-bit phase values $\varphi(n)$ are converted by means of a multi-level low pass delta-sigma modulator LP DSM$_P$ to an $N$-bit wide output that forms the multiplexer select signal. The loop filter for the LP DSM$_P$ has been chosen the same as for the LP DSM$_A$. The corresponding block diagram is shown in Fig. 6.3. The LP DSM$_P$ has to be fast enough since it is clocked at the carrier frequency.

![Fig. 6.3. Multi-level 2nd order LP DSM$_P$ with phase encoder.](image)

The simulation of the LP DSM$_P$ revealed that the quantizer full scale range, divided in $2^N+1$ levels, has to be extended by two more levels; one level below the minimum level and by one level above the maximum level in order to account for the overload case. Then, a phase encoder circuit converts a multilevel quantizer output to an $N$-bit wide multiplexer select signal.

For a DPM with 4 discrete square-waves, the simulated multilevel quantizer output of the LP DSM$_P$ and its corresponding input signal $\varphi(n)$ are shown in Fig. 6.4. As can be seen from Fig. 6.4, the quantizer output has 7 levels. Because of the circular property of a phase signal, some of the quantizer levels can be mapped onto the same output code by means of a
phase encoder (e.g. -90° and 270° etc). A graphical representation of the phase encoder truth table is shown in Fig. 6.5.

Fig. 6.4. Input phase signal \( \phi(n) \) and quantizer output of the LP DSM in a DPM architecture with 4 discrete phases.

Fig. 6.5. Discrete phase encoder function.

Depending on the phase \( \phi_{IN} \) at its input, the LP DSM \( P \) generates a corresponding select signal at the MUX which switches between the two square-wave signals at \( f_c \) shifted by \( \phi_1 \) and \( \phi_2 \) (\( \phi_1 < \phi_{IN} < \phi_2 \)), respectively, in order to approximate a square-wave at \( f_c \) with the input phase \( \phi_{IN} \). The phase shift between square-waves is determined by the number of generated square-wave signals in the MPG and generally can be expressed as

\[
\phi_2 - \phi_1 = \frac{2\pi}{2^N},
\]

where \( 2^N \) is the number of phase-shifted square-wave carriers.
As an example, consider a DPM with 4 discrete phases (DPM4) in the MPG (Fig. 6.6). If the input phase value \( \varphi(n) \) equals to 40° then the select signal of the MUX switches its output between the signals corresponding to the phase shifts of 0° and 90° degrees during \( 1/f_{BB} \) time period approximating a square-wave signal at the carrier frequency with the 40° phase shift.

![Diagram](image)

**Fig. 6.6. Example of the approximate square-wave signal generation with 40° phase shift by using of four phase-shifted square-waves.**

Finally, the constructed phase-modulated square-wave signal and the delta-sigma modulated amplitude signal are combined by means of an AND-gate resulting in a bi-level signal shown in Fig. 6.7 for a DPM4 pulse encoder. After amplification and bandpass filtering at carrier frequency, the signal \( s_{rx}(t) \) from (6.1) is obtained.

![Graph](image)

**Fig. 6.7. Output of a DPM4 pulse encoder.**
6.2 Performance estimation

DPM8 and DPM16 with 8 and 16 phase-shifted square-waves, respectively, have been simulated driven by a two-channel unclipped WCDMA signal with a PAPR of 9.9 dB which was used in Chapter 3. For the output spectra of DPM8 and DPM16, $2^{18}$ samples of the carrier period have been simulated. The output spectrum (Fig. 6.8 (a)) of the pulse encoder shows that selectivity requirements to the reconstruction filter are relaxed in comparison to the fully digital quadrature modulator considered in section 3.4.1. From the enlarged spectrum in Fig. 6.8 (b), it can be seen that DPM8 shows moderate ACLR value.

![Fig. 6.8. Output spectrum of the digital polar pulse encoder DPM8 driven by a 2-channel WCDMA modulated carrier (a) from DC to $2f_c$; (b) at $f_c$ with a 60 MHz span.](image)

At the next step the pulse statistic for both configurations has been analyzed. From the 4-phase MPG example (Fig. 6.6), it can be seen that the output pulse train contains not only pulses of $T_c/2$ width but also $T_c/4$ and $3T_c/4$. In the same situation for an 8-phase MPG, in the output pulse train pulses of width $3T_c/8, 3T_c/2$ and $5T_c/8$ dominate. This is because most of the time the DSM肝 output signal switches the MUX between neighboring square-wave signals. Generalizing this to an arbitrary number of discrete phases $N_p$, dominating pulse widths can be written as

$$\text{Pulse Width} = \left\{ \frac{T_c}{2} - \frac{T_c}{N_p}, \frac{T_c}{2}, \frac{T_c}{2} + \frac{T_c}{N_p} \right\}.$$

However, if analyzing the simulated output pulse width statistic (Fig. 6.9) of the examined DPM8 and DPM16, it can be seen that there are occurrences of pulses shorter than
those described by (6.3). The probability of occurrence of the short pulses is very small and the performance of the SMPA is not expected to be much degraded. Pulse occurrences shorter than $T_c / 2 - T_c / N_p$ or longer than $T_c / 2 + T_c / N_p$ are caused when an abrupt change in phase appears at the input of the DSM$_P$. Then the DSM$_P$ switches the multiplexer not to the neighboring phase but in larger steps.

From (6.3) also one important observation follows: the more discrete phases are used in the DPM, the closer the $T_c / 2 \pm T_c / N_p$ pulses approaches $T_c / 2$, which is preferable for conventional SMPA classes. However, the probability of occurrence of the dominant pulses described by (6.3) remains approximately the same for DPM8 and DPM16. Fig. 6.9 (a) and Fig. 6.9 (b) show the simulated pulse statistic of the DPM8 and DPM16 respectively.

Moreover, a decrease in the number of occurrences of the $T_c / 2 \pm T_c / N_p$ pulses can be achieved by decreasing $f_{DSM}$ relative to the carrier frequency $f_c$. In this case, the pulses of width $T_c / 2$ will prevail in the DPM output. The results of the corresponding simulation are shown in Fig. 6.10, where for $f_c / f_{DSM} = 4$ the $T_c / 2$ pulses dominate by a factor more than 15 over the neighboring pulses.
A parameter comparison of the different pulse encoders from Chapter 3 including DPM8 and DPM16 is shown in Table 6-1. Comparing DPM8 with DPM16, it can be seen that by increasing the number of phases, the in-channel power increases which causes an increase in coding efficiency and ACLR. By using more phase-shifted square-waves, a more accurate phase approximation can be achieved which consequently improves the EVM.

The DPM average output frequency is essentially lower than the carrier. This is due to the fact that the DSMₐ does not always operate at the full-scale; therefore, the output contains zero pulses of much longer duration than the carrier period \( T_c \). During the time period when the DSMₐ output is zero, the power transistor is in the OFF-state. For the same reason, the ON-time has to be lower in the proposed DPM pulse encoder. This may significantly decrease the conductive losses in the driven SMPA.
Table 6-1. Simulative performance comparison of pulse encoder architectures with a two-channel WCDMA signal introduced in Chapter 3 including the proposed DPM8 and DPM16 architectures [29].

<table>
<thead>
<tr>
<th>Pulse Encoder</th>
<th>CEff/%</th>
<th>$\frac{f_{\text{ave}}}{f_c}$</th>
<th>$t_{\text{on}}$/%</th>
<th>ACLR/dBc</th>
<th>EVM/ %</th>
<th>Pulse width with max. probability</th>
<th>PA class</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>3.6</td>
<td>1.7</td>
<td>0.5</td>
<td>-55.5</td>
<td>&lt; 1.5</td>
<td>0.31 Tc</td>
<td>D</td>
</tr>
<tr>
<td>RF-PWM</td>
<td>24.2</td>
<td>1</td>
<td>0.09</td>
<td>-57.8</td>
<td>&lt; 1.5</td>
<td>0.08 Tc</td>
<td>D</td>
</tr>
<tr>
<td>BP DSM</td>
<td>4.4</td>
<td>1</td>
<td>0.5</td>
<td>-63.5</td>
<td>&lt; 1.5</td>
<td>0.25 Tc</td>
<td>D</td>
</tr>
<tr>
<td>Polar</td>
<td>17.5</td>
<td>0.29</td>
<td>0.1</td>
<td>-39.8</td>
<td>&lt; 1.5</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
<tr>
<td>Dig. IQ</td>
<td>2.8</td>
<td>1</td>
<td>0.5</td>
<td>-26</td>
<td>5.8</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
<tr>
<td>DPM8</td>
<td>11.8</td>
<td>0.24</td>
<td>0.12</td>
<td>-28.7</td>
<td>4.9</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
<tr>
<td>DPM16</td>
<td>12.8</td>
<td>0.24</td>
<td>0.12</td>
<td>-32.7</td>
<td>3.1</td>
<td>0.5 Tc</td>
<td>E,F</td>
</tr>
</tbody>
</table>

Considering the pulse statistics of the proposed pulse encoder, it can be seen that most of the pulses in the output pulse train have a width of $T_c/2$. It allows using this encoder to drive class-E and class-F SMPAs. The average frequency of the pulse train is only $0.24f_c$ which is much lower than in another pulse encoding techniques. Thus, an SMPA driven by this DPM pulse encoder will have lower switching losses.

The EVM value in DPM architectures is relatively high compared to the architectures discussed in Chapter 3. This can be explained by the approximation of the phase in the phase-modulated carrier. Also, the proposed fully digital encoder architecture has to compromise with additional power consumption required for the generation of the phase-shifted square-wave carrier signals. This situation becomes more significant with the increase in phase-shifted square-wave signal numbers, which is advantageous in terms of other performance criteria. The power consumption of a DPM is not a problem as long as it is much lower than the output power of the complete system. On the other hand, the number of discrete phases $N_P$ is limited by the resolution of the multi-phase generator, because the delay between the square-wave carriers, which is equal to $T_c/N_P$, can be very small at given conditions. For example, at $f_c = 2$ GHz and $N_P = 32$, the delay between square-wave carrier signals equals to 15.6 ps.
6.3 Inverse class-F PA driven by DPM pulse encoder

6.3.1 Measurement setup

A one-channel CDMA signal with a PAPR of 9.5 dB has been chosen as a test signal for measurements. The DPM8 and DPM16 modulators with 8 and respectively 16 phase shifted square-wave signals generate bit sequences which are stored in a bit-pattern generator. The length of the recorded bit sequence is $2^{19}$ carrier periods $T_c$. In both cases, the LP DSMs are based on the second order loop filter transfer function as shown in Fig. 6.2 and Fig. 6.3. In the LP DSM$_p$ of the DPM8 and DPM16 modulators, respectively, 11 and 19 levels are implemented. The simulated pulse sequences have been uploaded to the bit-pattern generator, which drives the input of the available SMPA module. The output power of the module was measured by means of a spectrum analyzer in a 3.84 MHz bandwidth. In order to find optimal operation conditions for maximum efficiency and maximum power, the bias points of the PA have been swept by a Matlab script which controls the corresponding DC supply sources.

The measurement setup for the performance estimation of the inverse class-F module driven by different DPM pulse trains is shown in Fig. 6.11.

The measurement setup consists of

- a clock generator that provides a clock signal for a bit-pattern generator
- a bit-pattern generator that repeats the simulated DPM pulse trains
- a spectrum analyzer for measuring the channel output power
- a programmable DC supply
- a PC that controls the measurement equipment and performs automated measurements by means of Matlab
6.3.2 Measurement results

Correspondingly measured values of the output power and the drain efficiency are shown in Fig. 6.12 and Fig. 6.13, respectively, for DPM8 and DPM16 in comparison with a state-of-the-art fully digital modulation technique [30]. The DPM-driven SMPA shows higher output power and drain efficiency compared to an SMPA driven by the digital modulation technique described in [30] because of two reasons. Firstly, a higher coding efficiency value is achieved when the SMPA module is driven by the DPM pulse encoder. Secondly, the DPM output sequence causes lower switching and conductive losses when driving the PA. The average output frequency of the DPM output pulse train for the test input signal is $0.28 f_c$ compared to $f_c$ in case of the fully digital modulator from [30]. This gives almost a four times decrease in SMPA switching losses. Also, an approximately four times decrease in conductive losses is expected, because the DPM output stays in the on-state only for 13% of the operation time.
Fig. 6.12. Measured output power of the SMPA module for a 3.84 MHz CDMA signal at 2.14 GHz carrier frequency driven by DPM16, DPM8 and [30].

Fig. 6.13. Measured drain efficiency of the SMPA module for a 3.84 MHz CDMA signal at 2.14 GHz carrier frequency driven by DPM16, DPM8 and [30].

Fig. 6.14 shows the spectrum at the output of the SMPA module driven by the DPM16 pulse train. The results for the class-F PA module driven by DPM are summarized in Table 6-2. Despite that fact that the digital polar modulation is not optimal for a class-F PA in terms of pulse statistic, it shows a good improvement in the achievable power and efficiency comparing with the fully digital modulation technique proposed in [30].
Fig. 6.14. Measured SMPA module output spectrum for a 3.84 MHz CDMA signal at 2.14 GHz carrier frequency.

Table 6-2. Performance summary of an inverse class-F PA at $V_G = -2V$ (maximum $P_{OUT}$) driven by DPM pulse trains.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal BW</td>
<td>3.84 MHz</td>
</tr>
<tr>
<td>Signal PAPR</td>
<td>9.5 dB</td>
</tr>
<tr>
<td>Carrier frequency $f_C$</td>
<td>2.14 GHz</td>
</tr>
<tr>
<td>Coding efficiency</td>
<td>DPM8: 14.6 %, DPM16: 15.5 %, [30]: 4.1 %</td>
</tr>
<tr>
<td>Channel power $P_{ch}$</td>
<td>0.96 W, 1.05 W, 0.2 W</td>
</tr>
<tr>
<td>Drain efficiency ($P_{ch}/P_{dc}$)</td>
<td>10.2 %, 11 %, 2 %</td>
</tr>
</tbody>
</table>
6.4 Conclusion

A new fully digital polar modulator (DPM) architecture is presented in this chapter. The DPM is suitable for driving any SMPA type in a class-S transmitter, because the produced output pulse train contains pulses that have a width which is equal to half of the carrier period $T_c$. But the most advantageous case will be valid for SMPAs in class-F and class-E systems. Driven by DPM pulse train, they will have much less conductive losses compared to class-D.

The proposed fully digital polar pulse encoder is better or comparable to existing modulation techniques in terms of coding efficiency, pulse train statistic and average frequency. The DPM demonstrates moderate ACLR and EVM values which may limit the application of this pulse encoder. On the other hand, it shows almost four times better coding efficiency than the fully digital pulse encoder given in [30] by resulting in a higher output power. The proposed fully digital encoder and the pulse encoder in [30] have been compared for the case when they were driving a real class-F$^{-1}$ amplifier. The class-F$^{-1}$ PA demonstrates the output power of 1 W when it is driven by DPM pulse encoder and 0.2 W when it is driven by a pulse train generated by the modulator in [30]. This confirms that the coding efficiency is very important for getting higher output power.
Chapter 7. Conclusions and Future Work

Since more and more devices incorporate several transceivers occupying different frequency bands, a fully digital multistandard multiband transmitter is highly demanded to reduce the form factor and decrease the power consumption. A class-S PA is a potential approach for a corresponding transmitter. The properties of a class-S PA are highly dependent on the employed pulse encoding technique. In the framework of this thesis, pulse encoders for an SMPA have been investigated, implemented and characterized. The main characteristics and limitations of pulse modulators have been discussed.

In chapter 3, the definition of the pulse encoder parameters were given. Two groups of pulse encoders, direct conversion and upconverting have been considered. Within these types, the PWM, the bandpass DSM, the quadrature pulse modulator and the polar pulse modulator architectures have been investigated in terms of performance. The pulse encoders have been simulated by applying a high PAPR two-channel WCDMA signal in order to compare the achievable performance and to define pros and cons of each encoding technique. By comparing pulse statistics, an appropriate pulse modulation technique can be determined as a driver for a given SMPA class. The RF PWM showed the best coding efficiency among all considered pulse modulation techniques. However, it requires very high bandwidth of the driven SMPA. A bandpass DSM relaxes the switching requirements to an SMPA but this was not enough to design a complete class-S PA at 900 MHz and at 2 GHz input frequency, because of the bandwidth limitation in the available power transistors. At the beginning of the work, the maximum bit rate, set by power transistor, was 2.2 GS/s. At such condition, a DSM with a 900 MHz input has been developed. Moreover, this modulator was measured in a frequency converter configuration having the input at 900 MHz and the output at 2.2 GHz while clocked at 3.1 GHz. However, very low coding efficiency makes such an approach impractical. During the project, partners have developed a power transistor that moved the limit of the highest sampling rate of a bandpass DSM to 5 GS/s. Thus, a non-$f_s/4$ frequency bandpass DSM architecture was proposed to realize a pulse encoder at the 2.1-2.2 GHz input.
According to the proposed design procedure, a 5 GS/s 2.1-2.2 GHz CT bandpass DSM has been implemented. The measurement results proved the theoretical design approach. Chapter 4 presented the design procedure starting from the system level and ending at the circuit design level. It also includes an estimation of non-idealities and its influence on the modulator performance. Unfortunately, the coding efficiency of a bandpass DSM encoder is not high enough for signals with high PAPR.

The ideal modulator would have to fulfill these requirements: 1) high coding efficiency to achieve high in-channel power; 2) all pulses in the pulse train being equal to half of the carrier period $T_c$ in order to achieve maximum PA efficiency; 3) the average frequency of the pulse train being kept as low as possible to reduce switching losses in SMPA. Moreover, an ideal pulse encoder has to be fully-digital implementing a frequency upconverting function. On the other hand, the encoder output signal has to fulfill requirements such as EVM and ACLR. One of the candidates was the polar modulation. However, there was no fully digital encoder based on that principle. Within this work, a fully digital polar pulse encoder architecture has been proposed and investigated. Chapter 6 described the principle of operation of the proposed encoder. The provided analysis showed that the proposed DPM is better than or comparable to other existing pulse modulation techniques in terms of the three previously mentioned criteria. However, it shows moderate ACLR and EVM values. An improvement of the ACLR value is a topic of future research. In Chapter 6, the performance estimation of a 2.1-2.2 GHz class-F PA driven by the DPM pulse train was also reported. In-channel efficiency was 12% for a 5 MHz WCDMA modulated signal with high PAPR. At the same time, the modulated in-channel output power was higher than 1 W pointing to a good utilization of the power transistor.

Further research work related to the DPM is required. First of all, the influence of the envelope LP DSM on the overall performance has to be investigated. The introduction of additional quantization levels in the envelope LP DSM may improve the achievable ACLR of the pulse encoder. In the phase LP DSM, more attention has to be paid on how to avoid abrupt phase changes. By reducing the phase error, an improvement of the EVM value is expected. Secondly, the DPM has to be investigated as a driver for other SMPA classes e.g. class-E and class-D. With respect to this, further analysis of class-E and class-F amplifiers driven by non-periodic pulse trains containing pulses of half a carrier period has to be conducted.
Furthermore, higher output power can be expected if driving an H-bridge amplifier since it allows three different states. By producing a 3-state output, the DPM pulse train coding efficiency doubles. Implementation aspects have to be considered as well, since the power consumption of the pulse encoder may significantly affect the overall efficiency in case of low or medium output power of a class-S transmitter.
References


REFERENCES


Publications and Patents


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