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High Temperature Stability of Nitride-Based Power HEMTs

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***Abstract*—— The temperature stability of InAlN/GaN heterostructure FETs has been tested by a stepped temperature test routine under large signal operation conditions. Devices have been successfully operated up to 900 °C for 50 hrs. Failure is thought to be contact metallization related, indicating an extremely robust InAlN/GaN heterostructure.**

GaN heterostructures, InAlN/GaN HEMT, High-Temperature Electronics, Reliability

I. INTRODUCTION

During the last years InAlN/GaN has been emerged as a new material for high electron mobility transistors (HEMTs). Its high interfacial sheet-carrier density of $N_S = 2.8 \times 10^{13}$ cm^{-2} and the absence of mechanical stress in the heterojunction [1] in its lattice matched configuration are very promising for highly stable power FET operation. First experiments had already indicated that his heterostructure and its surface is indeed thermally, chemically and electrically highly stable as demonstrated in a short time operation at 1000 °C in vacuum [2]. Meanwhile, also a first analysis of possible degradation mechanisms has been reported [3].

The initial high temperature tests of InAlN/GaN HEMTs had indicated that the stability is presently not limited by the heterostructure, but by the passivation and contact schemes employed. To further investigate the stability a high temperature stepping test routine has been developed to identify failure mechanisms within a reasonable testing time. With this routine, InAlN/GaN HEMTs have been tested, under large signal conditions, operated at high temperature with 1 MHz input signal, up to failure.

II. TEMPERATURE CYCLING MEASURMENT

To test the high temperature stability, a temperature stepping experiment was designed, where the temperature is ramped up in steps of 100 °C every 250 hrs until device failure. A 250 hrs time interval had been chosen to identify device failure within a reasonable time frame. Usually, temperatures have been 500 °C and higher. The operating temperature was measured with a thermocouple calibrated by the melting points of specific metals. The devices were kept in vacuum and probed by tungsten carbide (WC) needles, because packaging and bond connections are not readily available for this temperature range. Contacting by needles lead to an estimated temperature difference of up to 30 °C, which may be higher or lower. On one hand the needle contact pressure may generate a better thermal contact between the heater and the substrate, or on the other hand the device may be cooled by the unheated needles. The individual devices have been operated in large signal class-A configuration at a frequency of 1 MHz, the frequency range being limited by the needle contact. An external load resistor was applied matching the maximum current level at $V_G = 0$ V and the maximum drain bias, typically 20 V, at pinch-off (see Fig. 1). The wave form of the input and output signals was recorded every 60 sec and the mean drain current ($I_{DS\ mean}$) calculated. In general $I_{DS\ mean}$ is usually less than half of $I_{DS}(V_{GS} = 0$ V).

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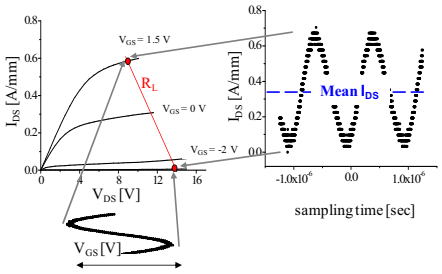

Fig. 1 Test arrangement of temperature stepping experiment. Input signal 1 MHz; bias point and amplitude adjusted as shown. Output termination by R_L. Output and input wave form recorded every 60 sec.

III. FABRICATION ROUTINE

The devices used in this study were fabricated from MOCVD grown $In_{0.18}Al_{0.82}N$/GaN (lattice matched configuration) heterostructures on SiC substrat. The thickness of the InAlN barrier layers was between 7 nm and 10 nm. Device isolation has been obtained by mesa etching in an Ar-plasma.

The metallization schemes of the source/drain and gate contacts need to withstand the high temperature cycling routine. Therefore two configurations have been employed. A first one based on the commonly used layer stacks topped with Au for high electrical conductivity and secondly with a Cu top layer. The reason for replacing Au with Cu is the softening of Au at high temperature, which had in fact been the main difficulty encountered in the first experiment reported in [2]. Thus, the ohmic contacts have been Ti/Al/Ni/Au and Ti/Al/Ni/Cu of various thickness ratios of the layers annealed at a temperature between 850 °C and 900 °C in N_2 atmosphere, resulting in a contact resistance of approx. 1 Ωmm (no ohmic contact recess employed). The gate length was 0.25 µm defined by e-beam lithography. Ni/Au and Cu were used as gate metallization followed by PECVD deposition of 200 nm of Si_3N_4. Finally the contact pads were opened by dry etching in RIE. Fig. 2 shows a schematic cross section based on the conventional contact metallization scheme.

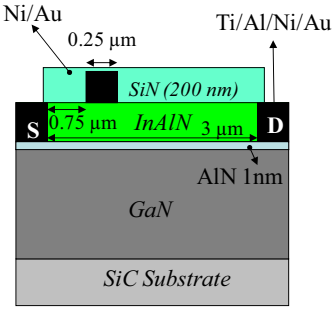

Fig. 2 General cross section of devices used.

IV. RESULTS AND DISCUSSION

A. Contact technologies

As mentioned, the first high temperature experiment had already indicated that this lattice matched heterostructure possesses high temperature stability, possibly beyond 1000 °C. Therefore, the contact materials used in the fabrication process as described briefly above would also need to possess a similar stability, and would need to form a stable interface with the surface of the InAlN barrier material and the GaN buffer layer in the areas outside the mesa. In addition, the entire structure needs to be passivated and firmly encapsulated, usually by Si_3N_4. The entire materials stack needs then in turn to be stress balanced.

The ohmic contacts to GaN and its ternary alloys like InAlN are commonly based on the formation of an alloyed metal nitride interface providing a path for electron tunneling. The common layer stack developed during the last decade has been Ti/Al with a Ni/Au overlay. According to their phase diagrams [4], many phases can be formed above the melting point of Al, essentially generating chemical activity of Ti for an interfacial reaction well below its melting temperature.

Thus, depending on the Ti:Al layer thickness ratio ohmic behavior has been reported for alloying temperatures between 600 °C [5] and 900 °C [6]. Aiming at a contact stability up to 1000 °C, a Ti:Al ratio according to the Ti_3Al phase is one possibility. As a consequence ohmic behavior is only obtained at high alloying temperature. To prevent Au from alloying with Ti and Al at a temperature as low as 500 °C, Ni is inserted. However, the diffusion constant of Ni in Au (8.459×10^{-10} cm^2/sec @ 900 °C, [4]) is one order of magnitude higher than that of Ni in Cu ($1.17\ldots6.72) \times 10^{-11}$ cm^2/sec @ 900 °C [4]), resulting in a slower intermixing of a contact with Cu overlay. Indeed annealing of contacts with Au overlay above 800 °C shows substantial intermixing, resulting in a typical texture (see Fig. 3), however negligible interdiffusion with the InAlN barrier material (even for a thickness of 3 nm). Nevertheless, under electrical stress, generated by the DC bias and the 1 MHz large signal applied, the contact metallization becomes completely unstable, blowing off the Si_3N_4 passivation layer covering the entire device surface [7]. Thus, the conventional contact metallization schemes based on Au-overlays limits the device stability to approx. 800 °C.

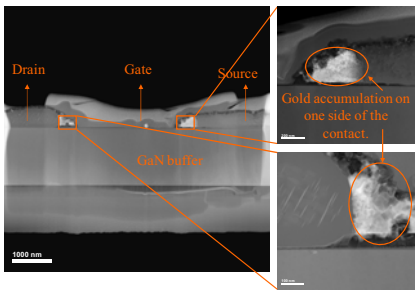

Fig. 3 High-Angle Annular Dark Field (HAADF) Scanning Tunneling Electron Microscopy (STEM) image of cross section of the device after 30 min annealing at 800 °C. Gold accumulation on one side of the ohmic contact could be identified.

As a consequence it was thought that a top metallization based on Cu may prevent this catastrophic reaction.

Obviously, a Au overlay should also be avoided for the Gate Schottky contact metal, which is typically Ni [7]. However, since the gate feed resistance is critical for high frequency operation, it needs to be replaced by a material of similar electrical conductivity. Such a material is again Cu. It has been used by a number of groups as the Schottky barrier material and overlay conductor simultaneously [9], [10]. Replacing the Ni/Au gate metallization by Cu has indeed resulted in stable device operation up to the 800 °C range, with the gate contact surviving large signal operation over the entire 250 hrs cycle. During the 900 °C cycle severe Cu electromigration could be observed leading to the interruption of the gate metal stripe (see Fig. 4), however not leading to shorts between gate and drain or source. Thus, in this degradation process no interdiffusion or alloying has occurred with the heterostructure barrier.

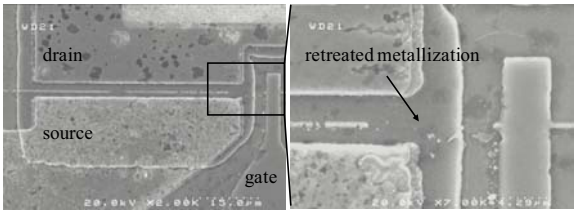

Fig. 4 Topography of InAlN/GaN HEMT after failing during 900 °C large signal RF operation.

The last step applied to these devices had been passivation by Si_3N_4. Si_3N_4 is the common passivation on nitride heterostructures providing a nitrogen linkage across the interface. It is deposited by sputtering, PCVD or ALD and is in general amorphic. It may deviate from stoichiometry, may be H-rich or Si-rich, is rather brittle and may contain a stress profile. Moreover, the tensile stress between the Si_3N_4 and the SiC-substrate is increasing with temperature, reaching its maximum in the range of 800 °C (Fig. 5). This can cause cracks in the Si_3N_4 especially with non-stoichiometric material. To reduce stress sometimes oxygen is added to the process gas, rendering the material an oxynitride [11]. In this case deposition has been by PCVD at 300 °C in SiH_4 and NH_3. After the highest temperature step of 900 °C isolated cracks could be identified mainly at mesa edges, partially leading to the interruption of the gate feed (Fig. 5).

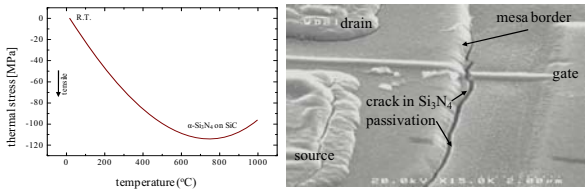

Fig. 5 Left: Thermal stress of Si_3N_4 on SiC substrate. Right: Crack in Si_3N_4 passivation due to high tensile stress at elevated temperature.

B. *Device Characteristics at high Temperature*

1) *DC characteristics*

Fig. 6 displays two typical output characteristics measured at R.T. before the thermal cycle and at the beginning of the 800 °C cycling period. The main feature is the drop in maximum output current (at V_G = 0 V). Several effects may contribute to this behaviour, like for example a change of 2DEG channel mobility with temperature, influencing the intrinsic FET behaviour as well as the parasitic series resistances, a change of 2DEG density due to change of a charge trapping balance of deep centres, a change of saturated velocity with temperature, and a change of gate barrier potential and free surface potential in the regions between the contacts.

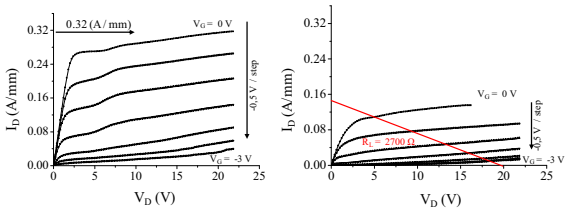

Fig. 6 Output characteristics of the InAlN/GaN HEMT. Left: device at R.T.; Right: device at 800 °C. Also shown the load line selected for 800 °C operation experiment.

As can be seen from the largely temperature independent pinch-off voltage (Fig. 7), deep trapping centers are not dominating the output current change.

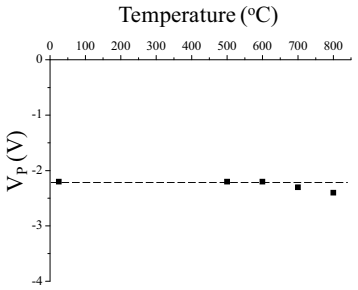

Fig. 7 Change of pinch-off voltage with temperature.

A second parameter of large influence may be the temperature dependence of the electron mobility (μ). Its influence on the FET characteristics is mainly observed at large gate-lengths and low mobilities. At R.T. with 2DEG mobilities above approx. 1000 cm^2/Vs the behaviour of HEMTs with 0.25 μm gate length is usually dominated by the carrier saturation velocity. Since this is a hot electron effect, its temperature dependence will be rather weak [12]. Thus, at high temperature with decreasing mobility the behaviour will turn over to the mobility and pinch-off dominated case. The dominating scattering mechanism will then be phonon scattering, in the case of an interfacial 2DEG channel the dependence will be $\mu \sim T^{-3/2}$. Plotting the temperature dependence of the maximum drain current density ($I_{DS,max}$) at 0 V gate bias for the device tested against this power law yields

indeed a widely linear relationship at high temperature. At low temperature the turn-over from the saturated velocity dominated short channel behavior to the mobility dominated behavior can be observed (Fig. 8).

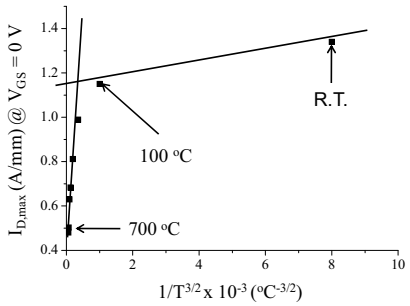

Fig. 8 Maximum output current density in dependence on the operation temperature.

2) 900 °C Experiment

The highest temperature interval, where failure occurred, has been the 900 °C cycle. This temperature is already close to the melting temperature of the Cu-overly metallization and indeed failure has been by electromigration under large signal operation as pointed out earlier. However, the measurement itself becomes difficult due to the thermal load of the sample holder and the microprobes. Individual contact probing has therefore been rather irreproducible, resulting in a high jitter and noise level of the measurement. In turn this means that reliable measurement methods for testing at such high temperatures are essentially lacking and need basic development. Fig. 9 shows, where the device failed after 50 hrs at 900 °C. This specific experiment was started at 800 °C. Both temperature steps were performed on the identical device. Due to thermally induced movement of mechanical parts, especially concerning the microprobes, these had to be lifted during each temperature transient and the device contacted after each temperature had settled. With raising temperature the maximum drain current decreased as discussed earlier. Inspection after cooling down from the last cycle showed furthermore that unbiased devices were still operational.

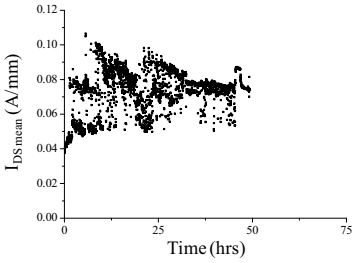

Fig. 9 Up to failure high temperature cycling of InAlN/GaN HEMT with Cu based metallization. 900 °C step shown.

V. CONCLUSION

Lattice matched InAlN/GaN based HEMTs have demonstrated the highest thermal stability of all heterostructure devices to date, operating them under large signal conditions close to 1000 °C. It seems that degradation is still induced by the metallization schemes used and not the semiconductor material itself. Indeed this seems to possess ceramic-like stability. This may enable the use of the InAlN/GaN system at extreme temperatures, like encountered in jet engines or in other high temperature environments. Further details on the experiments described here can also be found in [13].

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