Design and Comparison of Regenerative Dynamic Frequency Dividers in Different Configurations Using SiGe HBT Technology

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***Abstract*—In this letter, the authors present the design, analysis and comparison of a series of dynamic frequency dividers. These dividers, each consisting of a Gilbert cell mixer core, a transimpedance amplifier and an emitter-follower feedback network, are all based on the regenerative concept but differ in feedback configuration and dc power consumption, leading to different performance with respect to maximum operating frequency, input and output power. Analysis and comparison of the dividers are performed by simulation and verified by measurement. Design aspects for achieving high operating frequency, low input power and high output power are discussed.**

***Index Terms*—Heterojunction bipolar transistors (HBTs), millimeter wave integrated circuits.**

I. Introduction

DYNAMIC frequency dividers, which are based on the regenerative concept [1], are widely used at high frequencies because of their high operating frequency compared with the static dividers. A dynamic divider consists of a mixer and a low-pass filter. The input signal is applied to one of the input of the mixer, while the filter output is connected to the second input of the mixer. For the Gilbert cell mixer, which is frequently used in dynamic dividers, the two inputs are different, leading to two possible circuit configurations for the divider: feedback to the tranconductance stage and feedback to the switching quad. Both circuit configurations are being used and many dividers based on these two topologies have been published, e.g., [2]–[4]. However, the difference between the two circuit configurations has rarely been discussed and a direct comparison of the two configurations has not been reported so far. This letter shows the design, simulation and characterization of different dynamic dividers based on the two different circuit configurations. The performance differences of these dividers are analyzed and design guidelines for achieving different performance are discussed.

II. Circuit Design and Simulation

Four dynamic dividers have been realized for comparison. In the first divider [Fig. 1(a)], the input signal is applied to the switching quad, while the feedback is connected to the transconductance stage of the mixer. Two emitter followers (EFs) are inserted in the feedback path, which serve as both low-pass filter and dc level shifter. The circuit is optimized for maximum operating frequency with a 4 V supply. The second divider uses the same configuration, but operates with reduced current and then at lower frequencies. The base of Q_6 is connected to the base of Q_5, due to the low dc potential at the emitter of Q_5. In the third divider, the input signal is applied to the transconductance stage, while the feedback is connected to the switching quad of the mixer. "EF_2" is removed from the feedback path because of the low dc voltage drop in the path. This reduces the maximum operating frequency of the divider. So a fourth divider [Fig. 1(b)] is designed with the same configuration as the third divider, but the supply voltage is increased to 5 V so that both "EF_1" and "EF_2" can be kept in the feedback path to achieve higher operating frequency[1].

In each divider, the mixer is based on the Gilbert cell topology with a transimpedance amplifier (TIA) as the load. The input impedance of the TIA is much lower than the output impedance of the mixer core, resulting in a strong impedance mismatch in the loop, which increases the loop bandwidth (cutoff frequency), following the same concept as the Cherry–Hooper broadband amplifier [5]. Therefore, much better performance with respect to maximum operating frequency, safe broadband operation and high sensitivity can be achieved, compared with a single resistor as the load [6].

Small transistors ($5 \times 0.5\ \mu\mathrm{m}^2$ emitter finger size) are used in the mixer core and TIA, which provide sufficient gain with small current consumption. The four dividers have the same mixer core (slightly different current) and differ mainly in the TIA (R_1, R_2) and EFs (transistor and current). The detailed summary of the four dynamic dividers is provided in Table I.

The dynamic dividers usually operate at high frequency where the static dividers cannot operate, for instance, as the first stage of a divider chain. Therefore, the maximum operating frequency is an important characteristic of the dynamic dividers. In the regenerative divider, the maximum operating frequency is determined by the open-loop gain (referred to later as loop gain) bandwidth (where the open-loop gain drops to 1). When the loop gain is smaller than 1, the oscillation in the loop will not sustain and the divider cannot divide properly. Since the signal that travels in the loop is at half the input frequency,

[1]Two EFs can increase the loop gain at higher frequency (because of capacitive gain peaking) and extends the loop gain bandwidth.

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TABLE I
DETAILED PARAMETERS OF THE DYNAMIC DIVIDERS

Circuit ID	Feed-back	V_s (V)	I_t (mA)	I_1 (mA)	I_2 (mA)	R_1 (Ω)	R_2 (Ω)	I_3 (mA)	R_3 (Ω)	I_4 (mA)	R_4 (Ω)	I_5 (mA)	R_5 (Ω)	Q_4 (μm^2)	Q_5 (μm^2)	Q_6 (μm^2)
I	"A"	4	28.5	3	4.8	250	300	3.3	650	4.4	300	2.5	200	5×0.5	10×0.5	10×0.5
II	"A"	4	17.2	3	4.4	350	300	1.3	1.5k	1.3	800	2.1	500	5×0.5	5×0.5	5×0.5
III	"B"	4	28	3.7	4.4	300	250	4.3	450	-	-	5.4	200	10×0.5	-	10×0.5
IV	"B"	5	38.3	3.6	4.4	300	350	3.9	750	5.1	400	5.3	220	5×0.5	10×0.5	10×0.5

V_s: supply voltage, I_t: total current, "A": feedback to the transconductance stage, "B": feedback to the switching quad

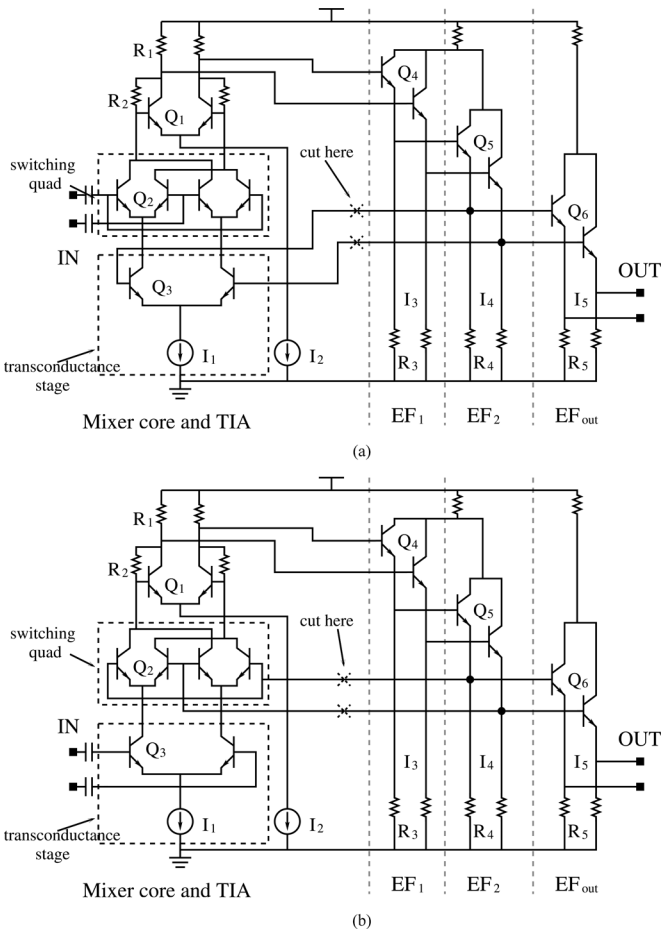

Fig. 1. Schematics of the dynamic dividers in different configurations, with (a) feedback to the transconductance stage (Divider I) and (b) feedback to the switching quad (Divider IV).

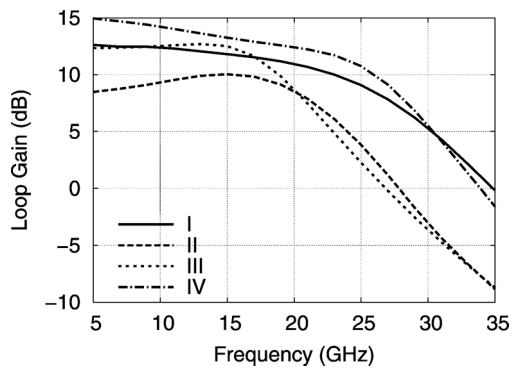

Fig. 2. Simulated loop gain of the dividers with 0 dBm input power.

the maximum input operating frequency is about twice the frequency where the loop gain drops to 1.

The loop gain is simulated in ADS using harmonic-balance simulation. To determine the loop gain, the dividers are cut at the feedback point, as shown in Fig. 1. A dummy mixer core and dummy "EFs" are inserted to present the same impedance matching conditions of the closed loop. For divider I and II, an input signal at frequency f_{in} is applied to the switching quad and another signal at frequency $f_{in}/2$ is applied to the base of Q_3. The gain is calculated as the power gain from the base of Q_3 to the emitter of Q_5 (at frequency $f_{in}/2$). For divider III and IV, an input signal at frequency f_{in} is applied to the base of Q_3 and another signal at frequency $f_{in}/2$ is applied to the switching quad. The loop gain is calculated as the the power gain from the base of Q_2 to the emitter of Q_5.

To achieve the highest operating frequency, the loop gain bandwidth must be maximized. Since the four dividers have the same mixer core, only the TIA and feedback EFs are optimized for highest bandwidth, by adjusting the resistors (R_1 and R_2) and currents in the TIA and EFs, as summarized in Table I. The simulated loop gain (with 0 dBm input power) is shown in Fig. 2. Although divider IV has the highest loop gain, the gain drops faster as the frequency increases, compared with divider I, which leads to less gain bandwidth. This is because the transconductance stage (Q_3) of divider I operates only at $f_{in}/2$ and hence has higher gain than divider IV, where Q_3 operates at f_{in}[2]. For the same reason, divider II has a higher bandwidth than divider III. From the loop gain simulation, divider I and IV can operate up to about 70 GHz, while divider II and III up to 55 GHz.

III. CHARACTERIZATION

The dividers are all realized in a 0.8 μm SiGe HBT process with $f_T/f_{\max}$ of 80/90 GHz [7] and characterized on-wafer. Due to the lack of differential signal sources, the input was fed using a "GSG" probe, with the second input grounded directly by the ground of the probe. The differential outputs were measured simultaneously using a spectrum analyzer and a power meter.

The measured input sensitivity curves are shown in Fig. 3. Divider I has the highest operating frequency of 67 GHz (limited by the measurement setup). Divider IV can operate up to 64 GHz, while divider II and III can operate slightly above 50 GHz. The measured maximum operating frequency agrees

[2]Although the switching quad operates at $f_{in}/2$ in divider IV, compared with f_{in} in divider I, this has very limited influence on the loop gain, because the transistors in the switching quad are already fully switched on and off in both dividers.

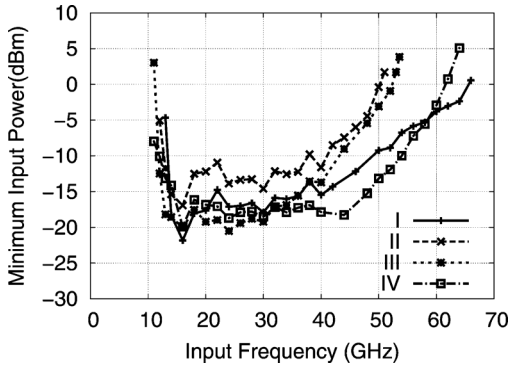

Fig. 3. Measured input sensitivity curve of the four dynamic dividers.

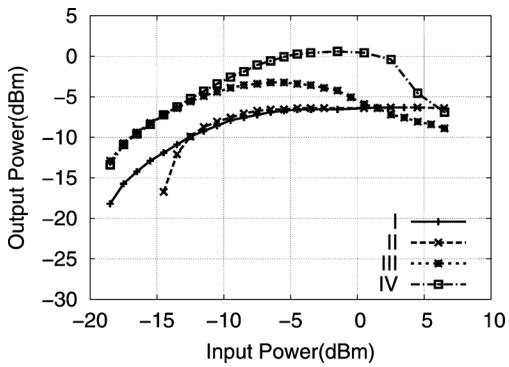

Fig. 4. Measured output power versus input power with 30 GHz input signal.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	Feed-back	Frequency (GHz)	f_m/f_T	Min. P_{in} (dBm)	Max. P_{out} (dBm)	DC (mW)
I	"A"	13 - 67	84%	-17	-6.5	114
II	"A"	12 - 51	64%	-15	-6.5	69
III	"B"	11 - 54	68%	-18	-3	112
IV	"B"	11 - 64	80%	-18	0.5	192
[2]	"A"	74 - 136	65%	-	-	118
[3]	"B"	51 - 168	78%	-14	-	105
[4]	"B"	304 - 331	88%	-	-12	85

f_m: maximum operating frequency, "A": feedback to the transconductance stage, "B": feedback to the switching quad

quite well with the expectation based on the loop gain simulation. At frequencies below 11 GHz, the dividers cannot divide properly, due to the not sufficiently suppressed higher mixing harmonics.

The loop gain of the dynamic divider decreases as the input signal power decreases. When the gain is less than 1, the divider stops operating. Therefore, the required minimum input power of the dynamic divider is mainly determined by the loop gain. As shown in Fig. 3, the required minimum input power for the four dividers are different. Divider II requires the highest input power due to the lowest loop gain. Generally, divider I and II requires higher input power than divider III and IV, because the loop gain drops faster as the input power decreases.

The output power of the dynamic divider is determined by the steady-state signal power in the loop (as in an oscillator). The power in the loop starts from noise level and increases until the gain decreases to 1. Then it remains constant. Fig. 4 shows the measured output power of the four dividers with increasing input signal power. At low input levels, the loop gain increases as the input signal power increases, leading to an increasing output power. At high input levels, the loop gain starts to saturate, due to the non-linearity of the circuit, especially in the transconductance stage, therefore the output power stops increasing. For divider III and IV, the feedback is connected to the switching quad of the mixer and the transconductance stage is not in the feedback loop, so the loop gain decreases (due to gain suppression in the TIA and EFs) to 1 at higher power level, compared to divider I and II. Therefore, the steady-state signal power in the loop in divider III and IV is higher than in divider I and II, leading to higher output power. It should also be noted that the output power of divider III and IV starts to decrease at high input levels, as shown in Fig. 4. This is because less power is needed at the switching quad to maintain the oscillation in the loop, due to the large input power at the transconductance stage. Therefore, for dividers with the switching quad as input, very high input power should be avoided.

A summary and comparison of the performance of all dividers is provided in Table II.

IV. CONCLUSION

A series of dynamic frequency dividers with two different configurations were analyzed and compared. For all dynamic dividers, the open-loop gain and bandwidth is the most important design parameter, which determines the operating frequency and required input power. The analysis and comparison shows that divider I (feedback to the transconductance stage) is more suited for wider bandwidth (higher operating frequency) and low dc power consumption, while divider IV (feedback to the switching quad) is more suited for lower minimum input power and higher output power. For divider II, at reduced dc power, the bandwidth decreases and the minimum input power increases, while for divider III, with about the same dc power as divider I, the input power is reduced and the output power is increased, but the bandwidth decreases.

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