Reprinted from
2013 IEEE Radio and Wireless Symposium, 20. – 23. January 2013 in Austin, Texas, USA

A Low-Cost, Wide-Band 60 GHz Down-Converter Module for Multi-Gigabit per Second Wireless Communication

Gang Liu, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher

Institute of Electron Devices and Circuits, Ulm University, Germany
Albert-Einstein-Allee 45, 89081 Ulm, Germany

***Abstract*— This paper presents a low-cost down-converter module for 60 GHz short-range multi-gigabit per second wireless applications. The 60 GHz down-converter IC, consisting of a mixer, a VCO, a frequency doubler and a PLL, is realized in a low-cost SiGe HBT technology and packaged using low-cost substrate material and wire-bonding techniques with compensated interconnect structures. The packaged module shows 2.5 dB conversion gain at 60 GHz and a very wide IF bandwidth of 10 GHz, covering the complete 60 GHz ISM band. The module has been tested in a short range 60 GHz system with up to 2 Gbit/s data rate and error-free transmission have been achieved.**

***Index Terms*— Millimeter-wave integrated circuits, heterojunction bipolar transistors.**

I. Introduction

The 60 GHz ISM band is very attractive for ultra-high-rate wireless communications due to the globally available wide bandwidth. The reported 60 GHz systems so far are all realized in advanced semiconductor technologies which are cost effective only for large market volumes, as in [1], [2]. This paper presents a 60 GHz down-converter module realized in a very cost-effective semiconductor technology suitable also for small volume production, and packaged using a low-cost substrate material and wire-bonding techniques. The down-converter has a very wide IF bandwidth, making it very suited for multi-gigabit wireless transmission. The IC is presently used in a system, where the down-converted IF signal (BPSK modulated) is directly demodulated by an analog QPSK/BPSK demodulator, realized in the same semiconductor technology. 2 Gbit/s error free transmission has been achieved limited by the transmitter.

II. Module Design

A. Circuit Design

The down-converter is realized in a mature 0.8 μm SiGe HBT technology with f_T/f_{max} of 80/90 GHz [3]. The complete process requires only 24 masks with 0.8 μm lithography resolution and is therefore very cost effective, but poses the challenge of very high ratio of operational frequency to f_{max}. The block diagram of the down-converter IC is shown in Fig. 1.

The down-converting mixer is an active mixer based on the Gilbert-cell topology. The switching quad works with a transimpedance amplifier load to extend the IF bandwidth. The mixer achieves 6 dB conversion gain and 11 GHz IF bandwidth. Further details of the mixer can be found in [4]. The LO signal is generated using a 30 GHz VCO (based on the Colpitts topology) and a push-push frequency doubler. The combination of the VCO and frequency doubler can deliver about -6 dBm output power at 66 GHz. Details of the VCO and frequency doubler can be found in [5]. An analog PLL, consisting of a divide-by-32 frequency divider, an analog phase detector and an active loop filter, is used to stabilize the VCO. The PLL has a loop bandwidth of about 60 MHz. The closed-loop phase noise is -106 dBc/Hz at 1 MHz offset. Details of the PLL can be found in [6].

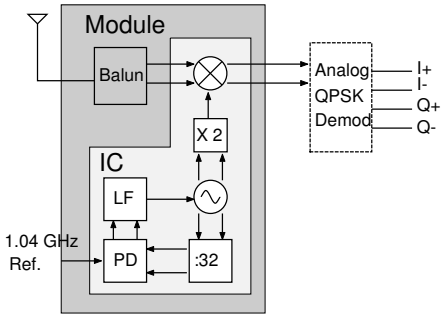


Fig. 1. Block diagram of the down-converter.

Fig. 2 shows the realized down-converter IC, which is very compact and occupies only 1 mm^2 chip area. The circuit draws 124 mA current from a 3.5 V supply. With an external reference of 1.04 GHz (LO of 66.56 GHz), the measured conversion gain versus RF frequency is shown in section III (Fig. 4).

B. Packaging

The packaged down-converter module is shown in Fig. 3 (a). The Rogers RT Duroid 5880 substrate (ϵ_r:2.2, 127 μm thickness, 17 μm copper cladding) is used as the carrier substrate. A high gain patch antenna has already been realized on the same substrate, but not integrated on the module. Instead, a V-connector is used for the RF input to ease characterization. A rat-race balun is realized on board to connect the differential input of the IC to the

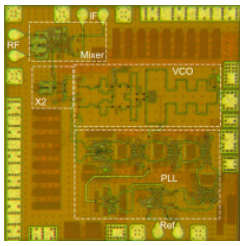
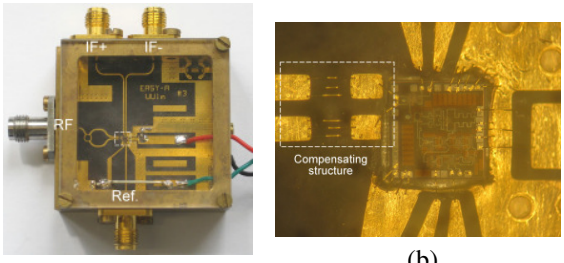


Fig. 2. Micrograph of the realized down-converter IC. The size is 1 × 1 mm^2.

single-ended antenna. The board is fixed in a brassing housing for measurement purpose. Fig. 3 (b) shows a close-up of the IC area. The IC is glued directly on the brass housing after cutting a recess in the board, which improves heat dissipation and performance.



(a) (b)

Fig. 3. (a) Photo of the realized receiver down-converter module. (b) Close-up of the bonding area.

Interconnects between the IC and the board are formed by bondwires (Au, 17 μm diameter). Due to the different thickness of the ICs (350 μm) and the substrate board (127 μm), the bondwire between the IC and the on-board microstrip line is cannot be less than 300 μm, which influences the performance significantly. Therefore, to compensate the influence of the bondwires, an L-C-L compensating structure is used, as shown in the dashed box in Fig. 3 (b). A small capacitor (realized using a microstrip patch) is inserted between the IC and the on-board microstrip line. Several long bondwires in parallel, instead of one short bondwire, is used to reduce the sensitivity to bondwire length variation. The bondwire interface has been tested and shown very low loss (0.1 dB at 60 GHz). More details about the L-C-L compensating structure can be found in [7].

III. Experimental Results

A. Characterization

The packaged module was characterized in a coaxial environment. The complete module consumes 440 mW DC power. The RF port was connected to a signal generator and the two IF outputs were connected to a power meter and spectrum analyzer, respectively. The 1.04 GHz reference signal was supplied by an external signal generator. The RF frequency was swept from 50 to 66 GHz. Fig. 4 shows the measured conversion gains of the module and the down-converter IC (on-wafer measurement). The conversion gain at mid-band is 2.5 dB and the 3 dB bandwidth is about 10 GHz, covering the complete 60 GHz ISM band. The conversion gain of the module is about 3 dB lower than obtained from on-wafer measurements of the down-converter IC, which agrees well with expectations (1 dB from V-connector, 1 dB from bondwire interface and on board baluan and another 1 dB from IF output microstrip lines and connectors). The measured input return loss of the module is also shown in Fig. 4, which is below -10 dB from 57 to 66 GHz.

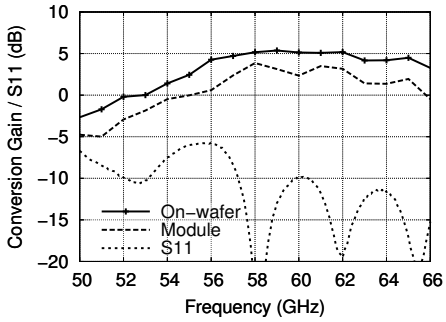


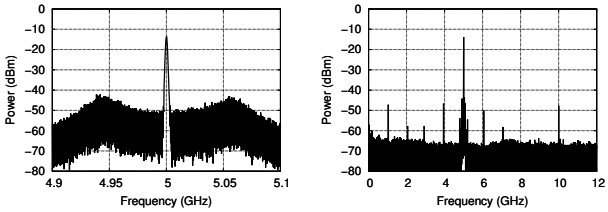
Fig. 4. Measured conversion gain versus RF frequency of the module compare to on-wafer measurement and the RF input return loss of the module.

The input P_{1dB} of the module is -27 dBm. The measured single-side-band (SSB) noise figure (NF) of the module is 25 dB, which is in line with expectations due to the rather low cutoff frequency of the technology. The NF of the module can be improved by 1 dB when the V-connector is removed and the antenna is directly integrated on the same board.

Fig. 5 shows a down-converted IF spectrum with 200 MHz and 12 GHz span. The LO was fixed at 66.56 GHz (1.04 GHz reference signal), the RF was injected at 61.56 GHz. The down-converted IF signal has the same reference spur as the LO signal. Furthermore, the second harmonic of the IF signal (at 10 GHz) and the reference signal also appear in the output due to non-linearity and unwanted coupling from the reference input to the output. However, these unwanted spectral components are well separated from the IF signal and the power is very low, so the influence is negligible.

B. Wireless Transmission

The down-converter module has been tested in a 60 GHz wireless system. The transmitter consists of a BPSK modulator and an up-converter with 56 GHz LO signal, which converts the signal (centered at 4.5 GHz) to 60.5 GHz. The baseband data is a random data stream (PN-31) generated by an FPGA board. The transmitter has about 10 dBm

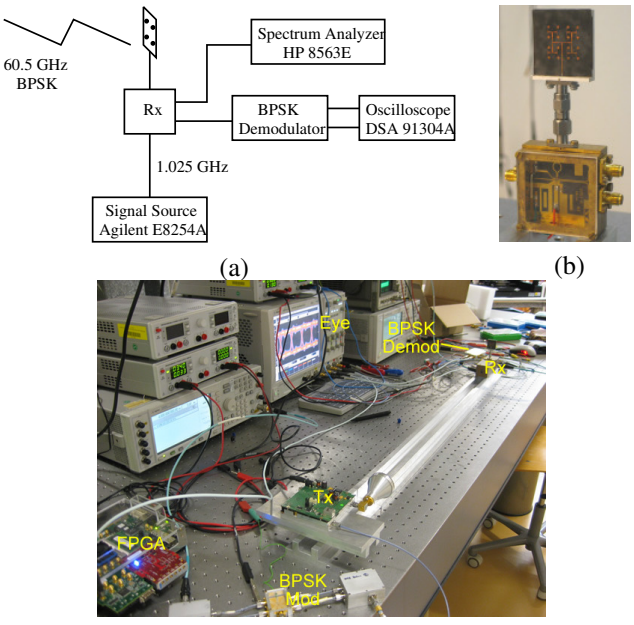


(a) (b)

Fig. 5. Down-converted 5 GHz IF spectrum in 100 MHz span (a) and 12 GHz span (b).

output power and is connected to a V-band horn antenna (20 dBi gain).

The receiver consists of the down-converter module and an analog synchronous BPSK demodulator [8]. Fig. 6 (a) shows a block diagram of the receiver. A 4×4 patch antenna is connected to the RF input of the receiver to receive the 60 GHz signal, as shown in Fig. 6 (b). The antenna is realized using the same substrate (Rogers RT Duroid 5880) as in the module, enabling further integration. It has 15 dB gain at 61 GHz, and the gain variation from 58 GHz to 63 GHz is less than 2 dB. Fig. 6 (b) shows a photo of receiver module connected with antenna.

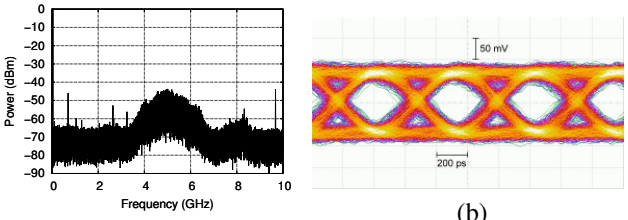


(a) (b)

(c)

Fig. 6. (a) Receiver block diagram. (b) Down-converter module with 4 × 4 patch antenna. (c) Wireless transmission setup.

For the wireless transmission, the transmitter and receiver modules were fixed on an optical rail. Fig. 6 (c) shows a photo of the test setup. By proper alignment of the transmitter and receiver, an error-free transmission could be achieved. Fig. 7 shows the received spectrum and eye diagram of the demodulated 2 Gbit/s data, which indicates



(a) (b)

Fig. 7. Down-converted BPSK spectrum and eye diagram of the demodulated data at a transmission distance of 1 meter.

error-free transmissions. The power of the IF signal from the down-converter module is about -20 dBm.

IV. Conclusion

This paper presented a wide-band 60 GHz down-converter module suited for multi-gigabit wireless transmission. The down-converter IC is realized in a low-cost, 80 GHz semiconductor technology and still achieves 5 dB conversion gain and 10 GHz IF bandwidth. To the authors' knowledge, this is the first 60 GHz down-converter realized in such low-cost technologies.

Acknowledgment

This work was funded by the German Federal Ministry of Education and Research (BMBF) under the project EASY-A. The authors thank all the project partners for the excellent cooperation.

References

[1] M. Ortner, H.P. Forstner, L. Verweyen and T. Ostermann, "A fully integrated homodyne downconverter MMIC in SiGe:C for 60 GHz wireless applications," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 145-148, Phoenix, Jan. 17-19, 2011.

[2] Y. Sun, F. Herzel, L. Wang, J. Borngraber, W. Winkler, and R. Kraemer, "An integrated 60 GHz receiver front-end in SiGe:C BiCMOS," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, San Diego, Jan. 18-20, 2006.

[3] A. Schüppen, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus, M. Averweg, "An 80 GHz SiGe production technology", *III-V Review*, vol. 14, pp. 42-46, Aug. 2001.

[4] Gang Liu, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "A 60 GHz Down-Conversion Mixer with 6.6 dB Gain and 11 GHz IF Bandwidth in an 80 GHz SiGe HBT Technology," *German Microwave Conference (GeMIC)*, Mar. 14-16, 2011.

[5] Gang Liu, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "64 to 86 GHz VCO Utilizing Push-Push Frequency Doubling in an 80 GHz f_T SiGe HBT Technology," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 239-242, New-Orleans, Jan. 11-13, 2010.

[6] Gang Liu, Andreas Trasser and Hermann Schumacher, "A 64 to 81 GHz PLL with Low Phase Noise in an 80 GHz SiGe HBT Technology," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 171-174, Santa Clara, Jan. 16-18, 2012.

[7] G. Liu, A. Trasser, A.C. Ulusoy, and H. Schumacher, "Low-loss, low-cost, IC-to-board bondwire interconnects for millimeter-wave applications", *International Microwave Symposium Digest*, pp. 1-4, Baltimore, Jun. 5-10, 2011.

[8] A.C. Ulusoy, and H. Schumacher, "A System-on-Package Analog Synchronous QPSK Demodulator for Ultra-High Rate 60 GHz Wireless Communications," *International Microwave Symposium Digest*, pp. 1-4, Baltimore, Jun.5-10, 2011.