Analog Synchronous Receiver for Short-Range Ultra-Wideband Wireless Communications

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Abstract

The need for higher speed data transfer has been continuously driven by Moore’s law in the last decades. As the data storage capabilities of user-end devices improved, it became necessary to transfer the large amount of stored data from one device to another with minimum delay, necessitating very high communication speeds.

Until today, such high speed data communication is still based on wired connections, such as a universal serial bus (USB) interface, while the available communication speed of wireless systems has lagged far behind that of wired solutions. A potential to circumvent this problem is to utilize the millimeter wave frequency bands, which would allow wireless communication speeds to be competitive to wired ones. Although there has been a lot of research in this field for more than a decade, there has been no breakthrough, and we are still “plugging-in” our devices to transfer the gigabytes of information.

In this thesis, a receiver analog frontend architecture is proposed which could provide a very low-cost solution for the implementation of ultra-wideband wireless communication networks. The proposed receiver performs the synchronization of the received signal in the analog domain, which relaxes the requirements from the digital baseband, substantially reducing the cost and complexity of the overall wireless receiver. In the thesis, design, implementation and experimental characterization of the proposed analog demodulation concept is provided. Finally, the results on a complete wireless system demonstrator with an excellent performance is presented, which includes a highly simplified digital baseband, made possible by the signal processing within the analog frontend.
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To Isabel Yağmur
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1 Introduction

1.1 Moore’s Law and More

In 1965, Intel co-founder Gordon Moore wrote an article on the future of integrated circuit (IC) technologies, pointing out that the complexity of ICs was showing a trend of doubling each year for a given cost [1]. In his article, Gordon Moore predicted the continuation of this trend in the following decades, estimating that the transistor count in an IC could be as high as several tens of thousands by 1980. The increase of complexity of ICs in the following years have shown that Gordon Moore was indeed right with his predictions, and in the meantime, these predictions led to the so called “Moore’s law”. In the most common form Moore’s law says that the number of transistors in a given silicon area doubles every two years [2]. This became a self-fulfilling prophecy, as it provides the foundation of the international technology roadmap for semiconductors (ITRS) [3], which has been driving the semiconductor industry in the last decades. Moore’s law has affected our life in many aspects as we have seen a tremendous development in IC technologies. Transistors have been scaled down, processors got faster, memories have become larger; and the number of transistors has seen such an inflation that while Gordon Moore was talking about tens of thousands of transistors in 1970s, we are talking of billions in the year 2012.

This trend of continuous increase is not only observed in memory sizes or processor speeds, but for instance can also be observed in the communication speed of wireless networks. In [4], Fettweis relates the data rate of wireless networks to Moore’s law, identifying more or less a doubling every one and a half years in the last two decades, in close relation to the increase of data storage sizes. Following this relation, for instance for short distance wireless communication links, a data rate of 10 Gb/s is claimed in 2010, and an astounding 100 Gb/s should be achieved in the year 2015. Although streaming applications and high definition (HD) displays are becoming increasingly popular, it may still be disputed whether such data rates are really needed. However, the investigations in this thesis concern the feasibility of such transmission speeds rather than the
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necessity. As a matter of fact, the feasibility is a valid concern, and the data rates of short range wireless communication links lag behind Moore’s law, while data transfer at multi-gigabit-per-second (multi-Gbps) rates still relies on wired connection.

Apart from keeping up with Moore’s law, it has been stated by several sources, including Gordon Moore himself [5], that Moore’s law is eventually coming to an end, and around 2020 a fundamental limit may be reached in terms of downscaling of transistors. This led to a new, so called “More than Moore” approach, where inclusion of new functionalities in a production technology is proposed as a means to reduce the overall system cost. This is depicted in the following figure, which is taken from a white paper published by the ITRS. The figure shows that an alternative path is recommended for the cost reduction of a system, in addition to the original “more Moore” approach. In the new, more than Moore approach, cost reduction is targeted by diversification, for instance by inclusion of more analog functions and/or passive components to the system.

![Figure 1.1: More than Moore approach as outlined in [3].](image)

Once more relating Moore’s law to wireless communication systems, a fundamental limit should also exist in terms of achievable communication speed, and at the same time
cost reduction. For instance, the implementation of analog to digital converters (ADCs) with continuously increasing speed while keeping a high resolution is considered to be a serious design challenge [6]. In some sources [7], this is even considered a system bottleneck in terms of cost and power consumption. While recent developments have shown that very high speed ADCs can be implemented with moderate resolution (∼5-bit) and reasonably low power consumption (<100 mW) [8, 9], digital signal processing at multi-Gbps data rates is still considered a major limitation, preventing the implementation of such high speed communication systems for mobile devices [10]. Keeping in mind that the available system clocks are still in the several 100 MHz range, digital processing at multi-Gbps rates requires massive parallelization [11], leading to a considerable increase of cost and complexity of the wireless system. This situation becomes more critical, when the wireless roadmap described in [4] is considered, that is, wireless links operating even in excess of 10 Gb/s data rates may eventually emerge. Therefore, there is a necessity to investigate new techniques to be able to make wireless communication systems operating at very high data rates a commodity.

## 1.2 Analog-Oriented Wireless Receiver

In this thesis, the design of a wireless receiver analog frontend (AFE) is described, which targets multi-Gbps data transmission over short distances. Following the techniques highlighted in the more than Moore approach, the proposed AFE includes more analog functions compared to a typical one. In the following figure, a wireless receiver concept is illustrated which utilizes the proposed advanced AFE, and is compared to a typical wireless receiver, which utilizes a “classical” AFE.

In the classical, digital-oriented approach, the AFE converts the received high frequency signal to a lower frequency, where it is converted to digital using high-speed and high-precision (e.g. 8-bit resolution) ADCs. In such an approach, the system benefits from the full capability of digital signal processing, so that, versatile and highly flexible systems can be realized. Thus, digital-oriented systems can address application scenarios where wide-area coverage, or operation in multi-user and non-line of sight (non-LOS) communication environments are required. However, as already mentioned, for increasing data rate these systems lose their attractiveness in terms of cost budget. The analog-oriented receiver shown in Fig. 1.2-b) can achieve cost reduction by simplifying the wireless system. Through analog carrier recovery and synchronization, which is achieved by the inclusion of an off-chip bandpass filter, the requirements on the digital
1 Introduction

Figure 1.2: Block diagram of a) a digital-oriented and b) an analog-oriented wireless receiver.

baseband is relaxed, leading to a potentially lower cost system. Such an approach only supports simple modulation formats. Through analog demodulation, the analog to digital conversion and the complete digital baseband can be realized with 1-bit resolution. This on the other hand limits the potential application scenarios to very specific cases, such as point-to-point links with exclusively LOS channel conditions.

1.3 Application Scenarios: Millimeter Wave Communications in a Glance

The proposed analog-oriented wireless receiver can address in general wireless communication scenarios that are free or not severely affected by multi-path propagation effects. Such application scenarios appear more often in the millimeter wave frequency range from 30 GHz to 300 GHz. At lower frequencies, the available communication bandwidth is comparably small, and a much wider area coverage is typically an important factor. In contrast, at the millimeter wave frequencies throughput is a more important factor, while coverage is not a strong demand due to the high path-loss and the low penetration properties of the signals. In the following, several properties of millimeter
wave frequency bands are itemized, which play a decisive role in creating application scenarios which could utilize an analog-oriented wireless receiver.

- **Large available bandwidth**: This allows communication speeds in the multi-Gbps range, using simple modulation formats such as binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK).

- **Short wave length**: High-directivity antennas can be implemented in a compact form factor.

- **Flat channel response**: By utilizing very high-gain antennas (e.g. >20 dBi\(^1\)), or targeting only very short transmission distances (e.g. <1 m), it is possible to achieve channel conditions which are only minutely affected by multi-path propagation. This alleviates the need for channel equalization, making data transmission possible without relying on high precision digital signal processing. Further considerations on the channel response are given in section 2.3.3.

- **Low interference**: As a consequence of the high path loss in the millimeter wave frequencies, interference from adjacent users is typically negligible. Furthermore, high loss through wall materials leads to room-confined transmission conditions [12], increasing the possibility for frequency re-use significantly.

- **High signal-to-noise ratio**: Owing to the well defined transmission conditions (e.g. short range or high antenna gain), typically a high signal-to-noise ratio (SNR) can be achieved on the receiver side.

The listed properties create a potential for application scenarios that can provide a very high data rate while utilizing a simple modulation format, and without the need for advanced digital signal processing. There are several frequency allocations in the millimeter wave frequencies that can be used for such applications. Especially the “industrial, scientific and medical band” (ISM band) allocated at around 60 GHz provides an excellent platform for commercial products. Multimedia streaming, wireless personal area networks, and cable replacement in vehicles are considered to be the most notable target applications which could utilize the 60 GHz ISM band [13, 14]. For instance, commercial products for uncompressed HD-video streaming have already emerged [15]. A further overview of realistic application scenarios are presented in [16]. Particularly, the wireless data kiosk and in-car entertainment scenarios described in [16] could benefit

\(^1\)In such a case antenna alignment needs careful consideration.
from the proposed analog-oriented wireless receiver concept, as both applications are limited to very short distances (<1 m), and to well-defined LOS channels.

In addition to the 60 GHz ISM band, a total of 10 GHz bandwidth allocated in the “E-band” (71-76 GHz & 81-86 GHz bands) [17, 18], and the frequencies allocated in the 92-95 GHz band [19] provide further potentials for point-to-point, multi-Gbps wireless communication scenarios. There is also increasing interest in the sub-millimeter wave frequencies, i.e. 200 to 300 GHz range, for highly directive wireless communications with data rates in excess of 10 Gb/s [20].

1.3.1 The Wireless Data Kiosk Scenario

The guiding application scenario in this thesis is the wireless data kiosk scenario, however the results and the approaches can be generalized to other applications. The data kiosk scenario was investigated within the framework of the German federal ministry of science and education (BMBF) funded project EASY-A (enablers for ambient services and systems - part A 60 GHz broadband links) [21]. The goal of the project was to find solutions to meet the increasing demand of higher data rates for wireless communication networks at short and medium distances.

![Diagram of the data kiosk scenario](image)

Figure 1.3: Illustration of the data kiosk short range wireless communications scenario.

The data kiosk scenario is illustrated in Fig. 1.3. It targets data transmission at multi-Gbps data rate from a fixed terminal to a mobile terminal at short distances. The fixed terminal can for instance be a vending machine placed in public areas, that provides information or sells products such as movies or music. The mobile terminal is at the user-end, and consists of devices such as smart-phones or notebook PCs. The wireless data kiosk scenario utilizes the 60 GHz ISM band, while only LOS communication with a transmission distance below one meter is considered. Therefore, the 60 GHz wireless
1.3 Application Scenarios: Millimeter Wave Communications in a Glance

Table 1.1: Specifications of the wireless data kiosk scenario

<table>
<thead>
<tr>
<th>Modulation</th>
<th>BPSK</th>
<th>QPSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Frequency</td>
<td>61.56 GHz</td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>4.32 GHz</td>
<td></td>
</tr>
<tr>
<td>Symbol Rate</td>
<td>3.456 GS/s</td>
<td></td>
</tr>
<tr>
<td>Code Rate</td>
<td>3/4</td>
<td></td>
</tr>
<tr>
<td>Net Data Rate</td>
<td>2.5 Gb/s</td>
<td>5 Gb/s</td>
</tr>
</tbody>
</table>

The channel can be assumed quasi-static, and without severe multi-path propagation affects. The highest supported net data rate is 5 Gb/s, while the data rate can be increased to 10 Gb/s if polarization multiplexing is employed. Such high data rates would result for instance in download of an HD-movie within 10-30 seconds. The specifications of the wireless data kiosk scenario are listed in Table 1.1.

As the receiver is incorporated within a mobile and battery operated device, cost, complexity and power consumption are very critical design criteria. In order to allow a low-cost receiver architecture, a simple modulation format is chosen, namely single-carrier QPSK modulation. This choice is made possible by the large available bandwidth in the 60 GHz ISM band. The system bandwidth follows the IEEE 802.15.3c and ECMA-387 channelization plans [23, 24], where bonding of two of the four standardized channels yields a total bandwidth of 4.32 GHz. With a guard band size of 20% that accounts for the slopes of pulse shaping filters, a symbol rate of 3.456 GHz is obtained. In addition to QPSK, BPSK modulation is supported as well, and the resulting net data rates are 5 Gb/s and 2.5 Gb/s for QPSK and BPSK modulations, respectively.

Table 1.2: Example link budget for the kiosk scenario

<table>
<thead>
<tr>
<th>Transmitted Power</th>
<th>10 dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver Noise Figure</td>
<td>10 dB</td>
</tr>
<tr>
<td>Total Antenna Gain</td>
<td>18 dBi</td>
</tr>
<tr>
<td>Effective Bandwidth</td>
<td>3.45 GHz</td>
</tr>
<tr>
<td>Path Loss (1 m)</td>
<td>69 dB</td>
</tr>
<tr>
<td>Thermal Noise</td>
<td>-78.6 dBm</td>
</tr>
<tr>
<td>SNR</td>
<td>27.6 dB</td>
</tr>
</tbody>
</table>

\(^2\)The feasibility of polarization multiplexing is investigated in [22].
1 Introduction

An example link budget calculation for the data kiosk scenario is presented in Table 1.2. When the link budget calculations are taken into account, implementation of an analog receiver frontend for the 60 GHz kiosk scenario seems highly feasible, even in low-cost technologies.

1.4 Thesis Outline

In this thesis, an analog synchronous receiver architecture is proposed, that relaxes the ADC and digital signal processor (DSP) requirements by means of analog carrier recovery and synchronization. Throughout the thesis, the implementation of the individual components, as well as the RF-modules are described in detail. Furthermore, results on system level characterization experiments are presented, including a wireless system demonstrator with a dedicated digital baseband, realized completely in 1-bit resolution.

The thesis is organized as following: In chapter 2, existing approaches in the literature are reviewed, and the proposed receiver architecture is described. Additionally, system simulations and feasibility investigations of the proposed receiver architecture are presented. In chapter 3, the prototype implementation of the analog synchronous demodulator is described in detail. The experimental validation of the realized demodulator is presented in chapter 4. In chapter 5, the results on 60 GHz wireless transmission experiments are presented, demonstrating the viability of the proposed wireless receiver approach. Finally, in chapter 6, the first results towards a miniaturized receiver implementation are described as an outlook, and the thesis is concluded in chapter 7.
2 Analog Synchronous Receiver Architecture

In this chapter, first a literature overview is given presenting some of the recent work on receivers for multi-Gbps wireless communication networks. Following this introductory overview, the proposed analog synchronous receiver architecture is presented, and the underlying analog feed-forward carrier recovery concept is explained. Furthermore, system level simulation results are presented demonstrating the feasibility, and estimating the performance of the proposed receiver.

2.1 Recent Work on Multi-Gbps Wireless Receivers

In the recent years, there has been increasing amount of research targeting multi-Gbps data rates for wireless communication networks. Wireless links operating in the submillimeter wave frequency range achieve data transmission speeds approaching that of fiber-optical communication links. For example, in [25], a 25 Gb/s wireless transmission experiment is presented operating at 220 GHz. Considering the data kiosk application scenario at 60 GHz, one can find numerous examples in the literature describing AFE implementations with sufficient performance, for instance [26] and [27] are notable ones.

In accordance with the introduction given in chapter 1, the main problem in the aforementioned or other similar AFE implementations is that the carrier acquisition and synchronization becomes very challenging at such high communication speeds, especially when mobile devices are under consideration. For instance, the same local oscillator (LO) source is used at the receiver and the transmitter in [25], relying on wired connection. Although [25] demonstrates that it is possible to implement “classical” AFEs capable of achieving such high data rates, a real wireless solution is not presented due to the lack of synchronization. Therefore, such AFEs rely on high-speed digital signal processing at the baseband for synchronization, making high-speed and high-precision analog to digital conversion mandatory. On the other hand, there are only very limited examples
of digital baseband implementations which are able to handle the targeted transmission speeds in real-time\(^1\). One such example can be found in [30, 31], where an optical data transmission system is presented using custom designed ADCs and application specific integrated circuits (ASICs). The authors demonstrate QPSK transmission at a data rate of 10 Gb/s by performing synchronization in the digital domain, achieving a bit error rate (BER) better than \(10^{-5}\). The downside is that the custom designed ICs used for these experiments consume a total of 12.8 watts of power, and occupy an IC area in excess of 35 mm\(^2\), making them not an option for a low-cost system.

There are a few examples in the recent literature, which propose different approaches for the realization of multi-Gbps wireless systems. Following the same guiding motivation as in this thesis, the authors propose to relax the digital system requirements by performing carrier synchronization in the AFE. For example, an E-band QPSK receiver is presented in [32], which performs analog synchronization utilizing a Costas loop carrier recovery circuit. In this work, the authors demonstrate analog demodulation capability up to a data rate of 2.5 Gb/s without relying on digital signal processing. Similarly, a simple feed-forward carrier recovery concept is proposed in [33] and [34] for QPSK and BPSK signals, respectively. Although no experimental results are presented, the high simplicity of this approach could prove very promising for low-cost wireless receiver implementations. In [35] and [36], simple differential demodulation for QPSK and BPSK signals are demonstrated, while in [35], the authors show analog demodulation capability up to a data rate as high as 10 Gb/s. As a different approach, mixed signal baseband modem circuits for BPSK, QPSK and minimum-shift keying (MSK) signals are presented in [37], [10] and [38], respectively. These examples utilize additional analog signal processing with reduced ADC resolutions.

In essence, a common argument that can be observed in these examples is that ADCs and DSPs are considered a bottleneck for the implementation of a multi-Gbps wireless communication system. In agreement with the discussion provided in the introduction chapter, it is similarly argued that one can achieve multi-Gbps wireless transmission speed in the millimeter wave frequency bands, without relying on high speed and precision digital signal processing. Further discussion of these examples, as well as a performance comparison to the receiver described in this thesis can be found in section 4.4.

\(^1\) Examples which utilize off-line signal processing can be found in the literature, demonstrating wireless data transmission speeds above 10 Gb/s [28, 29].
2.2 The Proposed Receiver Architecture

The proposed receiver AFE in this thesis utilizes a topology similar to the ones presented in [33] and [34]. It is based on a very simple feed-forward carrier recovery approach, and exhibits a much lower complexity compared to the other examples described above. It does not require any phase-locked loop (PLL) synchronization circuitry such as the Costas loop carrier recovery presented in [32], which brings issues like the need for separate phase and frequency acquisition, or precise gain control. Moreover, there is no need for an accurate true-time delay control, as would be required for differential demodulators described in [35] or [36]. The proposed analog demodulation is performed independent of the high speed digital circuitry, therefore the complete AFE can be implemented in a lower cost technology, compared to the sub-100-nanometer CMOS mixed-signal modem implementations described in [37, 38, 10]. The proposed receiver is simple, and can be implemented using low-cost techniques. Besides, it introduces the additional feature of phase noise suppression, which is a substantial advantage that could further reduce the complexity of the wireless system. These properties, and the operation principle will be detailed in the following.

![Block diagram of the proposed analog synchronous receiver.](image-url)

Figure 2.1: Block diagram of the proposed analog synchronous receiver.

The block diagram of the proposed receiver is displayed in Fig. 2.1. It is a superheterodyne receiver with an intermediate frequency (IF) of around 5 GHz. The received
60 GHz QPSK signal is first amplified by a low noise amplifier (LNA), and then down-converted to the IF, where it is divided into two branches. In one branch the signal goes through carrier recovery, while in the other branch it is directly fed to the demodulators. The carrier recovery method is based on frequency multiplication, which generates a modulation-free harmonic of the desired carrier signal. Also known as the “times-n” carrier recovery, n representing the PSK modulation order, this method was classically used in early analog receivers within PLL synchronization circuits [39]. The main difference in the proposed receiver is that the carrier recovery is without any feedback, i.e., it is arranged in a feed-forward manner.

In the carrier recovery branch, the QPSK signal is quadrupled in order to remove the modulation content, generating the fourth harmonic of the carrier signal. This signal is subsequently bandpass filtered and divided by four, regenerating the IF without any feedback loop. For the division, static frequency dividers are utilized which also generate the carrier signal in quadrature as required for QPSK demodulation. Finally, the quadrature components of the carrier signal go through phase shifters in order to compensate the delay experienced by the carrier recovery. The phase shift to be compensated has a fixed and deterministic value, depending only on the implementation of the carrier recovery components in the receiver, without being affected by the wireless channel or the transmitted signal. The recovered carrier is directly fed to the demodulators, and synchronously demodulated complex baseband symbols are acquired at the output. For further clarification, the carrier recovery method can be explained as following: If we consider a simple representation of a QPSK signal

\[
s(t) = S_C(t) \cos\left[\omega_{IF}t + \frac{\pi(2m-1)}{4} + \phi_{in}(t)\right],
\]

(2.1)

where \(S_C(t)\) is the amplitude, \(m\) is the modulation content which equals 0, 1, 2 or 3, while \(\omega_{IF}\) and \(\phi_{in}(t)\) represent the carrier frequency and phase to be recovered. Quadrupling this signal results in

\[
s^4(t) = \frac{3S_C^4(t)}{8} + \frac{S_C^4(t)}{2} \cos[2\omega_{IF}t + \frac{\pi(2m-1)}{2} + 2\phi_{in}(t) + \varphi_1]
+ \frac{S_C^4(t)}{8} \cos[4\omega_{IF}t + \pi(2m-1) + 4\phi_{in}(t) + \varphi_1].
\]

(2.2)

Here, \(\varphi_1\) is the phase shift caused by the frequency quadrupling, and has a constant value. In the next step, the quadrupled signal goes through a bandpass filter, centered
2.2 The Proposed Receiver Architecture

at $4\omega_{IF}$. This reduces (2.2) to

$$g(t) = G_C(t) \cos[4\omega_{IF} t + \pi(2m - 1) + 4\phi_{in}(t) + \varphi_2],$$

(2.3)

while $\varphi_2$ is the total phase shift caused by the frequency quadrupling and the bandpass filtering, and $G_C(t)$ represents the excess envelope fluctuations of the filtered signal. These fluctuations are strongly dependent on the bandwidth of the bandpass filter being used in the carrier recovery. Inserting the values of $m$ into (2.3), and making use of the periodicity of the cosine function, we arrive at

$$g(t) = -G_C(t) \cos[4\omega_{IF} t + 4\phi_{in}(t) + \varphi_2],$$

(2.4)

and after frequency division by four, we obtain

$$y(t) = Y_C \cos[\omega_{IF} t + \phi_{in}(t) + \varphi_3].$$

(2.5)

Equation (2.5) represents the desired carrier signal with the correct frequency but a constant phase error of $\varphi_3$, which is to be compensated by the phase shifters. It is assumed that the remaining amplitude fluctuations after the bandpass filtering are canceled by the frequency dividers, as they are only sensitive to the zero crossings of the input signal. Therefore, the output signal has a constant amplitude of $Y_C$.

The benefits of the proposed receiver with the simple carrier recovery concept can be summarized as following:

- **1-bit digital baseband resolution**: As the carrier recovery is performed in the analog domain, the need for digital frequency acquisition and constellation adjustment is eliminated. Therefore, the requirements from the digital baseband are strongly simplified for specific application scenarios. As will be experimentally shown in chapter 5, the complete digital baseband can be implemented in 1-bit resolution.

- **Low hardware effort**: Even in a “digital-oriented” system, an analog frontend is required, which should convert the received high frequency signal to a manageable range for the digital circuitry (typically baseband). For instance, when compared to a highly efficient sliding IF receiver presented in [40], the only additional components required for the proposed receiver are the frequency quadrupler, the phase shifters and the bandpass filter. Therefore, the proposed receiver requires only
very little additional hardware effort compared to other approaches presented in the literature.

- **Phase noise suppression**: The proposed receiver has the additional unique advantage of phase noise suppression due to its feed-forward carrier recovery architecture. As the recovered carrier is extracted from the modulated signal itself, the instantaneous phases of the recovered carrier and the modulated signal are almost the same, including undesired phase fluctuations. Therefore, the accumulated phase noise from the receiver and the transmitter frequency synthesizer can be suppressed during demodulation. This feature, and its limitations are detailed in section 2.3.2, and experimental verification results are presented in section 4.3.6.

Apart from the advantages itemized above, a clear disadvantage of the proposed receiver is that a relatively sharp bandpass filter is required centered at the fourth IF harmonic. Therefore, a system-on-chip (SoC) implementation of the receiver is not feasible due to the required bandwidth as shown in section 2.3.1. Within this thesis, a very compact and narrow-band bandpass filter is described, which is included in the receiver package by simple integration techniques, mitigating this disadvantage. The details on this filter and the integration technique are presented in chapter 3.

### 2.3 System Level Simulations

System level simulations of the proposed receiver are performed in order to determine its feasibility and the expected performance. The main simulation environment is the Agilent Advanced Design System (ADS) Ptolemy, which is a powerful simulation tool to characterize complete systems using behavioral circuit models. An additional Matlab interface is included in order to introduce measured channel responses to the simulations. The channel responses in Matlab were provided by the Fraunhofer Heinrich Herz Institute within the collaborative research project EASY-A [21].

The block diagram of the simulation setup is shown in Fig. 2.2. An ideal transmitter generates the modulated signal at 61.56 GHz, using two independent pseudorandom bit pattern generators. Ideal root-raised-cosine (RRC) filters with a roll-off factor of 0.35 are used in the transmitter and the receiver as pulse shaping filters, in order to emulate band-limited transmission, compliant with the 60 GHz ISM-band spectral regulations. The ideal modulated signal can be exported to Matlab, where the data kiosk channel can be applied, or it is directly fed to the receiver. Additive white Gaussian noise (AWGN) is
2.3 System Level Simulations

Figure 2.2: Block diagram of the system simulation setup.

inserted to the signal before feeding it to the receiver in ADS, while the signal amplitude is carefully calibrated to achieve accurate SNR values.

In Fig. 2.2, the proposed receiver is displayed in a generic way, where N represents the PSK modulation order. For testing the BPSK performance (N = 2), one of the data branches is simply disconnected. The frequency multiplication and division are performed using the existing harmonic generator component in ADS, which generates only the harmonic component of the desired order. An additional processing step is the differential encoding and decoding, as seen in the block diagram. The differential encoding is included in order to resolve the $2\pi/N$ phase ambiguity, which is an inherent property of carrier tracking loops in general [41]. The phase ambiguity means that the initial phase of the recovered carrier is unknown, and it may settle to any of the phase states of the modulated signal. By differentially encoding the data stream, the phase ambiguity is resolved with a relatively low SNR penalty of around 0.6 dB [41, 42]. An alternative way of ambiguity removal is implementing training sequences in the beginning of each data frame. This technique is not used in the simulations, but it is utilized in the wireless demonstration experiments in addition to differential encoding, which are
presented in chapter 5.

As a final results of the simulations, BER curves are acquired via Monte Carlo simulations, by direct comparison of the transmitted and received symbols for swept AWGN density. For all cases the symbol rate, $f_s$, equals 3.5 GS/s, and the IF is fixed at 5 GHz. The simulations are performed for a duration of $10^6$ symbols, and the time step used in the simulations results in 30 points per symbol.

### 2.3.1 Influence of the Carrier Recovery Bandwidth

In section 2.2, the quadrupled QPSK signal is described in (2.2). Considering this equation, it can be seen that additional undesired terms are present, such as a second harmonic component, or the envelope fluctuations represented by $S_C^4(t)$. In the simulations, the second harmonic signal is not existent due to the nature of the harmonic generator component, and in a realistic case it is not very critical as it can be easily eliminated. On the other hand, the function $S_C(t)$ has an impact on the carrier recovery performance, as its influence is raised by an order of four (two for BPSK). Therefore, a bandpass filter with a sufficiently narrow bandwidth is required in order reduce the influence of the envelope fluctuations.

In an intuitive approach, one may assume a very direct solution to resolving the envelope fluctuations would be using a limiting amplifier, rather than a sharp bandpass filter. Although this approach is valid, the amplitude fluctuations may in some cases be so high that an amplifier with a very high sensitivity would be required. Furthermore, due to the high peak to minimum amplitude ratio of this signal, severe amplitude modulation to phase modulation (AM to PM) conversion is as well expected. In order to further clarify the need for a sharp bandpass filter, the simulated input QPSK signal, and the resulting fourth harmonic signal after quadrupling and bandpass filtering are displayed in Fig. 2.3.

In Fig. 2.3-a), the input signal is displayed which is a 3.5 GS/s (7 Gb/s) modulated, differentially encoded QPSK (DE-QPSK) signal. As seen in Fig. 2.3-b), a strong carrier signal is generated at four times the IF by frequency quadrupling. The envelope fluctuations appear as an increase of the noise floor, and additional distinct spurious components are observed at frequencies $4f_{IF} \pm f_S$. When the corresponding time domain signal is examined, it is seen that the carrier signal practically “fades” for certain periods of time, making direct division or limiting not possible. Bandpass filtering eliminates this fading behavior by suppressing most of the undesired spurious spectrum, as seen in Fig. 2.3-c). For these simulations, a bandpass filter with a 3-dB bandwidth of
### 2.3 System Level Simulations

#### Figure 2.3: Simulated input QPSK signal and the resulting quadrupled fourth harmonic signal in frequency and time domain. The resolution bandwidth (RBW) equals 1 MHz for the frequency domain representations.

500 MHz is used, which sufficiently clears the carrier signal spectrum, resulting in a time domain signal which can be directly frequency divided without further amplification.

Theoretically, offset-QPSK could be utilized to reduce the envelope fluctuations by avoiding $180^\circ$ phase transitions. On the other hand, this would require the implementation of a half-period symbol delay in the receiver and the transmitter, increasing the complexity of the wireless system and is not considered here. The investigations within the thesis are limited to DE-QPSK and DE-BPSK modulation formats only.

In order to determine the required bandwidth of the bandpass filter, BER simulations are performed for different bandwidth values. All the filters are ideal 3rd order Chebyshev bandpass filters with a suppression of 20 dB at twice the passband. The resulting BER versus SNR-per-bit curves are displayed in Fig. 2.4, for DE-QPSK and
DE-BPSK modulations. The ideal DE-QPSK and DE-BPSK curves are also included for comparison, which are acquired by using an ideal carrier signal for demodulation at the receiver.

![Simulated BER for different 3-dB bandwidth values of the bandpass filter, for a) DE-QPSK and for b) DE-BPSK.](image)

It is seen from the figure that the performance of the analog carrier recovery depends strongly on the carrier recovery bandwidth. BER floors are observed for larger filter bandwidths, indicating that data-pattern dependent effects dominate, such as the jittering of the recovered carrier signal. Therefore, for a reasonable receiver performance the carrier recovery bandwidth has to be chosen sufficiently small. As seen in Fig. 2.4-a) for DE-QPSK modulation, a close to ideal performance is achieved for a filter bandwidth of 100 MHz. This is a very stringent requirement, as 100 MHz means a relative bandwidth (RBW) of 0.5% at 20 GHz. This renders the realization of a SoC receiver impractical for QPSK modulation. On the other hand, the bandwidth requirement is much more relaxed for DE-BPSK modulation, although the spectral efficiency is only halved. Even for a filter bandwidth of 1 GHz (RBW of 10%), the analog receiver performs close to an ideal receiver.

An alternative approach to relax the demanding filter requirement would be to reduce the symbol rate, while keeping the signal bandwidth constant. This would still result in a channel-compliant signal spectrum, whereas the available bandwidth would be utilized in a non-optimum way. As an example case, the BER performance for DE-QPSK modulation is simulated, when the symbol rate is reduced by 10% to 3.15 GS/s, while the 3-dB bandwidth of the RRC filters are fixed at 1.75 GHz. The results are presented...
in Fig. 2.5, and the results from Fig. 2.4 are included as well for a direct comparison.

Figure 2.5: Simulated BER for different 3-dB bandwidth values of the bandpass filter in case of 10% reduced symbol rate

As seen in this figure, 10% reduction of the date rate already relaxes the component requirements drastically. Data pattern dependant effects observed in the high SNR region mostly disappear for a filter bandwidth of 500 MHz, and a significant improvement in the BER performance is achieved. However, for a larger filter bandwidth of 1 GHz, the receiver still shows poor performance in the high SNR region. Nevertheless, based on these results it can be concluded that non-optimum usage of the channel bandwidth is a viable solution for the analog-oriented wireless system, as this would greatly relax the bandpass filter requirement, simplifying the receiver implementation.

Experimental results on the carrier recovery are presented in section 4.3.1. Further results are provided in the Appendix A, where a dedicated BPSK carrier recovery IC is described which performs carrier recovery without an off-chip BPF, in consistence with the simulation results presented in this section.

2.3.2 Phase Noise Suppression

The proposed receiver exhibits a very promising feature of phase noise suppression, owing to the feed-forward nature of the carrier recovery method. In other words, the recovered carrier is extracted from the modulated signal, and is fed to the demodulators without any feedback. Therefore, the instantaneous phases of the recovered carrier and
the modulated signal are the same, excluding the modulation content. However, in a realistic case, the recovered carrier not only experiences a phase shift, which can be easily compensated, but also a certain amount of true-time delay. On the one hand, this time delay can still be seen as a phase shift because the recovered carrier is a periodic, continuous time signal; on the other hand, a large amount of time delay will lead to a reduced phase noise coherence between the recovered carrier and the modulated signal. Considering this, a better representation of the recovered carrier in comparison to (2.5) is

\[ y(t) = Y_C \cos[\omega_{IF}(t + \Delta t) + \phi_{in}(t + \Delta t) + \varphi_N(t + \Delta t) + \varphi_{CR}] \]  

(2.6)

Here, \( \Delta t \) represents the true-time delay experienced through the carrier recovery, while the additional term \( \varphi_N \) stands for the accumulated phase noise from the transmitter and the receiver frequency synthesizer. A further phase term \( \varphi_{CR} \) is included, which accounts for the additional phase distortion that could occur within the carrier recovery, for instance by the bandpass filtering. Following that, the total phase amount to be compensated equals

\[ \varphi_{tot} = \omega_{IF}\Delta t + \varphi_{CR}, \]

(2.7)

while \( \varphi_{tot} \) is still a fixed and deterministic value, which depends only on the implementation of the carrier recovery components. Due to the quasi-static nature of the wireless channel, it can also be assumed that

\[ \phi_{in}(t + \Delta t) \approx \phi_{in}(t), \]

(2.8)

which reduces (2.6) to

\[ y(t) = Y_C \cos[\omega_{IF}(t) + \phi_{in}(t) + \varphi_N(t + \Delta t) + \varphi_{tot}] \]

(2.9)

Thus, the only parameter affected by the true-time delay would be the phase noise suppression, and only for a sufficiently small \( \Delta t \) strong phase noise suppression can be achieved. For a complete suppression of the accumulated phase noise, the true-time delay needs to be compensated as well.

In order to determine the influence of the delay error between the recovered carrier and the modulated signal, BER simulations are performed in the presence of phase noise. The delay error between the recovered carrier and the modulated signal is varied.
through an artificial delay line. To emulate a noisy carrier, the phase noise modeling tool available in ADS Ptolemy is used. In this tool, the phase noise is modeled as a sum of tones that modulate the phase of the main signal tone. These tones are distributed in random frequency steps within the frequency offset range and the corresponding power levels specified by the user. In these simulations, a total of 1000 tones are inserted to the main carrier to acquire accurate results. A box-shaped phase noise profile is used, approximating a frequency stabilized signal source with a certain loop bandwidth and a constant relative noise power level within this bandwidth. Two cases are considered: For the first case the loop bandwidth is kept constant, and the noise level is swept; while for the second case, the noise power is kept constant, and the loop bandwidth is swept.

![Figure 2.6](image-url)

Figure 2.6: Simulated spectrum of the noisy carrier signal at the receiver for a) a fixed loop bandwidth and swept noise power, and for b) a fixed noise power and swept loop bandwidth. For all simulations the carrier frequency equals 56.56 GHz giving an IF of 5 GHz.

The simulated noisy carrier signals are displayed for both cases in Fig. 2.6. In Fig. 2.6-a), the loop bandwidth is fixed at 1 MHz, and the noise power density relative to the carrier within the loop bandwidth is swept from -70 dBc/Hz to -80 dBc/Hz. For the second case displayed in Fig. 2.6-b), the total noise power within the loop bandwidth is fixed at -15 dBc (single sideband), while the loop bandwidth is swept from 1 MHz to 10 MHz. The phase noise profile for all cases is adjusted to have a 20 dB/decade drop of the noise power level outside the given loop bandwidth.

The resulting BER curves are presented in Fig. 2.3.2-a) and -b), for swept delay error.
The modulation type is DE-QPSK with a symbol rate of 3.5 GS/s, the SNR-per-bit is set to 25 dB, and the carrier recovery bandwidth is fixed at 500 MHz.

![Simulated BER for different delay errors in case of a noisy downconversion oscillator](image)

Figure 2.7: Simulated BER for different delay errors in case of a noisy downconversion oscillator. The phase noise profile is varied for a) a fixed loop bandwidth and swept noise power, and for b) a fixed noise power and swept loop bandwidth.

As seen in the figure, when the delay error is sufficiently small, a strong phase noise suppression can be achieved leading to a drastic improvement of the BER performance. It can be observed in Fig. 2.7-a) that even very strong phase noise can be suppressed, such as the case with a noise level of -70 dBc/Hz within the 1 MHz bandwidth. For this case, the total noise power exceeds that of the carrier signal, and still a good BER performance can be achieved if the delay error is sufficiently small. On the other hand, examining Fig. 2.7-b), it is seen that the phase noise suppression characteristic is strongly affected by the loop bandwidth. When the noise power is concentrated around the carrier, meaning that the synthesizer has a small loop bandwidth, a large amount of delay error can be tolerated. On the contrary, if the noise is spread over a large frequency span, a low delay error is required to be able to suppress the noise components that are spectrally far from the carrier signal. This is in agreement with the qualitative understanding of the phase noise suppression mechanism, and the noise bandwidth that can be suppressed is inversely proportional to the delay error. For instance, as the loop bandwidth is increased by a factor of 10 from 1 MHz to 10 MHz, the delay error has to be reduced approximately by the same factor to achieve an equal BER performance, as can be seen in Fig. 2.7-b).
In section 3.3.2, it is shown that the estimated delay within the carrier recovery is less than 2 ns. If we consider state of the art 60 GHz frequency synthesizers in the literature [43, 44, 45], the loop bandwidth is typically chosen smaller than 1 MHz. Considering the small delay error, this would mean that a very strong phase noise cancellation can be achieved, even if the noise level is very high. On the other hand, when a synthesizer with a larger loop bandwidth is utilized, it is expected that the phase noise suppression degrades. However, the noise level in such synthesizers is usually much lower. For example, the synthesizer presented in [46] exhibits a loop bandwidth of 50 MHz, while the noise level is as low as -106 dBc/Hz at an offset frequency of 1 MHz.

As a conclusion, it can be stated that the presented simple feed-forward carrier recovery concept can improve the performance of the wireless system through the phase noise suppression capability. Furthermore, the complexity of the wireless system can be reduced by relaxing the frequency synthesizer requirements, keeping in mind that a very high noise level can be tolerated, as long as the loop bandwidth is kept sufficiently small.

2.3.3 Influence of the Wireless Channel

The dispersion through the wireless channel plays a critical role on the validity of the proposed analog-oriented wireless receiver concept. The presented simple receiver can only be utilized when it is assured that multi-path propagation will not lead to significant inter-symbol-interference (ISI), and will not cause severe frequency domain distortions.

Investigations in the literature indeed show that the typical 60 GHz indoor channel is not multi-path free [47], however, the root mean square (RMS) delay spread through the wireless channel depends strongly on the measurement conditions and the antenna directivity. For instance, ray tracing simulations reported in [48] show RMS delay spread values ranging from below 1 ns to 100 ns for different configurations of the antenna locations, antenna gain and misalignment. Therefore, in order to verify that it is possible to transmit multi-Gbps signals wirelessly with the simple receiver concept, channel measurement campaigns were performed in the framework of the collaborative research project EASY-A. The channel responses are acquired under measurement conditions resembling the data kiosk scenario described in section 1.3.1. The transmit antenna is fixed and placed at a height of 78 cm, while the receive antenna is hand-held directly facing the transmit antenna at a similar height. Open-ended wave guides with a moderate gain of approximately 8 dBi are used as antennas on both sides. The channel
responses are captured with a vector network analyzer (VNA) in 4MHz steps, while only strict LOS conditions are taken into consideration. More detailed information on these measurements can be found in [22].

![Figure 2.8](image.png)

Figure 2.8: Channel frequency responses for the 60 GHz data kiosk scenario for 0.5 m and 1 m distances and a center frequency of 61 GHz. Channel 1 and 3 are measured with well aligned antennas, Channel 2 and 4 are measured with angular mismatch and a disturbing person in the LOS vicinity.

In Fig. 2.8, four example channel frequency responses (CFRs) are shown which are extracted from the measurements within the validity bandwidth of 13.824 GHz. For the shown CFRs, the center frequency equals 61 GHz. The distance between the receive and the transmit antennas equals 0.5 m for the channel 1 and 2 responses, while the channel 3 and 4 are measured at a distance of 1 m. For channel 1 and 3 the antennas are well aligned, while channel 2 and 4 are measured with a deliberate angular mismatch (∼ 27°), and a disturbing person in the vicinity of LOS resulting in noticeable frequency selectivity.

In order to determine the potential influence of the 60 GHz channel, BER simulations are performed after passing the signal through the extracted channel responses from the measured data. The resulting BER curves are displayed in Fig. 2.9 for the four CFRs displayed in Fig. 2.8. The simulations are performed for DE-QPSK modulation with a rate of 3.5 GS/s, and a fixed carrier recovery bandwidth of 100 MHz. The BER curve for the simple AWGN channel is also included in the figure for comparison. It can be seen
2.3 System Level Simulations

Figure 2.9: Simulated BER for four different measured 60 GHz LOS channel responses.

from the results for channel 1 and 3 responses that as long as the antenna alignment is
good enough, the channel is relatively flat and does not cause any noticeable penalty for
both distances. On the other hand, for channel 2 and especially for channel 4 responses,
there is a slight degradation of the system performance. Nevertheless, it can still be
concluded that data transmission is possible with the presented analog demodulation
method, without relying on digital channel equalization filters. The slight SNR penalty
observed in Fig. 2.9 is in principle negligible, considering the high SNR of the received
signal based on the link budget calculations presented in Table 1.2.

2.3.4 Summary of the Simulation Results

The simulation results presented in this chapter confirm that the proposed analog-
oriented receiver is feasible. The sharp bandwidth requirement within the carrier re-
covery necessitates external bandpass filtering, whereas the required bandwidth can
be relaxed by reducing the system rate. The phase noise suppression feature is very
promising, and considering the phase noise profile of a realistic frequency synthesizer, a
significant improvement in the system performance should be expected. Finally, simu-
lations using measured channel data confirm that the wireless data kiosk channel is not
severely effected from multi-path propagation, and reliable data transmission is possible
at multi-Gbps rate using moderate gain antennas.
3 Synchronous Demodulator Implementation

In this chapter, detailed information is given on the implementation of the individual components for the presented analog synchronous demodulation. All the IC components are characterized individually, whereas a combined version is realized as well, which includes all the necessary active building blocks. As a final implementation, a demodulator module is realized that includes the required bandpass filter as an off-chip component within its package, and performs synchronous demodulation of QPSK signals centered at around 5 GHz.

3.1 IC Components

3.1.1 Technology

The active components required for the synchronous demodulation are realized as integrated circuits in Telefunken Semiconductors SiGe2RF technology. SiGe2RF is a double heterojunction bipolar transistor (HBT) technology, with a minimum lithographic resolution of 0.8 µm. The npn-HBTs have a maximum specified transit frequency ($f_T$) of 80 GHz, and a maximum frequency of oscillation ($f_{max}$) of 90 GHz. The collector-emitter breakdown voltage (BVCE0) of the transistors is 2.4 V. Although SiGe2RF is not a state of the art technology, it is low cost, owing to the relaxed lateral scaling. Furthermore, the available transistors have sufficient performance for the synchronous demodulator design, considering the highest operation frequency is 20 GHz.

The SiGe2RF technology features three metal layers, as well as scalable inductor, metal-insulator-metal (MIM) capacitor and transistor models. The IC designs are performed using the foundry provided models in Agilent ADS.


3 Synchronous Demodulator Implementation

3.1.2 Bias Circuit

The schematic of the basic bias circuit used in the designed ICs is displayed in Fig. 3.1. The bias circuit is described here once, and will be omitted in the following IC descriptions for simplicity. It consists of a commonly used current mirror structure with added base resistors, $R_{B,1}$ and $R_{B,2}$, to reduce signal leakage in case the input is applied to the base of $T_1$.

![Schematic of the basic bias circuit used in the designs.](image)

The transistor $T_2$ is chosen to be as small as possible to reduce the power dissipation within the bias circuit. The sizes of the transistors are defined by the emitter length $L_E$, while the emitter width is fixed at 0.8 $\mu$m. Based on the collector current of $T_1$, the values of the base resistors and the size of $T_2$ are chosen using the following equality

$$\frac{L_{E,1}}{L_{E,2}} = \frac{R_{B,2}}{R_{B,1}} \approx \frac{I_{C,1}}{I_{C,2}}. \quad (3.1)$$

For all designs, $R_{B,1}$ is chosen to be at least 1 k$\Omega$ to provide a sufficiently high impedance to prevent signal leakage. Finally, the value of $R_C$ follows from $V_C$ and $V_{REF}$.

3.1.3 Frequency Quadrupler

The frequency quadrupler needs to generate a fourth harmonic signal from the wide-band modulated input signal centered at the IF. In principle, there are many ways of generating the desired harmonic component, for instance by simply exploiting device non-linearities. Naturally, not all solutions are equally efficient. For example, it is claimed and experimentally supported in [49] that the most efficient frequency multiplier topology is the push-push type. For the application in question however, there are more important design criteria rather than designing for highest efficiency. These design
criteria are itemized in the following:

- **Low input drive**: Typical frequency multipliers require high input power levels in order to operate at maximum gain. This is needed because the operation principle is typically based on exploiting the inherent non-linearities of the active or passive devices used in the multiplier. For the most common applications, where the frequency of a single tone signal (e.g. LO signal) is to be multiplied, a driver amplifier preceding the frequency multiplier can easily resolve this issue. On the other hand, for the carrier recovery application, the input signal is an ultra-wideband modulated signal, which consequently would require a dedicated broadband power amplifier design increasing the complexity of the system. Therefore, the frequency quadrupler should be able to operate with low input signal levels, without causing excessive conversion loss.

- **Low sensitivity to amplitude fluctuations**: As described in section 2.2, the input signal to be frequency quadrupled does not have a constant envelope, but rather a varying amplitude depending on the modulation content. Furthermore, if the amplitude of this signal is raised by an order of four to generate a fourth harmonic, the influence of the envelope fluctuations become very critical as shown in section 2.3.1. It would therefore be desirable to have a frequency quadrupler which can generate four times the argument of the input signal without quadrupling the magnitude.

In consideration of these two criteria, the topology chosen for the design of the frequency quadrupler is two cascaded self-mixing stages as shown in Fig. 3.2. The mixer cores are modified Gilbert cell mixers [50], where the only modification is the removal of the tail current sources in order to reduce the supply voltage. The inputs of the lower pair (T$_1$ and T$_4$ pairs) and the upper quad transistors (T$_2$, T$_3$ and T$_5$, T$_6$ pairs) are combined together to realize the self-mixing. The two stages are cascaded with the tuned amplifier principle; that is, the output of the first stage is conjugately matched to the input of the second stage at 10 GHz, while the output of the second stage is matched to a 100 Ω differential load at 20 GHz. The impedance matching is performed using L-C networks, under the condition that the upper quad transistors are in one of the switching states (one pair is off and the other pair is on). Owing to the negligible DC voltage drop on the reactive loads, a relatively low supply voltage of 2.5 V can be used. The additional MIM-capacitors at the input are included for DC-blocking. The biasing is performed using the circuit presented in the previous section, but is not displayed in figure 3.2 for
3 Synchronous Demodulator Implementation

The frequency quadrupler is optimized to operate at low input signal levels and to have a low gain dependence on the variations of the signal power. The target behavior corresponds to the switching regime operation of the mixers, where the conversion gain becomes independent of the input signal power\(^1\). To achieve switching regime operation at low signal levels, the dimensions of the switching quad transistors are chosen relatively large, unlike the conventional approach where the switching transistors are chosen typically as small as possible to maintain high speed operation [52]. Simulations show that through this approach the input signal level required for switching regime operation is reduced by 4 dB, while the gain of the circuit is reduced by approximately the same amount.

The chip photograph of the realized frequency quadrupler is shown in Fig. 3.3. The IC is characterized on-wafer, using ground-signal-ground-signal-ground (GSGSG) wafer probes with a pitch of 100 µm. A custom designed ultra-wideband balun is used at the input in order to provide a differential stimulus. The output is measured single-endedly, by terminating one of the output ports with a 50 Ω load.

In Fig. 3.4, the measured conversion gain versus input power is displayed, for an input frequency of 5 GHz, and an output frequency of 20 GHz. The output power is measured by a spectrum analyzer, and the losses of the measurement setup are calibrated. It is

\(^1\) The switching regime of a mixer means that the input power is sufficiently high to bring the upper quad transistors to full switching. In this condition the circuit operates as a mixer, while it operates as an analog multiplier if the input power is not high enough. Please see appropriate literature, e.g. [51].
Figure 3.3: Chip-photograph of the realized frequency quadrupler.

Figure 3.4: Conversion gain of the frequency quadrupler for swept input power. The input frequency equals 5 GHz, while the output is measured at 20 GHz.

seen from this figure that the maximum conversion gain is achieved at a low input power of -10 dBm, and the conversion gain remains within a 3-dB range for input power levels from -14 dBm to -1 dBm.

The measured conversion gain versus the input frequency is displayed in Fig. 3.5. For these measurements the available input power is fixed at -9 dBm at the probe tips, and the output power is measured at four times the input frequency. It is seen from the figure that the maximum conversion gain equals 1.6 dB, which is obtained for an input
frequency of 5.1 GHz. As the input frequency is increased or reduced, the conversion gain starts to decrease, which shows that the intended power matching is achieved. The measured 3-dB bandwidth at the output equals 2.8 GHz. It should be noted that the bandwidth limitation takes places at the output, not at the input, therefore this does not have any influence on the carrier recovery performance. The total power consumption is 55 mW from a 2.5 V DC voltage source.

Table 3.1: Comparison of the designed frequency quadrupler to the state of the art

<table>
<thead>
<tr>
<th>Technology</th>
<th>Conversion Gain (dB)</th>
<th>Frequency range (GHz)</th>
<th>Input power range for 3-dB gain var. (dBm)</th>
<th>P_{DC} (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This</td>
<td>0.8 \mu m HBT</td>
<td>1.5</td>
<td>5 to 20</td>
<td>-14 to -1 (13 dB)</td>
</tr>
<tr>
<td>[49]</td>
<td>0.8 \mu m HBT</td>
<td>4.5 †</td>
<td>18 to 36</td>
<td>2.2 to 8 (5.8 dB) †</td>
</tr>
<tr>
<td>[53]</td>
<td>0.4 \mu m HBT</td>
<td>6.5</td>
<td>10.5 to 42</td>
<td>-18.5 to -12 (6.5 dB) †</td>
</tr>
<tr>
<td>[54]</td>
<td>90 nm CMOS</td>
<td>-2.5</td>
<td>7 to 28</td>
<td>1 to 8.5 (7.5 dB) †</td>
</tr>
<tr>
<td>[55]</td>
<td>0.25 \mu m pHEMT</td>
<td>15</td>
<td>9 to 36</td>
<td>-1.5 to 4 (5.5 dB) †</td>
</tr>
</tbody>
</table>

† Graphically estimated
* Frequency doubler

The results are summarized in Table 3.1. Other published frequency multipliers from the literature are included as well for comparison. Taking the previously introduced design criteria into account, the designed frequency quadrupler outperforms the other reported frequency multipliers. The circuit requires low input signal power for saturated
gain, and the gain remains constant for a large input power range. Only the frequency quadrupler described in [53] operates with even less input power, however with a much higher power consumption, while it is realized using the same frequency quadrupler topology described in this thesis.

### 3.1.4 Frequency Divider

As previously described in section 2.2, frequency dividers are needed in order to divide the bandpass filtered fourth harmonic signal by four, which regenerates the carrier at the IF. Furthermore, the need for frequency division can be exploited by generating the divided carrier in quadrature, as needed for QPSK demodulation. Frequency dividers are commonly used for quadrature LO-signal generation, and several examples can be found in the literature proposing different techniques [56, 57, 58]. On the other hand, a simple and common approach is to utilize static frequency dividers [59], which is the preferred technique in this thesis. The static frequency dividers are typically implemented using the smallest transistors available in a technology for highest possible speed, therefore power consumption can be kept relatively low. Furthermore, unlike other approaches, the circuit topology is only based on emitter coupled logic (ECL), and does not require any resonance circuit or magnetic coupling.

![Simplified circuit schematic of a single D-latch](image)

**Figure 3.6:** Simplified circuit schematic of a single D-latch. The component values are given for the D-latches within the first and second division stages.

The basic ECL cell is displayed in Fig. 3.6, which is used as the building block for the frequency divider. It realizes a D-latch in current mode [60], where the clock input is
applied to the T₁ pair, steering the tail current between a reading block (T₂ pair) and a storing block (T₃ and T₄ pairs).

Figure 3.7: The block diagram of the static frequency divider in master-slave D flip flop topology with a division ratio of two.

The block diagram of the divide-by-two static frequency divider is displayed in Fig. 3.7, which consists of two D-latches in master-slave topology. The latches alternate in opposite polarity between the reading and the storing modes, resulting in an output signal at half the clock frequency. The resulting logic table of the frequency divider is displayed in Table 3.2 in order to clarify the operation.

Table 3.2: Logic table of the divide-by-two static frequency divider

<table>
<thead>
<tr>
<th>Clk</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Q1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Q2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

To realize the logic table Q₂ = 1 is chosen as a starting condition. As it can be seen, the output (Q₂ - Q₂) alternates at half the clock rate. Furthermore, it is seen that the reading input of the second latch (D₂ - D₂) precedes the output by a symbol, meaning that this node differs from the output by a quarter period. This property facilitates the generation of the divided output in quadrature.

For the carrier recovery, the frequency divider is optimized to have a peak division sensitivity at around 20 GHz. The sensitivity behavior is dominated by the delay experienced within the latches, which depends strongly on the transistor sizes, and on the R-C constant at the collector nodes. Therefore, small transistors and small collector
resistors are preferred as the target division frequency is in the range of $f_T/4$. For the second division stage, the peak sensitivity is shifted to a lower frequency by choosing larger collector resistors.

![Matching inductor, 0.4 nH](image)

**Figure 3.8:** Chip-photograph of the realized divide-by-four static frequency divider.

The chip photograph of the designed divide-by-four frequency divider is displayed in Fig. 3.8, which consists of two cascaded divide-by-two frequency dividers. For this design, one of the clock inputs is connected to ground, while the other input is matched to 50 Ω at 20 GHz by including a shunt inductor of 0.4 nH. This is required, because the divider needs to interface the external bandpass filter.

The frequency divider is characterized by measuring its sensitivity versus the input frequency. It is seen in Fig. 3.9 that the desired sensitivity behavior is achieved with a peak sensitivity less than -30 dBm at 20 GHz. The generation of the divided signal in quadrature is verified indirectly during the characterization of the complete demodulator in section 4.3. The total power consumption of the divide-by-four frequency divider equals 85 mW from a 2.5 V DC voltage source.

The performance of the designed circuit is compared to other published static frequency dividers in Table 3.3. The typical figure of merit (FOM) used in the literature is included in the table, which is defined by the maximum operating frequency divided by the power consumption. In addition to this FOM, a second FOM is included as well, which takes the transit frequency of the technology into account.
Figure 3.9: Measured sensitivity of the designed divide-by-four static frequency divider versus input frequency.

Table 3.3: Comparison of the designed frequency divider to the state of the art

<table>
<thead>
<tr>
<th>Technology</th>
<th>Maximum Division Frequency (GHz)</th>
<th>P&lt;sub&gt;DC&lt;/sub&gt; (mW)</th>
<th>FOM1 † (GHz/mW)</th>
<th>FOM2 * (W&lt;sup&gt;−1&lt;/sup&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This 0.8 µm HBT</td>
<td>24.5</td>
<td>45†</td>
<td>0.54</td>
<td>6.8</td>
</tr>
<tr>
<td>[61] 0.8 µm HBT</td>
<td>19</td>
<td>130</td>
<td>0.14</td>
<td>1.82</td>
</tr>
<tr>
<td>[62] 0.13 µm BiCMOS</td>
<td>100</td>
<td>122</td>
<td>0.82</td>
<td>3.56</td>
</tr>
<tr>
<td>[63] 0.7 µm InP DHBT</td>
<td>87</td>
<td>700</td>
<td>0.12</td>
<td>0.6</td>
</tr>
<tr>
<td>[64] 90 nm CMOS</td>
<td>61.4</td>
<td>22</td>
<td>2.8</td>
<td>18.6</td>
</tr>
</tbody>
</table>

† FOM1 = f<sub>div</sub>(GHz)/P<sub>DC</sub>(mW) [59]
* FOM2 = f<sub>div</sub>(GHz)/f<sub>T</sub>(GHz)/P<sub>DC</sub>(W)
†† Power consumption of the divide-by-two divider

It is seen from the table that the realized frequency divider achieves very good performance, and is well suited for the carrier recovery application. Only the divider presented in [64] shows even better performance, whereas in that work inductive peaking is utilized at 60 GHz. In principle, this technique is also applicable for a design at 20 GHz, but not necessarily required since a good performance is already achieved.

3.1.5 Phase Shifter

The phase shifters are required to compensate the phase shift experienced through the carrier recovery. Although the phase shift to be compensated is fixed and in principle
deterministic, it is preferred to have a tunable phase shifter for a prototype implementation. There are well practiced approaches in the literature to realize phase shifters with sufficient performance, like using all-pass filter (APF) networks [65] or vector summation [66]. These solutions are based on active circuits which typically consume power and have limited linearity. On the contrary, for passive approaches the dimensions and the loss become the limiting factor. For instance, in [67] varactor loaded artificial transmission lines (TL), or in [68] a reflective type phase shifter is presented, both achieving 360° phase tuning range at 5 to 6 GHz. However, both ICs occupy an area larger than 1 mm², and they have a transmission loss of 6 to 7 dB.

Considering the large dimensions of passive approaches, an active tunable phase shifter approach is preferred. As amplitude control is not required, a vectorial approach becomes too complex for the target application. Therefore, a tunable second-order APF network is designed to realize the active phase shifter. Typically, a second-order APF transfer function can be represented as a subtraction of half of the input signal from its bandpass filtered version at the resonant frequency [69]. The simplified schematic of the designed APF circuit is displayed in Fig. 3.10, which realizes this subtraction in current mode [70].

As seen in the schematic, T₁ and T₂ are in common-emitter and common-base configuration, respectively, and generate signal currents with opposite polarities. The input signal is fed to T₂ through a series LC connection, and the signal current from T₂ represents the bandpass filtered version of the input signal. Thereby, the desired APF

Figure 3.10: Simplified circuit schematic of the designed second-order APF phase shifter.
characteristic is achieved by the subtraction of these two currents at the load resistor \( R_C \). If we make the assumption that the dynamic emitter resistances of \( T_{1,2,3} \) are negligible in comparison to the emitter degeneration resistors \( (1/g_{m1,2,3} \ll R_{1,2,3}) \), and if we neglect the parasitics of the transistors, the simplified voltage gain of the half-differential circuit yields

\[
\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{R_C}{R_1} \frac{s^2 + s \frac{R_2 - R_1}{L} + \frac{1}{LC}}{s^2 + s \frac{R_2}{L} + \frac{1}{LC}}. \quad (3.2)
\]

By setting \( R_1 = 2R_2 \), (3.2) becomes an all-pass transfer function with a resonant frequency of \( \omega_n = 1/\sqrt{LC} \). The capacitor \( C \) is realized as a series combination of a capacitor and a varactor diode, hence a tunable \( \omega_n \), and a tunable phase shift for the designed APF is achieved. However, it should be kept in mind that (3.2) is derived with several simplifying assumptions, and in reality the circuit has a more complex transfer function. During the design procedure, the simplified transfer function gives an insight into the circuit operation, while an optimization process is needed to acquire the desired performance.

![Chip-photograph of the realized APF phase shifter.](image)

A differential topology is preferred in order to reduce the effects of common node parasitics, which typically have a large impact on the group delay performance.
shown in Fig. 3.10, the resistor $R_{EE}$ is used as a common current source. The output of the APF is buffered with common-collector stages in order to allow for different load values. The chip photograph of the designed phase shifter is displayed in Fig. 3.11. The chip area is $0.42 \text{mm}^2$, which is still dominated by the inductors, but is much smaller than a potential passive approach.

![Figure 3.12: Measured insertion phase and transmission coefficients of the phase shifter for varying tuning voltage.](image)

In Fig. 3.12, the measured insertion phase and the forward transmission coefficients ($S_{21}$) of the realized IC are displayed, for varying tuning voltage. As seen, a phase tuning range of $170^\circ$ is achieved, while the magnitude variation remains within 4 dB. The circuit has around 3 dB more loss than predicted by the simulations, which may be explained by the model inaccuracy of large inductors and varactors used in the design. Apart from this discrepancy, the designed circuit achieves sufficient performance for the carrier recovery application, while it is realized within a compact area. The total power consumption is 39 mW from a 2.5 V DC voltage source.

In Table 3.4, the results are summarized and compared to other reported phase shifters in various topologies. As seen from the table, the designed APF phase shifter combines compact size, low power consumption and high linearity, while achieving a tunable insertion phase of $170^\circ$. Furthermore, it is the only fully differential phase shifter design in the literature, which is a major advantage when more practical concerns are taken into account, such as common node parasitics that arise during packaging.
### 3.1.6 Demodulator

The demodulator is realized making use of common design techniques, while the design criteria are to achieve sufficient bandwidth and linearity, maintaining a low power consumption. The design comprises a Gilbert cell mixer, which performs the demodulation by mixing the modulated signal with the recovered carrier. The circuit schematic is displayed in Fig. 3.13.

![Simplified circuit schematic of the designed demodulator.](image)

The standard port notations for mixers are used in the schematic. For demodulation, the recovered carrier is applied to the switching quad (LO-port), while the modulated signal is applied to the transconductance pair (RF-port). The resistor $R_{EE}$ acts as a common current source to improve common mode rejection ratio (CMRR). Relatively
large emitter degeneration resistors ($R_1$) are used to maintain linear operation up to an input signal power level of 0 dBm. This is required in order to maintain a large dynamic range under variations of the transmission distance. For instance, when the sample link budget calculations presented in Table 1.2 are taken into account, the input power equals -41 dBm at the receiver antenna interface for a transmission distance of 1 m. Assuming a downconversion gain of 20 dB, the IF power can potentially get as high as -1 dBm, when the transmission distance is reduced to 0.1 m. Consequently, the demodulator is designed to have a high linearity. On the other hand, this requires high current at the output buffers, which considerably increases the power consumption of the circuit.

![Chip-photograph of the realized demodulator](image)

Figure 3.14: Chip-photograph of the realized demodulator.

The chip photograph of the realized demodulator is shown in Fig. 3.14. The IC is very compact with an area of 0.27 mm$^2$. For the on-wafer measurements, a single-ended LO signal is applied, while the RF input and the output are connected differentially using external UWB baluns. The simulations are performed similarly by applying a single-ended LO signal.

The measured conversion gain for swept LO and RF power are displayed in Fig. 3.15-a) and -b), respectively. For these measurements, the RF signal is fixed at 6 GHz and the LO signal at 5.01 GHz, while the output is measured at 0.99 GHz. These measurement conditions resemble the target operation, where the modulated signal is to be downconverted to the baseband. As seen in the figure, there is a very good agreement between the measurements and the simulations. The conversion gain is around 2.5 dB, while an LO power of at least -10 dBm is required for a lossless demodulation. Furthermore, the
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Figure 3.15: Measured conversion gain of the designed demodulator for swept LO and RF power.

Figure 3.16: Measured conversion gain of the designed demodulator versus the RF frequency.

circuit is highly linear as intended, with a measured $P_{1\text{dB}}$ of 0.25 dBm.

In Fig. 3.16, the measured conversion gain is displayed when the RF frequency is swept from 6 to 11 GHz, while the LO frequency is fixed at 5.01 GHz. Through this measurement, the 3-dB bandwidth of the demodulator is determined, which equals 3.7 GHz as
seen in the figure. As a rule of thumb, the output bandwidth is sufficient to demodulate data rates up to 5.6 Gb/s. The total power consumption equals 44 mW from a 2.5 V DC voltage source.

Table 3.5: Comparison of the designed demodulator to the state of the art

<table>
<thead>
<tr>
<th>Technology</th>
<th>Gain (dB)</th>
<th>Input Frequency Range (GHz)</th>
<th>Output Bandwidth (GHz)</th>
<th>$P_{\text{DC}}$† (mW)</th>
<th>$P_{\text{1dB}}_{\text{in}}$ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This</td>
<td>0.8 µm HBT</td>
<td>2.5</td>
<td>1 to 9</td>
<td>0 to 3.7</td>
<td>11.7</td>
</tr>
<tr>
<td>[72]</td>
<td>0.8 µm HBT</td>
<td>8.5</td>
<td>3 to 9.5</td>
<td>0 to 7.5</td>
<td>170</td>
</tr>
<tr>
<td>[73]</td>
<td>0.18 µm CMOS</td>
<td>2</td>
<td>8 to 10</td>
<td>0 to 2</td>
<td>15.7</td>
</tr>
<tr>
<td>[74]</td>
<td>0.13 µm CMOS</td>
<td>14.5</td>
<td>8.7 to 17.4</td>
<td>0 to 8.7</td>
<td>40</td>
</tr>
<tr>
<td>[75]</td>
<td>0.13 µm BiCMOS</td>
<td>-7</td>
<td>53 to 67</td>
<td>0 to 10</td>
<td>8</td>
</tr>
</tbody>
</table>

† Without output buffers

In Table 3.5, the designed demodulator is compared to published wide-band mixers. The designed mixer represents a very good compromise between large output bandwidth, high linearity and low power consumption.

### 3.1.7 Variable Gain Amplifier

An IF variable gain amplifier (VGA) is designed to be included between the downconversion and synchronous demodulation stages, as shown in the receiver schematic in Fig. 2.1. By this means the dynamic range of the receiver can be increased. Furthermore, the VGA should act as a buffer amplifier to drive the low impedance presented by the synchronous demodulator.

In order to achieve a sufficient gain while maintaining high linearity and large bandwidth, impedance mismatch is utilized at the output of the amplifier to improve the gain bandwidth product. This extends the frequency response of the amplifier by lowering the R-C constant at the output node. The basic idea dates back to the original work of E. M. Cherry and D. E. Hooper [76], where it is suggested to cascade series and shunt feedback circuits. There are several examples in the literature which utilize the so called “Cherry-Hooper amplifier” for the design of limiting amplifiers [77, 78] as well as variable gain amplifiers [79, 80].

The simplified circuit schematic of the designed VGA is displayed in Fig. 3.17. The gain control is achieved by applying a control voltage $V_{\text{ctrl}}$, which steers the collector current between the amplifying $T_2$ pair, and the non-amplifying $T_3$ dummy pair. The load of $T_2$ consists of a transimpedance amplifier in shunt feedback topology, realized
mainly by the common-emitter transistor T₄, and the feedback resistor R_F. T₄, R_F and R₂ construct the conventional Cherry-Hooper amplifier, whereas in this design the T₅ emitter follower stage is tapped between R₁ and R₂, and is included in the feedback path as an additional modification. This modified structure results in enhanced gain in comparison to the conventional Cherry-Hooper amplifier [81, 82]. The gain enhancement is achieved through division of the output voltage swing between R₁ and R₂, thus controlling the voltage drop on the feedback resistor R_F. Derivations in [82] show that if R₁ and R₂ are chosen with a ratio 0 < R₁/R₂ < 2.5, gain enhancement can be achieved without distorting the amplifier response.

The chip photograph of the realized VGA is shown in Fig. 3.18. The IC occupies an area of 0.3 mm², and the total power consumption equals 89 mW from a 3.3 V DC voltage source. The measurements are performed on-wafer, and external UWB baluns are utilized at the input and the output for single-ended to differential conversion.

The measured gain of the VGA versus the control voltage is shown in Fig. 3.19-a). As it can be seen from the measurements, a variable gain range from 17.5 dB to -3 dB is achieved for a control voltage variation from 2 V to 2.27 V. At the mid-gain region (i.e., control voltage from 2.1 to 2.2 V) a gain peak as large as 3 dB is observed around 10 GHz. The reason of this behavior is investigated, and is mainly associated with unaccounted parasitics at the supply voltage terminal. Although the virtual ground at this common-node terminal should suppress the parasitic effects, due to the imperfections of the measurement setup a perfect differential stimulus can not be provided, leading
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Figure 3.18: Chip-photograph of the realized VGA.

Figure 3.19: Measured gain of the designed VGA for different values of the control voltage.

to undesired circuit performance. In Fig. 3.19-b), the measured insertion phase and the calculated group delay is displayed for a control voltage of 2.15 V. A curve fitting is performed on the acquired group delay data, and is displayed in Fig. 3.19-b) superimposed on the actual data from the measurements. It can be seen that a similar peaking behavior is observed for the group delay response. Nevertheless, within the band of interest from 3 to 8 GHz, the group delay variation remains under +/- 10 ps which would result in an acceptable signal distortion [82].

In Fig. 3.20, the measured gain of the VGA is displayed for swept input power in four gain configurations. For these measurements the signal frequency is fixed at 5 GHz. As
Figure 3.20: Measured gain of the designed VGA for swept input power. Signal frequency is fixed at 5 GHz.

can be seen, the circuit is highly linear, and it can deliver an output power of more than 0 dBm for all gain configurations. This performance is achieved by designing the input stage to be highly linear regardless of the value of the gain. Consequently, the gain compression takes place at the output for higher gain configurations, and at the input when the gain is lowered. Therefore, as the gain of the circuit is reduced, the P1dB improves, and the circuit is able to deliver an output power as high as 5 dBm in the maximum gain configuration.

Table 3.6: Comparison of the designed VGA to the state of the art

<table>
<thead>
<tr>
<th>Technology</th>
<th>Gain (dB)</th>
<th>Bandwidth (GHz)</th>
<th>P1dB_{out,max} (dBm)</th>
<th>P_{DC} (mW)</th>
<th>FOM†</th>
</tr>
</thead>
<tbody>
<tr>
<td>This</td>
<td>-3 to 17.5</td>
<td>0.5 to 13</td>
<td>5</td>
<td>87</td>
<td>44</td>
</tr>
<tr>
<td>[83] 0.35 µm BiCMOS</td>
<td>-4 to 20</td>
<td>1.6 to 12.1</td>
<td>-2</td>
<td>40</td>
<td>26</td>
</tr>
<tr>
<td>[84] 0.25 µm BiCMOS</td>
<td>0 to 11.5</td>
<td>0 to 30</td>
<td>12</td>
<td>560</td>
<td>42</td>
</tr>
<tr>
<td>[85] 0.5 µm InP DHBT</td>
<td>-30 to 17</td>
<td>0 to 50</td>
<td>0.4</td>
<td>627</td>
<td>2</td>
</tr>
<tr>
<td>[86] 90 nm CMOS</td>
<td>-29 to 23</td>
<td>0 to 1.25</td>
<td>8</td>
<td>31.2</td>
<td>26.2</td>
</tr>
</tbody>
</table>

† FOM = \frac{\text{Bandwidth (GHz)} \cdot \text{Gain} \cdot \text{P1dB}_{\text{out, max}} (\text{dBm})}{\text{P}_{\text{DC}} (\text{mW}) \cdot f_T (\text{GHz})} [84]

The performance of the designed VGA is summarized in Table 3.6, and compared to other published VGAs in the literature. The designed circuit combines a large dynamic range with a large bandwidth and high output power. It can be seen that the achieved performance is comparable or better than the published VGAs in various technologies.
in the literature. As shown in chapter 6, the designed VGA is included as a buffer stage within the complete receiver between the downconverter and the synchronous demodulator.

3.2 Bandpass Filter

The bandpass filter is the most critical component that effects the performance of the carrier recovery. In section 2.3.1, it is shown that a BPF with a 3-dB bandwidth of 100 MHz is required to achieve a close to ideal receiver performance. This corresponds to a filter with a relative bandwidth of only 0.5% at 20 GHz.

Considering the bandwidth requirement, an IC solution becomes very challenging due to the low quality factors (Q-factor) of the on-chip passive components (in the range of ~10). In the literature, there are IC examples which alleviate this problem through inclusion of positive feedback architectures, artificially increasing the Q-factor of the passive components [87, 88, 89]. It is shown that these so called “Q-enhanced” filters can achieve sufficiently narrow bandwidth for the carrier recovery application. However, these ICs suffer from certain drawbacks. First of all, as the target bandwidth is very narrow, and the value of the bandwidth is determined mainly by the positive feedback gain, these filters are highly susceptible to process variations. Furthermore, due to the operation principle that inherently shows a tendency towards instability, the positive feedback gain has to be precisely controlled. Therefore, a certain degree of tunability is required to guarantee stable operation and to overcome process variations. Another major limitation is the poor linearity of such structures. As the amplified output signal is fed back to the input, these ICs tend to suffer from gain compression at very low input levels. Moreover, the gain compression reduces the positive feedback, leading to an increase of the bandwidth of the filter. Hence, these circuits can handle only very low input power levels. Due to these limitations, active approaches are not further investigated.

There are many approaches to design such sharp filters at the target frequency range using off-chip, passive components. For instance by utilizing dielectric resonators (DR) [90, 91], quality factors in the range of several thousands can be achieved. On the other hand, such structures are typically bulky and their integration into a compact system is not possible. In this thesis, a simpler solution for the integration is investigated, and in this respect utilizing a planar technology is the most promising technique.

The techniques to realize sharp and compact planar BPFs are well investigated. In
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In general, it is possible to achieve the target bandwidth utilizing classical filter structures, like a hairpin filter [92, 93]. Even though this is a viable solution, considering the required bandwidth, such a filter would have a very high order, leading to a high insertion loss and large dimensions. To overcome these limitations, a better and a more common approach is introducing transmission zeros to the filter characteristics, which result in highly selective filters with tolerable insertion loss and reduced dimensions. Typical methods to realize transmission zeros are using dual-mode resonators [94], utilizing cross-coupling between the resonators of the filter [95, 96], or using asymmetric feed lines [97, 98].

3.2.1 Theory

The BPF design technique chosen in this thesis is utilizing asymmetric feed lines for the transmission zero generation. In Fig. 3.21, a generic structure of an asymmetrically-fed, coupled-resonator filter is shown. It consists of two λ/2 resonators, coupled mutually from both ends. The resonators are tapped asymmetrically, leading to two different line length sections of \( L_1 \) and \( L_2 \). The coupling between the two resonators is simply expressed by a capacitance \( C \) [99].

![Figure 3.21: Generic structure of an asymmetrically-fed, coupled-resonator filter (based on [96]).](image)

The simplest way to analyze the shown structure is using the \( ABCD \) matrix form, and divide the filter into three sections:

\[
S_1 = \begin{bmatrix}
\cos \beta L_1 & jZ_0 \sin \beta L_1 \\
jY_0 \sin \beta L_1 & \cos \beta L_1
\end{bmatrix}, \tag{3.3}
\]

\[
S_2 = \begin{bmatrix}
1 & \frac{1}{j \omega C} \\
0 & 1
\end{bmatrix}, \tag{3.4}
\]
3.2 Bandpass Filter

\[ S_3 = \begin{bmatrix} \cos \beta L_2 & j Z_0 \sin \beta L_2 \\ j Y_0 \sin \beta L_2 & \cos \beta L_2 \end{bmatrix}. \]  

Equation (3.5)

Here, \( S_1 \) and \( S_3 \) represent the \( ABCD \) matrices of the \( L_1 \) and \( L_2 \) transmission line segments, respectively, and \( S_2 \) represents the series connection of the capacitor \( C \). Both line segments are assumed to have the same geometry and material properties, with a propagation constant of \( \beta \) and a characteristic impedance of \( Z_0 \). In this case, the \( ABCD \) matrices of the upper and the lower half of the filter will consist of these three sections multiplied in reverse order:

\[ \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{upper}} = S_1 S_2 S_3, \]  

Equation (3.6)

\[ \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{lower}} = S_3 S_2 S_1. \]  

Equation (3.7)

These matrices are then converted to Y-matrices, and the addition of the two gives the complete Y-matrix of the filter. Finally, the Y-matrix is converted to S-matrix for evaluation. This leads to the following forward transmission coefficient

\[ S_{21} = \frac{8j (\omega C Z_0 \sin \beta L - \cos \beta L_1 \cos \beta L_2)}{8 \omega C Z_0 + \frac{2}{\omega C Z_0} (\cos \beta L_1 \cos \beta L_2 + 2 j \omega C Z_0 \cos \beta L + (j - \omega C Z_0) \sin \beta L)^2}, \]  

Equation (3.8)

where \( L = L_1 + L_2 \). Examining this equation, one can see that the forward transmission will go to zero when the numerator of (3.8) goes to zero, necessitating the following equality

\[ \omega C Z_0 \sin \beta L - \cos \beta L_1 \cos \beta L_2 = 0. \]  

Equation (3.9)

Considering that around the center frequency \( \beta L \) equals approximately 180°, and assuming that the coupling capacitor is relatively small, (3.9) can be reduced to

\[ \cos \beta L_1 \cos \beta L_2 = 0. \]  

Equation (3.10)

This leads to the conclusion that the filter will have two transmission zeros around the center frequency, at which the electrical length of \( L_1 \) and \( L_2 \) equals 90°. This is in agreement with the qualitative understanding of the filter behavior; that is, the
transmission zeros are generated by $\lambda/4$ conversion of open-ended line segments to shorts at the feed taps. This is as well only valid, if the coupling capacitor $C$ is sufficiently small, so that the line segments can be approximated by open-ended transmission lines. A too large gap capacitance will lead to a loading of the line segments $L_1$ and $L_2$, distorting the filter behavior. In contrast, a too small gap capacitance will lead to unnecessary transmission loss. Therefore, the coupling between the resonators has to be optimized for each filter design.

### 3.2.2 Design

The layout of the designed filter is displayed in Fig. 3.22. The filter structure suggested in [98] for operation at 2 GHz is modified into a compact form which is more suited for higher frequency designs. The $\lambda/2$ resonators are placed in close proximity, and the coupling occurs at the sides of the resonators determined by two dimensions, the coupling gap $S$ and the length $d$. This modification was required mainly due to the reduced wavelength at 20 GHz, which leads to line lengths that are too short to realize the ring resonator structures suggested in [98].

![Figure 3.22: Modified filter structure suited for 20 GHz operation.](image)

Several filters are designed for a center frequency of 20 GHz, using the Agilent Momentum software for electromagnetic (EM) simulations. The substrate material is Rogers RO3003 with an $\epsilon_r$ of 3, and a thickness of 128 $\mu$m. A thin substrate was essential to prevent any potential substrate modes which would distort the desired filter performance. Different bandwidth values are achieved by adjusting the length of $L_1$ and $L_2$, which changes the location of the transmission zeros below and above the passband. The coupling strength between the resonators is adjusted by fixing the resonator overlap $d$, and varying the coupling gap $S$. 
In Fig. 3.23, the simulated transmission coefficients of the designed BPFs are displayed, and in Table 3.7 the corresponding dimensions, the transmission zero locations and the 3-dB bandwidth values are given. For all designs, the widths of the lines equal 350 µm, corresponding to a characteristic impedance of 50 Ω, and the resonator overlap \( d \) is fixed at 1.1 mm. As seen in Fig. 3.23 and Table 3.7, the filter bandwidth can be determined by proper choice of the transmission zero locations, and by adjusting the coupling strength between the resonators simultaneously. The simulated insertion losses of the designed filters are 3.5 dB, 2.8 dB, 1.5 dB and 0.8 dB from the sharpest to the broadest filter, respectively. All filters are matched well at the center frequency, with an input/output return loss better than 15 dB.

Table 3.7: Filter dimensions and the corresponding 3-dB bandwidth and transmission zero locations

<table>
<thead>
<tr>
<th></th>
<th>( L_1 ) (µm)</th>
<th>( L_2 ) (µm)</th>
<th>( S ) (µm)</th>
<th>( f_{1,2} ) (GHz)</th>
<th>BW (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>filter1</td>
<td>2930</td>
<td>1950</td>
<td>150</td>
<td>16.8, 24.1</td>
<td>2.0</td>
</tr>
<tr>
<td>filter2</td>
<td>2760</td>
<td>2120</td>
<td>260</td>
<td>18.0, 22.3</td>
<td>1.0</td>
</tr>
<tr>
<td>filter3</td>
<td>2640</td>
<td>2240</td>
<td>380</td>
<td>18.7, 21.1</td>
<td>0.5</td>
</tr>
<tr>
<td>filter4</td>
<td>2600</td>
<td>2280</td>
<td>425</td>
<td>19.0, 20.7</td>
<td>0.35</td>
</tr>
</tbody>
</table>

These design examples show that using the presented filter structure, it is possible to design very compact filters with a bandwidth as low as 350 MHz (RBW: 1.7%). Nevertheless, taking potential variations in the filter production into account, the target
bandwidth is set to 500 MHz for the implementation. Based on the system simulations presented in section 2.3.1, this filter bandwidth would lead to an SNR penalty of around 4 dB for a BER of $10^{-4}$, when the system is operated at the maximum symbol rate. For 10% reduced symbol rate (Fig. 2.5), simulations indicate a very low BER, with an SNR penalty of only 1 dB.

### 3.2.3 Implementation

In Fig. 3.24 the photograph of the realized filter is displayed. The substrate material is RT/Duroid 5880, which has a lower dielectric constant of 2.2 compared to the substrate used in the previous designs. The substrate choice is mainly determined by the antenna implementation within the framework of the collaborative research project EASY-A [21], and the filter designs are converted to this substrate material in order to allow a potential system-in-package integration (SiP) of the complete system including the antennas.

![Photograph of the realized filter](image)

Figure 3.24: Photograph of the realized filter with the following dimensions: $L_1 = 2.64$ mm, $L_2 = 2.24$ mm, $L_3 = 2.8$ mm, $s = 0.38$ mm, $d = 1.1$ mm, $w_1 = 0.37$ mm, $w_2 = 0.6$ mm.

For the design shown in Fig. 3.24, transmission line segments with a lower characteristic impedance are included at the input and the output of the core filter structure, in order to further improve the matching performance. The realized filter is characterized with end-launch connectors specified up to 50 GHz.

The measured S-parameters are displayed in Fig. 3.25. As seen in general, there is a very good agreement between the measurements and the simulations. The measured
3.2 Bandpass Filter

Figure 3.25: Measured S-parameters of the realized filter with the connector interface a) Span of 4 GHz, b) Span of 40 GHz. The total connector losses is estimated to be 1.6 dB center frequency is shifted to 20.2 GHz from the intended 20 GHz, which is a variation of only 1%. The measured insertion loss equals 4.55 dB, whereas 1.6 dB is estimated for connector losses by a through line measurement. This leads to an estimated actual filter loss of 2.95 dB, which is only 0.2 dB higher than the simulated value. The measured bandwidth equals 520 MHz which is slightly higher than predicted. The measured out of band rejection of the filter is better than 20 dB up to 37 GHz. For frequencies around twice the passband the rejection of the filter gets as low as 13 dB, which is a typical property of filters utilizing $\lambda/2$ resonators. The reduced suppression at higher frequencies is not critical for the carrier recovery application, as the spurious spectrum to be filtered out is only centered around the carrier signal.

Table 3.8: Comparison of the designed BPF to the state of the art

<table>
<thead>
<tr>
<th>Filter Type</th>
<th>Material</th>
<th>$f_c$ (GHz)</th>
<th>3-dB Bandwidth (GHz)</th>
<th>Insertion Loss (dB)</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This</td>
<td>Microstrip RT/Duroid 5880</td>
<td>20.2</td>
<td>0.52 (2.5%)</td>
<td>3</td>
<td>2.3x3</td>
</tr>
<tr>
<td>[100]</td>
<td>Microstrip RT/Duroid 5880</td>
<td>10.1</td>
<td>0.33 (3.2%)</td>
<td>3.3</td>
<td>5.9x5.9</td>
</tr>
<tr>
<td>[101]</td>
<td>Cavity LTCC</td>
<td>20.6</td>
<td>0.62 (3%)</td>
<td>2.4</td>
<td>17 mm²</td>
</tr>
<tr>
<td>[102]</td>
<td>DR Ba(Sn,Mg,Ta)O₃</td>
<td>28</td>
<td>0.19 (0.6%)</td>
<td>0.75</td>
<td>10x10x21</td>
</tr>
<tr>
<td>[103]</td>
<td>Lumped 90 nm CMOS</td>
<td>20</td>
<td>3.7 (18%) †</td>
<td>5</td>
<td>0.45x0.7</td>
</tr>
</tbody>
</table>

† Graphically estimated

The performance of the realized filter is summarized in Table 3.8, and compared to
other narrow band BPFs published in the literature. It is seen from the table that a superior performance can be achieved using DR based structures [102], but with a substantial increase of size. On-chip implementations provide size reduction and high integration, but are limited to a fractional bandwidth in the range of 20% [103]. The designed filter achieves a very small fractional bandwidth, in combination with low insertion loss and compact size. It provides an excellent solution for the carrier recovery application without substantial increase of the system complexity.

3.3 Synchronous Demodulator Module

3.3.1 Synchronous Demodulator Chip

The active components presented in section 3.1 are included within a single IC to be used in an SiP integrated module. The photograph of the realized synchronous demodulator chip is displayed in Fig. 3.26. The IC includes the necessary active circuit blocks for carrier recovery and synchronous demodulation, namely a frequency quadrupler, a divide-by-four static frequency divider, two active phase shifters and two demodulators.

Figure 3.26: Chip photograph of the realized synchronous demodulator chip.
The pad configuration allows on-wafer characterization using connectorized BPFs. The input is applied with a differential GSGSG probe from the north. The output of the quadrupler can be taken with a GSG probe from the south (the other output is left open), and connected to the external BPF. The output of the BPF is applied to the divider from the east with a power-ground-signal-ground-power (PGSGP) probe, which as well provides the required DC voltages through the two additional power pins. Finally the demodulated I/Q-Output or the recovered carrier is measured with a differential GSGSG probe on the west side.

The IC occupies an area of $1.7 \times 2.2 \text{ mm}^2$ and is operated from a single supply voltage. To prevent supply line leakage, on-chip RC filter networks are included to the DC-supply nodes of each active block to improve stage to stage isolation as suggested in [104]. This leads to an increase of supply voltage to 2.8 V, and the total power consumption of the IC equals 380 mW.

### 3.3.2 IC-Bandpass Filter Interface

For the IC-BPF wire-bond interface, two potential configurations are considered, which are displayed in Fig. 3.27. In principle the IC-BPF interface is a microstrip to coplanar wave guide transition; that is, the ground signal should be transferred from the bottom metal to the top metal for the microstrip and the coplanar modes, respectively. The interface displayed in Fig. 3.27-a) relies on conventional via-holes for this transition. The drawback of this approach is that a physical distance is added to the ground path, which may potentially cause undesired mismatch losses. The other approach shown in Fig. 3.27-b) realizes the transition via utilization of radial-stubs. The radial stubs provide the ground transition by capacitive coupling, which excites the microstrip mode.

![Figure 3.27: IC-BPF wire-bond interfaces realized with a) via holes, and b) radial stubs.](image-url)
by open to short conversion at the center frequency. This approach has the drawback that the radial stubs have relatively large dimensions, and the ground connection is performed only around the center frequency.

Figure 3.28: Illustration of the IC-BPF wire-bond interface characterization setup.

The two approaches are compared by measuring the realized BPF in a test setup. The realized filter is wire-bonded to through-line test structures on Si/SiGe ICs at both ends, utilizing one of the two interfaces as shown in Fig. 3.28. The SiGe chips have a height of 350\,\mu m, therefore, taking the height difference between the filter substrate and the SiGe chips into account, the bond wire lengths are estimated to be in the range of 450\,\mu m to 550\,\mu m. The filters are measured by contacting the through-line ICs with wafer probes.

Figure 3.29: Measured S-parameters of the realized filter for different wire-bond interfaces.
The measurement results are displayed in Fig. 3.29. It is seen in the figure that the radial-stub interface shows only slightly better performance. Both filter measurements show an increase of the center frequency to 20.5 GHz, and a reduced 3-dB bandwidth of 460 MHz. The measured transmission loss is 4.9 dB. When the losses of the through line ICs are subtracted, the BPFs including the bond wires and the interfaces show a loss of around 4 dB, which is 1.2 dB higher than the simulated value. Part of this loss can be explained by the tapered lines at the interfaces which show a total simulated loss of 0.14 dB at 20 GHz. The remaining loss of around 1 dB may occur on the one hand due to the relatively long wire-bonds, on the other hand due to production related tolerances. The increase in center frequency and the reduced bandwidth indicate a fabrication related over-etch of the structures, which is assumed to be the dominant factor for the increased insertion loss.

Clearly, the via-hole based wire-bond interface shows sufficient performance at 20 GHz, and it is the preferred interface type as it provides a broadband ground connection. At higher frequencies, i.e. above 30 GHz, the radial-stub interface should be preferred, as the added physical distance of the via-holes would further degrade the performance. Apart from the ground connection, it would be necessary to include wire-bond compensation structures as well to alleviate the increasing mismatch losses [105].

Figure 3.30: Phase response of the realized filter with the via-hole based wire-bond interface.
3 Synchronous Demodulator Implementation

In Fig. 3.30, the measured phase response of the test filter with the via-hole interface is displayed. The group delay is calculated by taking the derivative of the phase measurement. Due to the narrow bandwidth and the abrupt transitions at the transmission zero frequencies, the filter can not be considered to be a distortionless component. Therefore, a direct relation can not be established from the measured group delay data to the true-time delay of the filter. This is seen at the transmission zero frequency of 21.7 GHz, where a negative group delay is calculated. On the other hand, around the center frequency the filter has a flat magnitude response, thus it can be considered locally distortionless around 20.5 GHz. As seen in Fig. 3.30, the calculated group delay of the BPF in the passband region is around 1 ns. Therefore the true-time delay of the BPF, including the wire-bond interface is estimated to be 1 ns as well. Furthermore, it can be assumed that the total delay experienced through the carrier recovery is dominated by the BPF, as only a minor contribution is expected from the on-chip components, while simulations show a total of 275 ps true-time delay for the frequency quadrupler, the divider and the phase shifter.

3.3.3 Module Implementation

The photograph of the packaged modulator in an aluminum housing is displayed in Fig. 3.31-a). Two versions are realized, one with and the other without a preamplifier. The close-up photographs of both versions are shown in Fig. 3.31-b) and -c). The substrate material is RT/Duroid 5880. The ICs are glued on the metal carrier through an opening in the substrate for better heat conduction. The bandpass filter is connected to the IC with wire-bonds using the via-hole based interface described in the previous section. The IC-BPF interface characterization setup displayed in Fig. 3.28 is included in the same housing. The IF input and the baseband outputs are connected to 50 Ω microstrip transmission lines which lead to coaxial connector interfaces.

For the module v1 shown in Fig. 3.31-b), one of the baseband outputs (Q-Out) is left single-ended, and the other SMA connector port is connected to the carrier recovery test pad available on the IC (see Fig. 3.26). This way the recovered carrier can be measured and analyzed using this module. The preamplifier in the second version is included to improve the sensitivity of the analog demodulation. The amplifier is simply glued beneath the demodulator chip and connected with wire-bonds, as shown in Fig. 3.31-c). The preamplifier was available from a separate project, which is a differential ultra-wideband LNA with a measured gain of 20 dB and a noise figure of around 3 dB [106]. The LNA is operated from a separate voltage source of 3.5 V and draws 22 mA.
The characterization of the analog demodulation using the presented modules is described in the next chapter.
4 Experimental Characterization of the Analog Demodulation

In this chapter, the experimental verification and characterization of the analog synchronous demodulation concept is presented. The experiments are performed at an intermediate frequency using the demodulator modules described in section 3.3.3. The multi-Gbps input signals for the testing are generated using custom designed modulators and a field programmable gate array (FPGA) evaluation board.

In the first part of this chapter, the modules that are designed for these experiments are described, and in the second part the multi-Gbps test signal generation setup which uses these modules is introduced. In the third part, the results of the experimental characterization are presented, and in the last part, a summary is provided, comparing the achieved results to other published analog demodulators in the literature.

4.1 Component Design for the Verification Experiments

4.1.1 Modulators

In order to effectively test the synchronous demodulation concept, QPSK modulated test signals are required with symbol rates in the range of several GS/s. The commercially available arbitrary wave form generators are usually limited to lower data rates, such as the Agilent 4438C which was available for the experiments, and provides a modulation rate of only 50 MS/s. Therefore, custom modulators are designed which are able to generate broadband BPSK modulated signals up to 10 GHz, while two of these modulators are utilized in a signal generation setup in order to generate the multi-Gbps QPSK test signals. The schematic of the designed BPSK modulator is displayed in Fig. 4.1.

The IC is designed in IHP’s 0.25 µm SG25H3 SiGe-C BiCMOS technology, which provides HBTs with specified $f_T/f_{max}$ of 110/180 GHz. The core modulator is a Gilbert
Experimental Characterization of the Analog Demodulation

Figure 4.1: Simplified schematic of the designed multi-Gbps BPSK modulator.

Cell mixer. For the modulation the carrier signal is applied to the RF-port, and the data-stream to the LO-port. The LO-port is driven through a limiting amplifier, which on the one hand converts single-ended inputs to differential, on the other hand guarantees a voltage swing sufficient to operate the mixer in the switching regime. The output signal is BPSK modulated, and is provided through two stages of cascaded common-collector buffer stages. The circuit is operated from a 3.3 V DC voltage source and draws 30 mA current.

Figure 4.2: Photograph of the BPSK modulator module.

One of the packaged BPSK modulator in an aluminum housing is displayed in Fig. 4.2. The board material is RO4003 with a dielectric constant of 3.3 and a thickness of 508 µm. Off-chip broadband single layer capacitors with a value of 100 pF are used at
4.1 Component Design for the Verification Experiments

the input and the output for DC-blocking. The IC is glued on to the substrate, and all interfaces are based on conventional wire-bonding.

Figure 4.3: Measured conversion gain of the packaged BPSK modulator for swept LO and RF power.

The measurements of the packaged modulators are performed using UWB baluns at the RF and output ports, while the LO port is fed single-endedly. The measured up-conversion gain of one of the realized packaged modulators is displayed in Fig. 4.3 for swept RF and LO power. For these measurements, the RF frequency is fixed at 5 GHz and the LO frequency at 1.5 GHz, while the output is taken at 3.5 GHz. These conditions resemble BPSK modulation at a data rate of 3 Gb/s. Owing to the limiting amplifiers at the LO-port, the switching regime operation of the mixer is achieved for LO input power levels from 5 to -20 dBm. This allows flexibility for the choice of the baseband signal generator, as the mixer is not affected by the signal power at this port. The modulator is highly linear, and the measured input 1 dB compression point equals 1.3 dBm.

The measured conversion gain versus the LO frequency is displayed for both packaged modulators in Fig. 4.4. For these measurements, the RF frequency is fixed at 5 GHz with a power of -20 dBm, while the LO frequency is swept from 0.1 to 5 GHz with a power of -10 dBm. As can be seen, the modulators exhibit a very wide bandwidth, and provide flat gain up to an output frequency of 10 GHz. A gain ripple at around 8.5 GHz is observed for both modules, which potentially arises due to the measurement setup. In general, there is a very good agreement between the measurements and the simulations.
except a gain reduction of around 1 dB. The modulators provide sufficient broadband performance and high linearity, and are well suited to generate multi-Gbps test signals.

### 4.1.2 Limiting Amplifiers

Limiting amplifier modules are required in order to perform the BER characterization of the analog demodulation. These amplifiers should guarantee sufficient voltage swing as required for the proper functioning of the symbol detection at the BER evaluation boards used in the experiments. One of the realized limiting amplifier modules is displayed in Fig. 4.5. The board material is RO4003. The ICs that are used in these modules were available from a separate project, and are realized in Telefunken Semiconductors SiGe2RF technology. They consist of two stage limiting amplifiers in modified Cherry-Hooper topology. The amplifier exhibits a measured small signal gain of 37 dB, delivering an output peak-to-peak voltage ($V_{p-p}$) swing of approximately 600 mV for an input signal level down to 44 mV $V_{p-p}$ [107]. The limiting amplifier modules are operated from a 5 V DC voltage source, each drawing 110 mA current.

As seen in Fig. 4.5, lowpass filters are included on the board material at the input of the amplifier. The filter consists of two radial stubs and a high impedance line in between, acting as a C-L-C lowpass structure. The filters are included in order to suppress undesired higher harmonic components, such as the significant energy present at twice the IF frequency which arises during the demodulation. Separate connectorized
4.1 Component Design for the Verification Experiments

filters are prepared as well for eye-diagram measurements without the limiting amplifiers. One of these filters is shown in Fig. 4.6, and the measurements are displayed in Fig. 4.7.

The measurements show a 3-dB bandwidth of 3.7 GHz and a suppression of more than 35 dB at 10 GHz. The high suppression is achieved by generating two transmission zeros around 10 GHz, through open to short conversion using the radial stubs. However, the filter has a non-flat group delay response, with a measured deviation from 300 ps to 350 ps within 3 GHz. A flat group delay response is essential in order to avoid inter symbol interference, and distortion of the output waveform. Taking this into consideration, the filter is intentionally designed with a wider bandwidth than required, in order to reduce the effect of potential distortions. Using a wide bandwidth lowpass filter is possible due to the high SNR of the received signal, which makes noise filtering less critical.

In order to further emphasize that the realized filters would cause only minimal distortion, a 3.124 Gb/s data pattern generated from a Xilinx ML605 Virtex6 FPGA evaluation board is measured with and without lowpass filtering. It is seen in Fig. 4.8 that the filtered waveform is only minimally distorted compared to the original data, despite
4 Experimental Characterization of the Analog Demodulation

Figure 4.7: Measurements of the realized lowpass filter.

Figure 4.8: Measurements of 3.124 Gb/s bit-sequence a) without and b) with lowpass filtering.

the non-flat group delay response of the lowpass filters.

4.2 Test Signal Generation

The QPSK signal generation setup is displayed in Fig. 4.9. It generates the QPSK modulated signal by combining two multi-Gbps BPSK modulated signals in quadrature. The quadrature generation, or rather the 90° phase shift between the two BPSK signals, is acquired by utilizing two separate signal generators, which are synchronized using the 10 MHz reference signals. The custom UWB baluns are used to differentially feed the frequency-synchronized carrier signals to the BPSK modulators. In one branch a
4.2 Test Signal Generation

directional coupler (Krytar, Model 1821) is included to divide a trigger signal for the real-time oscilloscope measurements. The data inputs are supplied from the Xilinx ML605 FPGA evaluation board using the available BER-test software [108]. The evaluation board is extended with an FMC XM104 connectivity card, and is able to generate two independent pseudorandom data streams up to a symbol rate of 3.124 GS/s. As a result, two independent BPSK signals are generated at the output of the modulators, and the phase shift in between is adjusted from the separate signal generators. Finally, the two signals are combined using two custom UWB power combiners (Appendix B), generating the QPSK modulated output signal.

Figure 4.9: Block diagram of the multi-Gbps QPSK test signal generation setup.

The phase or amplitude errors due to the imperfections or unavoidable asymmetries within the setup are not critical in terms of quadrature performance, as the phase and the amplitude of the carrier signal can be adjusted accurately in order to achieve a good performance at the output. Such a case is displayed in Fig. 4.10, showing all four phase states measured at the output of the QPSK modulator for a 5.1 GHz carrier signal. The four phase states are acquired by applying DC-voltages to the LO ports of the BPSK modulators, forcing them to one of the switching states. For the measurement in Fig. 4.10, an amplitude imbalance of 0.3 dB, and a phase imbalance less than 1° was determined.

The measured spectra of the generated QPSK signals are displayed in Fig. 4.11 for a center frequency of 5.1 GHz and for three different data rates. Except some spurious
4 Experimental Characterization of the Analog Demodulation

Figure 4.10: Measured phase states at the output of the QPSK modulator for a carrier frequency of 5.1 GHz.

components, which arise especially at multiples of the symbol rate from the carrier, the measured spectra look as expected with a completely suppressed carrier signal.

Figure 4.11: Measured spectra of the generated QPSK signals centered at 5.1 GHz for a) 1.562 Gb/s, b) 3.124 Gb/s and c) 6.248 Gb/s data rates.
4.3 Verification Experiments

The complete verification experiment setup is shown in Fig. 4.12. For these experiments, the output of the QPSK generation setup is directly connected to the synchronous demodulator, and the power level is controlled by the signal generators. The output of the demodulator is either fed through the limiters to the FPGA evaluation kit for BER measurements, or fed through the lowpass filters to the real-time oscilloscope for eye diagram measurements.

For all BER measurements, the longest pseudorandom binary sequence (PRBS) of $2^{31}-1$ length is used, and the measurements are performed for a duration of $10^{11}$ received symbols. The lowest BER that can be measured therefore equals $10^{-11}$, meaning that no errors could be detected during the measurement period. Unless stated otherwise, the carrier frequency is fixed at 5.1 GHz, the input power at -18 dBm and the tuning voltage at 0.8 V for all experiments.

![Figure 4.12: Photograph of the verification experiments setup.](image-url)
4 Experimental Characterization of the Analog Demodulation

4.3.1 Carrier Recovery

As a first step, the recovered carrier signal is measured and analyzed. In order to analyze each step of the carrier recovery, the demodulator IC is measured on-wafer using a 4-port measurement setup which is displayed in Fig. 4.13. The demodulator IC is contacted following the pad-configuration described in section 3.3.1, as shown in the right hand side of the Fig. 4.13. For the bandpass filtering, the connectorized BPF described in section 3.2.3 is utilized. The input is supplied from the previously described multi-Gbps QPSK test signal generation setup, while the data rate equals 6.248 Gb/s, the carrier frequency is 5 GHz, and the input power is set to -6 dBm.

![Figure 4.13: 4-port on-wafer measurement setup for the experimental validation of the carrier recovery.](image)

In Fig. 4.14, the measured spectra after each step of the carrier recovery are displayed. It can be seen that the frequency quadrupling cancels the QPSK modulation, and a strong carrier signal is generated at 20 GHz. The spurious spectrum arises mainly due to the envelope fluctuations (see section 2.3.1), and the spur level is measured to be 27 dB below the carrier signal. The resulting signal can not be divided by the static frequency dividers, unless the spurious components are filtered out. This is seen on the left hand side of Fig. 4.14, where the measured spectrum of the recovered carrier is displayed when the output of the quadrupler is directly fed to the dividers, without bandpass filtering. In such a case, a noisy spectrum at around 5 GHz is acquired, which can not be used for demodulation. The bandpass filtering removes most of the unwanted spectrum, except for some remaining spurs close to the carrier signal as seen in Fig. 4.14-c). The signal power is measured to be -26 dBm after bandpass filtering, while 4.5 dB should be added taking the losses of the measurement setup into account. Therefore, the
4.3 Verification Experiments

Figure 4.14: The measured spectrum after each step of the carrier recovery, a) QPSK input, b) quadrupled QPSK spectrum, c) quadrupled QPSK spectrum after bandpass filtering and d) recovered carrier.

The actual carrier signal power is in the range of -20 dBm, which is sufficient for the frequency dividers. After the frequency division, the correct carrier frequency is regenerated, and the spurious components are almost completely suppressed. The suppression takes place due to the insensitivity of the frequency dividers to envelope fluctuations, while the
measured spur level is close to the noise floor, as seen on the right hand side of Fig. 4.14-d).

In order to characterize the carrier recovery performance, and to determine potential effects which can not be captured by a spectrum analyzer, the recovered carrier signal is measured using a real-time oscilloscope with a sampling rate of 40 GS/s, and a bandwidth of 13 GHz. These measurements are performed using the packaged demodulator v1 (see section 3.3.3). The input frequency is shifted to 5.1 GHz, as an IF of 5 GHz is no longer tolerable due to the measured frequency shift of the in-package BPF (section 3.3.2). This change is not critical, as in a system level it only corresponds to a readjustment of the receiver frequency synthesizer. Furthermore, such a large deviation of the BPF characteristic is not expected in a mature fabrication process\(^1\).

![Figure 4.15: Measured recovered carrier signal for an input QPSK signal at 5.1 GHz with a data rate of 6.248 Gb/s.](image)

In Fig. 4.15, the measurement of the recovered carrier signal is displayed for an input QPSK signal centered at 5.1 GHz with a data rate of 6.248 Gb/s. The measured period of the recovered carrier signal equals 196 ps, corresponding to the correct carrier frequency. As seen in the figure, a certain amount of jitter can be determined, however with a very low standard deviation less than 2 ps. The recovered carrier is modulation free and stable, and is synchronous with the QPSK input signal. This is verified by changing the value of the modulated carrier frequency/phase, and observing the same change in the recovered carrier.

\(^1\) In a mature printed circuit board fabrication process the tolerance is typically determined by the metal thickness, which corresponds to 18 \(\mu\)m for the RT/Duroid 5880 substrate material. Simulations show only a slight shift of the filter frequency response when this tolerance is taken into account.
4.3 Verification Experiments

In Fig. 4.16, the measured standard deviation of the recovered carrier period versus the data rate is presented. As can be seen, there is a very slight dependence on the data rate, and the standard deviation increases from 1.3 ps for the lowest data rate (1.562 Gb/s) to 1.85 ps for the highest data rate (6.248 Gb/s). This is more or less expected, as the crucial parameter which effects the stability of the recovered carrier signal is the bandpass filter within the carrier recovery. The measured jitter is sufficiently low to cause only a slight performance penalty (less than one dB SNR penalty for all cases, [109]), and the recovered carrier is suitable to be used in demodulation.

4.3.2 Eye Diagrams

In the next step of the verification experiments, the eye diagrams of the demodulated I and Q data patterns are measured. For these measurements the demodulator v2 is used, while the baseband outputs are connected to the real-time oscilloscope through the lowpass filters described in section 4.1.2.

In Fig. 4.17, the measured eye diagrams of one of the demodulated baseband outputs are displayed for 1.562 Gb/s, 3.124 Gb/s, 3.906 Gb/s and 6.248 Gb/s data rates. As seen from these figures, an open eye is observed for all data rates, which means that successful carrier recovery and synchronization is achieved. On the other hand, an obvious degradation of the eye quality can also be determined for increasing data rate. This is presented more clearly in Fig. 4.18, where the measured eye quality factor of the I and Q streams versus the data rate is presented, using the following eye quality factor

Figure 4.16: Measured standard deviation of the recovered carrier period versus data rate
Figure 4.17: Measured eye diagrams at one of the baseband output of the synchronous demodulator for input QPSK signals with a data rate of a) 1.562 Gb/s, b) 3.124 Gb/s, c) 3.906 Gb/s and d) 6.248 Gb/s.

The eye quality factor gives a measure of the vertical eye opening, where $V_{\text{top}}$ and $V_{\text{base}}$ correspond to the mean horizontal signal levels within the eye window, while $\sigma_{\text{top}}$ and $\sigma_{\text{base}}$ are the standard deviations of these voltage levels. The eye window was set to 40% of the symbol rate for these measurements, which determines the area of the eye-opening in the time-axis, to perform the eye quality factor measurements.

As seen in the figure, the eye quality factor declines continuously with increasing data rate. This cannot be explained by a worse carrier recovery performance, because the recovered carrier shows only slight degradation for increasing data rate. It is believed that the main factors effecting the quality of the eye diagrams are the limitations of the QPSK generation setup. One potential reason is the standing wave patterns that arise due to the modular implementation of the multi-Gbps QPSK signal generation. The port impedances of the realized modules do not provide perfect 50 $\Omega$ terminations, especially
4.3 Verification Experiments

Figure 4.18: Measured average eye quality of the demodulated I and Q streams versus the data rate.

at higher frequencies. Within the setup, the effect of the standing wave patterns are partially mitigated by inclusion of 3-dB attenuators at each module interface. Still, the reflected signals are not completely suppressed, and the effect gets more severe for increasing data rate and signal bandwidth, further degrading the demodulated signal quality.

This effect can be further verified when the measurement results displayed in Fig. 4.19 are observed. These measurements are performed using a much simpler experimental setup using BPSK modulated signals. The designed demodulator can demodulate BPSK signals, for which the 180° phase transitions are converted to 720° by the quadrupling. This simplification of the experimental setup leaves out only one module interface between the BPSK modulator and the synchronous demodulator. For the BPSK test signal generation the data-pattern is supplied from a commercial pattern generator (Anritsu MP1763B) that is able to deliver higher data rates than the FPGA evaluation board.

The eye diagram measurements for the BPSK signals are performed for data rates of 4 Gb/s and 5 Gb/s. The designed lowpass filters are not suitable for these measurements due to the increased symbol rate, therefore the lowpass filtering is performed using digital filtering function of the real-time oscilloscope. As seen in Fig. 4.19-a), at a symbol rate of 4 GS/s the demodulated signal quality is still very high, and first at 5 GS/s modulation rate an obvious degradation is observed. Using the simplified setup, the influence of the standing wave patterns are eliminated, and a superior performance is achieved. The 5 GS/s symbol rate is an expected limit, based on the measurements of the modulators.
4 Experimental Characterization of the Analog Demodulation

(a) 4 Gb/s  b) 5 Gb/s

Figure 4.19: Measured eye diagrams of the demodulated signal for BPSK input signals at a data rate of a) 4 Gb/s and b) 5 Gb/s.

(section 4.1.1) and the demodulators (section 3.1.6). Based on these results, it can be concluded that the realized synchronous demodulator can potentially demodulate QPSK signals with a rate of up to 10 Gb/s.

4.3.3 Sensitivity

The sensitivity of the analog demodulation is determined by BER measurements. The demodulated I and Q streams are fed to the FPGA evaluation kit through the limiting amplifiers, and the BERs of both streams are observed simultaneously. From this data, an average BER value is calculated, and is presented as the final result. The input power to the demodulator module is swept by adjusting the carrier power from the signal generators, and the exact incident average modulated power is measured using a power meter.

The measured average BER versus input power for different data rates is displayed in Fig. 4.20. As can be seen, at an average input power ranging from -5.5 dBm to -31 dBm no errors are detected for data rates of 1.562 Gb/s and 3.124 Gb/s. The same is true for an input power of -29 dBm, and a data rate of 3.906 Gb/s. The maximum power of - 5.5 dBm is the limit of the signal generation setup. These results show that the presented carrier recovery and demodulation concept is only weakly dependent on the input power. This is expected, as the fundamental limitation of the carrier recovery is the sensitivity of the frequency dividers placed after the bandpass filter. These dividers are sensitivity matched to 20 GHz and have a measured sensitivity below -30 dBm (section 3.1.4). From the results in Fig. 4.20, it can be concluded that no precise gain control is needed for successful synchronous demodulation. As done in this thesis, a preamplifier with a gain of around 20 dB already results in a dynamic range of 23.5 dB with a BER
4.3 Verification Experiments

Figure 4.20: The measured average BER versus input power for different data rates.

of $10^{-11}$ at a data rate of 3.906 Gb/s.

For the highest data rate of 6.248 Gb/s no errors are detected for only a very limited input power range from -17 dBm to -21 dBm. The exact reason of such a limitation is not completely clear, but there should be a strong influence of the standing wave patterns that arise due to the QPSK signal generation setup. It should also be noted that a signal level of -15 dBm already exceeds the 1 dB compression point of the preamplifier, which may explain the sudden decline at higher input signal levels at 6.248 Gb/s data rate. No such effect can be observed for the lower data rates, indicating that the influence of non-linear distortions alone are not very critical at reduced rates.

4.3.4 Variations in IF

Another interesting point is to determine the sensitivity of the analog demodulation to variations of IF. This is an important aspect, as during a wireless transmission there would be no synchronization between the transmitter and the receiver frequency synthesizers, leading to an IF uncertainty. In order to determine how much IF variation can be tolerated, the carrier frequency of the QPSK signal is varied and the resulting BER values are measured. The data rate is fixed at 3.906 Gb/s, which is the highest data rate where the analog demodulation performance is not degraded, according to the measurements in Fig. 4.20.

During these experiments it is determined that, as the IF is varied, the tuning voltage of the phase shifters has to be adjusted as well. This is due to the different phase
4 Experimental Characterization of the Analog Demodulation

Figure 4.21: Dependence of the phase shifter tuning voltage to input frequency variations for a BER of $10^{-11}$.

responses of the carrier recovery components at different frequencies, which in effect requires a different amount of phase compensation. This effect can be eliminated if the true-time delay error between the recovered carrier and the modulated signal is compensated, while delay compensation is a much more involved process compared to the phase compensation.

In Fig. 4.21, the required tuning voltage region for a BER of $10^{-11}$ is highlighted for varying IF. Through these measurements, it is determined that the carrier recovery is possible for a maximum frequency variation of 125 MHz, in agreement with the measured 3-dB bandwidth of the bandpass filter. Although such a large frequency variation can be tolerated, it is not very desirable that the tuning voltage needs to be adjusted accordingly. From Fig. 4.21, it can be seen that if the tuning voltage is fixed at a certain value, a frequency variation of up to 30 MHz can still be tolerated for a BER of $10^{-11}$. This frequency tolerance is sufficiently high, considering the frequency stability of commercially available reference sources (such as the ECS-3525 [110] used in the wireless experiments in chapter 5), which would lead to a maximum IF uncertainty in the range of 10 MHz, when used both at the transmitter and the receiver sides.

4.3.5 I/Q Imbalance

One advantage of the signal generation setup used in the verification experiments is that the QPSK signal is generated as a summation of two independent BPSK signals,
and the phase and amplitude imbalance between the two can be adjusted as desired. This gives the opportunity to characterize the analog demodulation performance against I/Q imbalance.

![Figure 4.22](image)

**Figure 4.22:** Measured phase states at the output of the QPSK modulator with an artificial phase imbalance of 11°. The IF equals 5.1 GHz.

In Fig. 4.22, a measurement case is displayed where a phase imbalance of 11° is artificially inserted to the QPSK signal. Similar to the shown case, by adjusting the relative phase and the amplitude of the carrier signals from the two signal generators, all the possible combinations of phase and amplitude imbalance can be tested.

![Figure 4.23](image)

**Figure 4.23:** Measured BER versus I/Q imbalance

In Fig. 4.23, the measured BER is displayed in a two dimensional plot with the y-axis standing for amplitude imbalance, and the x-axis for phase imbalance. The region of
phase and amplitude imbalance that can be tolerated for a BER of $10^{-11}$ is highlighted. The measurements are performed for more than 40 points, whereas in the plot in Fig. 4.23 only the limit conditions are displayed. As in the previous experiment, the data rate is fixed at 3.906 Gb/s. As seen, for a phase error up to 12.5° no errors are detected when no amplitude error is present. Similarly, for no phase error, an amplitude error of 6 dB can be tolerated. These results are promising, as state of the art transmitter frontends typically show a much better quadrature performance. In Fig. 4.23, the detection limit is plotted as well, where the I/Q imbalance gets too high for a stable carrier recovery. At the detection limit, the frequency dividers start to lose lock to the correct carrier frequency, leading to a continuous swapping of the I and Q streams due to the phase ambiguity. Since the FPGA evaluation kit used within these experiments is unable to detect such swapping of the baseband streams, an unstable carrier signal leads to a false detection of all symbols. Therefore, in a case where differential encoding is implemented, a higher detection limit can still be achieved.

### 4.3.6 Phase noise suppression

As a final test, the phase noise suppression capability of the proposed analog demodulation concept is experimentally verified. In order to perform this, a modification of the signal generation setup is required. To be able to generate QPSK signals with artificial phase noise, the carrier signal needs to be generated from only one signal generator. For this case, only the Agilent 4438C arbitrary waveform generator is used, which is able to apply a frequency modulation up to a symbol rate of 50 MS/s. The required 90° phase shift between the two BPSK signals is simply generated by proper choice of the cable lengths. However, this limits the carrier frequency to a very specific value, which is fixed at 5.0865 GHz. Already 6 MHz above or below this specific frequency, a phase error of 14° is measured, setting the limit to the maximum frequency deviation that can be tested.

In order to emulate a noisy carrier signal, two cases are considered. In the first case noisy FM modulation is applied to the carrier signal, and in the other case 16 FSK modulation with a symbol rate of 50 MS/s. In Fig. 4.24 the resulting BER measurements are displayed for different amounts of maximum frequency deviations. As can be seen, no errors are detected up to a maximum frequency deviation of 5 MHz, meaning that the recovered carrier follows the high speed frequency variations at the input. However, starting from a frequency deviation of 6 MHz, the phase error exceeds 12° leading to bit errors, and at a frequency deviation of 8 MHz no detection is possible.
4.3 Verification Experiments

Figure 4.24: Measured BER versus maximum frequency deviation of the artificially inserted phase noise

Figure 4.25: Measurements of the recovered carrier for a) no noise, b) FM noise with a maximum frequency deviation of 5 MHz, and c) 16 FSK modulation with a maximum frequency deviation of 5 MHz and a symbol rate of 50 MS/s.
4 Experimental Characterization of the Analog Demodulation

In Fig. 4.25, the measured spectra of the recovered carrier are displayed for no noise, the FM noise and the FSK modulation cases, while the maximum frequency deviation is fixed at 5 MHz. For these measurements the module v1 is used, and the input power is increased to -6 dBm. As seen the recovered carrier contains the artificially inserted phase noise for both FM and FSK cases.

The achieved phase noise suppression performance is expected based on the simulations presented in section 2.3.2, and the estimated true time delay within the carrier recovery as presented in section 3.3.2. Furthermore, the demodulator can potentially suppress phase noise with an even larger bandwidth than 5 MHz, while the experiments presented here are limited by the inherent phase error of the signal generation setup. It should also be kept in mind that realistic signal sources present a much more stable signal spectrum than the cases shown in Fig. 4.25. Therefore, it can be concluded that a substantial amount of phase noise cancellation should be expected, when the presented demodulator is used in a real system.

4.4 Summary

The results of the experimental characterization is summarized in Table 4.1. The results from other published demodulators in the literature are included as well for comparison.

As shown in the table, the presented synchronous demodulator achieves a very high data rate, exceeding those presented in [32] and [37]. Furthermore, as explained in section 4.3.2, the presented demodulator can potentially demodulate up to a data rate of 10 Gb/s, and such a high data rate is demonstrated only in [35] and [10].

In [35], the high data rate is achieved through differential demodulation, which requires the received signal to be delayed by an exact symbol duration. This needs to be precisely controlled, and even a reference signal would be required, because a constant clock frequency at the transmitter can not be guaranteed. The demodulator presented in this thesis requires a tuning voltage for the phase shifters as well, though its value is fixed, and is completely independent of the transmitter implementation and the data rate.

Excellent performance is demonstrated in [10], where a baseband demodulator is presented which includes carrier and clock recovery, as well as an adaptive channel equalizer. The drawback is that the carrier recovery is performed by a phase rotator, and the frequency offset between the transmitter and the receiver is not eliminated, but rather tolerated. This means that the QPSK constellation continuously spins, and the phase
### Table 4.1: Summary of the Results

<table>
<thead>
<tr>
<th>Technology Type</th>
<th>Modulation Type</th>
<th>Method</th>
<th>Data Rate (Gb/s)</th>
<th>BER</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>This</strong></td>
<td>0.8 µm SiGe HBT</td>
<td>QPSK</td>
<td>Feed-forward carrier recovery</td>
<td>6.248</td>
<td>$&lt;10^{-11}$</td>
</tr>
<tr>
<td>[32]</td>
<td>65 nm CMOS</td>
<td>QPSK</td>
<td>Costas loop carrier recovery</td>
<td>2.5</td>
<td>$&lt;10^{-9}$</td>
</tr>
<tr>
<td>[35]</td>
<td>100 nm InP HEMT</td>
<td>QPSK</td>
<td>Differential demodulation</td>
<td>10</td>
<td>$&lt;10^{-10}$†</td>
</tr>
<tr>
<td>[37]</td>
<td>90 nm CMOS</td>
<td>BPSK</td>
<td>Mixed Signal demodulator</td>
<td>2.5</td>
<td>$&lt;10^{-12}$†</td>
</tr>
<tr>
<td>[10]</td>
<td>65 nm CMOS</td>
<td>QPSK</td>
<td>Mixed Signal demodulator</td>
<td>10</td>
<td>$&lt;10^{-12}$†</td>
</tr>
</tbody>
</table>

† Short PRBS length of $2^7-1$

* Including RF-frontend

The phase rotator is continuously readjusted to follow these changes. This leads to a very limited range of frequency offset that this demodulator can tolerate, which is specified to be only 3 MHz in [10]. This requirement is very challenging to achieve, if not possible. Furthermore, the maximum frequency offset of 3 MHz is determined in a close to ideal measurement environment, and it is not clear if the phase rotator can follow this offset when other signal imperfections are present. Therefore, the baseband modem in [10] can benefit from the synchronous demodulator presented in this thesis, as it completely eliminates the frequency offset, alleviating the need for a continuous phase adjustment.

A drawback of the presented demodulator is clearly the high power consumption, especially when compared to the CMOS implementations. However, it should be mentioned that this does not arise from the proposed demodulation concept itself, but is rather due to the 0.8 µm HBT technology used for the prototype implementation, which requires substantially higher current drive for a proper operation of the transistors. Furthermore, the robustness against process variations needs careful consideration. In this thesis, two different prototype implementations are tested, and they are operated using the same tuning voltage for the phase shifters. This already indicates that the variations due to different implementations may not be very critical.

In summary, the presented demodulation concept is very simple, and needs only very little additional hardware effort compared to the other examples. The results show a demodulation capability of above 6 Gb/s data rate, high dynamic range, robustness
4 Experimental Characterization of the Analog Demodulation

against frequency variations, and most notably strong suppression of the accumulated phase noise of the transmitter and the receiver frequency synthesizers. The presented demodulator is very promising for short range, multi-Gbps wireless links, and it may as well be considered for optical links where the phase noise suppression can prove very beneficial.
5 Wireless Demonstration

In this chapter, the results on several wireless system demonstration experiments are presented. These experiments are performed as a part of the collaborative research project EASY-A (see section 1.3.1), utilizing the transmitter and the digital baseband realized by the project partners. In the first part of this chapter, the wireless demonstration setup is described in more detail, and the components realized by the project partners are shortly introduced. In the second part, the results on the wireless experiments are presented, where successful demodulation and detection of QPSK and BPSK modulated signals are achieved for a symbol rate of 3.456 GS/s, and for transmission distances of up to 1 m. Finally, the results of the wireless demonstration experiments are summarized in the last section.

5.1 Wireless Demonstration Setup

A simple block diagram of the wireless demonstration setup is displayed in Fig. 5.1. It consists of a transmitter frontend module, and a receiver chain consisting of a down-converter and the synchronous demodulator. The limiting amplifiers are included at the output of the synchronous demodulator in order to interface the digital baseband for BER testing.

The implementation of the shown setup has involved several project partners, with the following task assignments: The transmitter AFE was designed in the chair for Circuit and Network Theory within the technical university of Dresden (TUD-CCN). The receiver AFE was realized in the institute of Electron Devices and Circuits within Ulm university. The digital baseband design was performed in the Mobile Communications Systems chair in the technical university of Dresden (TUD-MNS). Finally, the antennas were designed in TES Electronics solutions. Short descriptions of these components are provided in the following.
5 Wireless Demonstration

5.1.1 Antennas

For the 60 GHz wireless demonstrator setup, custom designed antennas from TES Electronic Solutions [111] are used. The antennas consist of a 4x4 patch-array structure with double-sided printed circular dipoles. The substrate material is RT Duroid/5880 with a thickness of 128 µm and an $\epsilon_r$ of 2.2. The simulations show a 3-dB beamwidth of 12°, with a peak gain of 19 dBi, at a center frequency of 62 GHz. The measurements show 18 dBi gain in agreement with the simulations. More details are given in [112].

5.1.2 Transmitter Frontend

The block diagram the transmitter frontend is displayed in Fig. 5.2-a). It is a direct-conversion type transmitter, which consists of a frequency synthesizer, a vector modulator and a power amplifier. The frequency synthesizer is stabilized with a division ratio of 1024, and requires an external 60 MHz reference signal. The measured phase noise of the synthesizer equals -71 dBc/Hz at a 1 MHz offset frequency from the carrier centered at 61.44 GHz [113], while the loop bandwidth equals 1.6 MHz. The 90° phase shift of the oscillator signal is realized on the vector modulator with proper dimensioning of the routing lines. The vector modulator exhibits a low amplitude imbalance of 0.3 dB, whereas a phase imbalance as high as 20° is measured [114]. The stand alone on-wafer measurements of the power amplifier show an output 1 dB compression point of 8 dBm [115].
5.1 Wireless Demonstration Setup

Figure 5.2: Block diagram of the transmitter frontend and the module photograph. PFD: Phase frequency detector.

The realized transmitter frontend module is displayed in Fig. 5.2-b). It is a single board, multi-IC module, with the 60 GHz synthesizer, the vector modulator and the power amplifier ICs glued in a single cavity on the same carrier substrate. All the ICs are realized in IHP’s SG25H1 SiGe-C BiCMOS process ($f_T$ and $f_{max} \approx 190 \text{GHz}$). The substrate material is RT/Duroid 5880 on an FR-4 carrier, and the previously described 4x4 patch array antenna, and the 60 MHz reference oscillator (ECS-3525) are included on the board. The frequency response of the transmitter including the antennas are presented in section 5.2.1.

5.1.3 Receiver Frontend (Downconverter)

The block diagram of the receiver frontend is displayed in Fig. 5.3-a). It consists of an LNA, a downconversion mixer, a frequency doubler, and a subharmonic 32 GHz frequency synthesizer. The LNA is realized in IHP’s 0.25 $\mu$m SG25H1 SiGe-C BiCMOS technology, and on-wafer measurements show a gain of around 24 dB and a noise figure of 7 dB [116]. The other components are realized as a fully differential downconverter IC in 0.8 $\mu$m Telefunken Semiconductors SiGe2RF HBT technology. The on-wafer measurements of the downconverter show a gain of 5 dB and a bandwidth above 10 GHz. The frequency synthesizer exhibits a frequency stabilization loop with a division ratio of 64, and it requires an external reference signal with a frequency of around 1.024 GHz. The measured phase noise of the synthesizer equals $-106 \text{dBc/Hz}$ at an offset frequency of 1 MHz [46], while the loop bandwidth equals 50 MHz.
In Fig. 5.3-b), the photograph of the realized receiver frontend module can be seen. The substrate material is Rogers RT/Duroid 5880 with a thickness of 128 µm and an $\epsilon_r$ of 2.2. The LNA and the downconverter ICs are included in a single package, and glued on to a brass carrier through an opening in the substrate. An on-board rat race BALUN is included at the input of the LNA for differential to single-ended conversion. The input signal is applied through a V-band connector, and the previously described 4x4 patch array antenna can be connected to this interface as shown in Fig. 5.3-b).

The downconverter module is directly characterized through the V-band connector interface. The measurements show a gain of 24 dB, and a 3-dB IF bandwidth of approximately 10 GHz covering the whole 60 GHz ISM band. The measured input 1 dB compression point equals -27 dBm. From the measurements and the mixer simulations, a worst case NF of 11 to 12 dB is estimated [117].

5.1.4 Digital Baseband

Fig. 5.4 gives an overview of the digital baseband processing and illustrates the mapping of the processing blocks on a multi-FPGA hardware platform.

The multi-FPGA prototyping platform from the Dini Group [118] has been used for the hardware implementation. The platform is the same for the transmitter and receiver. It consists of a DN7006K10PCIe-8T board with six Altera Stratix III(3SL340) FPGAs, which is extended by a DNMEG.2SGX daughter-card with an Altera Stratix II GX FPGA. The multi-gigabit transceivers of the Stratix II GX enable the 1-bit
5.1 Wireless Demonstration Setup

![Diagram of wireless demonstration setup]

Figure 5.4: Overview of the digital baseband processing mapped on a multi-FPGA hardware platform. S/P: Serial to parallel converter.

data conversion which serves as the interface to the AFE. Symbol clock recovery at the receiver side is realized within the analog clock recovery unit (CRU) of each multi-gigabit transceiver using the analog training sequences of the received data frames. Each data frame consists of a payload part and a preamble, while the digital baseband is designed for a burst-wise data transmission. The preamble consists of:

- an analog training sequence of length 2048 with alternating 1 and 0 for data clock recovery at the receiver,

- a digital training sequence of length 1024 for frame detection and ambiguity correction, and

- a signaling field that can carry up to 32 header bits for the medium access control (MAC) layer, which are encoded with a spreading sequence of length 32.

The digital training sequence is an M-sequence of 1023 +1 bits, which is different for the in-phase and quadrature-phase. This allows to resolve phase ambiguities of 90° digitally at the receiver. The payload configuration accounts for the limited clock rate of 108 MHz through a massive parallelization. That is, the payload of each data
frame is composed of 64 lower rate data sequences that can be processed in parallel. For error-correction, the payload data is encoded with a convolutional code of rate 1/3. Termination and puncturing are used to achieve an effective code rate of 3/4, as described in [119]. Differential modulation is used for robustness against interruptions and phase ambiguity that could occur during the reception of a data frame. A detailed description of the baseband algorithms that realize the frame generation at the transmitter and the data detection and decoding at the receiver can be found in [11].

The digital baseband implementation at the receiver side includes a BER calculation, which allows to evaluate the system performance when pseudorandom data is transmitted. The calculation compares the decoded data bits of all received frames to the pseudorandom data sequence. Finally, the BER result can be transferred to a Host PC via a JTAG interface for visualization.

5.2 Results

A photograph of the wireless demonstration setup is displayed in Fig. 5.5. For the wireless experiments, the receiver and transmitter frontends are placed at a distance varying from 10 to 100 cm, while the antennas are facing each other. The reference
signal of the downconverter module is supplied from a signal generator, and is adjusted to have an IF of around 5.1 GHz. At the receiver baseband, power splitters are utilized after demodulation to acquire BER and eye diagram measurements simultaneously.

### 5.2.1 Frequency Response

In order to characterize the wireless link, the transmitted power is measured at the receiver antenna interface. For these measurements, the receiving 4x4 patch array antenna is connected to a spectrum analyzer and placed at a distance of 30 cm to the transmitter. In order to acquire a frequency response of the wireless link, one of the baseband inputs of the transmitter is driven by a sinus signal, while the other input is terminated. By sweeping the frequency of the input signal, the frequency response of the transmitter module in combination with the antennas and the wireless channel is extracted.

![Figure 5.6: Measured power versus frequency at the receiver antenna interface for a transmission distance of 30 cm.](image)

The result is displayed in Fig. 5.6. As can be seen, a non-flat frequency response is determined, with a 3-dB bandwidth of 1.4 GHz centered at 61.5 GHz. Furthermore, gain ripples of up to 6 dB are observed within 59 to 64 GHz range. As the high gain antennas are placed in close proximity for these measurements, it is assumed that the non-flat behavior is mainly dominated by the transmitter characteristics. Still, the non-flat frequency response should be tolerable based on the simulations presented in section
2.3.3, although with a higher SNR penalty than the simulated cases.

Due to the low signal power at the antenna interface, the modulated signal spectrum is measured after the downconversion, which provides an amplification of more than 20 dB. The measured spectrum of a QPSK modulated signal with a symbol rate of 3.456 GS/s is displayed in Fig. 5.7, which is received at a transmission distance of 30 cm. Strong spurious components are noticeable at a distance of half the symbol rate to the carrier, which occur due to the training sequences at the beginning of each data frame. The received power after downconversion is sufficiently high for the analog demodulation, which is measured to be in the range of -10 dBm to -20 dBm, depending on the distance and the alignment of the receive and transmit antennas.

**5.2.2 Recovered Carrier**

As a first step to verify the analog synchronous demodulation, the spectrum of the recovered carrier signal is measured. Similar to the verification experiments presented in section 4.3.1, the demodulator v1 is utilized for these measurements. In Fig. 5.8, the measured spectrum of the recovered carrier signal is displayed for two different measurements spans.

It is seen in Fig. 5.8 that two independent phase noise profiles are superimposed on the
5.2 Results

Figure 5.8: The measured spectrum of the recovered carrier signal for a) a span of 250 MHz and b) a span of 10 MHz.

The measured spectrum of the recovered carrier signal. For the measurement with a span of 250 MHz, the phase noise profile of the receiver frequency synthesizer can be observed with a loop bandwidth of approximately 50 MHz. On the other hand, for a measurement span of 10 MHz the phase noise profile of the transmitter frequency synthesizer is clearly visible with a loop bandwidth of approximately 1.5 MHz. Furthermore, the reference spurs of both frequency synthesizers are detectable as well in the spectrum of the recovered carrier. These results are in agreement with the expectations, based on the system simulation results presented in section 2.3.2, as well as the stand alone measurements of the transmitter and receiver frequency synthesizers presented in [46] and [113], respectively.

It is seen in Fig. 5.8-b) that the transmitter frequency synthesizer exhibits a very high phase noise, with a relative power level of -70 dBc/Hz at an offset frequency of 1 MHz. Unless eliminated, such high phase noise would lead to a strong degradation of the system performance (for instance see Fig. 2.7 in section 2.3.2). The transmitter is intentionally designed with a larger loop bandwidth to achieve a fast settling time of 4 µs, however resulting in a high noise level due to the high division ratio of 1024. A fast settling time is required by the system specifications, which foresee a time-duplexing operation [113]. Considering the estimated delay within the carrier recovery in section 3.3.2, a very strong suppression of the transmitter phase noise is expected, as the loop bandwidth is sufficiently small, based on the predictions presented in section 2.3.2.
However, when the receiver phase noise profile is considered, a degraded phase noise suppression is expected due to the larger loop bandwidth as shown in Fig. 5.8-a). On the other hand, owing to the small division ratio of 64, the noise level of the receiver frequency synthesizer is much lower compared to the transmitter or the simulated cases in section 2.3.2. Therefore, despite the degraded phase noise suppression, it can be assumed that the receiver frequency synthesizer would have a low effect on the system performance.

### 5.2.3 Eye Diagrams

In the next step, the eye diagrams of the demodulated bit-streams are measured. In order to evaluate the signal quality, these measurements are performed before the limiting amplifiers, and the required lowpass filtering is performed using the digital filtering function of the real-time oscilloscope.

The eye-diagrams of the demodulated I/Q patterns for QPSK transmission at a distance of approximately 35 cm are displayed in Fig. 5.9. For the target symbol rate of 3.456 GS/s shown in Fig. 5.9-b), the demodulated signal quality is poor, with visible disturbances in the eye diagram which would lead to bit errors. The QPSK performance is limited mainly by two factors: On the one hand the strong phase imbalance of 20° inherent to the transmitter frontend, on the other hand the limited 3-dB bandwidth of 1.4 GHz of the wireless link as shown in Fig. 5.6. The influence of the phase imbalance is partially alleviated by adjusting the tuning voltage of the phase shifters in order to acquire a setting, which leads to an equal amount of phase error for both I and Q patterns. The phase adjustment is performed by simply observing the demodulated eye patterns, until a point is achieved where both patterns look similar. This approach is valid as long as the phase error at the transmitter is known and remains constant. It should also be noted that a phase imbalance of 20° is not typical for a vector modulator [120], and a better performance can be achieved by a redesign of the transmitter.

Apart from the phase imbalance, the limited bandwidth of the wireless link leads to an unavoidable distortion of the demodulated signal, observed as a vertical closure of the eye diagram. When the symbol rate is halved, a much better performance can be achieved as seen in Fig. 5.9-a). For this symbol rate, the signal does not suffer from the limited bandwidth, and a superior demodulated signal quality is achieved. No degradation of the eye quality factor is determined for varying transmission distances from 15 cm to 90 cm, which was the mechanical limit of the setup. On the other hand, a maximum transmission distance of three meters is estimated, based on the measured
5.2 Results

(a) 1.728 GS/s QPSK (2.5 Gbit/s net)

(b) 3.456 GS/s QPSK (5 Gbit/s net)

Figure 5.9: The measured eye diagrams of the demodulated I and Q streams after wireless transmission over a distance of 35 cm for a QPSK symbol rate of (a) 1.728 GS/s and (b) 3.456 GS/s.

received power and the sensitivity of the analog synchronous demodulator presented in section 4.3.3.

A further way to improve the link performance is to reduce the modulation format to BPSK, by disconnecting one of the baseband inputs of the transmitter. This eliminates the influence of the phase imbalance, which leads to a much better demodulated signal quality. This can be seen in Fig. 5.10, where the demodulated bit-stream for a 3.456 GS/s BPSK input signal is displayed.
5.2.4 Bit Error Rate Measurements

After the demodulation, the baseband I and Q symbols are amplified by the limiting amplifiers, which are described in section 4.1.2. The amplitude limited baseband patterns are then fed to power splitters, which divide the signals for simultaneous eye diagram measurements and BER testing. This can be seen in Fig. 5.5, which shows QPSK transmission at a symbol rate of 3.456 GS/s, resulting in a net data rate of 5 Gb/s. For the QPSK transmission at full-rate the link performance is relatively poor, with a net bit error rate in the range of $10^{-5}$. The poor performance is rather expected due to the large phase imbalance of 20° inherent to the transmitter, and the limited bandwidth of the wireless link. Based on the verification experiments in chapter 4, it is known that these limitations are close to the detection limit of the analog demodulation. Still, despite the imperfections of the wireless setup, the synchronously demodulated signal can be detected without any frame loss, showing successful implementation of the full system demonstrator, and successful real time packet detection and decoding in the digital baseband at the full target transmission speed.

Although a much better QPSK performance can be achieved at a reduced transmission rate as seen in Fig. 5.9-a), the receiver digital baseband timing could not be adapted to the reduced symbol rate within the limited time reserved for the experiments. Therefore, no BER measurements could be performed for the reduced-rate QPSK signals. On the other hand, the digital baseband could be adapted for BPSK detection by providing the same data pattern to the I and Q branches, and the BER performance is tested for BPSK signals operating at full-rate.

In Fig. 5.11, the eye-diagram of the demodulated 3.456 GS/s BPSK signal, and the
Figure 5.11: The demodulated bit-stream for 3.5 GS/s (2.5 Gb/s net) BPSK transmission over a distance of 40 cm.

corresponding BER measurement results are displayed. The eye-diagram measurements are performed after the limiting amplifiers, and as seen from the figure, a completely open-eye is measured. The digital baseband can detect this signal without any frame or bit-loss, resulting in an error-free transmission at a net data rate of 2.5 Gb/s.

Table 5.1: Summary of the Results

<table>
<thead>
<tr>
<th>Module</th>
<th>Power Consumption</th>
<th>Modulation</th>
<th>Data Rate</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Demodulator</td>
<td>575 mW(^{\dagger})</td>
<td>QPSK</td>
<td>5 Gb/s</td>
<td>(\approx 10^{-5})</td>
</tr>
<tr>
<td>Limiters</td>
<td>1.1 W</td>
<td></td>
<td>(6.9 Gb/s raw)</td>
<td></td>
</tr>
<tr>
<td>Downconverter</td>
<td>500 mW</td>
<td>BPSK</td>
<td>2.5 Gb/s</td>
<td>(&lt; 10^{-10})</td>
</tr>
<tr>
<td>Transmitter</td>
<td>819 mW</td>
<td></td>
<td>(3.4 Gb/s raw)</td>
<td></td>
</tr>
</tbody>
</table>

\(^{\dagger}\) Includes IF LNA and operated from a single supply voltage of 3.5 V
5 Wireless Demonstration

5.3 Summary

In general, the presented wireless demonstrator proves the validity of the proposed analog demodulation concept. The results on the full system demonstrator experimentally confirm that wireless data transmission is possible at multi-Gbps rates, without relying on advanced digital signal processing. With only 1-bit analog to digital conversion, successful frame detection and data correction is achieved at a net data rate of up to 5 Gb/s. Furthermore, excellent performance is demonstrated when the modulation type is reduced to BPSK, alleviating the strong phase imbalance of the transmitter. An error free, net data rate of 2.5 Gb/s is achieved for a wireless transmission distance of up to 1 m. Apart from the successful synchronous demodulation of such high data rate signals, it can be claimed that the phase noise suppression feature of the presented demodulator has greatly improved the wireless demonstrator performance. Unless suppressed, the large amount of phase noise inherent to the transmitter frequency synthesizer should result in poor link performance. Therefore, when the demodulated signal quality is examined, and the resulting BER measurements are taken into account, it can be concluded that the wireless system demonstrator benefits from the phase suppression feature of the presented demodulation concept. The achieved results are summarized in Table 5.1.

Further results on wireless demonstration experiments can be found in Appendix C, where measurements with hand-held antennas are presented using a separate wireless demonstration setup. These results show that the synchronous demodulation is robust, and is unaffected from the variations of the antenna position and distance, confirming that the proposed analog-oriented wireless receiver concept is promising to be used in mobile applications.
6 Outlook: Towards Miniaturization

Within this thesis, the presented circuit components serve as prototype implementations with large dimensions and bulky housing. The experimental results acquired using the prototype modules show the validity of the proposed analog synchronous receiver concept. In this chapter, an outlook is provided by introducing potential techniques towards a miniaturized system, and the first results towards such a system are presented.

6.1 System in Package Integration

It is mentioned in the introduction chapter of this thesis, that there is a trend in the recent literature towards utilizing more in package integrated systems, which benefit for instance from external passive components such as antennas and filters within a single compact RF-module. Such SiP components can provide potentially lower cost solutions, as they can include more functionalities, and their design can be performed within a substantially shorter time period [121].

The RF-modules presented in this thesis, which are realized as prototypes for proof of concept of the analog demodulation, already represent example cases for SiP integration. The synchronous demodulator module presented in section 3.3.3 includes a very compact and sharp bandpass filter within its package, which is an essential and crucial component for the whole system. The transmitter module presented in section 5.1.2 includes a 4x4 patch array antenna, which interfaces the power amplifier IC through conventional wire-bonds. These off-chip components are realized on the same low-cost substrate material (RT/Duroid 5880), and in principle they can be integrated within a single RF-module. This would provide a very low-cost solution, which would be promising for applications where the component cost has the highest priority.

However, with respect to dimensions, a more advanced approach found in the literature is to utilize high performance multi-layer material stacks as board material such as LTCC (Low temperature co-fired ceramics). Although LTCC is a much more expensive process compared to conventional Teflon material, utilization of an LTCC or a similar process can
provide a much better solution towards a miniaturized system. An excellent example of such a system from the recent literature can be found in [122], where a 4-element phased array transceiver is introduced operating at 60 GHz, which occupies an area of only 4 cm$^2$. Such integration is very well suited for the presented receiver as well, as passive off-chip components are essential for the carrier recovery. In Fig. 6.1, a potential SiP integrated analog-oriented wireless receiver is illustrated.

Figure 6.1: Illustration of a potential “System in Package” integrated analog-oriented wireless receiver.

In such an integrated receiver, ICs in different technologies can be utilized within the same package, as has already been done in this thesis. For instance, the low-cost 0.8 μm HBT technology can be utilized for the demodulator and downconverter implementation, while the high performance 0.25 μm BiCMOS technology may be preferred for the LNA realization. The passive components can be implemented in the top-most metal, as well as in the intermediate metal-layers, utilizing the area below the ICs. High gain antennas can be realized in relatively small dimensions [123], [124], making use of cavities in the board material.

### 6.2 Monolithic Integrated Receiver

For the experimental results presented throughout the thesis, the analog-oriented wireless receiver consists of two separate RF-modules, namely a downconverter and the synchronous demodulator. This technique was preferred, in order to allow separate characterization and verification of the analog demodulation concept. As a final implementation, a monolithic integrated IC is realized towards a miniaturized system, which includes the two functional blocks (downconversion and demodulation) as shown in Fig. 6.2.

The IC occupies an area of 4.86 mm$^2$, and is operated from two supply voltages of 2.8 V and 3.5 V, while the total power consumption equals 750 mW. The variable gain
amplifier presented in section 3.1.7 is included between the synchronous demodulator and the downconverter as a buffer stage. In combination with a high-performance LNA, the presented IC can be utilized towards a miniaturized SiP as illustrated in Fig. 6.1.

6.3 LTCC Bandpass Filter

A further step towards a miniaturized system is to facilitate improved integration techniques for the bandpass filter required for the carrier recovery. As an initial result towards such an integration, an LTCC module is realized within the framework of the collaborative research project EASY-A. The design is performed by Benedikt Schulte in EADS Innovation Works in Ottobrunn, Munich. The photograph of this module is displayed in Fig. 6.3.

The LTCC module is designed for the demodulator IC presented in section 3.3.1, but a similar module can be designed for the monolithic integrated receiver shown in Fig. 6.2 as well. The BPF design used in this module is described in [101]. It is an evanescent mode cavity (EMC) filter, and the measurements show a 3-dB bandwidth of 350 MHz centered at 20 GHz, and an insertion loss of 3.7 dB. The filter is integrated below the IC area as foreseen in Fig. 6.1, substantially reducing the dimensions of the LTCC module.
In order to verify the operation, functional tests were performed on the LTCC module using a test fixture setup, and successful carrier recovery is demonstrated. These results are presented in Appendix section D. The presented LTCC module represents a first step towards a completely miniaturized SiP, occupying a total area of only 0.7 cm².
7 Summary and Conclusion

In this thesis, an analog receiver frontend for short-range ultra-wideband wireless communication applications was presented. The proposed receiver is unique, compared to wireless receiver architectures investigated in the last 20 years. While a typical analog frontend performs the amplification and the downconversion of a received signal to a frequency range suitable for analog to digital conversion, the proposed receiver performs an additional function of analog synchronization, without assistance from the digital part of the system. The proposed “analog-oriented” receiver is very promising compared to a “digital-oriented” receiver for specific application scenarios, which target very high speed data transmission over short distances wirelessly.

The proposed analog-oriented receiver was investigated in a simulation environment to determine its feasibility and the expected performance. A very promising observation was that the proposed receiver performance is only minutely affected by the wireless channel at short transmission distances, based on system simulations performed using measured channel data. Furthermore, the highly interesting feature of phase noise suppression was investigated in detail, again showing very promising results which indicate that the proposed receiver can improve the performance of the wireless system to a great extent through the phase noise suppression capability. In addition, through this feature the complexity of the complete system can be further reduced, by eliminating the demanding requirements from the frequency synthesizers. A drawback of the proposed receiver determined through these simulations was the need for a very sharp bandpass filter. This requirement makes the implementation of a system on chip not possible, however, in the thesis solutions were investigated which easily mitigate this disadvantage.

Further along the thesis, detailed information was given on the implementation of a prototype analog synchronous demodulator module, which performs the core analog signal processing part of the proposed receiver. Each individual component towards this module was described in detail and compared to the state of the art, either showing comparable, or better performance.
The realized module was characterized through custom generated multi-Gbps modulated QPSK signals. Synchronous demodulation capability up to a data rate of 6.248 Gb/s was shown, and demodulation potential up to a data rate of 10 Gb/s was demonstrated. Furthermore, it was determined that the realized module shows a very high dynamic range above 20 dB, and that it can tolerate large variations of the input frequency. The phase noise suppression capability was experimentally validated as well, by showing demodulation of signals with artificially inserted phase noise.

For a “real” verification of the proposed analog-oriented wireless receiver architecture, results on a complete system demonstrator were presented. Within the system demonstrator the digital baseband design was completely realized in 1-bit resolution, without including dedicated analog-to-digital converters. Excellent performance was demonstrated, showing successful demodulation and detection of QPSK signals with a data rate of as high as 5 Gb/s (6.912 Gb/s raw). The QPSK performance was relatively poor with a measured BER in the range of $10^{-5}$, whereas the performance was mostly associated with the strong quadrature phase error inherent to the transmitter used in the experiments. Superior performance was achieved for BPSK transmission with a net data rate of 2.5 Gb/s (3.456 Gb/s raw), achieving error-free transmission wirelessly for distances below 1 m.

Finally, an outlook towards a miniaturized implementation of the proposed receiver was provided, which could go far beyond the prototype implementations presented in the thesis, and the first results towards such integration were shown.

In conclusion, the proposed unique but simple receiver architecture is very promising for short-range ultra-wideband wireless communications. The proposed receiver can substantially reduce the cost of a wireless system by simplifying it. However, the price paid is the flexibility of the system, and such an analog-oriented receiver can target only very specific, but valid application scenarios. Nevertheless, it was shown in this thesis that performing signal processing in the analog domain is a reasonable approach. Therefore, a general conclusion can be derived that as the data rates of communication systems continue to increase, the importance of analog signal processing to assist the digital systems will grow. Thus, we should expect seeing more frontends with various analog signal processing capabilities in the near future.
Appendix

A Compact BPSK Carrier Recovery

In this part, a compact BPSK carrier recovery IC is introduced, which performs BPSK carrier recovery without relying on off-chip bandpass filtering. The BPSK carrier recovery is verified by on-wafer measurements, and the results on successful carrier recovery is presented. These results support the conclusions of the system simulations presented in section 2.3.1, and show that BPSK modulation may still be preferred for very low cost and compact systems.

In chapter 4, it is mentioned that the realized analog QPSK demodulator is able to demodulate BPSK modulated signals, and this is experimentally demonstrated in section 4.3.2. However, BPSK carrier recovery can be achieved in a much simpler way, and it is not necessary to generate a fourth harmonic signal to eliminate the modulation content, but a second harmonic generation is sufficient. This can easily be seen when the following BPSK signal is examined

\[ s(t)_{\text{BPSK}} = S_C(t) \cos[\omega_C t + m \cdot \pi + \phi_{in}(t)], \quad (A\ 1) \]

where \( S_C(t) \) represents the amplitude, \( m \) equals -1 or 1, and \( \omega_C \) and \( \phi_{in}(t) \) are the carrier frequency and phase to be recovered. As seen it is sufficient to generate a second harmonic component to suppress the modulation content by expanding the 180° phase transitions into 360°.

Another important aspect is the less demanding bandpass filter requirement for BPSK carrier recovery. Based on the system simulations presented in section 2.3.1, it is seen that the BPF requirement for BPSK modulated signals is much more relaxed in comparison to the QPSK modulation case. For example, the simulations show that a 3-dB bandwidth of 1 GHz would already be sufficient to achieve a close to ideal receiver performance. When the input signal is only to be frequency doubled, a BPF with a fractional bandwidth of 10% would be sufficient, if IF is kept at 5 GHz. Therefore, a complete on-chip implementation becomes feasible, without relying on external filtering.
Figure A.1: Block diagram of the proposed BPSK carrier recovery circuit

The block diagram of the proposed simple BPSK carrier recovery method is displayed in Fig. A.1. It consists of a single frequency doubler and a single frequency divider. The filtering is achieved by utilizing a resonant circuit at the doubler-divider interface, realized by shunt inductors and the parasitic capacitors of both stages.

In Fig. A.2, the chip photograph of the realized BPSK carrier recovery circuit is displayed. It consists of a frequency doubler and a divider, directly connected together without contact pads. The IC is realized in Telefunken Semiconductors SiGe2RF 0.8 µm HBT technology. The IC is very compact with a total area of 0.33 mm², and is operated from a single supply voltage of 2.5 V drawing 22 mA current.

The frequency doubler and the frequency divider used in the design of the BPSK carrier recovery circuit uses the same topologies presented in sections 3.1.3 and 3.1.4. The only modification is that the output of the doubler is power matched to the input of the frequency divider instead of a 100 Ω load impedance, and the divider is sensitivity matched to 10 GHz instead of 20 GHz. The simulations show a 3-dB bandwidth of 2 GHz (RBW 20%) at the doubler-divider interface. Based on the system simulations, the achieved bandwidth should already be sufficient for successful BPSK carrier recovery.

The BPSK carrier recovery circuit is tested on-wafer. The BPSK modulated input signal is generated using one of the packaged modulators presented in section 4.1.1, and the Xilinx ML605 FPGA evaluation kit. The jitter of the recovered carrier signal is measured at the output of the BPSK carrier recovery IC, using a real-time oscilloscope.

The measured standard deviation of the jitter versus data rate is displayed in Fig. A.3. The results for QPSK demodulation from chapter 4 are included as well for comparison.
As can be seen in the figure, the carrier signal can be recovered for all the measured data rates, and the measured jitter is still tolerable, especially considering that the BPSK modulation is less susceptible to phase error. Due to the lack of a BPF, the recovered carrier performance shows a slightly higher dependence on the data rate, compared to the QPSK carrier recovery. Furthermore, a strong dependence on the input power is
determined, as shown in Fig. A.4.

![Figure A.4: Measured standard deviation of the recovered carrier period versus the input power for 3.124 Gb/s BPSK modulation.](image)

Apart from the strong dependence of the jitter characteristic on the input power, it can be further deduced from Fig. A.4 that the BPSK carrier recovery is only possible for a very limited input power range from -12 dBm to -18 dBm. Interestingly, the required input power is very low compared to the QPSK case, for which the highest power of -5.5 dBm available from the signal generation setup can be used. This indicates potential leakage effects, such as the fundamental signal at the divider doubler interface. The tuned L-C load at this interface is insufficient to completely suppress this component, which leads to carrier recovery failure at high input signal levels.

This behavior makes the sensitivity of the dividers very critical, as for such low input power levels the second harmonic power at the output of the doubler decreases quadratically. Therefore, this leads to the suspicion that the BPSK carrier recovery may be highly susceptible to the variations of the supply voltage, which would change the sensitivity behavior of the dividers. In order to test this, the input power is fixed at -15 dBm, and the supply voltage is varied from 2.2 V to 2.8 V. The results show only a very slight dependence on the supply voltage, where the standard deviation of the recovered carrier period varies only slightly from 3.2 ps to 3.6 ps.

The presented results are all in agreement with the expectations. For the QPSK carrier recovery, the performance is mainly determined by the bandwidth of the BPF and the dependence on the data rate and the input power is very low. This is not the
case for the BPSK carrier recovery circuit, as there is no dedicated filter included. In conclusion, the performance is acceptable, and the presented BPSK carrier recovery IC may be used towards a completely monolithic integrated BPSK receiver with very compact dimensions and low power consumption. The performance can be further improved by including a dedicated on-chip filter at the doubler-divider interface, such as a tuned amplifier.

B Measurements of the Baluns and the Power Dividers

In this part, the measurements of the ultra-wideband baluns and power dividers are provided. These components were available from a previous project [125], and they are used within this thesis without any modification.

Figure B.1: S-parameter measurements of the baluns.

In Fig. B.1, the S-parameter measurements of the two baluns are displayed. The
baluns exhibit a 3-dB bandwidth from 1.3 GHz to 9.4 GHz, and from 1.3 GHz to 9.8 GHz, respectively. The measured insertion losses for balun1 and balun2 are 1.3 dB and 0.9 dB at 5 GHz. For both baluns, the phase error remains within ±5 degrees up to 13 GHz. On the other hand, the return losses decrease below 4 GHz and around 8 GHz. This behavior leads to measurement inaccuracies when differential calibration is performed using these baluns.

In Fig. B.2, the S-parameter measurements of the two power dividers are displayed. The power dividers are extremely broadband, with a 3-dB bandwidth in excess of 15 GHz. The measured insertion loss for both power dividers is 0.5 dB at 5 GHz. Furthermore, for both components the phase error remains below 5 degrees up to 11 GHz, and the return losses are higher than 10 dB from 1 to 11 GHz.
C Measurements with Hand-Held Antennas

Following the guiding data kiosk application scenario described in section 1.3, the wireless data transmission is tested using a hand-held antenna in a separate wireless demonstrator. For these experiments a prototype transmitter module is utilized, which is developed by TES Electronic Solutions [111]. The module has a very limited 3-dB IF bandwidth of 0.6 GHz centered around 4 GHz, which strongly limits the maximum data rate that can be demonstrated. As shown in Fig. C.1, this transmitter module is used to upconvert BPSK modulated signals to 60 GHz. The modulation type is limited to BPSK in order to simplify the experimental setup, and for the modulation the custom designed BPSK modulators (section 4.1.1) and the ML605 Xilinx FPGA evaluation-kit is used. The receiver frontend is described in section 5.1.3, for the demodulation the module v2 (section 3.3.3) is used, and at the baseband the lowpass filters described in section 4.1.2 are included.

![Block diagram of the wireless demonstration setup utilizing hand-held antenna at the transmitter side.](image)

The photograph of the experimental setup is displayed in Fig. C.2. As seen the transmit antenna is hand-held, which is a W-band circular horn antenna with a gain of around 20 dBi at 60 GHz. The hand-held antenna is used at the transmitter side.
to ease the mechanical setup. The receiver antenna is the 4x4 patch array antenna described in section 5.1.1, and its position is fixed. During these experiments, the wireless transmission distance is continuously varied from 30 cm to a maximum distance of 225 cm, which was the mechanical limit of the setup. The resulting eye diagram measurements for 1 Gbit/s BPSK transmission for the maximum and the minimum transmission distances is displayed in Fig. C.3.

As seen, successful synchronous demodulation is achieved up to a transmission distance of above 2 m, whereas the measured eye-quality factor is only slightly degraded, and equals 14.5 for a transmission distance of 30 cm, and 12.3 for a transmission distance of 225 cm. Furthermore, through these experiments it is determined that the analog demodulation concept is suitable to be used in mobile devices, and is unaffected by effects which would arise in typical applications such as slight antenna misalignment, unstable antenna position, and variations in the transmission distance. In these experiments, successful demodulation is achieved for large transmission distances, owing to the high antenna gain both at the transmitter and the receiver sides. On the other hand, this requires careful alignment of the antennas, especially for larger transmission distances, which is undesirable. For real applications, more omni-directional antennas should be preferred which would ease alignment, but may limit the maximum transmission distance due to multi-path propagation.
D Measurements of the LTCC Module

In this part, measurement results are provided on the LTCC module with the EMC cavity filter presented in Chapter 6. Detailed description of the module properties and the BPF design can be found in [101]. For the characterization of the LTCC module, a test fixture is realized which is displayed in Fig. D.1.

The substrate material is RO4003 with a dielectric constant of 3.3, and a thickness of 508 µm. The LTCC module is directly glued on an aluminum carrier through an opening in the substrate. The LTCC is connected to the RO4003 substrate via conventional wire-bonding, and the outputs are provided by SMA connectors. Functional tests of this test fixture are performed by applying BPSK signals at the input. The BPSK modulator is...
Figure D.1: The LTCC module with the EMC cavity filter mounted on a test fixture.

described in section 4.1.1, and the baseband signal is supplied from the Virtex6 FPGA evaluation-kit described in section 4.2. At the output, the recovered carrier and the demodulated bit-stream are measured.

Figure D.2: Measured standard deviation of the recovered carrier period versus data rate for the LTCC module.

In Fig. D.2, the measured standard deviation of the recovered carrier period versus the data rate is displayed. The results from section 4.3.1 are included for comparison. As can be seen, the LTCC module achieves only a very slight performance improvement. As a reminder, the BPF within the RT/Duroid 5880 module has a measured 3-dB bandwidth of 460 MHz (section 3.3.2), whereas the EMC filter within the LTCC
module exhibits a 3-dB bandwidth of 350 MHz. The main reason for no discernible performance improvement is that the modulated test signals used in these experiments are not band-limited. According to the system simulations presented in section 2.3.1, when the modulated signal is not strongly band-limited, a filter bandwidth of 500 MHz should already result in close to ideal receiver performance. Therefore, the presented measurement results coincide with the conclusions from the simulations, and for both modules the carrier recovery performance is very good.

In Fig. D.3, the measurement of the demodulated data pattern is displayed, for a 3.124 Gb/s BPSK modulated input signal. As expected, successful demodulation is achieved, resulting in an open-eye with an eye quality factor of 5.4. However, the signal quality is worse when compared to demodulated BPSK signals presented in section 4.3.2. It is assumed that the main reason is the LTCC to RO4003 interface, which introduces a discontinuity, distorting the signal. As can be seen in the right hand side of Fig. D.1, there are large gaps at these interfaces, leading to wire-bond lengths in excess of 500 µm. This is critical especially at the input, where a ultra-wideband signal is applied at 5 GHz. In a future design, this interface can be optimized, which should result in a better performance.

As a conclusion, the functionality of the synchronous demodulator is verified in a very compact SiP module. The measurement results meet the expectations, whereas the poor demodulated pattern quality can be improved in a future design. The LTCC module occupies an area of only 0.7 cm², which demonstrates a great potential towards a completely miniaturized wireless receiver.
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog to digital converter</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced design system</td>
</tr>
<tr>
<td>AFE</td>
<td>Analog frontend</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude modulation</td>
</tr>
<tr>
<td>APF</td>
<td>Allpass filter</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application specific integrated circuit</td>
</tr>
<tr>
<td>AWGN</td>
<td>Additive white Gaussian noise</td>
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<tr>
<td>BER</td>
<td>Bit error rate</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass filter</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary phase-shift keying</td>
</tr>
<tr>
<td>CFR</td>
<td>Channel frequency response</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common mode rejection ratio</td>
</tr>
<tr>
<td>DE</td>
<td>Differentially encoded</td>
</tr>
<tr>
<td>DR</td>
<td>Dielectric resonator</td>
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<tr>
<td>DSP</td>
<td>Digital signal processor</td>
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<tr>
<td>EM</td>
<td>Electromagnetic</td>
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<tr>
<td>EMC</td>
<td>Evanescent mode cavity</td>
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<tr>
<td>FM</td>
<td>Frequency modulation</td>
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<tr>
<td>FOM</td>
<td>Figure of merit</td>
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<tr>
<td>FSK</td>
<td>Frequency-shift keying</td>
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<tr>
<td>FPGA</td>
<td>Field programmable gate array</td>
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<tr>
<td>Gbps</td>
<td>Gigabit-per-second</td>
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<tr>
<td>GSG</td>
<td>Ground-signal-ground</td>
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<tr>
<td>IC</td>
<td>Integrated circuit</td>
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<tr>
<td>IEEE</td>
<td>Institute of electrical and electronics engineers</td>
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<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-symbol interference</td>
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<tr>
<td>Acronym</td>
<td>Description</td>
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</tr>
<tr>
<td>ISM</td>
<td>Industrial scientific medical</td>
</tr>
<tr>
<td>ITRS</td>
<td>International technology roadmap for semiconductors</td>
</tr>
<tr>
<td>HBT</td>
<td>Hetero-junction bipolar transistor</td>
</tr>
<tr>
<td>HD</td>
<td>High definition</td>
</tr>
<tr>
<td>LNA</td>
<td>Low-noise amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local oscillator</td>
</tr>
<tr>
<td>LOS</td>
<td>Line of sight</td>
</tr>
<tr>
<td>LTCC</td>
<td>Low temperature co-fired ceramics</td>
</tr>
<tr>
<td>MAC</td>
<td>Medium access control</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-insulator-metal</td>
</tr>
<tr>
<td>MSK</td>
<td>Minimum shift keying</td>
</tr>
<tr>
<td>MTT-S</td>
<td>Microwave theory and techniques society</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked loop</td>
</tr>
<tr>
<td>PRBS</td>
<td>Pseudorandom binary sequence</td>
</tr>
<tr>
<td>PM</td>
<td>Phase modulation</td>
</tr>
<tr>
<td>RBW</td>
<td>Relative bandwidth</td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square</td>
</tr>
<tr>
<td>RRC</td>
<td>Root-raised cosine</td>
</tr>
<tr>
<td>SiP</td>
<td>System in package</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to noise ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System on chip</td>
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<tr>
<td>QPSK</td>
<td>Quadrature phase-shift keying</td>
</tr>
<tr>
<td>USB</td>
<td>Universal serial bus</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra-wideband</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable gain amplifier</td>
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vol. 59, no. 9, pp. 3470–3473, September 2011.

List of Publications

Parts of this thesis have been published in peer-reviewed journals and conferences:

1. **Ulusoy, A. C.**; Schumacher, H. “Multi-Gbps analog synchronous QPSK demodulator with phase noise suppression” IEEE Transactions on Microwave Theory and Techniques - accepted


8. **Ulusoy, A. C.**; Liu, G.; Peter, M.; Felbecker, R.; Abdine, H.; Schumacher, H. “A BPSK/QPSK receiver architecture suitable for low-cost ultra-high rate 60 GHz wire-


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