

Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT $\Sigma\Delta$ Modulator

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Abstract—In this paper, a comparison between three different current readouts for micro-potentiostats is presented: resistive transimpedance amplifier (R-TIA), capacitive transimpedance amplifier (C-TIA), and current-mode continuous-time sigma-delta modulator (Current-CTSDM). The comparison is carried out on the signal transfer function, the required amplifier gain-bandwidth (GBW), its input referred noise current, required area and power, and dynamic range. Each approach and its limitations are separately discussed. The three systems have been simulated using VerilogA models and the results are compared. It is shown that each system comes with its own limitations, however current-mode CTSDM are more beneficial due to their intrinsic digitization.

I. INTRODUCTION

With the progress in integration of electrochemical impedance spectroscopy (EIS), cyclic voltammetry (CV), chronoamperometry (CA), or scanning ion-conductance microscopy (SICM), there is a continuous need for high-performance potentiostats, needing current readout circuits with high dynamic range and partially high temporal resolution. Such micropotentiostats consist of a signal generator, sample under test, a current recording system, and a subsequent processing unit, cf. Fig. 1. The potentiostats usually require very small detection limits for the input currents from pA to μ A within a frequency range from DC to few MHz, depending on the application scenario. State of art current readout circuits are realized as resistive feedback transimpedance amplifiers (R-TIA) [1], capacitive feedback transimpedance amplifiers (C-TIA) [2], and current-mode continuous-time (CT) sigma-delta modulators (Current-CTSDM) [3], [4]. E. g. in [5], an R-TIA has been presented, which utilizes a highly-modified pseudo-resistor as feedback element which achieves a high robustness versus temperature and process variations. R-TIAs are very common due to their simple architecture. However, inherent trade-offs such as transimpedance versus bandwidth make them not very suitable for high frequency applications.

A C-TIA, which utilizes a small capacitance as feedback element for high sensitivity, has been presented in [2]. The presented C-TIA achieves a very high frequency range. C-TIAs overcome the trade-offs of R-TIAs by utilizing two stages, i. e., integrator and differentiator. These advantages come along with disadvantages of increased complexity of the system as well as a bandpass signal transfer function.

Another approach is to use a current input CTSDM which has been applied in [3], [4]. CTSDMs are a popular implementation for voltage mode ADCs and can obviously be used for current sensing once the input resistor of the first integrator is removed. They come with the advantage of implicit digitiza-

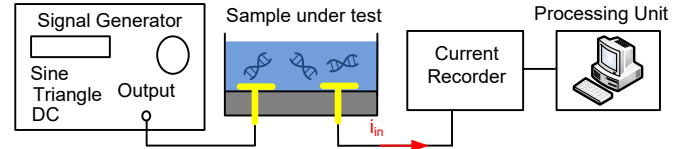


Fig. 1. Typical set-up of an biochemical experiment, such as EIS and SICM.

tion, but disadvantageously the concept of CTSDM relies on oversampling and noise-shaping. Thus, the operating speed is much higher than the required input bandwidth, the utilized opamps need to operate at this high frequency, and the high-frequency quantization noise from the feedback DAC might impact the sensitive input signal.

Consequently, these three architectures all come with advantages and disadvantages, but a thorough comparison study is not yet presented. This paper is organized as follows: The three different current sensing circuits are reviewed and analysed in the Sections II, III, and IV. An exemplary specification is implemented and simulated in Sections V, which are compared in Section VI, before the paper is concluded in Section VII.

II. RESISTIVE TRANSIMPEDANCE AMPLIFIER

The opamp-based R-TIA is the most common sensing circuit, cf. Fig. 2a. Ideally, the R-TIA consists of an opamp and a feedback resistance R_F , which defines the transimpedance (gain) of the system. However, due to the parasitic capacitance C_P at the input of the amplifier, a feedback capacitor C_F needs to be introduced to ensure the stability of the TIA. Assuming an opamp as single-pole system with DC gain $A_0 \gg 1$ and gain-bandwidth product $GBW \gg \frac{1}{2\pi R_F C_F}$, and assuming $C_F/C_P \ll 1$, the transfer function of the R-TIA becomes:

$$\frac{V_{out}}{I_{in}} = \frac{-R_F}{\frac{R_F C_P}{2\pi GBW} s^2 + R_F C_F s + 1}. \quad (1)$$

Since C_P introduces a second pole, it is efficient to design the transfer function with a second-order Butterworth low-pass characteristic [1]. C_F can be calculated using Eq. 1 to obtain a Butterworth low-pass characteristic with corner frequency f_{MAX} and quality factor $Q = \frac{1}{\sqrt{2}}$:

$$C_F \approx \sqrt{\frac{2}{2\pi R_F GBW}} \sqrt{C_P}. \quad (2)$$

Naturally, R-TIA has a DC-path from input to output, which means that the achievable lower corner frequency $f_{MIN} = 0$.

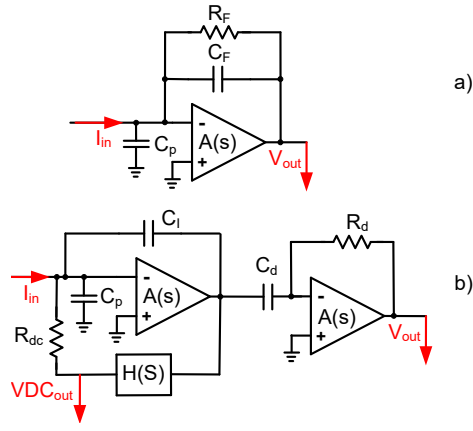


Fig. 2. Schematics of a) resistive-TIA and b) capacitive-TIA.

The upper corner frequency f_{MAX} is:

$$f_{MIN} = 0, f_{MAX} = \sqrt{\frac{GBW}{2\pi R_F C_P}}. \quad (3)$$

As it can be seen in Eq. 3, there is a trade-off between upper corner frequency f_{MAX} , TIA gain R_F , and required gain-bandwidth product GBW of the amplifier. f_{MAX} decreases when the transimpedance R_F is increased for constant GBW . Also, for constant f_{MAX} , the GBW needs to be increased if R_F is increased. Furthermore, GBW needs to be increased quadratically in order to linearly increase the operating frequency f_{MAX} for a constant transimpedance R_F . This shows the main limitation of R-TIAs: high gain and high speed are very costly to achieve, since the opamp speed needs quadratical increase.

For the R-TIA, the equivalent input noise PSD is:

$$S_{\Delta I_{n,eq}^2} = \frac{S_{\Delta V_{n,OA}^2}}{|R_F| |1/j\omega C_P| |1/j\omega C_F|^2} + \frac{4k_B T}{R_F} \left[\frac{A^2}{\text{Hz}} \right], \quad (4)$$

where $S_{\Delta V_{n,OA}^2}$ is the equivalent input noise PSD of the opamp, k_B the Boltzmann constant, and T the absolute temperature. The equivalent input noise can thus be reduced by increasing R_F . The implementation of large resistors not only consumes huge area, but also introduces parasitic capacitances which degrade the speed. Alternatively, large resistances can be implemented using pseudo-resistors in order to decrease area and parasitics, which are usually very non-linear. Even though, e.g. in [1] linearization could be achieved by the series-connection of multiple pseudo-resistors in a highly modified form, this came at the disadvantage of needing an SOI process to reduce the parasitic capacitances and thus the associated speed degradation, and still the implementation had limited linearity [5].

III. CAPACITIVE TRANSIMPEDANCE AMPLIFIER

Capacitive TIAs have been investigated to achieve current sensing at higher signal frequencies. A state of the art C-TIA is the integrator-differentiator structure [2], cf. Fig. 2b. It features an integrator as the first stage followed by a differentiator in order to have a flat overall gain within the desired signal bandwidth:

$$\frac{V_{out}}{I_{in}} = \frac{C_d}{C_I} R_d, \quad (5)$$

where C_I is the feedback capacitance of the integrator and C_d and R_d form the external circuitry of the differentiator. Thereby, this C-TIA provides more degrees of freedom to choose the overall gain against noise and speed.

Disadvantageously, the integrator suffers from saturation of the output voltage for low frequency and DC input signals. Therefore, an additional DC feedback path must be introduced to prevent saturation. In the DC feedback path, [2] introduced the filter $H(s)$ which operates at low frequencies as integrator, in order to keep the DC voltage at the output at zero, and as an attenuator within the signal band. The output of $H(s)$ generates the voltage over R_{DC} to sink the DC input or low frequency current and to provide a separate DC output. Therefore, the overall characteristic of the C-TIA becomes a bandpass, where the lower corner frequency is defined by the feedback capacitance C_I , the feedback resistor R_{DC} , and the attenuation γ of $H(s)$. The upper corner frequency f_{MAX} is described by the gain-bandwidth product of the amplifier that is decreased by the capacitive divider formed by parasitic input capacitance C_P and feedback capacitance C_I :

$$f_{MIN} = \frac{1}{2\pi R_{DC} C_I \gamma}, f_{MAX} = GBW \frac{C_I}{C_I + C_P}. \quad (6)$$

The trade-off between the achievable f_{MAX} and GBW is decreased to a proportional dependency, which makes it less costly to realize high-speed TIAs. However, due to the loading effect of C_d , the integrated amplifier needs to invest more power to achieve the required GBW cf. Fig. 2b. This will be discussed with an example in Sec. V.

If $C_I \ll C_d$ is assumed, the noise of the differentiator gets negligible as well as a high overall current gain is achieved, cf. Eq. 5. Then, the equivalent input noise PSD is described as:

$$S_{\Delta I_{n,eq}^2} = \frac{S_{\Delta V_{n,OA}^2}}{|R_{DC}| |1/j\omega C_P| |1/j\omega C_I|^2} + \frac{4k_B T}{R_{DC}} \left[\frac{A^2}{\text{Hz}} \right]. \quad (7)$$

Since R_{DC} has no influence on the overall gain, cf. Eq. 5, it can be increased independently to decrease the equivalent input noise. This also addresses the disadvantageous trade-off between noise and gain in R-TIAs. However, the value of R_{DC} is constrained to the required f_{MIN} , cf. Eq. 6, and the maximum DC input current, which needs to be compensated. Since R_{DC} is not part of the signal path, it can be usually realized as pseudo-resistor whose non-linearity would not influence the SNDR of the passband [2]. However, the design of [2] suffers from shot noise generated by the realization of R_{DC} with pseudo-resistors for large DC input currents.

One of the drawbacks of C-TIA is its frequency dependent dynamic range. The minimum detectable input current is defined by the integrated input referred noise in the signal band and it is not dependent on the input signal frequency. On the other hand, the maximum input current becomes limited at very low frequencies and DC by saturation of the output voltage of $H(s)$ as:

$$I_{MAX,DC} = V_{FS}/R_{DC}, \quad (8)$$

where V_{FS} is defined to be equal to the full scale output voltage (maximum output voltage). At the lower end of the signal band, after $H(s)$ corner frequency, the integrator output limits the achievable maximum input current due to its increasing

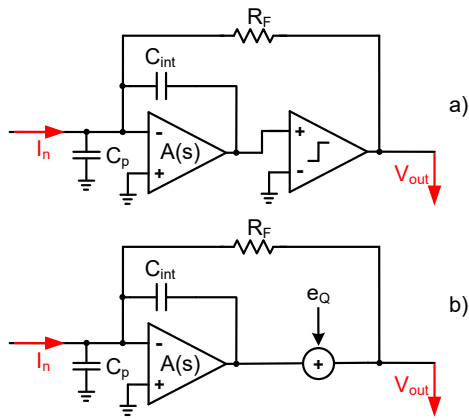


Fig. 3. Schematic of a) 1st order Current-CTSDM and b) with quantizer modeled as additive noise.

gain for decreasing frequency. Therefore, the maximum input current at f_{in} is limited to [2]:

$$I_{MAX,AC} = V_{FS} \times 2\pi f_{in} C_1. \quad (9)$$

This clearly shows the trade-off between the input signal frequency f_{in} and the maximum input current. Furthermore, for frequencies where the differentiator gain is greater than one, the maximum input current becomes limited by the output of the differentiator and can be calculated as:

$$I_{MAX,AC} = V_{FS} / \left(\frac{C_d}{C_1} R_d \right). \quad (10)$$

As it can be seen, the maximum input current is a function of input signal frequency and needs to be calculated separately. This leads to frequency dependent dynamic range.

IV. CURRENT-MODE CT $\Delta\Sigma$ MODULATOR

Most state of the art CTSDM are used to digitize voltages [6]. However, they can be easily adapted to a current digitization system by removing their input resistor. Fig. 3a depicts a 1st order current-mode CTSDM, which is used for simplicity in the following. By comparing the Current-CTSDM structure with a R-TIA (cf. Fig. 2a), only by introducing a comparator into the R-TIA feedback implicit digitization is achieved. The quantizer adds quantization noise e_Q , cf. Fig. 3b. However, e_Q can be designed and shaped properly in order to have negligible influence to the signal band of interest [6]. Disadvantageously, the high-frequency quantization noise requires high integrator dynamics and disturbs the virtual ground node, which is the current sensing input, making the first integrator in Current-CTSDM power hungry [3], [4].

In the signal band of interest, the signal transfer function (STF) of the Current-CTSDM with feedback resistor R_F cf. Fig. 3a can be designed as:

$$STF_{IB} = \frac{V_{out}}{I_{in}} = -R_F. \quad (11)$$

In order to calculate the frequency requirements of a Current-CTSDM, a single-pole operational amplifier with C_{int} as the integration capacitance is assumed. For an RC integrator to have an almost undisturbed transfer function, the opamp DC-gain $A(s) \gg 1$ and the $GBW \geq 10 \times \frac{1}{R_F C_{int}}$ must be guaranteed. In CTSDM, the value of $R_F C_{int}$ is related to the

sampling frequency F_S and the modulator scaling coefficient a_1 :

$$GBW \geq 10 \frac{1}{R_F C_{int}} = 10 a_1 F_S. \quad (12)$$

Regarding the unavoidable parasitic C_P at the input node, the GBW needs to be further increased yielding:

$$GBW \geq 10 a_1 F_S \frac{C_{int} + C_P}{C_{int}}. \quad (13)$$

According to [6], the required GBW can be reduced with significant loss in the inband-noise by compensating for finite GBW by loop filter scaling and phase compensation. Since the STF of a CTSDM features a low pass characteristic, the detectable frequency range spans from DC to f_{MAX} , which is the inband frequency of the CTSDM given by $F_S/2 \times OSR$ which results by reusing Eq.13:

$$f_{MIN} = 0, f_{MAX} = \frac{F_S}{2 OSR} \leq \frac{GBW}{20 a_1 OSR} \frac{C_{int}}{C_{int} + C_P}. \quad (14)$$

The total input referred (thermal) noise PSD of a Current-CTSDM can be derived by assuming that e_Q in the signal band is negligible and other stages do not contribute to the noise [6]:

$$S_{\Delta I_{n,eq}^2} = \frac{S_{\Delta V_{n,OA}^2}}{\left| R_F \| 1/j\omega C_P \| 1/j\omega C_{int} \right|^2 + \frac{4k_B T}{R_F}} \left[\frac{A^2}{\text{Hz}} \right]. \quad (15)$$

The feedback path of Current-CTSDM can be realized using resistors R_F or current sources (CS) since the CTSDM output is binary [6]. The realization with CS will make the implementation much more area efficient. However, the noise performance of CS is worse compared to a resistor. Alternatively, a pseudo-resistor as in [1] can be beneficially applied since for single-bit CTSDM linearity of the feedback elements are not important as single-bit DACs are inherently linear [6].

Dynamic range for CTSDM can not be analytically calculated since their stability is dependent on scaling and input signal level. Therefore, the maximum input amplitude must be found out through simulations [6].

V. SIMULATIONS

As a case study for the comparison of the 3 current sensing architectures, all circuits have been implemented and simulated using Verilog-A models to prove the reported equations and compare the requirements and results. The three systems have been specified to have a transimpedance gain of 20 M Ω , an input frequency range of 2 MHz, and a parasitic input capacitance of $C_P = 2$ pF. Tab. I shows the summary of the simulated values. The required GBW for the R-TIA with a gain of $R_F = 20$ M Ω , using Eq. 3, is approx. 1 GHz. As a consequence, with Eq. 2, C_F becomes 5.6 fF, which corresponds to the assumption $C_P \gg C_F$. Note that since the feedback capacitor has a very small absolute value, $C_L = 0.5$ pF as the dominant load from subsequent stages has been added to the output of the amplifier. This has been done for all three implementations.

The C-TIA features more degrees of freedom, since the number of design parameters are more. As the first step, the value of C_1 must be chosen. Big values of C_1 lead to

TABLE I. SPECIFICATIONS OF THE THREE SYSTEMS FOR DESIRED OVERALL GAIN AND SIGNAL BANDWIDTH.

$f_{\text{MAX}} = 2 \text{ MHz}, \text{Gain} = 20 \text{ M}\Omega, C_P = 2 \text{ pF}, V_{\text{FS}} = 1 \text{ V}$			
	R-TIA	C-TIA	Current-CTSDM
GBW	1 GHz $C_L = 0.5 \text{ pF}$	42 MHz $C_L = 20 \text{ pF}$	660 MHz $C_L = 0.5 \text{ pF}$
Maximum input @ $V_{\text{FS}} = 1 \text{ V}$	40 nA	0.25 nA @ 0.5 kHz 40 nA @ 0.5 MHz	25 nA
$I_{n,\text{rms}}$ (0.1 k – 2 MHz)	105 pA _{rms}	115 pA _{rms}	110 pA _{rms}

decreased influence of C_P , which means that the required GBW will be smaller, cf. Eq. 6. In contrast, small values of C_I yield higher gain and decreased input referred noise, cf. Eq. 7. Therefore, C_I was fixed to 100 fF to satisfy this trade-off. In order to obtain an overall gain of 20 M Ω and by satisfying the assumption of $C_d \gg C_I$ to decrease the influence of R_d in thermal noise, R_d and C_d are chosen to be 100 k Ω and 20 pF, respectively. To justify our choices, [2] utilized equal values in a circuit implementation. The required GBW is 42 MHz, cf. Eq. 6; however, due to the loading effect of $C_d = 20 \text{ pF}$, achieving this GBW becomes more challenging in terms of power. Comparatively, R-TIA needs a $GBW = 1 \text{ GHz}$ cf. in Tab. I with the dominant load of 0.5 pF (parasitic loading of subsequent stages), whereas C-TIA needs about $GBW = 42 \text{ MHz}$ with a dominant load of $C_d = 20 \text{ pF}$. Therefore, even though the C-TIA needs less GBW in respect to the R-TIA, due to the loading of C_d , it needs to invest more power (transconductance G_m) to achieve the required GBW . For the implementation of $H(s)$ to achieve $f_{\text{MIN}} = 0.1 \text{ kHz}$, it should be noted that it consists of a leaky integrator with very low corner frequency, which consumes a large area and needs an additional opamp, which are not included in the comparison. R_{DC} is chosen to be 20 M Ω in order to have the same transimpedance gain for low input frequencies.

The design of the Current-CTSDM was done using www.sigma-delta.de. A third-order chain of integrator feedback (CIFB) CTSDM with NRZ DAC has been chosen. To achieve enough SQNR, $OSR = 32$ is chosen, with which the inband frequency of 2 MHz leads to $F_S = 128 \text{ MHz}$. In order to reduce the required GBW , the CTSDM input scaling coefficient was lowered to $a_1 = 0.01$ to reduce the GBW requirement according to Eq. 12. Then, the required GBW (without the effect of C_P) becomes $a_1 \cdot F_S = 12.8 \text{ MHz}$. Extensive picking in the STF of CTSDM was avoided by constraining the STF to have a max. gain of 6 dB [7]. Using www.sigma-delta.de and these specifications, the optimized CTSDM (using ideal models for the 2nd and 3rd filter stage) achieves maximum SQNR of 75 dbFS. With $R_F = 20 \text{ M}\Omega$, $a_1 = 0.01$, $C_P = 2 \text{ pF}$, $F_S = 128 \text{ MHz}$, and using Eq. 13, $C_{\text{int}} = 39 \text{ fF}$, leading to a required GBW of $52 \times 12.8 \text{ MHz}$.

Assuming only thermal noise for resistors and amplifiers, three cases have been simulated using Pnoise analysis in Cadence. Fig. 4a shows the input referred noise PSDs of the three different systems. The input noise PSD of the amplifiers ($S_{\Delta V_{n,\text{OA}}^2}$) are defined in respect to their G_m , which explains the rise at high frequency spectrum behaviour of Fig. 4a, since at high frequencies (assuming $C_P \gg C_{\text{int}}$), the frequency dependent term $2\pi f C_P S_{\Delta V_{n,\text{OA}}^2}$ dominates the noise PSD, cf. Eq. 15. At low frequencies, the C-TIA shows increase in noise PSD, cf. Fig. 4a, which is due to its bandpass signal characteristic, cf. Fig. 4b. Therefore, the integrated noise bandwidth is from 0.1 kHz to 2 MHz.

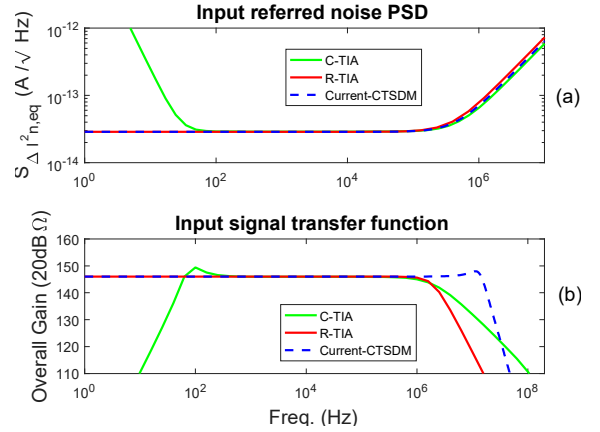


Fig. 4. a) Input referred noise PSD, b) input signal transfer function of R-TIA, C-TIA, and Current-CTSDM with Gain of 20 M Ω and $C_P = 2 \text{ pF}$.

VI. FURTHER DISCUSSION

For the same input bandwidth, transimpedance and parasitic input capacitance, as it was expected, the R-TIA has the highest needs in terms of GBW . On the other hand, the comparison shows that even though C-TIA needs almost a factor of 15 times less GBW than Current-CTSDM, it needs almost a factor of 1.5 more transconductance than the Current-CTSDM, due to capacitance C_d , to achieve the required bandwidth, which means Current-CTSDM will consume less power for the realization of the first integrator than the C-TIA.

Since the three architectures need same range of G_M for their amplifiers, respectively, it leads to a very similar values of $S_{\Delta V_{n,\text{OA}}^2}$ and therefore, the three architectures show comparable integrated input referred current noise cf. Tab. I and Fig. 4.a, which validates the reported equations. Disadvantageously, the C-TIA has a frequency dependent dynamic range, since the integrator in the forward path must be compensated for low frequency signals by feedback, which leads to a bandpass characteristic cf. Fig. 4.b. In terms of complexity of the system, the R-TIA is the simplest and most straight forward architecture since it consist of only one amplifier. On the contrary, the C-TIA is more complex to design due to more components such as integrator, differentiator, and DC feedback. Current-CTSDMs basically offer the best trade-off by offering similar degrees of freedom as the C-TIA, and obtaining approx. the same noise performance of the R-TIA. Additionally, Current-CTSDM implicitly digitizes input signal, which eliminates need of a ADC present in R-TIA and C-TIA.

VII. CONCLUSION

In this paper, we presented the Current-CTSDM and its efficiency in comparison to conventional transimpedance amplifiers using resistive and capacitive feedback. It has been proven by calculations and simulations that Current-CTSDM have the similar requirements and the same performance range as R-TIAs and C-TIAs, while their inherent trade-offs such as GBW requirements versus overall gain, bandpass signal transfer function are removed. Furthermore, Current-CTSDMs are an attractive choice since no additional ADC is required.

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