Evaluation of Single-Bit Sigma-Delta Modulator DAC for Electrical Impedance Spectroscopy

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Abstract—In this paper, single-bit sigma-delta modulator based digital-analog conversion (DAC) is evaluated as potential driver in multichannel electrical impedance spectroscopy (EIS) arrays. The sinusoidal excitation with typical frequency range of a few Hz to a few MHz is a challenging task, which only very few state of the art implementations are even able to realize on chip, where the corresponding DAC consumes major amounts of area and power. Sigma-delta modulators offer signal generation with 1-bit representation, which could be advantageously multiplexed, distributed, and used on switches to generate analog output; thus its use could potentially lower the area and power consumption. This paper investigates the use of a single-bit sigma-delta DAC as direct driver for EIS experiments. Performances and limitations of the proposed system are experimentally analyzed and discussed. EIS experiments of micro-electrodes could be successfully conducted in a range from 20 Hz to 1 MHz and matched with reference measurements to better than 95 % accuracy.

I. INTRODUCTION

Diseases such as pleura, bronchial tree, trachea, upper respiratory tract and respiratory muscles and nerves are some of the most often seen respiratory diseases with major health impact [1]. As a result, research is conducted on the reasons of respiratory diseases as well as finding ways to cure them at the alveolar tissue level. One research tool is thereby, the analysis of lung epithelium, in vitro, its integrity and response to drugs. This integrity can beyond other methods be tested with Electrical Impedance Spectroscopy (EIS), where the transepithelial resistance would be one of the measures [1] along with various other applications [2].

EIS is thereby, a very useful non-invasive tool to observe the properties of such cell layers and tissues; it is conducted by exciting the observed system with an alternating voltage and with a small amplitude (typically 10 mVpp) over a certain frequency range of interest, commonly from a few Hz up to even a few MHz, depending on the application [3], [1]. A measurement of the current flow, due to this excitation, gives the equivalent impedance and phase shift of the system under investigation. It has been shown in [1] that by using EIS abnormal cells would show different EIS response than normal cells. Similarly, epithelial cell layer integrity and other cell studies can be performed. Besides the non-invasiveness, EIS has further advantages such as being non-destructive, label free detection [1], but also being able to provide spatial resolutions, which is known as Electrical Impedance Tomography (EIT) [4]. However, to employ this, better spatial resolution by using multichannel EIS is required, which is why multichannel, integrated EIS systems have been researched before. In most state of the art (SoA) of multichannel implementations, the realization of the AC signal source - realized by a DAC - became a real bottleneck. Partially, integrated solutions still used external signal generators, which lacked full integrability of the system. Also, routing of the higher frequency sinusoidal signals (MHz region) and distributing it to various electrodes limited system performances due to parasitic effects. [3] integrated an 8-bit R2R DAC, but the reported power and area consumption showed that this could not be realized several times for high channel count EIS, but that it rather had a dominating impact on power and area of the overall IC. Another issue in SoA is that the single DACs need to be able to drive individual, but also a multitude of electrodes, which puts stringent requirements on the DAC. In [3], 16 channels were thus simultaneously excited. This consequently yields the lack of exciting different electrodes with different frequencies or phases, which limits the flexibility of the system.

In this paper, we investigate the usefulness of employing a Sigma-Delta Modulator (SDM) DAC as signal generator. This has been previously proposed in [5] for discrete realization, but especially its application on integrated circuits would be highly beneficial: its single-bit output carries the AC signal as well as shaped, high-frequency quantization noise. If the latter would not disturb the EIS, with a single-bit digital excitation a very area and power efficient DAC could be realized at every electrode, as indicated in Figure 1. SDM DACs consist of two parts: a digital modulator and an analog reconstruction filter. The modulator works with oversampling and quantization noise shaping. Thus, the output of the SDM has a very low bitwidth, which can be even truncated to single-bit. Figure 2 shows an exemplary output spectrum of a single-bit third-order SDM. The large out-of-band quantization noise must usually be filtered in the analog domain, in order to achieve high inband signal-to-noise ratio (SNR). This filtering can be implemented actively or passively. As an example, [5] implemented this filter with discrete passive elements.
Alternatively, this paper investigates to omit the lowpass filter, by feeding the single-bit SDM output directly into the electrode within an EIS experiment. The high-frequency quantization noise would pass the device under test (DUT), and be low-pass filtered in the current measurement circuit, e.g. by a transimpedance amplifier (TIA). For further enhancement of the EIS resolution, the digitized output of the measurement can be applied to lock-in detection, where - due to known input frequency - the integrated noise is limited to a small band around the input frequency [3].

Consequently, even though significant high frequency quantization noise is present at the digital output of SDM DAC and at the output of the electrode and TIA, the weak signal at the input frequency of interest can still be detected. This technique basically solves the mentioned problems of SoA, which is easy AC signal generation over a significant frequency band, easy signal routing within a multichannel system, easy DAC realization at each electrode and individual drivability at every electrode site: digital signals are easily multiplexed, less sensitive to coupling and noise, easily routed, and the single-bit SDM DAC can switch between two voltage levels, making the implementation effort minimal. The goal of the paper is to investigate this implementation as a non-integrated prototype by measuring SDM output as AC source in an EIS setup; thereby, allowing to analyze which influence the large, high-frequency out-of-band quantization noise has on the EIS experiment.

II. SYSTEM ARCHITECTURE

The overall EIS system mainly consists of three parts: AC signal generator, device under test as electrodes with e.g. biological samples, and a potentiostat (performing the current measurement). Figure 1 shows the architecture of the proposed EIS system. One global or several distributed digital SDM-DAC generates the AC excitation signals at a single or several frequencies with same or different phases. In order to avoid tonal behaviour, a higher order SDM is preferred, such that together with the sinusoidal excitation, only white noise and shaped quantization noise are generated. A single-bit digital output is globally multiplexed to a selection of local EIS electrodes, where the DUT is excited. The recording section includes e.g. a TIA to convert the generated current from the DUT into a voltage, which can then be either locally or globally digitized by an analog to digital converter (ADC) and further processed by e.g. digital lock-in detection.

To generate the excitation signal, in this work we have chosen a third order, single bit SDM built as a chain-of-integrators with feedback compensation (CIFB), which was designed and simulated in Matlab and then implemented in a National Instruments NI PXIe-5451. The output spectrum of this SDM-DAC with a sampling frequency of 20 MHz and a sinusoidal signal of 10 mV at 3.2 kHz is shown in Figure 2.a. Various TIAs have been presented in the literature for potentiostat realizations, e.g. [3]. For our first non-integrated investigations, we realized the TIA by using a low noise current pre-amplifier (Stanford Research SR570) with a gain of 10 kΩ, a bandwidth of 1 MHz, and an input referred current noise of 100 pA. The NI PXIe-5122 was then used to realize the ADC following the SR570. All data is then processed in Matlab to generate the EIS plots. A spectrum of a recorded output from an exemplary measurement including Au-electrode as DUT is shown Figure 2.b. Obviously, there is still shaped quantization noise visible at high frequencies, but overall the spectrum is reasonably flat and the excitation frequency is clearly visible. In order to compare the results of the proposed system with a reference measurement, a VersaSTAT 4 Potentiostat (Princeton Applied Research) is used. Figure 3 shows the complete setup being used in the following to investigate the SDM based excitation in EIS experiments.

![Figure 2](image2.png)

Fig. 2. a) Output spectrum of a 3rd SDM DAC with -40 d BFS input signal, b) Output spectrum of the measured voltage of TIA for shown input signal.

![Figure 3](image3.png)

Fig. 3. Complete setup of the proposed EIS system.

In order to test the proposed EIS system in an in-vitro environment with reproducible data, a commercial multielectrode array (MEA) using gold micro-electrodes from Multichannel Systems is used (MCS 24W700/100F-288). The MEAs consist of a 24 well plate, where each well plate contains twelve Au-electrodes on FR4 substrate with one internal Au-reference electrode in each well plate. Each electrode has a diameter of 100 µm and a pitch of 700 µm. To have similar conditions as with biological samples, Dulbecco’s Phosphate-Buffered Saline (DPBS) has been added to the electrode wells before EIS experiments.

As the intention of this work was to evaluate if the SDM excitation is feasible for EIS experiments, before setting the excitation parameters in the SDM, it should be investigated which charge density and charge per phase are allowed. The safe operation of macro-electrodes is usually approached by limiting the delivered charge per phase (Q) and charge density (D) at the electrode. This relation is described by the Shannon equation as [6]:

$$\log(D) = k - \log(Q)$$

(1)

where k would have typically reported values between 1.5 to 2. The charge per phase (Q) of the proposed single-bit SDM excitation can be calculated as:

$$Q = \frac{V_p}{f_sR_s}$$

or

$$Q = \frac{V_n}{f_sR_s} \left[ \frac{Q}{\text{ph}} \right]$$

(2)
where \( f_s \) is the sampling frequency of the SDM, \( V_p \) and \( V_n \) are the positive and negative output of the DSM DAC in Figure 1, and \( R_s \) is the solution resistance of the electrode and the biological sample in the high frequency domain. For the used MEA and DPBS, \( R_s \) was estimated and measured to be between 5 kΩ to 10 kΩ. Because of the very small input sinusoidal signal (-40 dBFS), when AC signal has 10 mV amplitude with a full scale (FS) voltage of ±1 V, it can be assumed that the output of SDM-DAC toggles very frequently, and we assume for simplicity almost every clock cycle (1/\( f_s \)). The resulting charge density (\( D \)) of the electrodes can then be calculated as:

\[
D = \frac{Q}{\text{Area}} \left[ \frac{Q}{\text{cm}^2} \right] 
\]

where \( Q \) is the charge per phase and \( \text{Area} \) is the geometric surface area of the electrodes, which is \( 3.14 \times 10^{-4} \text{cm}^2 \) large in the chosen MEAs.

It must be noted, that Shannon criteria is explicitly only valid for macro electrodes and it does not take into consideration other factors such as pulse frequency, duty cycle, and micro-electrode size [6]. This means that safe limits in the proposed system need to be carefully investigated by measurements [6].

### III. Measurement Results and Discussion

To prove the functionality of the proposed system, a reference DUT has been measured, first, by using a lumped electrode model i.e. a RC high-pass filter with resistor and capacitor of 10 kΩ and 1 nF, respectively. Figure 4 shows the measurement results of the SDM excitation vs. the results measured with the lab equipment using the VersaSTAT 4. The excitation using the SDM single-bit output and a \( V_{p,n} = ±1 \text{ V} \) matches very closely with the reference measurements; only at high frequencies the mismatch grows because of the 1 MHz bandwidth limitation of the used TIA. This proves the basic functionality of the system. The minimum measured frequency (20 Hz) was limited due to the available buffer size of the signal generator and the correspondingly limited number of SDM output samples.

Shannon’s charge per phase and charge density limits, which is also proposed in [6]. Thus, the sampling frequency (\( f_s \)) was chosen to be \( 20 \text{ MHz} \) and the single-bit SDM DAC output levels were \( V_{p,n} = ±1 \text{ V} \), respectively. These values lead to a charge per phase of \( Q=10 \text{ pC/cm}^2 \) (Equation 2) and a charge density of \( D=32 \text{ nC/cm}^2 \) (Equation 3).

Then, the SDM based EIS measurement was continuously run for 6 days on the same electrodes in order to investigate what effect the high-frequency quantization noise might have to the measurement on short and long-term. In order to track the electrode condition, EIS of the electrode was also performed by the reference system using VersaSTAT 4 at regular time intervals. Figure 5 shows the results of this six day long measurement. Firstly, it should be mentioned that the SDM based EIS and the reference EIS matches very closely, which is shown in Figure 5: the SDM measurement, which is continuously running during the whole experiment and the reference measurement after one day matches very reasonably (black starred line and black line with circles). Also it is seen that during the first hours, a typical “burning in” of the fresh electrode is seen with slight variation in the electrode impedance, both in the capacitive and the resistive behaviour. But after several hours and days, a very significant change in the electrode impedance is seen, which lets us assume continuous electrode damaging. For further investigation, the electrode chamber was imaged after the experiment, which is shown in Figure 6. It was observed that during the stimulation, deposited gold of the electrode was removed, which corresponds to the increase in the capacitive impedance. Since the electrodes are mounted on FR4 substrate, after gold was dissolved, copper surface was exposed to the chamber. As it is
shown in [7], copper reacts with water at around 150 mV and forms copper hydroxide \((Cu(OH)_2)\), which has a blue color, which is visible in Figure 6.

Thus, the SDM excitation of the electrode gives reasonably good EIS measurement, but apparently the chosen excitation destroys the electrode. Practically, two factors could be changed in the SDM excitation in order to prevent this: the sampling frequency \((f_s)\) or the SDM DAC output binary voltage levels \((V_{p,n})\) in Figure 1, which both would reduce the charge per phase and charge density to the electrode during EIS. In order investigate this, a fresh MEA was chosen and excited by a much higher sampling frequency \((f_s=100 MHz)\), while the DAC output levels were still chosen as \(V_{p,n}=\pm 1 V\), respectively. The chosen variables lead to charge per phase of \(Q=2 \ pm Q/Ph\) (Equation 2) and charge per density of \(D=6.4 \ nQ/cm^2\) (Equation 3). The intention of this speed increase was also to investigate if it might be possible to increase the excitation by quantization noise to a frequency which would not allow electrochemical reactions to happen. With this setup, the same experiment was conducted with several days of continuous EIS to the micro-electrodes in a MEA using again DPBS buffer. However, as it is shown in Figure 7, after three days, the same phenomena occurred as before. In this setup, the electrode change was even more severe and consequently, the increased sampling frequency even led to a faster destruction of the electrode.

As a last setup, the sampling frequency was again set to 20 MHz and the binary SDM DAC output voltage levels reduced to \(V_{p,n}=\pm 100 mV\), respectively. These voltage levels are, even when being applied as DC voltage, too small to cause irreversible reactions at the electrodes. These chosen values would lead to charge per phase \((Q)\) and charge density \((D)\) of \(1 \ pm Q/Ph\) and \(3.2 \ nQ/cm^2\), respectively. Figure 8 shows the results of the measurements done with this setup over six days continuously performing EIS with the SDM setup and reference EIS using VersaStat 4 in regular time intervals. As it can be seen, the electrode shows a very stable impedance during the six days of measurements and the shown measurement using SDM based EIS matches the measurement using the VersaStat 4 very well. Consequently, this setup is very feasible for multichannel EIS measurements using the proposed single-bit SDM DAC as AC excitation source.

**Fig. 7.** EIS of the electrode measured with VersaStat 4, within 3 days of SDM based EIS experiment with \(f_s=100 MHz\) and \(V_{p,n}=\pm 100 mV\).

**Fig. 8.** EIS of the electrode measured with VersaStat 4, within 6 days of SDM based EIS experiment with \(f_s=20 MHz\) and \(V_{p,n}=\pm 10 mV\).

**IV. CONCLUSION**

In this paper we propose to use a single-bit sigma-delta DAC without analog output filter as AC excitation source in multichannel EIS measurements. Due to its binary digital output, it offers very advantageous features such as digital routing, noise immunity, multiplexing as well as very small area and power at the electrode site, which makes its implementation on integrated circuits for electrochemical measurements very promising. It was shown that in order to have a safe continuous operation, the binary output levels of SDM DAC should be kept small in order to prevent electrode damage. Using a prototyped setup on Au micro-electrodes, very good matching of the SDM DAC based EIS was found with a reference measurement using standard EIS lab equipment. The proposed EIS signal generator promises to allow area and power efficient implementation for multichannel chip integration.

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**REFERENCES**


