Analog Synchronous Receiver for Multi-Gigabit Wireless Communications

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***Abstract*— In this work, we present a synchronous receiver architecture utilizing analog carrier recovery, to be used in multi-gigabit wireless communication systems. Carrier phase and frequency synchronization in the analog receiver drastically reduces cost and simplifies the system design by enabling the usage of 1-bit resolution analog to digital converters (ADC). The focus of this work is mainly the analog carrier recovery, which forms the basis of the proposed receiver. Simulation and experimental results are presented, demonstrating the applicability of the presented analog receiver concept for multi-gigabit communication links.**

***Index Terms*— Bandpass filters, demodulation, millimeter wave communication, MMIC receivers, phase shift keying, synchronous detection.**

I. Introduction

The license-free allocated band at 60 GHz enables wireless communications at ultra-high data rates for commercial applications. Most application scenarios target mobile, hand-held devices which makes power consumption and cost an important criterion for the system design. In this respect, ADCs tend to become the bottleneck of these systems, as their cost and power consumption is typically very high [1]. The ADC bottleneck is addressed in [2], where it is suggested to utilize lower precision ADCs in order to reduce cost and power consumption. However, this approach limits the application scenario to AWGN-like channels ,i.e. line-of-sight (LOS), and carrier phase and frequency synchronization still remains a big challenge.

In this work, we present a multi-gigabit receiver architecture which performs carrier phase and frequency synchronization in the analog domain. Similar to the proposed conditions in [2], the receiver targets ultra-high rate (UHR) wireless data transmission at 60 GHz for short-range LOS channel conditions. The proposed receiver is very promising for application scenarios under these conditions (e.g. data upload/download kiosk scenario) as it replaces high-precision, high-speed ADCs with simple 1-bit sample and hold circuits, eliminating the ADC bottleneck from the system design perspective.

II. Proposed Analog Synchronous Receiver

The schematic of the proposed analog synchronous receiver is presented in Fig. 1.

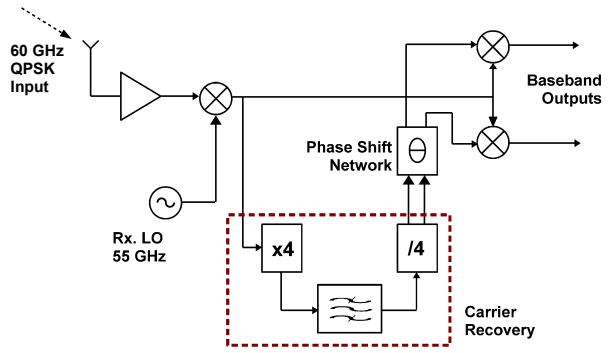

Fig. 1. Schematic of the proposed analog synchronous receiver

The proposed receiver is of super-heterodyne type with an intermediate frequency (IF) of 5 GHz. The synchronization is performed at the IF, and it is based on single-carrier (SC) QPSK modulation and carrier recovery by frequency quadrupling [3]. Frequency quadrupling generates a strong carrier component at four times the IF, which is bandpass filtered and divided by four to be used in demodulation. Since the carrier component is extracted from the modulated signal itself, no additional phase and frequency synchronization is required. However, a constant deterministic phase correction needs to be done, in order to compensate for the phase shift caused by the carrier recovery branch.

Within the carrier recovery, the bandpass filter is a key component and has a strong influence on the stability of the recovered carrier. Therefore, to estimate the expected performance and the feasibility of an analog implementation, system simulations based on behavioral circuit models are performed using different bandpass filters. The simulations are performed for 10^6 symbols at a symbol rate of 3.5 GS/s. The channel is an AWGN-channel and the

modulation format is differentially-encoded QPSK (DE-QPSK). It should be noted that differential encoding is required to resolve phase ambiguity, which is an inherent problem of carrier tracking loops [4], while the detection method remains coherent.

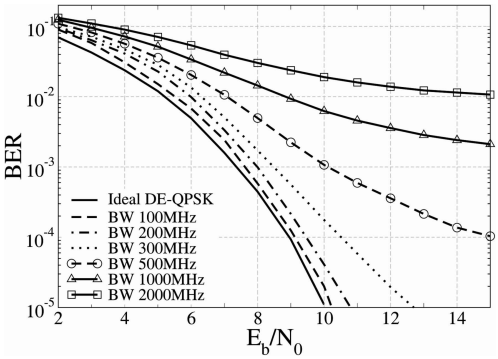

Fig. 2. Simulated BER performance of the proposed receiver for different bandpass filters

In Fig. 2, the simulated bit-error-rate (BER) curves of the proposed receiver are plotted against SNR-per-bit for different bandpass filters. They are all ideal 3^{rd} order Chebyshev bandpass filters, centered at 20 GHz. As can be seen in Fig. 2, BER floors are observed for larger bandwidth values of several GHz, which indicates that the recovered carrier jitters. On the other hand, for lower bandwidth values of around 100 MHz to 200 MHz, close to ideal performance is observed, indicating a stable recovered carrier. Obviously, strong jitter of the recovered carrier causes a large SNR penalty which may not be tolerable for most systems. Therefore, integrating a sharp bandpass filter into the proposed receiver is a critical issue. While on-chip realization of such sharp filters is very challenging, the required bandwidth can be achieved off-chip, for example by using planar technologies, as will be shown in the following. This kind of filter can be included in the package of the receiver IC (System-in-Package (SiP)).

III. Experimental Results

In this section, the core function of the proposed receiver, namely the carrier recovery is experimentally demonstrated for multi-GBit/s modulated signals. The carrier recovery branch that is shown in the dashed box in Fig. 1 is realized in a configuration allowing on-wafer characterization with external filters. This setup is shown in Fig. 3.

In the displayed test structure the frequency quadrupler and the divider ICs are arranged in a way that the output of the quadrupler can be connected to the input of the divider through an off-chip bandpass filter. The ICs are manufactured in Telefunken SiGe2RF HBT technology. The quadrupler consists of two Gilbert cell mixers modified as

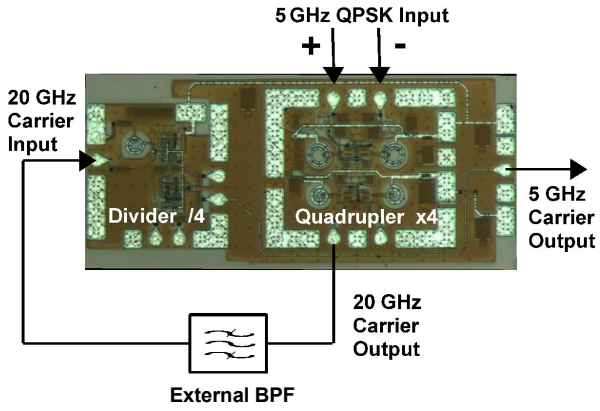

Fig. 3. Carrier recovery test IC for on-wafer measurements

squaring devices. The output of the first squaring device is matched to the input of the second one at 10 GHz, and the output of the second squaring device is matched to a 100 Ω differential load impedance at 20 GHz. Thereby a tuned characteristic is achieved for an input frequency of 5 GHz and an output frequency of 20 GHz. Detailed description of the frequency quadrupler circuit can be found in [5]. The frequency divider IC is a static divide-by-four frequency divider in master-slave flip-flop topology. The input of the frequency divider is matched to a single-ended 50 Ω impedance at 20 GHz in order to maintain proper operation of the external filter. In the test setup in Fig. 3, both ICs are operated from a single 2.5 V DC voltage supply, consuming 140 mW.

A. Bandpass Filter

As previously mentioned, a BPF realized in a planar technology would enable the SiP integration of the proposed receiver. Therefore, a compact, very narrow bandwidth planar BPF with tolerable insertion loss is investigated to be used within the carrier recovery. In the literature, several filters are reported operating in the 2 GHz range with the specified requirements [6]. These filters utilize transmission zeros above and below center frequency, which enables the realization of very sharp BPFs with reduced size and lower loss. This approach is chosen for the design of the BPF. The transmission zeros are generated via asymmetric tapping of the filter resonators. The substrate material is R03003 with an ϵ_r of 3, and a substrate thickness of 128 μm. Layout and photograph of the manufactured BPF are displayed in Fig. 4. The filter core is very compact and occupies an area of 2.2 x 2.8 mm^2.

The measured S-parameters of the realized filter can be seen in Fig. 5. The center frequency of the BPF is 20 GHz, with a 3 dB bandwidth of 450 MHz (2.2% relative). The filter is well matched at 20 GHz, with a measured return loss above 20 dB. The measured insertion

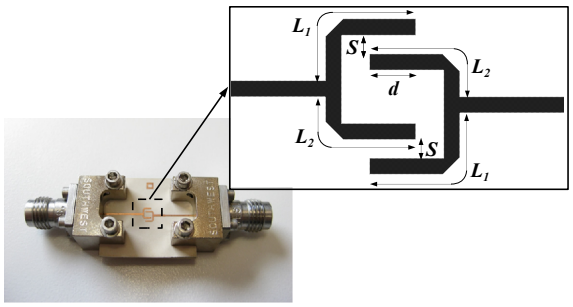

Fig. 4. Layout and photograph of the realized BPF. L_1 = 2.64 mm, L_2 = 2.24 mm, S = 0.38 mm, d = 1.1 mm, Linewidth = 0.35 mm

loss is 5.2 dB, whereas by a through line measurement, 1.6 dB of loss is estimated for the connectors. While the measured insertion loss is relatively high, in consideration of the the narrow bandwidth, and the simple, compact structure, the presented BPF performs reasonably well, and is suited for the application in question.

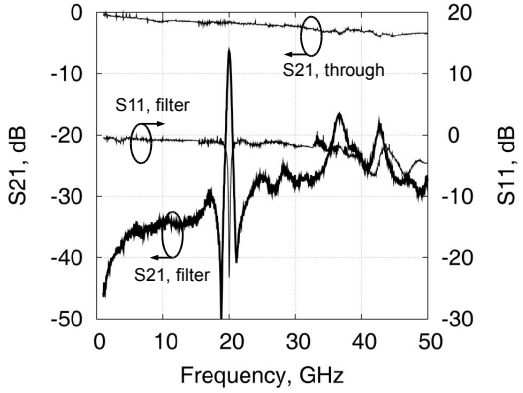

Fig. 5. Measured S-parameters of the realized BPF

B. UHR BPSK Modulator

For proper testing of the carrier recovery, a multi-GBit/s QPSK input signal is required. Due to the lack of such high data rate signal generators, a custom BPSK modulator is designed. BPSK modulation is preferred because it simplifies the design of the custom modulator, and BPSK modulated test signals can serve as a proof of concept for the QPSK carrier recovery.

The schematic of the designed modulator is displayed in Fig. 6. The core of the modulator is a Gilbert cell mixer, which performs the modulation by mixing the data pattern with the carrier. The carrier signal is applied to the lower-pair transistors, while the data signal is applied to a limiting stage which is connected to the upper-quad transistors. The limiting stage guarantees the switching operation of the upper quad transistors, keeping the Gilbert cell in the saturated mixing regime. For this design, large emitter degeneration resistors are used to provide high linearity and stability.

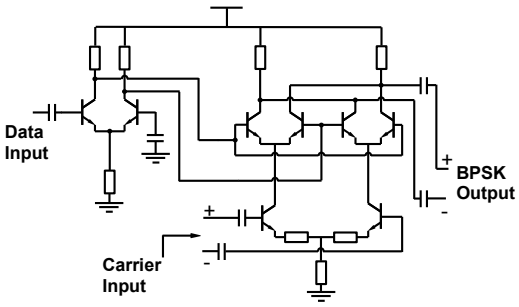

Fig. 6. Schematic of the UHR BPSK modulator

The modulator circuit is realized in IHP SG25H3 technology. The modulator IC is mounted on a prototype test package, which can be seen in Fig. 7. The carrier input and the BPSK output ports are differential, while the data input is applied single-ended. The packaged modulator has a measured 1 dB output compression point of 0 dBm, and a measured output bandwidth exceeding 10 GHz. Therefore, it can generate high quality BPSK modulated signals to be used in the carrier recovery experiments.

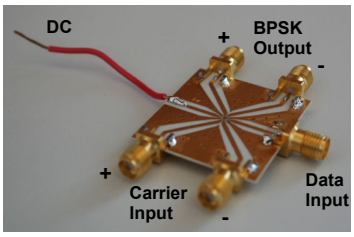

Fig. 7. Photograph of the prototype test package

C. Carrier Recovery Experiments

Carrier recovery experiments are performed by on-wafer measurements using the carrier recovery test IC, the realized BPF, and the custom BPSK modulator. For the BPSK modulation, a carrier signal of 5 GHz and a pseudorandom bit sequence with a 3.5 Gbit/s rate is supplied. In Fig. 8, the measured spectrums after each step of the carrier recovery are displayed. It can be seen that, the frequency quadrupling cancels the BPSK modulation, and a strong carrier component is generated at 20 GHz, together with a rich spectrum mostly due to envelope fluctuations. It is clear that the resulting signal can not be divided by the static frequency dividers, unless the spurious components are filtered out. The bandpass filtering removes most of the unwanted spectrum, except for some remaining spurs with relatively low power close to the carrier component. After the frequency division, a very pure spectrum is measured at 5 GHz using smaller spans (shown in the inset in Fig. 8 for a 100 MHz span), while for larger measurement

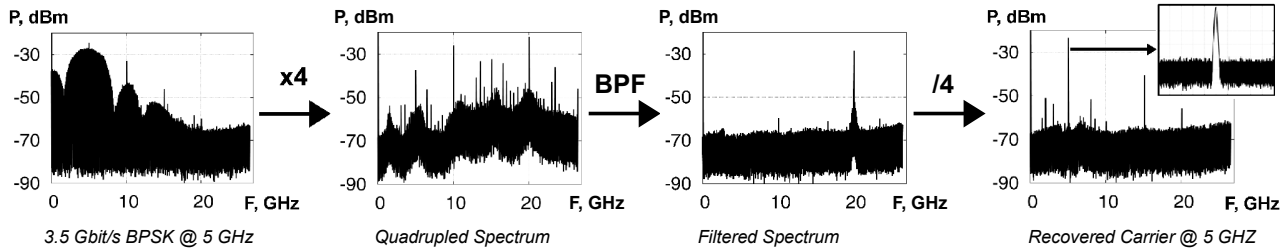

Fig. 8. The measured spectrums after each step of the carrier recovery. (from left to right : BPSK input, quadrupled BPSK spectrum, quadrupled BPSK spectrum after bandpass filtering, recovered carrier)

spans undesired components were detected at a distance of 2-3 GHz from the carrier signal. These components are mostly associated with data pattern dependent effects, and their power is measured to be around 30 dB below the desired carrier signal.

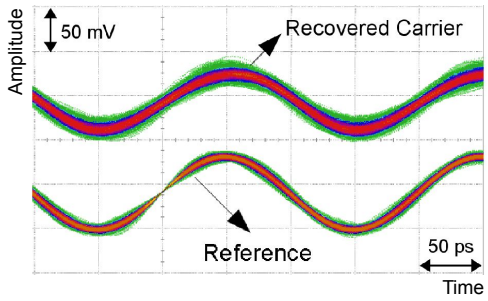

Fig. 9. Real-time measurement of the recovered carrier

Real-time measurements of the recovered carrier are performed at a sampling rate of 40 GS/s, in order to observe any possible unexpected behavior that could not be detected during the spectrum measurements. In Fig. 9, the recovered carrier is displayed in color grading together with a 5 GHz reference signal supplied from a separate signal generator, which is also used to trigger the real-time oscilloscope. The first observation is that a stable carrier is recovered without any phase jumps, that can be used for the demodulation. Furthermore, by changing the phase/frequency of the BPSK modulated carrier and by observing the same change at the recovered carrier, it was determined that the recovered carrier is phase/frequency synchronous with the BPSK signal. On the other hand, an obvious broadening of the recovered carrier in comparison to the reference signal can be determined in Fig. 9, indicating that the recovered carrier jitters. Nevertheless, this is in agreement with the system simulation results shown in Fig. 2, as a BER floor is still to be expected for a bandpass filter bandwidth of 450 MHz. The recovered carrier quality can be further improved by simply using sharper BPFs. Using the presented BPF topology, a 3 dB bandwidth down to 250 MHz can be achieved with the same substrate material, which would already drastically improve the recovered carrier performance.

IV. Conclusion

In this work, we presented an analog synchronous receiver architecture which is promising for short-range, LOS, multi-gigabit communication systems at 60 GHz, as it eliminates the need for high-speed, high-precision ADCs. System simulations of the receiver were presented, showing that there is a strict requirement for the BPF within the carrier recovery, and it was shown that with sufficiently sharp BPFs, the performance of the proposed receiver was close to ideal. Within the work, a custom BPF was presented, realized in a standard PCB manufacturing process that could be integrated in the receiver package. Carrier recovery, being the basis of the presented synchronous receiver, was successfully demonstrated for multi-gigabit BPSK modulated signals, experimentally showing that the presented receiver concept is applicable to low-cost, low-power, UHR wireless communication systems.

Acknowledgment

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