A PLL with Ultra Low Phase Noise for Millimeter Wave Applications

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Abstract—An ultra low noise phase locked loop (PLL) for millimeter wave applications is presented. The complete design includes a mixer type phase detector, a divide-by-32 frequency divider, a VCO and an off-chip active low pass filter. A method for the phase noise optimization of the PLL is described. The chip was designed using a 0.8 µm SiGe HBT technology. The frequency can be tuned from 29.9 GHz to 33.1 GHz. The output phase noise is around -112 dBc/Hz at 1 MHz offset.

I. INTRODUCTION

In wireless communication systems, when the operating frequency increases up to the millimeter wave range, the noise performance becomes more and more a critical factor that limits the overall performance of the systems. The spectrum purity of the local oscillator can directly influence the noise level of the transceiver. For example, in Synthetic Aperture Radar (SAR) applications, the phase noise will consequently degrade the SAR imaging [1]. Therefore, frequency synthesis of local oscillator signals requires a well behaved PLL with low phase noise.

Phase noise, spur level and lock time are 3 main parameters in PLLs designs, which all highly depend on the loop bandwidth \( \omega_n \). For the phase noise at offset frequencies lower than \( \omega_n \), the noise of the phase detector, the low pass loop filter and the divider dominates the overall phase noise, while for the noise at offset frequencies higher than \( \omega_n \), the phase noise of the VCO dominates the overall phase noise. As a rule of thumb, the loop bandwidth is in the range of 0.1 to 0.01 of the comparison frequency [2]. The lock time is inversely proportional to the loop bandwidth. Therefore, a higher comparison frequency is required to achieve fast locking. A more conventional PLL topology for frequency synthesis in modern communication systems is using a 3-state phase frequency detector (PFD) for phase error detection [3][4][5]. However, this type of phase detector has certain limitations in terms of noise performance and operating speed. The low frequency noise, here especially the 1/f noise, around the DC component will influence the overall phase noise performance. When the comparison frequency increases, the noise of the PFD becomes critical for the phase noise of the PLL at the offset frequencies lower than the loop bandwidth. In this work, a mixer type phase detector was chosen to achieve better noise performance.

II. CIRCUIT TOPOLOGY

A 3rd order linear type PLL was designed in this work as shown in Fig. 1, which included a mixer type phase detector, a divide-by-32 frequency divider, a VCO and an active low pass filter. The phase detector, divider, and VCO were integrated on chip; the loop filter was designed off chip due to the technology limitation to achieve sufficient output voltage swing for tuning the VCO frequency. The complete circuit was designed in differential structures using a 0.8 µm SiGe HBT technology. The SIC-npn transistor (with selectively implanted collector) improves the \( f_T \) from 50 GHz (for non-SIC npn transistor) to 80 GHz, at the price of a lowered collector-emitter breakdown voltage \( (BV_{CEO}) \) of 2.4 V (4.3 V for non-SIC npn transistor).

![Fig. 1. Block diagram of the 3rd order linear PLL](image)

A. Phase detector

Instead of the 3-state PFD, a mixer type phase detector was used for this design as its noise is relatively lower and quasi independent on the comparison frequency. However, it has a very poor phase detecting range, which is limited to 180°. For practical applications in wide locking range PLLs, a phase frequency detector can be used as assistant to enlarge the phase detecting range in the phase locking process [6].

Fig. 2 shows the topology of the mixer type phase detector, which combines a Gilbert mixer core and an output buffer. The low frequency noise, here especially the 1/f noise, around the DC component will influence the overall phase noise performance. Since the 1/f noise in the transconductance will be up converted to the high comparison frequency, the low frequency noise at the phase detector output will mainly...
depend on the mixer switching pairs [7]. 1/f noise in HBT is proportional to the current density of the collector [8]. However, a too low collector current density will limit the speed of the transistors, which will degrade the phase detecting range. Trade-off was made between the noise performance and the phase detecting range. Two capacitors were added in parallel with the load resistors to attenuate the up converted components at the detector output.

B. Frequency dividers

Two types of frequency dividers are suitable for millimeter wave and microwave signals dividing: dynamic frequency divider and static frequency divider. Dynamic frequency dividers are well known for their high operating frequency, while static frequency dividers have relatively large input dynamic range and better output signal waveforms. Here, a divide-by-32 divider was designed using 5 stages. The first two stages were dynamic dividers with additional transimpedance amplifiers, and the remaining 3 stages were static frequency dividers. More details were discussed in [9].

C. VCO

A differential negative resistance VCO was used as shown in Fig. 3. The VCO is a modified design from the one in [10] with smaller tuning range. Diode varactors were used for frequency tuning. The inductors were realized using Thin Film Microstrip Lines (TFMSL). Compared with the spiral inductors, the inductance of microstrip lines is easier to adjust. The TFMSLs were simulated using EM simulation tools (Momentum and Sonnet). Capacitive degeneration was used to generate a negative resistance looking into the base node, and the base inductor was used to complete the resonance circuits. A common-base stage was cascaded to the VCO core as an output buffer to increase the output power and isolate the VCO core from the load. The VCO has two differential output branches, which can feed the mixer and the frequency divider respectively.

D. Low pass loop filter

An active PI low pass filter was designed off chip which is shown in Fig. 4. The operational amplifier is a 350 MHz low noise high speed amplifier TSH4021 from Texas Instruments. As compared with the passive and other types of active filters in the PLLs design, the advantage of this type of loop filter is that it has an infinite hold-in range as long as the output voltage swing of the op-amps is sufficient [11].

III. PHASE NOISE SIMULATION

The overall phase noise of this PLL can be estimated from [2], as shown in Eq. 1:

\[
P_{NPLL} = (P_{NRef} + P_{NPD} \cdot \frac{1}{K_\phi} + P_{NFlt} \cdot \frac{1}{K_\phi Z(s)} + P_{NDiv}) \cdot \frac{G}{1 + GH} + P_{Nvco} \cdot \frac{1}{1 + GH}
\]

where \( P_{NRef}, P_{NDiv} \) and \( P_{NVCO} \) are the phase noise of the reference signal, frequency divider and VCO; \( P_{NPD} \) and \( P_{NFlt} \) are the intrinsic voltage noise of the phase detector and the low pass filter; \( G \) is the loop gain and \( H \) represents the feedback factor as in Eq. 2 and Eq. 3:

\[
G = K_\phi Z(s) \frac{K_{VCO}}{s} \quad (2)
\]

\[
H = \frac{1}{N} \quad (3)
\]

where \( K_\phi \) is the phase error gain of the phase detector, \( K_{VCO} \) is the gain of the VCO, and \( Z(s) \) is the transfer function of the loop filter and \( N \) is the divider ratio of the frequency divider. The simulated phase error gain of the phase detector \( K_\phi \) is
1 V/rad; the gain of the VCO $K_{VCO}$ is 1.2 GHz/V at 32 GHz center frequency.

To simulate the overall phase noise, the noise parameter of each block of the PLL should be known. The noise performances of the phase detector and frequency divider were achieved from the simulation results, due to measurement difficulties; the phase noise of the VCO was assessed directly from the measurement results of the free running VCO; the low frequency noise of the active filter was modeled following the data sheet of the noise performance of the operational amplifier; and the phase noise of the 1 GHz reference was taken from the data sheet of a SAW crystal oscillator CCSO- 914X3-1000 from CRystek. Fig. 5(a) shows the noise performance of each individual block of the PLL.

The loop bandwidth needs to be designed properly to achieve good phase noise performance, the following method can be simply used: First, assume the loop bandwidth is infinite large, which means $GH >> 1$, the overall phase noise is contributed by the other blocks of the PLL but the VCO; as for this design, the phase noise of the PLL will be the phase noise of the free running VCO. Now, the optimum loop bandwidth will be the offset frequency where the VCO has the phase noise of -120 dBc/Hz, which is around 20 MHz. However, the reference spur level is also dependent on the loop bandwidth; a high loop bandwidth implies a high spur level. The simulated spur attenuation value at 2 GHz offset for the 20 MHz loop bandwidth is around 130 dB. Therefore, the spur noise can be neglected in this design.

Fig. 5(b) shows the noise contribution of each block to the overall output noise: for low offset frequencies up to around 300 KHz inside the loop bandwidth, the reference dominated the output noise; for medium offset frequencies from around 300 KHz to 15 MHz inside the loop bandwidth, the noise was dominated by the divider and the phase detector; and the VCO dominates the phase noise at offset frequencies outside the loop bandwidth.

IV. LAYOUT AND MEASUREMENT

The layout of the phase detector, frequency divider and VCO is shown in Fig. 6(a), which has chip area of 1.2 mm$^2$. Transmission lines were folded to save chip area. The chip size and shape were not optimized for this evaluation version.

The off-chip active loop filter was mounted on a PCB as shown in Fig. 6(b). The useful frequency range of the active low pass filter has an upper limit of approximate tens of MHz; widths of the signal lines on board were optimized to reduce the parasitic effect as much as possible.

On wafer measurement was done using an Agilent 8565 EC spectrum analyzer to measure the output spectrum of the PLL. The reference signal generator was an Agilent 8254A. While sweeping the reference signal from 934 MHz to 1.03 GHz, the PLL maintains the locked state, resulting in the output...
frequency between 29.9 GHz and 33.1 GHz, which covers the complete tuning range of the free running VCO. The differential output power of the PLL at 32 GHz is around 0.3 dBm by taking into account of the cable and probe losses. The output spectrum at 32 GHz is shown in Fig. 7 with a span of 100 MHz. The bandwidth of the PLL is around 15 MHz.

The phase noise was also measured using the Agilent 8565 EC, as shown in Fig. 8, with the offset frequency varying from 1 KHz to 100 MHz at a center frequency of 32 GHz. The phase noise at 1 MHz offset is -112 dBc/Hz, which is 8 dB higher than the simulation result. This is mainly caused by the poor noise performance of the signal generator. The power consumption of the chip is around 628 mW at 4 V supply, and 56 mW at 8 V supply for the active filter. The measured performance is summarized in Table I and compared with some prior published works.

![Image](image_url)

**Fig. 7.** Spectrum of the PLL output in the lock state with a span of 100 MHz

**Fig. 8.** Measured phase noise of the PLL output at 32 GHz center frequency

| TABLE I |
|------------------|---|---|---|---|
| **MEASURED PERFORMANCE COMPARED WITH PRIOR PUBLISHED WORKS** | [3] | [4] | [5] | **This Work** |
| Frequency (GHz) | 32 | 18 | 20 | 32 |
| Tuning Range (GHz) | 3.5 | 1.4 | 1.8 | 3.2 |
| Phase Noise (dBc/Hz) | -81 | -110 | -101.2 | **-112** |
| Power (mW) | 287.5 | - | 480 | **684** |
| Technology | 0.25 µm BiCOMS | 0.25 µm BiCMOS | 0.13 µm CMOS | 0.8 µm HBT |

V. CONCLUSIONS

An ultra low phase noise PLL was realized for millimeter wave applications using a SiGe HBT technology. Methods for the loop bandwidth design and the phase noise simulation of the PLL were discussed. Measurement results showed that this PLL had achieved very good phase noise performance of around -112 dBc/Hz at 1 MHz offset at 32 GHz oscillation frequency; it has a tuning range of around 3 GHz.

REFERENCES