33–43 GHz and 66–86 GHz VCO With High Output Power in an 80 GHz f_T SiGe HBT Technology

Gang Liu, *Student Member, IEEE*, Andreas Trasser, and Hermann Schumacher, *Member, IEEE*

***Abstract*—This letter presents a signal generation circuit that combines a wide tuning range voltage controlled oscillator (VCO) and a frequency doubler. The VCO provides two differential outputs with different power levels. A push-push frequency doubler is designed and cascaded to the high power output of the VCO, while the low power output is reserved to drive a frequency divider in a PLL. The VCO can be tuned from 33 to 43 GHz, with around 0 dBm output power at the low power output. Simultaneously, signal generation from 66 to 86 GHz is achieved at the doubler output, with a maximum output power of −1.1 dBm at 74 GHz (−2.5 dBm at 81 GHz). The measured phase noise at the VCO output and the doubler output are −91 dBc/Hz and −83 dBc/Hz at 1 MHz offset (−112 dBc/Hz and −106 dBc/Hz at 10 MHz offset), respectively. The circuit is realized in a 0.8 μm SiGe heterojunction bipolar transistor process, with f_T/f_{max} of 80/90 GHz. The VCO consumes 81 mA current while the doubler consumes an extra 17 mA from a 4 V supply. The circuit demonstrates the possibility of wide-band signal generation up to f_{max} with sufficient output power (e.g. to drive a mixer) in a conservatively scaled, low-cost process.**

***Index Terms*—Frequency multiplication, heterojunction bipolar transistors, signal generators, voltage controlled oscillators (VCOs).**

I. Introduction

VOLTAGE controlled oscillators (VCOs) are crucial components in most wireless systems. One important parameter of the VCO, the output frequency, is usually limited by the maximum oscillation frequency (f_{max}) of a technology. Fundamental oscillation beyond half of f_{max} is generally difficult to achieve, which limits the potential applications of the technology. One way to extend the output frequency range is to use push-push oscillators. However, as the frequency approaches f_{max}, the output power from a push-push oscillator is usually low, as reported in [1], [2]. The output power can be improved through a tuning network at the output, but only for a narrow bandwidth [3]. We have reported a wide band VCO [4], combined with a frequency doubler for wide band signal generation at frequencies close to f_{max} [5]. But the output power is low when a simultaneous fundamental output is taken from the VCO. In this letter, a different VCO and frequency doubler targeting higher output power with simultaneous differential fundamental output will be shown.

Manuscript received May 05, 2010; revised July 26, 2010; accepted August 02, 2010. Date of publication September 07, 2010; date of current version October 06, 2010. This work was supported by the German Federal Ministry of Education and Research (BMBF) under the project EASY-A.

The authors are with the Institute of Electron Devices and Circuits and the Competence Center on Integrated Circuits in Communications, Ulm University, Ulm, Germany (e-mail: gang.liu@uni-ulm.de; andreas.trasser@uni-ulm.de; hermann.schumacher@uni-ulm.de).

Digital Object Identifier 10.1109/LMWC.2010.2066262

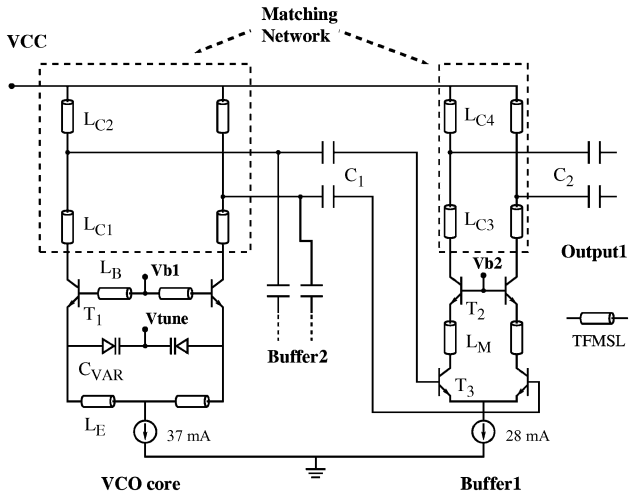

Fig. 1. Simplified schematic of the wide-tuning range VCO. T_1 is $30 \times 0.5\ \mu m^2$, T_2 and T_3 are $20 \times 0.5\ \mu m^2$. C_{VAR} has a stripe area of $20 \times 0.54\ \mu m^2$. C_1 is 300 fF and C_2 is 500 fF. Lengths of L_B, L_E, L_M, L_{C1}, L_{C2}, L_{C3} and L_{C4} are 135 μm, 800 μm, 180 μm, 155 μm, 100 μm, 300 μm and 200 μm. All transmission lines are 3 μm wide.

II. Technology Overview

The technology used in this work is the SiGe heterojunction bipolar transistor (HBT) process from Telefunken Semiconductors GmbH, Germany. It features a minimum drawn emitter width of 0.8 μm and f_T/f_{max} of 80/90 GHz. The process offers two types of npn transistors, SIC (Selectively Implanted Collector) and non-SIC, with different f_T (80 GHz and 50 GHz) and breakdown voltages (4.5 V and 2.5 V). Three metal layers, four types of resistors, varactor diodes, as well as MIM capacitors are available. Two types of silicon substrate (1000 Ωcm and 20 Ωcm) can be chosen. In this work, the low-cost 20 Ωcm substrate was used.

III. Circuit Design

The signal generation circuit consists of a VCO and a frequency doubler. The design criteria of the VCO are to have a wide tuning range and high output power to drive the frequency doubler. Meanwhile, the VCO should also provide an additional output with sufficient power to drive a frequency divider, which is necessary for locking the VCO with a PLL. Fig. 1 shows a simplified schematic of the VCO.

The VCO core is a negative resistance type, as described in [6]. Biasing voltages $Vb1$ and $Vb2$ are generated on chip. All the inductors and matching networks are realized with thin-film microstrip lines (TFMLs), with quality factors of around 8 at 35 GHz. The oscillation frequency is mainly determined by the base inductor L_B, degeneration capacitance C_{VAR} and L_E. C_{VAR} is realized with a varactor diode (150 fF to 600 fF tuning

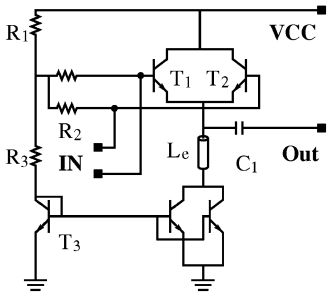

Fig. 2. Schematic of the push-push frequency doubler. All transistors are $20 \times 0.5\ \mu\mathrm{m}^2$, except for T_3, which is $5 \times 0.5\ \mu\mathrm{m}^2$. R_1, R_2 and R_3 are 550 Ω, 4.5 kΩ and 900 Ω. L_e is 100 μm and C_1 is 300 fF.

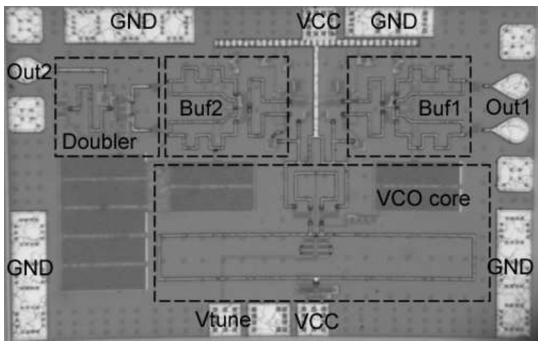

Fig. 3. Photo of the signal generation circuit. The size is $1.2 \times 0.75\ \mathrm{mm}^2$, including the pads.

range, Q of 12, at 35 GHz). By changing the voltage across the varactor diode, the oscillation frequency can be tuned. The transistors of the VCO are biased at the current for maximum $\mathrm{f_T}$, which simultaneously maximizes $\mathrm{f_{max}}$.

Different from [5], where a common-base stage was used as an output buffer, two independent cascode amplifiers (only one is shown in Fig. 1) are used to buffer the VCO core. This gives the advantages that the two outputs are well isolated from each other and the two buffers can be designed separately. One buffer is designed to have higher output power, which is needed to drive the frequency doubler, while the other buffer is designed for less power consumption with still sufficient output power to drive a frequency divider. The high power buffer directly drives a push-push frequency doubler (Fig. 2) that can operate at frequencies close to $\mathrm{f_{max}}$, as described in [5]. However, the L_e is realized with a TFML instead of an inductor, which results in slightly lower conversion gain but wider bandwidth.

IV. Measurement Results

The VCO and frequency doubler were simulated using ADS 2008. The TFMLs were modeled using a lumped-element Π model, and the parameters for the model were extracted from the EM simulation data of the line. The layout of the IC was kept as symmetric as possible to preserve the differential characteristic of the circuit, which is important for the conversion efficiency and the suppression of the fundamental signal at the doubler output. Fig. 3 shows a photo of the VCO and frequency doubler. The circuit is very compact and occupies only 0.9 mm^2, including the bond pads.

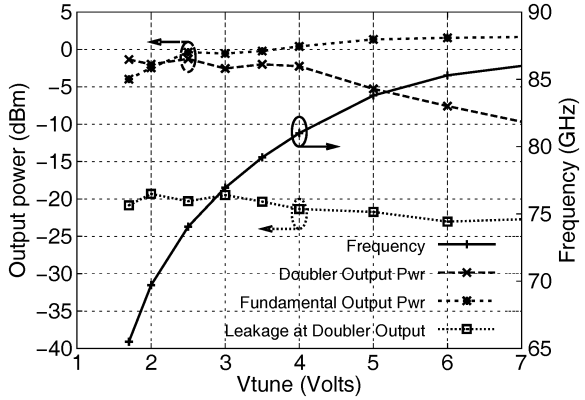

Fig. 4. Measurement of output power and frequency of the frequency-doubled signal, leakage of the fundamental signal at the doubler output, and the differential output power at the fundamental output.

The circuit was characterized on wafer. Multi-contact dc wedges were used to supply the dc voltages. The fundamental output ("Out1") was connected through a GSSG probe to a spectrum analyzer and a 50 Ω load, while the doubler output ("Out2") was connected through a 110 GHz GSG probe to a harmonic mixer (Agilent 11970 V), which extends the frequency range of the spectrum analyzer to V-band. Both outputs were monitored simultaneously. The circuit draws 98 mA current from a 4 V supply. Fig. 4 shows the measured frequency and output power of the circuit.

The oscillation frequency of the VCO can be continuously tuned by changing the tuning voltage from 1.6 V to 7 V. The output power at the doubler output is around -2 dBm from 66 to 81 GHz, with a maximum -1.1 dBm at 74 GHz, and decreases to -10 dBm at 86 GHz.[1] The decrease of the output power is due to the increase of the conversion loss of the frequency doubler. By increasing the supply voltage to 4.5 V (112 mA), 0 dBm at 66 GHz and -4.5 dBm at 86 GHz can be achieved. The leakage of the fundamental signal at the doubler output (< -20 dBm), which is mainly influenced by the symmetry of the circuit, is well below the wanted signal. The differential output power at the fundamental output varies from -4 dBm to 1.5 dBm, which is quite sufficient to drive a frequency divider that has been realized in the same technology. Fig. 5 shows a measured spectrum at the fundamental output with 20 MHz span and 300 kHz resolution bandwidth (RBW). 4 dB should be compensated for the cable and probe losses.

The phase noise of the VCO is difficult to measure, because of the jitter of the spectrum, caused by the noise from the supply and tuning voltages. In this work, the phase noise is roughly measured using the Phase Noise Utility of the spectrum analyzer (Agilent 8565E). Fig. 6 shows the measurement results. The phase noise of the doubler output is -83 dBc/Hz at 1 MHz offset (-106 dBc/Hz at 10 MHz offset), roughly 6 dB higher than the phase noise of the fundamental output, because of the frequency doubling.

A separate VCO without doubler was also fabricated and tested. The measured differential output powers are 8 dBm

[1]The power at frequencies above 75 GHz is underestimated, due to the higher conversion loss of the harmonic mixer.

TABLE I
COMPARISON OF SIGNAL GENERATION CIRCUITS OPERATING AT FREQUENCIES CLOSE TO f_{max}

Ref	Technology f_T/f_{max} (GHz)	f_{osc}	f_{osc}/f_{max}	Tuning Range	Pwr(dBm)	PN(@1MHz)	Fundamental Output	DC (mW)	Topology
[1]	InGaP HBT 50 / -	60	1.2 (f_{osc}/f_T)	2.3%	-14	-77.5	Yes	-	VCO+doubler
[2]	0.14μm SiGe:C HBT 200 / 275	278	1.01	1.5%	-20	-	No	132	Push-push
[3]	0.5μm InP D-HBT 405 / 335	287	0.85	4%	-3	-	No	-	Push-push
[5]	0.8μm SiGe HBT 80 / 90	86	0.96	29.3%	-8	-83	Yes	247	VCO+doubler
[7]	0.14μm SiGe:C HBT 200 / 275	190	0.69	3.9%	-4.5	-73	No	215	Push-push
[8]	0.13μm CMOS - / -	192	>1	0.7%	-20	-100 at 10MHz	No	16.5	Push-push
[9]	90nm CMOS - / 160	324	2	1.2%	-46	-78	No	12	Linear superposition
This	**0.8μm SiGe HBT 80 / 90**	**86**	**0.96**	**26.3%**	**-2.5**	**-83**	**Yes**	**392**	**VCO+doubler**

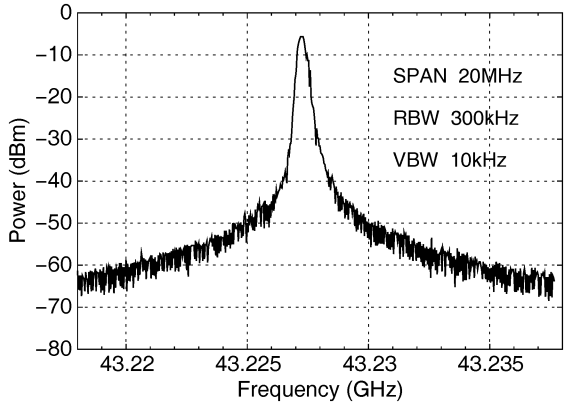

Fig. 5. Measured output spectrum from the fundamental output with a span of 20 MHz.

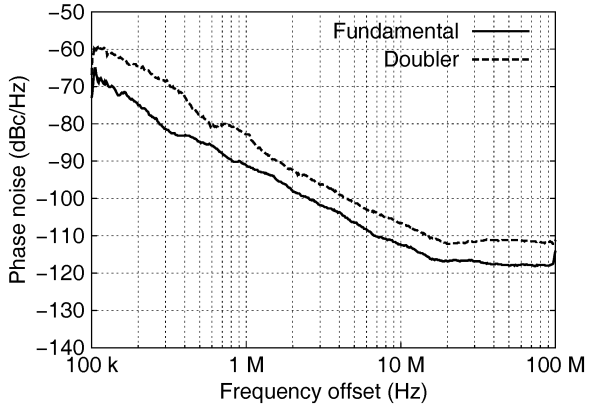

Fig. 6. Measured phase noise at the fundamental and doubler output. The VCO was tuned at 43 GHz.

(from buffer 1) and 0 dBm (from buffer2), respectively. The tuning range and phase noise performance remains the same.

Table I compares the performance of this work and some previously reported signal generation circuits that operate at frequencies close to and above f_{max} [7]–[9]. This circuit achieves the highest output power with a very wide tuning range.

V. CONCLUSION

A fully integrated signal source consisting of a wide tuning range VCO and a frequency doubler has been presented. The circuit is realized in a cost effective, 0.8 μm SiGe HBT process with f_T/f_{max} of 80/90 GHz, yet it can generate signals from 66 to 86 GHz (26.3% tuning range), with acceptable power and phase noise performance. The simultaneous differential output (from 33 to 43 GHz) enables further frequency division and locking the circuit to a PLL. By removing the frequency doubler, a high power (8 dBm and 0 dBm, simultaneously), differential, Q-band (33 to 43 GHz) signal source has also been realized.

REFERENCES

[1] O. Lee, J.-G. Kim, K. Lim, J. Laskar, and S. Hong, "A 60 GHz push-push InGaP HBT VCO with dynamic frequency divider," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 10, pp. 679–681, Oct. 2005.

[2] R. Wanner, R. Lachner, and G. R. Olbrich, "A SiGe monolithically integrated 278 GHz push-push oscillator," in *IEEE MTT-S Int. Dig.*, Jun. 2007, pp. 333–336.

[3] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y. K. Chen, "Highly efficient harmonically tuned InP D-HBT push-push oscillators operating up to 287 GHz," in *IEEE MTT-S Int. Dig.*, Jun. 2007, pp. 341–344.

[4] G. Liu, S. Chartier, A. Trasser, and H. Schumacher, "Fully integrated millimeter-wave VCO with 32% tuning range," in *Proc. Topical Meeting Silicon Monolith. Integr. Circuits RF Syst. (SiRF'09),*, Jan. 2009, [CD ROM].

[5] G. Liu, A. C. Ulusoy, A. Trasser, and H. Schumacher, "64 to 86 GHz VCO utilizing push-push frequency doubling in a 80 GHz fT SiGe HBT technology," in *Proc. Topical Meeting Silicon Monolith. Integr. Circuits RF Syst. (SiRF'10)*, Jan. 2010, pp. 239–242.

[6] H. Li and H.-M. Rein, "Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe production technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 184–191, Feb. 2002.

[7] R. Wanner, R. Lachner, and G. R. Olbrich, "A monolithically integrated 190-GHz SiGe push-push oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 12, pp. 862–864, Dec. 2005.

[8] C. Cao, E. Seok, and K. K. O, "192 GHz push-push VCO in 0.13 μm CMOS," *Electron. Lett.*, vol. 42, no. 4, pp. 208–210, Feb. 2006.

[9] D. Huang, T. R. Larocca, L. Samoska, A. Fung, and M.-C. F. Chang, "324 GHz CMOS frequency generator using linear superposition technique," in *IEEE ISSCC Tech. Dig.*, Feb. 2008, pp. 476–477.