Fully Integrated Millimeter-Wave VCO with 32% Tuning Range

Gang Liu, Sébastien Chartier *, Andreas Trasser and Hermann Schumacher

gang.liu@uni-ulm.de
Institute of Electron Devices and Circuits, University of Ulm
Albert-Einstein-Allee 45, 89081 Ulm Germany
* now with Fraunhofer-Institut für Angewandte Festkörperphysik - IAF
Tullastrasse 72, 79108 Freiburg i. Br. Germany

***Abstract*—In this paper, the authors present a fully integrated VCO with 32% tuning range centered at 38.9 GHz. The VCO was designed using a commercially available, inexpensive 0.8 μm Si/SiGe HBT technology with f_T and f_{max} of 80 and 90 GHz, respectively. It consumes 195 mW DC power and provides an output power of more than 5 dBm. A phase noise of -93 dBc/Hz at 1 MHz offset was measured for the free running VCO.**

***Index Terms*—Millimeter-Wave VCO, SiGe HBT, wide tuning range.**

I. Introduction

As spectral congestion increases at lower frequencies and cost-effective semiconductor technologies with cut-off frequencies approaching or surpassing 100 GHz, millimeter-wave applications are receiving more and more attention. The VCO in this work covers a wide frequency range from 32.6 GHz to 45.2 GHz, which makes it suitable for many different applications. At the lower side of the spectrum window, 35 GHz is suited for Synthetic Aperture Radar (SAR) applications [1]. 30 GHz can be doubled to the 60 GHz ISM band and 38/39 GHz can be doubled for 77/79 GHz automotive radar applications. The technology used in this design is a Si/SiGe HBT technology with 0.8 μm minimum drawn dimensions, which provides a transit frequency $f_T = 80$ GHz and a maximum frequency of oscillation $f_{max} = 90$ GHz. The goal of our work is to demonstrate that millimeter-wave applications can be addressed well by this cost-efficient technology, accelerating the pick-up of millimeter-wave techniques for commercial and consumer applications. While amplifiers operating at 36, 40 and 50 GHz have already been designed and realized using the same technology [2], this work demonstrates its work in high-performance millimeter-wave oscillators.

II. Technology Overview

The technology used in this work is the Si/SiGe HBT process commercially available from Atmel GmbH (Germany) [3]. It is a 0.8 μm technology with a minimum effective emitter size of 0.5 x 1.1 μm^2. The SIC-npn transistor (with selectively implanted collector) improves the f_T from 50 GHz (for non-SIC npn transistor) to 80 GHz, at the price of a lowered collector-emitter breakdown voltage (BV_{CEO}) of 2.4V (4.3V for non-SIC npn transistor). pn, Zener, and varactor diodes are also implemented in this process. Three aluminum metal layers and four types of resistors are provided as well as MIM and nitride capacitors. Two types of substrate (1000 Ωcm and 20 Ωcm) are available; the inexpensive, low resistivity (20 Ωcm) substrate was used throughout this work.

III. Circuit Description

The VCO is a negative resistance type VCO. Varactor diodes were used for the frequency tuning. Inductors were realized using Thin Film Microstrip Lines (TFMSL). The circuit is fully differential and has two differential output branches, which can be used to feed a differential mixer and frequency divider respectively. A common-base stage was used as an output buffer to increase the output power and isolate the VCO core from the load.

A. TFMSL

TFMSLs were used in this design to realize the inductive reactances. Compared with spiral inductors, the inductance of a short-ended microstrip line is more easily tunable, which makes the design and redesign much easier. The quality factor can be increased by shielding the signal from penetrating into the lossy substrate. The chip size will also be acceptable, because of the short effective wavelength in the millimeter-wave range.

The TFMSLs utilize the top metal layer (2.5 μm thick) and the bottom metal layer (0.85 μm thick) of the process. The top layer serves as the signal and the bottom layer as the ground, which shields the signal from the lossy substrate. Silicon dioxide is filled in between the metal layers. The distance between the top and bottom metal layer is 3.3 μm, comparable to the thickness of the top metal, so the lines cannot be treated as ideal microstrip lines where the metalization thickness is assumed to be negligible. To model these TFMSLs, a Π model was used as shown in Fig. 1. 10 stages were used to represent the distributive characteristic of transmission lines, which also solves the problem caused by self resonance of the Π model [4]. The TFMSLs were first simulated using EM simulation tools (Momentum and Sonnet), then the parameters

9781-4244-2831-1/09/$25.00 ©2009 IEEE

were extracted from the simulation data, as described in [5]. The model is scalable in length. Good agreement between the model and the simulation was achieved for different line lengths.

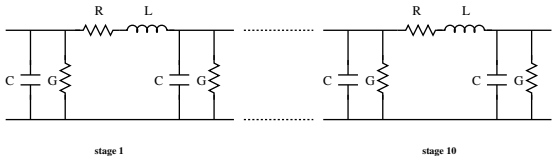

Fig. 1. 10 stage Π model used to model the TFMSL. Parameters can be extracted from simulation or measurement.

B. VCO Core

The VCO utilizes a negative resistance type VCO core, based on the topology presented in [6]. Capacitive degeneration was used to generate a negative resistance looking into the base. A base inductor was used to complete the resonance circuit. As shown in Fig. 2, L_E and C_{VAR} are in parallel and show capacitive behavior in total. L_E also facilitates biasing, it needs to be chosen carefully to guarantee that L_E and C_{VAR} in parallel still behave capacitively in the operating frequency range. L_B serves as the base inductor. Due to the

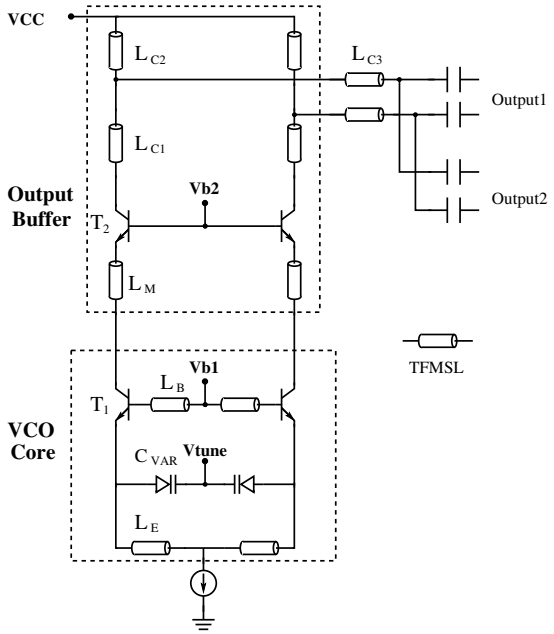

Fig. 2. VCO core schematic with output buffer. TFMSLs are used as inductors for the resonant circuit and output matching.

differential topology, biasing nodes Vb1, Vb2 and Vtune are virtual grounds, which decreases their influence on the VCO core.

C. Output buffer

Output power and frequency of a VCO tend to vary as the load changes, which is a disadvantage if the VCO must drive different loads like mixers, frequency dividers, etc. To overcome this problem, an output buffer was added in this design. As shown in Fig. 2, a common-base stage was cascaded to the VCO core, which isolates the VCO core from the loads and also increases the output power. Furthermore, a transmission line L_M was added in between the VCO core and the buffer to improve the matching conditions between the two stages. As the VCO was intended to drive a differential mixer and a differential frequency divider, the output was split into two branches, as shown in Fig. 2. L_{C1}, L_{C2} and L_{C3} improve the output matching condition. The lengths of these lines were optimized for maximum output power.

IV. Simulation and Layout

A. Simulation

To determine the oscillation frequency, only half of the circuit needs to be analyzed, as shown in Fig. 3. Small signal S-parameter simulation was performed for the start-up condition. Z_1 has negative real and imaginary parts, which

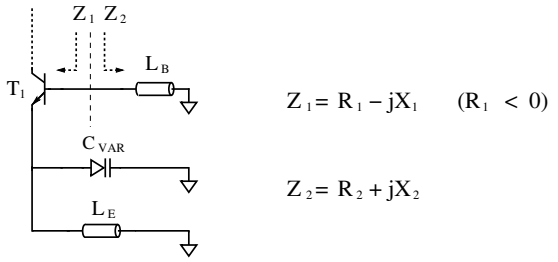

Fig. 3. Simulation of the input impedance, seeing into the base of T_1 and the base inductor L_B.

is the result of the capacitive degeneration. Z_2 has a small positive real part and positive imaginary part, which represents the impedance of the base inductor. The oscillation will finally sustain at the frequency where $Z_1+Z_2=0$. However, to start the oscillation, $|R_1| > 1.2R_2$ should be fulfilled [7]. It is shown

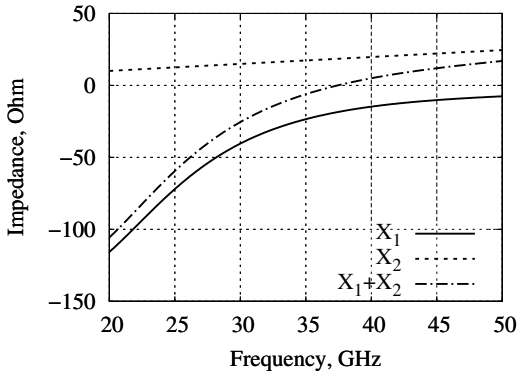

Fig. 4. Simulated imaginary part of Z_1 and Z_2. The oscillation starts at 37.8 GHz, where the sum of X_1 and X_2 equals zero.

in Fig. 4 that X_1 and X_2 cancel out at 37.8 GHz, while R_1 at this frequency is negative and the value is much larger than R_2, which is sufficient to start the oscillation, as shown in Fig. 5.

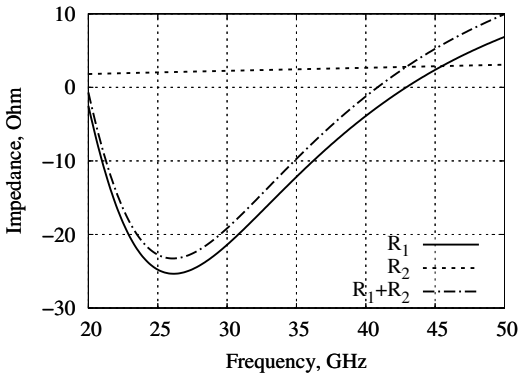

Fig. 5. Simulated real part of Z_1 and Z_2. At the oscillation frequency, $|R_1|$ is much larger than R_2, which is sufficient to start the oscillation.

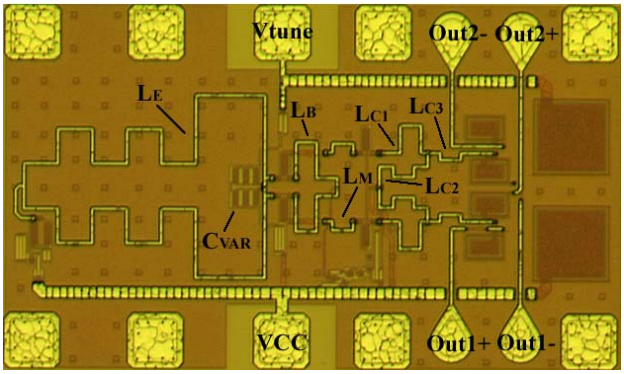

Fig. 6. Chip photo of the VCO shown in Fig. 2. The chip size is 893 × 530 μm^2, including pads.

The frequency of oscillation is mainly determined by L_B, C_{VAR} and L_E. The varactor diode was formed by connecting three small diodes in parallel, which increases the quality factor of the varactor diode. L_B was then tuned to reach the targeted oscillation frequency. L_E has little influence on the frequency, but it was chosen to be quite large to guarantee the capacitive behavior of C_{VAR} and L_E in parallel and efficiently filter the noise generated by the current source [6]. When the tuning voltage is changed from 0 to 5V, the simulated frequency is continuously tunable from 35 GHz to 47 GHz.

To estimate the output power and phase noise, a large signal Harmonic-Balance simulation was performed. The simulated output power was 6 ± 1 dBm through the whole tuning range. The suppression of second and third harmonics were more than 30 dB. The simulated phase noise ranged from -94 dBc/Hz to -88 dBc/Hz at 1 MHz offset from the oscillation frequency.

The layout of the VCO was made as symmetrical as possible, although some asymmetries were unavoidable. Since all the TFMSLs are on the top metal layer while the transistors are all on the bottom metal layer, vias had to be used for connecting the TFMSLs. The vias were not included in the simulations, which decreased slightly their accuracy. The lines used to connect the three diodes also influence the oscillation frequency. A post-layout simulation showed that these lines actually lower the oscillation frequency. The transmission lines were folded to save chip area. As this was the evaluation version, the chip was not optimized for minimum size. Fig. 6 shows a photo of the fabricated VCO, which occupies 893 × 530 μm^2 chip area, including the pads.

V. Measurement

The VCO was measured on wafer. An Agilent 8565EC spectrum analyzer was used to measure the output spectrum. The VCO has two differential output branches (indicated in Fig. 6). In this measurement, because of the difficulty of manipulating probes, "Out2+" and "Out2-" were left open. "Out1+" was connected to the spectrum analyzer and "Out1-" was terminated with a 50Ω load. This is different from the simulation where the four output nodes were all terminated with 50 Ω loads and will cause the total output power to be 1 dB lower (verified by simulation). The VCO oscillates from 32.6 GHz to 45.2 GHz while the tuning voltage was changed from 0V to 8V. It is slightly lower than the simulation because of the influence of the vias and the lines used to connect the three varactor diodes and also the possible inaccuracy of the transmission line models. But it can be very easily corrected by slightly shortening the length of L_B.

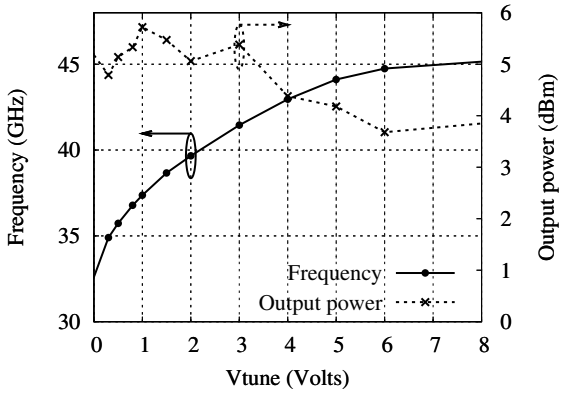

Fig. 7. Measured oscillation frequency and output power vs. tuning voltage. The frequency can be tuned continuously between 32.6 GHz and 45.2 GHz. A total output power of around 4.7 dBm was measured.

The measured total output power was 4.7 ± 1 dBm over the whole tuning range. Fig. 8 shows the measured dependency of oscillation frequency and output power on the tuning voltage. Because of the wide tuning range, the gain of the transistors in the VCO core and output buffer decreases at higher frequencies, so the output power decreases slightly at higher frequencies. The chip consumes 49mA current at 5V supply. When lower output power is needed, the DC power consumption can also be significantly reduced by lowering the supply voltage. The chip consumes only 19.5 mA at a 3V voltage supply and can still generate 0.6 dBm total output power.

Phase noise is also an important parameter to evaluate the performance of an oscillator. It is difficult to get an accurate phase noise measurement on chip while the tuning voltage is supplied, because the DC needle that is used to supply

the tuning voltage deteriorate the phase noise performance significantly. So the phase noise was first measured without attaching the tuning voltage. To make a good contact, a coplanar probe was used to contact the "VCC" pad instead of DC needles. The VCO oscillates at 42.677GHz without applying a tuning voltage.

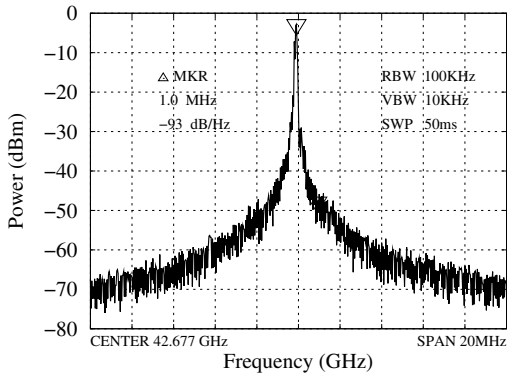

Fig. 8. Measured spectrum of the VCO without tuning voltage using an Agilent 8565EC with a span of 20 MHz. The VCO oscillates at 42.677 GHz. A phase noise of -93 dBc/Hz was measured at 1 MHz offset.

Fig. 8 shows the output spectrum at the "Out1+" node, the phase noise at 1 MHz offset is -93 dBc/Hz, which agrees well with the simulation. The losses from the cables, probes and the measurement setup should be compensated to get the real output power and 3 dB more should be added to get the total output power due to the differential topology.

The phase noise was also measured using the Phase Noise Utility of the Agilent 8565EC, which is a built-in software specialized to measure the phase noise of an oscillator at different offset frequencies or to continuously measure the phase noise at one spot offset frequency. Fig. 9 shows the measured phase noise from 100 kHz to 100 MHz offset. The phase noise at 1 MHz offset is around -92 dBc/Hz, which agrees quite well with the simulation and the first phase noise measurement.

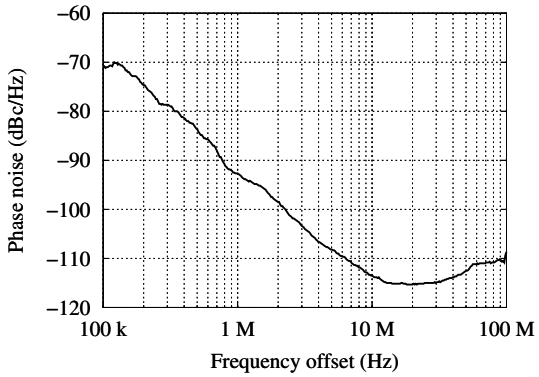

Fig. 9. Measured phase noise of the VCO without tuning voltage. The oscillation frequency is 42.667 GHz. Phase noise was measured from 100 kHz to 100 MHz offset, using the Phase Noise Utility of Agilent 8565EC. -92 dBc/Hz at 1 MHz offset was measured.

To accurately measure the phase noise through the whole tuning range in the future, the chip will be mounted on a test structure and large capacitors will be placed to filter the noise contributions of the tuning voltage.

VI. Conclusion

A fully integrated VCO that covers a 32% tuning range centered at 38.9 GHz was designed using a commercially available, low-cost SiGe HBT technology. The VCO achieved good performance in terms of frequency tuning range, output power and phase noise. It successfully demonstrated the suitability of this 0.8 μm process for millimeter-wave applications.

Acknowledgment

The authors wish to thank Atmel GmbH (Germany) for their continuous excellent collaboration and the fabrication of the IC.

References

[1] K. Tomiyasu, "Conceptual reconfigurable antenna for 35 GHz high-resolution. spaceborne synthetic aperture radar," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 39, no. 3, pp. 1069- 1074, Jul. 2003.

[2] S. Chartier, E. Sönmez, H. Schumacher, "Millimeter-wave amplifiers using a 0.8 μm Si/SiGe HBT technology," *Proceedings of the 2006 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 18-20 Jan. 2006.

[3] A. Schüppen, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus, M. Averweg, "An 80 GHz SiGe production technology," *III-V Review*, vol. 14, pp 42-46, Aug. 2001.

[4] S. Bleuler, "A Static Frequency Divider in InP-DHBT Technology for Process Control," *Diploma Thesis*,2002.

[5] W. Dürr, U. Erben, A. Schüppen, H. Dietrich and H. Schumacher, "Investigation of microstrip and coplanar transmission lines on lossy silicon substrates without backside metalization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46 (No. 5), pp. 712-715, May 1998.

[6] H. Li and H.-M. Rein, "Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe production technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 184-191, Feb. 2002

[7] G. Vendlin, A. Pavio, U. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. J. Wiley & Sons, 1990