Compact SiGe HBT Low Noise Amplifiers for 3.1-10.6 GHz Ultra-Wideband Applications

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Abstract — **Two compact SiGe HBT low noise amplifiers for ultra-wideband (UWB) applications are presented. The measured noise figure of the first approach is 2.4dB at 7GHz and below 2.9dB in the UWB bandwidth from 3.1GHz up to 10.6GHz. The circuit delivers 17.3dB peak gain with gain variations of less than 1.6dB within the entire band. The measured input 1-dB compression point at 7GHz is -13.5dBm with 16.6mA total current consumption from a 3.3V supply. The second approach exhibits noise figures between 2.8dB and 3.2dB within the UWB band. Measurements show 23.5dB of gain with 0.6dB variation over the full bandwidth. The measured input 1-dB compression point at 7GHz is -19.5dBm with a 18.2mA bias current at a 3.0V supply. The first and second design occupy a chip size of 0.39mm x 0.38mm and 0.44mm x 0.38 mm, respectively.**

Index Terms — **Ultra-wideband, UWB, low noise amplifier, SiGe HBT**

I. INTRODUCTION

The basic idea of UWB radio systems, namely the transmission of data at very low power levels by spreading the energy of the radio signal over a very large bandwidth, has its origin in the early 1960s [1]. However, the FCC's legalization [2] of unlicensed UWB devices operating at defined power levels, invoked numerous research activities regarding UWB communication systems. Low noise amplifiers are one of the most challenging building blocks in UWB radio systems. A low noise figure, a high gain and a small occupied die area are major design goals when developing UWB low noise amplifiers. Commonly used techniques in designing broad-band amplifiers are feedback, inductive and capacitive peaking methods or distributed amplification. Power consumption and necessary die area are major draw-backs of distributed amplification. Concentrated amplifiers with lumped elements generally consume a much smaller die area. This is especially true for designs that achieve the necessary bandwidth in the absence of large on-chip spiral inductors. In this work we present two UWB amplifiers that have the advantage of a lower noise figure and a smaller chip size compared to previously published work on UWB amplifiers in a comparable gain range [3]–[5].

II. TECHNOLOGY

The presented circuits have been designed and fabricated using the commercially available ATMEL SiGe2 HBT technology [6]. All active devices utilize the selectively implanted collector option of this process which yields a device transit frequency of $f_T = 80$GHz. The passive and active devices are realized on low-resistivity 20Ωcm substrate. The process offers three metallization layers.

III. CIRCUIT DESIGN

A. Two-Stage Amplifier

The first approach is a two-stage amplifier with two AC-coupled common emitter stages. The schematic circuit diagram is shown in Fig. 1.
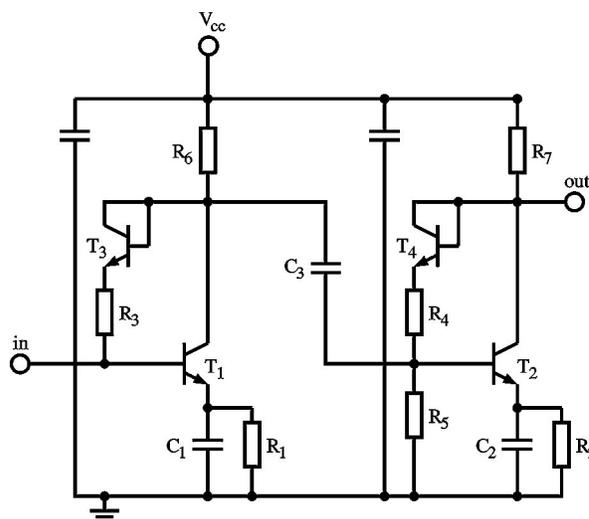

Fig. 1.   Schematic circuit diagram of the two-stage amplifier

A combination of local series feedback (R_1, R_2) with capacitive emitter degeneration (C_1, C_2) and local shunt feedback is applied to broaden the operating frequency

range in terms of gain, linearity and noise matching. The diodes in the feedback paths increase the collector-emitter voltage of transistor T_1 and T_2, resulting in a higher f_{max} of the transistors through a decreased base-collector capacitance together with an improved large signal behavior [7]. The shunt feedback paths use the base-emitter diode of transistor T_3 and T_4 together with the resistors R_3 and R_4, R_5, respectively. The main noise contributor to the overall noise figure is transistor T_1 which has been sized as a compromise between optimum current density for minimum noise and achievable bandwidth. The effective emitter window of T_1 has a size of 0.5µm x 29.7µm. The CBEB transistor configuration with two base contacts reduces the critical base series resistance which negatively affects the noise performance and the maximum frequency of oscillation. The complete chip, pads included, has a size of 0.39mm x 0.38mm. A microphotograph of the circuit is shown in Fig. 2.
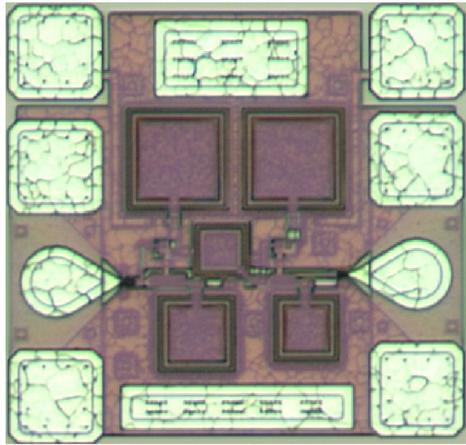

Fig. 2.   Microphotograph of the two-stage amplifier

The additional rectangular ground-pads at the edges of the chips can be used to provide low-impedance ground connections on the topside of the chips when mounting the amplifiers. This is necessary as no backside metallization and no substrate via holes are available.

B. Three-Stage Amplifier

The second approach is a three-stage amplifier with a common emitter stage which is succeeded by an emitter follower and an additional common emitter stage. The schematic circuit diagram is shown in Fig. 3. Both common emitter stages use series feedback (R_1, R_2) with capacitive emitter peaking (C_1, C_2). Global shunt feedback between the first and second stage is done via resistor R_3. The overall feedback offers a high degree of bias stability and reduced sensitivity to device tolerances. The noise figure of the amplifier is mainly determined by the noise

contribution of transistor T_1. The effective emitter window of T_1 has a size of 0.5µm x 19.7µm. As in the first approach, a CBEB configuration has been chosen to minimize the base series resistance of the transistors. The parasitic input capacitance of the final common emitter stage is partly compensated by inductor L_1, which is realized as an inductive transmission line between the second and third stage. The last stage uses the base-emitter diode of transistor T_4 together with resistor R_4 in the local shunt feedback path.
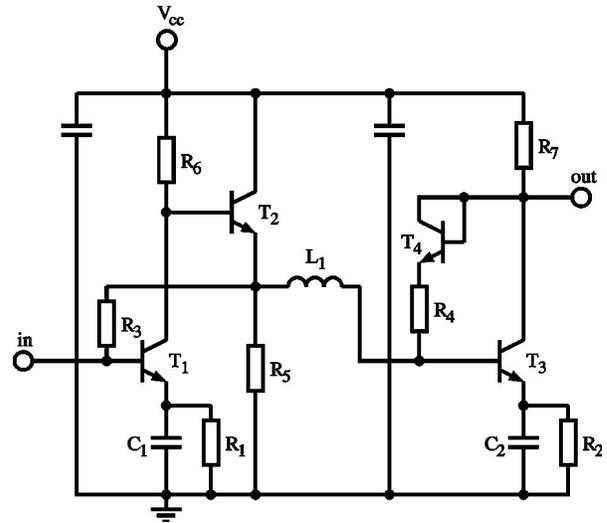

Fig. 3.   Schematic circuit diagram of the three-stage amplifier

All stages are DC-coupled, which results in a flat frequency response down to DC. The complete chip, pads included, has a size of 0.44mm x 0.38mm. Fig. 4 shows a microphotograph of the circuit.
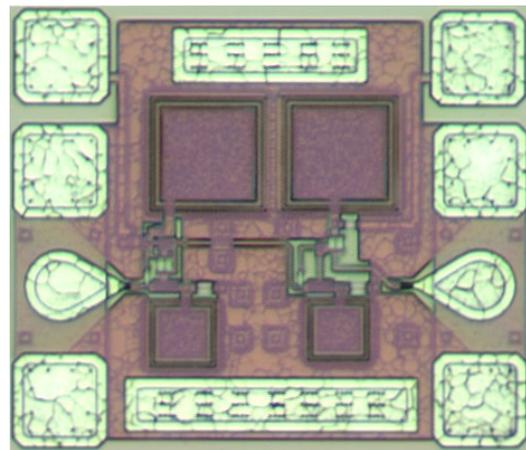

Fig. 4.   Microphotograph of the three-stage amplifier

IV. MEASUREMENT RESULTS

Measurements were performed on-wafer in a 50Ω test environment using a vector network analyzer. Two on-wafer ground-signal-ground microwave probes were used to contact the input and output ports of the circuits. The two-stage amplifier is biased with 16.6mA and operates at a 3.3V supply. The bias current of the three-stage amplifier is 18.2mA at a 3.0V supply.

A. Small-Signal Measurements

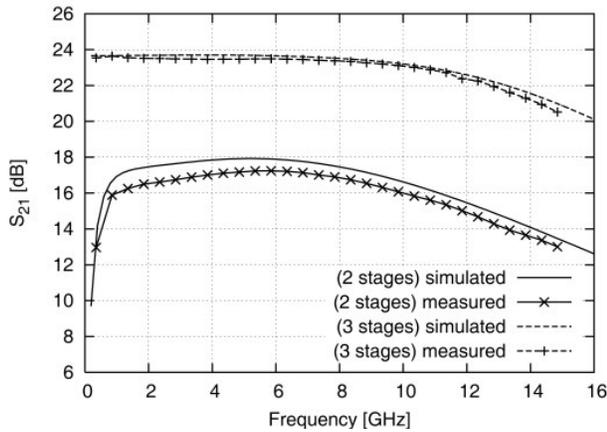Fig. 5 and Fig. 6 show the measured and simulated scattering parameters of both circuits.
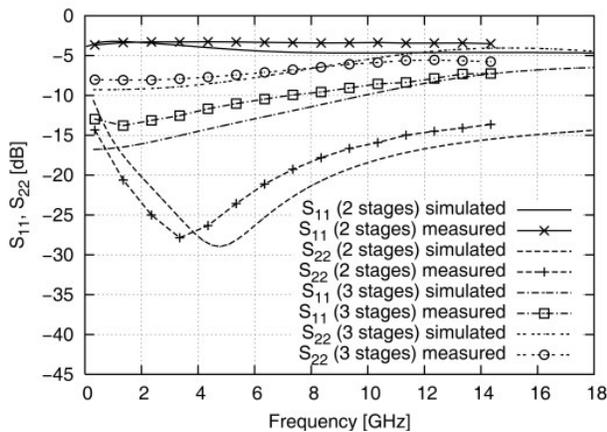

Fig. 5.   Measured and simulated gain

Fig. 6.   Measured and simulated input (S_{11}) and output (S_{22}) return loss

The two-stage amplifier shows 17.3dB peak gain with gain variations of less than 1.6dB within the UWB frequency band. The three-stage amplifier delivers 23.5dB of gain with 0.6dB variation over the full bandwidth. Input (S_{11}) and output (S_{22}) return losses of the two-stage amplifier

vary from -3.4dB to -3.2dB and -28dB to -15.8dB, respectively. Measured S_{11} and S_{22} parameters of the three-stage amplifier vary from -12.8dB to -8.5dB and -8dB to -5.8dB, respectively. The measured and simulated noise figures are depicted in Fig. 7. The noise figure of the two-stage amplifier is 2.4dB at 7GHz and below 2.9dB in the UWB bandwidth.
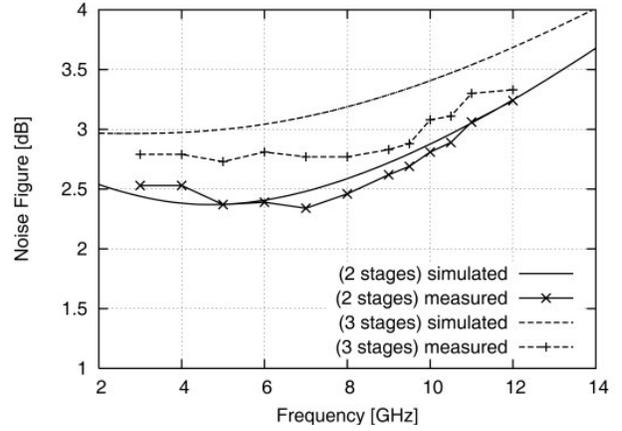

Fig. 7.   Measured and simulated noise figure

The three-stage amplifier exhibits noise figures between 2.8dB and 3.2dB across the band. Fig. 8 shows the phase responses of the circuits, which are almost linear over a frequency range exceeding the UWB band.
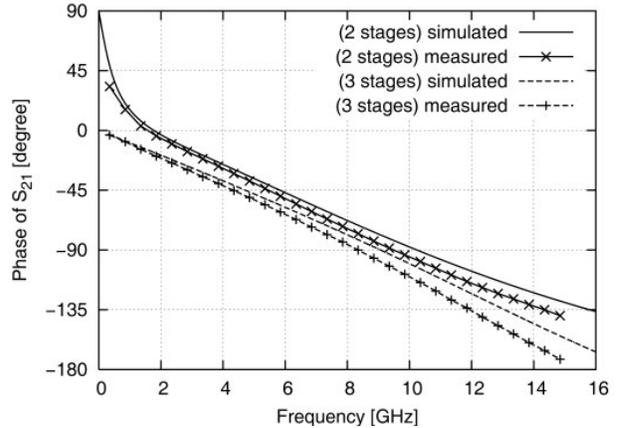

Fig. 8.   Measured and simulated phase delay versus frequency

Excellent agreement with the simulations has been achieved for all measurements.

B. Large-Signal Measurements

Amplifier linearity is evaluated by measuring the 1-dB compression point and the third-order intercept point.

Measurements were done using a conventional setup using RF sources and spectrum analyzer. Fig. 9 and Fig. 10 display the large-signal behavior of the amplifiers.
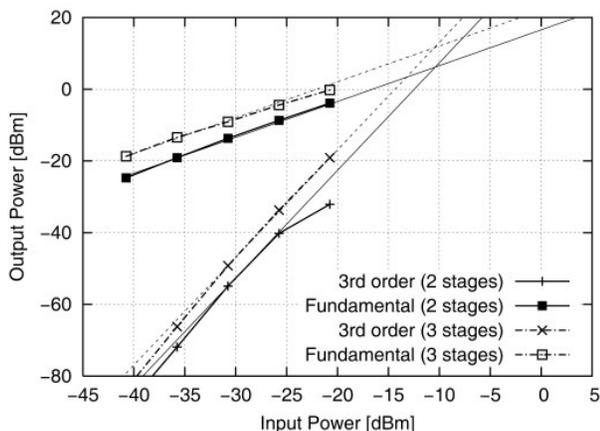

Fig. 9.   Measurement of third-order intercept point

The measured input-referred third-order intercept point at 7GHz (200MHz tone-spacing) equals -10.5dBm for both amplifiers. The measured input 1-dB compression point at 7GHz equals -13.5dBm for the two-stage amplifier and -19.5dBm for the three-stage amplifier, respectively.
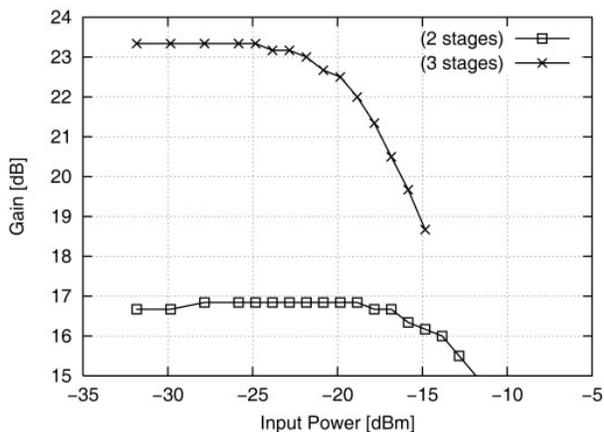

Fig. 10.   Measurement of 1-dB compression point

V. CONCLUSION

Two ultra-compact UWB low noise amplifiers fabricated on a commercially available Si/SiGe HBT process have been presented. Both designs exhibit an extremely low noise figure of less than 2.9dB and 3.2dB, respectively, across the UWB frequency band from 3.1GHz up to 10.6GHz. The high gains (17.3dB and 23.5dB), the flat passband characteristics, the linear phase responses and the input compression points (-13.5dBm and -19.5dBm) along with a moderate power consumption (55mW) make these circuits ideally suited for UWB applications.

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