InP–based and metamorphic devices for multifunctional MMICs in mm–wave communication systems

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Abstract

In this paper, the performances of our InP–based and metamorphic HFETs are compared. Measurements on the RF as well as the noise behaviour are presented. Furthermore, first results are demonstrated on the integration of the InP–based PIN diode and HFET on one InP–substrate. Using these two devices, we integrated three different MMIC designs on one wafer: SPDT switch, phaseshifter and a combination of SPDT switch and LNA for a multifunctional MMIC.

I. Introduction

THE enormous rise of mm–wave communication systems as well as the growing interest in sensor systems with increased resolution are driving the demands for circuits suitable for these applications. Most commonly today, the MMICs in the systems are packaged in multi-chip modules [1]. However, when attempting to use mm–wave frequencies, one has to face some major drawbacks using this assembling technology. The interconnections between the MMICs with bonding wires are difficult to realize reproducibly and the area consumption of the hole assembly is intensive. Furthermore, the testing of every chip is time and money consuming. In this paper, we propose an approach to overcome these drawbacks. The basic idea of this approach is to integrate the different devices, needed for the realization of the different MMIC functionalities, on one single wafer [2]. The number of chip interconnections, the testing and assembling effort are reduced considerably while the optimum performance of the multifunctional chip is maintained by integrating different devices. Additionally, the chip size can be reduced by using interstage networks between the active devices instead of matching every MMIC to the 50–Ω environment.

Currently, we are working on the integration of the PIN diode and the HFET process to establish the basis for multifunctional MMICs. Switches with PIN diodes as active devices showed superior performance at mm-wave frequencies [3], [4], [5], [6] and could furthermore be used for attenuators, limiters or phaseshifters. The InP-based HFETs demonstrated the lowest noise figures and high associated gains for the use in LNAs [7], [8] and could also be the active device in a mixer.
In this paper a comparison of the performance of our InP–based and metamorphic HFET processes will be given and first results of the integration of the PIN diode and the HFET on one substrate will be presented. Furthermore, the results from three different MMICs on one wafer (SPDT, phaseshifter and a SPDT–LNA combination) are demonstrated.

II. InP–based vs. metamorphic HFET

During the last year the InP process was improved in terms of DC and RF performance as well as with regard to process stability. The first step to improve the performance was the reduction of the gate-length to 120 nm. In two additional steps we changed the substrate heating temperature during the growth and the layer structure was adjusted to achieve a reliable selective gate recess. While optimizing the InP-based process, we adopted these experiences to the metamorphic technology. To compensate the lattice–mismatch, an InAlAs buffer layer with a linearly graded indium content is used which results in a relaxation level of 94 percent. All active layers except for the channel are lattice-matched to InP. For the channel, we are using a graded layer with a higher In–content. The DC–results we obtained with our HFET processes are summarized in Table I.

The maximum extrinsic transconductance of $g_m > 1000\,\mathrm{mS/mm}$ is achieved for V_{GS} of -0.5 V and V_{DS} of 1.7 V for both devices. But even at a lower $V_{DS} = 1\,V$, the metamorphic HFET still demon-

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	$g_{m,max}$ (mS/mm)	$I_{DS,gm,max}$ (mA/mm)	I_{DSS} (mA/mm)
InP	1100	545	1150
Meta	1061	467	1120

TABLE I
DC–characteristics of $2x60\,\mu m$ HFETs

strates an extrinsic transconductance of 880 mS/mm with a corresponding current of 340 mA/mm. The following Table II gives an overview on the RF and noise performance of the two technologies.

	f_T (GHz)	f_{max} (GHz)	F_{min} (dB)	G_{ass} (dB)
InP	163	182	0.75	12.1
Meta	155	162	1.0	11.4

TABLE II
RF performances at maximum f_T bias condition and noise characteristics at 22 GHz of $2x60\,\mu m$ HFETs

The devices were biased for maximum f_T at a V_{DS} of 0.9 V and a current of 52 mA for the metamorphic (43 mA for the InP–based) device. The second column of the table shows the corresponding f_{max} values. The cut–off frequencies are slightly higher for the InP–based device. Comparing the noise performance of these devices one can observe, that the minimum noise figure of the metamorphic device is slightly higher, indicating the need for further optimization. The associated gain which is achieved in the range of the optimum drain current is approximately the same for both devices. In Fig. 1, the measured noise performance of the two 2x60 μm HFETs at a drain bias of $V_{DS} = 0.7$ V and at a frequency of 22 GHz is depicted. The optimum drain current for the minimum noise figure seems to be a little bit lower for the metamorphic HFET.

III. Technology for heterointegration

A first step to integrate the different MMIC functionalities of a mm–wave frontend on one single wafer is to integrate a PIN diode and a HFET device on the same substrate. This enables us to design switches, phaseshifters, limiters, attenuators, LNAs, MPAs and mixers. For the integration of these two devices, the layers for the PIN diode are grown on top of the HFET layers in a single growth process by MBE. The heterointegration technology is a merger of the two sin-

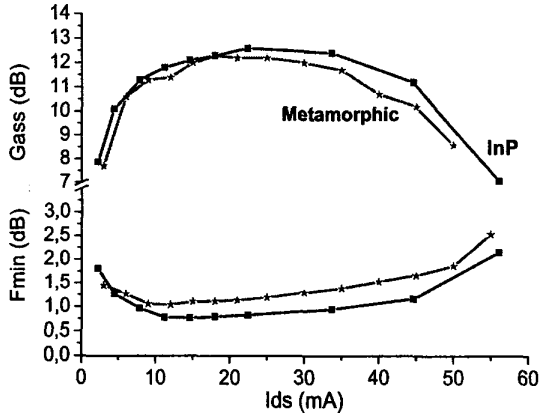

Fig. 1. Minimum noise figure and associated gain at 22 GHz and $V_{DS} = 0.7\,V$

gle technologies. The devices are selectively etched and then, combined processes are used for the evaporation, sputter and passivation processes.
The first process steps are the evaporation of the p^+–ohmic contacts, the etching of the p–MESA and of the larger n–MESA. Between the n^+–region of the PIN diode and the cap layer of the HFET is an InP etch stop layer to ensure that the cap layer of the HFET is not removed during n–MESA etching. After removing the stop layer with a HCl–based acid, the HFET–MESA is etched and TaN is deposited for the resistors in the MMICs. Then, n^+–ohmic contacts for the PIN and HFET are evaporated and the gate openings are defined by ebeam lithography. After the selective recess with succinide acid, the aluminum-based gate is deposited. Finally, all devices are passivated with SiN_x and electro–plated gold completes the MMIC process.

IV. Integrated PIN and HFET devices

With the above described technology, a first process run was performed and the different devices were characterized. The PIN diodes showed the same performance as before in [4] with a cut–off frequency of approximately 5 THz, a breakdown voltage of -16 V and a power handling capability of at least 25 dBm [9].
For the first approach, we used a simplified HFET structure compared to section II with no graded channel. The HFETs had a very low contact resistance of 0.08 Ωmm and demonstrated an extrinsic transconductance of $g_m = 729$ mS/mm with a corresponding drain current of $I_{DS} = 205$ mA/mm at a drain–source voltage of $V_{DS} = 1$ V. The maximum current was $I_{DS} = 544$ mA/mm at $V_{DS} = 1$ V which is a little bit

less than what we achieve with devices from single–HFET wafers. The RF–performance was measured up to 118 GHz and a cut–off frequency of $f_T = 155$ GHz was extrapolated at a $V_{DS} = 1$ V with a corresponding drain current of 26 mA.

V. MMICs on heterointegrated wafer

To demonstrate the multifunctionality of this approach, we designed different coplanar MMICs such as switches, phaseshifters and LNAs to be processed simultaneously on the same substrate with a stacked layer structure.
The SPDT switch had one PIN diode in shunt configuration in each branch, four DC–blocking capacitors and on–wafer biasing for the PIN diodes. The diode in the off–state was biased at −5 V and in the on–state at +0.75 V which corresponds to a current of $I_D = 45$ mA. The measured performance up to 120 GHz of the SPDT is shown in Fig. 2.

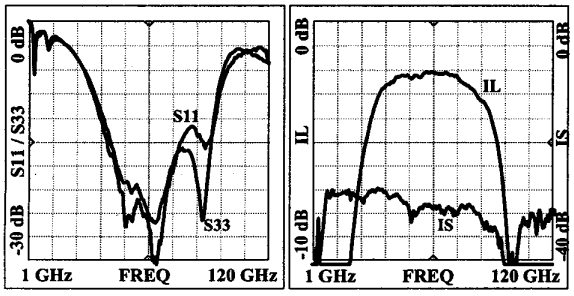

Fig. 2. Measured performance of the PIN diode SPDT switch

The switch was designed for 58 GHz and exhibits an extremely broad input matching of better than -10 dB over a frequency band from 36 GHz up to 93 GHz at the PA input port (S11) as well as at the antenna port (S33). The insertion loss (IL) is smaller than 2.5 dB from 40 GHz to 74 GHz with a minimum at 58 GHz of 2.0 dB. The ultra–broad band isolation (IS) of this switch was more than -27 dB over the whole measured frequency range from 1 to 120 GHz.

Another example, where PIN diodes are used, is a two–bit phaseshifter which is depicted in Fig. 3. The first bit on the left side of the MMIC was designed using the loaded–line concept. The transmission line is loaded with two short stubs of different line length depending on the biasing of the PIN diodes. The short stub is either shunted by the diode biased in forward direction or by the parallel MIM capacitor commonly used by both diodes. The phase shifting in the second bit is realized by switching two transmission lines of different length and circuitry. The biasing of the

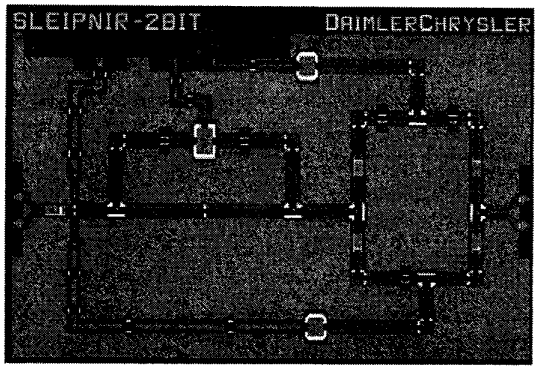

Fig. 3. 2–bit PIN diode phaseshifter

diodes in the on– and off–state is the same as in the SPDT switch. Table III summarizes the performance of this phaseshifter at the design frequency of 58 GHz.

	Bit 0	Bit 1	Bit 2	Bit 3
S11(dB)	-18.8	-22.0	-22.8	-21.2
S21(dB)	-4.1	-4.0	-4.1	-4.2
φ(58 GHz)	ref	26°	50°	76°
$\Delta\varphi$(54 – 62 GHz)	ref	2.6°	3.9°	7°

TABLE III
RF performance of the 2–bit phaseshifter at 58 GHz

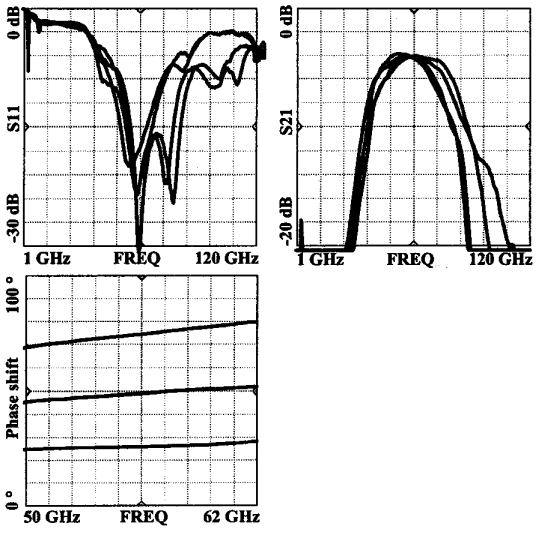

Fig. 4. Measured s–parameters of the 2–bit–phaseshifter

Important figures of merit for a phaseshifter are identical input matching and losses for all states and the total amount of phase shifting with little shift error across the desired frequency band. Fig. 4 illustrates

the measured s–parameters of the two bit phaseshifter. The MMIC achieves very good input matching (S11) of less than -10 dB over a frequency range from 52 GHz to 70 GHz for all states. The measured insertion loss (S21) is less than -4.5 dB for all bits from 54 GHz to 62 GHz and has a nearly identical value of -4.1 dB at the design frequency of 58 GHz.

The third MMIC which is presented in this paper is a multifunctional MMIC. We designed a SPDT switch and a LNA and combined these two circuits at the 50–Ω interface. Thus, we integrated the first two functionalities of a receiver chain in a mm-wave front–end on one MMIC. A photograph of this chip is shown in Fig. 5.

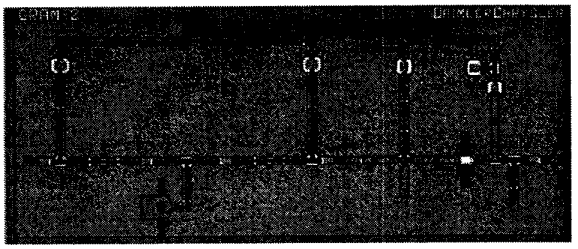

Fig. 5. Multifunctional MMIC (SPDT switch and LNA)

The SPDT switch is on the left side of the picture with the antenna port turned to the left in order to be able to perform 2–port measurements. The active device in the single–stage LNA is a 2x60μm HFET with additive source inductances to improve the stability of the device and to enhance the simultaneous noise and power match at the input port. In Fig. 6, the measured s–parameters of the multifunctional MMIC are depicted. The input matching (S11) is better than -10 dB for 36 GHz to 57 GHz and the output matching (S22) is in a frequency range of 36 GHz to 42 GHz smaller than -10 dB. The gain at 40 GHz is around 5.4 dB including the losses in the switch. As indicated by the k– and the μ–factor which are larger than 1 over the whole frequency band, the circuit is unconditionally stable for all frequencies.

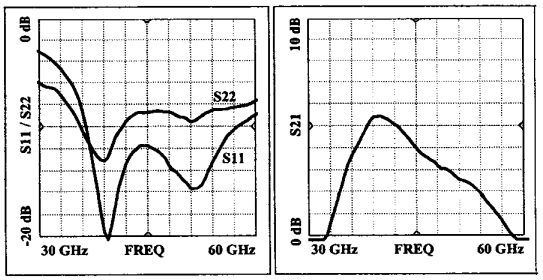

Fig. 6. Measured s–parameters of the SPDT–LNA–MMIC

V. Conclusion

In this paper, we presented a comparison between the RF and noise performance of our InP–based and metamorphic HFETs. Furthermore, PIN diode and HFET devices were successfully integrated on one InP–substrate with the HFET demonstrating a f_T of 155 GHz. Using these two devices, three different MMIC designs were integrated on one wafer: a SPDT switch, a 2–bit phaseshifter and a multifunctional MMIC consisting of a combination of a SPDT switch and a LNA. This integration opens the road for optimized versions of future low–cost and high–performance mm–wave modules.

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