The Impact of Layout and Technology on the DC and RF Performance of AlGaN/GaN HFETs

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Abstract

An analysis of the impact of device layout and technology on the DC and RF performance of AlGaN/GaN HFETs is presented. For this analysis AlGaN/GaN HFETs fabricated on SiC substrate were extensively characterized by DC, small signal RF measurements and RF power measurements. In addition to the characterization results, we present a simulation study on how to improve the performance based on pure device layout variations and we will show which parameters are dominating. Furthermore, we will analyse the electric field distribution in the device and show that a slanted gate profile is beneficial, while the electric field in the gate-drain region can be optimized by the incorporation of a source-terminated field plate (STFP).

Introduction

Gallium nitride-based devices handle very high signal and bias points due to three terminal breakdown voltages of several hundreds of volts, allowing power densities ten times higher than for GaAs. Very high power densities result then in power added efficiencies (PAE) close to the theoretical maximum for each amplifier class. While this is promising, device design and processing key to reaching good DC and RF performance. However, in general it is not clear what dominates the device characteristics. E.g., the contact resistance spread is quite large as shown in [1] and [2]. Does this high spread severely impact device performance or do layout-effects dominate, providing an easier path to performance improvements? Another crucial point is the electric field distribution in the device at high bias conditions. Although the critical breakdown field strength is large in GaN high electron mobility field effect transistors (HEMTs), the electric field distribution needs to be optimized to prevent electric field peaks exceeding the critical breakdown field strength, which will result in an increase in leakage currents, and in the worst case to catastrophic failure.

Device Characterization and Simulation

AlGaN/GaN HEMTs were fabricated by MOCVD on SiC substrate. The epitaxy is completely undoped. The process utilizes a dielectric assisted gate process with an asymmetrically aligned gate with a L_g=500nm and a Γ-gate with various dimensions. Ohmic contacts are based on Ti/Al/Ni/Au/Pt and the source-gate and gate-drain distance are 1.5µm and 4µm, respectively. Measured contact resistances ranged from 0.25Ωmm to 1.5Ωmm. Furthermore, Γ-gates had overhangs to the drain contact of 100nm, 500nm,

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750nm and 1000nm. Devices with 500nm Γ-gate-overhang were also available with and without source-terminated field plate (STFP).

Impact of the ohmic contact resistance: Acceptability of a certain contact resistance level depends on the device itself and its application. AlGaN/GaN HEMTs are devices dedicated to high power RF applications, necessitating a look at their large-signal RF performance. Fig. 1(a) and Fig. 1(b) show load-pull measurement results of devices with a mean value for the contact resistance of 0.25Ωmm and 1.5Ωmm, respectively. These devices had a Γ-gate with 500nm overhang to the drain, a STFP with 2.3µm overhang and 0.8mm gate periphery. For each contact resistance value, two devices were measured. The comparison of these measurement results shows that the contact resistance has absolutely no influence on the large-signal performance of the devices. Both types of devices have a very high saturation power density of 10W/mm, a high linear transducer gain of 17dB and a peak efficiency of 55%. The reason for this is that the contact resistance is not the dominating parameter for the RF performance. To understand this, two dimensional device simulations were performed using SILVACO ATLAS. First, we analyse the contact resistance dependence of output and transfer characteristic. The simulation was performed for contact resistances from 0.1Ωmm to 1.0Ωmm. The results are depicted in Fig. 2(a) and Fig. 2(b). The maximum current in Fig. 2(b) varies in the range of only 10%, whereas the knee-voltage V_k, which is limiting the maximum voltage swing, is not affected by the contact resistance. This explains the good power performance even at high contact resistance level. The weak influence of the contact resistance on power performance indicates a domination of V_k by the bulk resistance which is part of the access resistance. In Fig. 2(a) the simulation result (dashed line) for a reduced gate-drain distance of 3µm is compared with the former gate-drain distance of 4µm. The results show that the reduction of the gate-drain distance by 1µm leads to a reduction of V_k by 1V. This confirms the assumption that the access resistance is dominated by the bulk resistance and gives the possibility to improve the RF power performance by adjusting the layout of the device.

Impact of the gate module layout: Fig. 3(a) shows the measurement results for four different Γ-gate configurations. Each device was separately tuned for maximum output power. What we observe is an increase in the saturation output power from 36.9dBm (4.9W/mm) to 37.6dBm (5.75W/mm) with increasing Γ-gate-overhang. On the other hand, the gain decreases directly with the Γ-gate-overhang due to the increase in the feedback capacitance which becomes clearer when looking at S-parameter measurements depicted in Fig. 3(b). The increase in $|S_{12}|$ indicates a strong increase in the gate-drain capacitance C_{gd}. This observation shows that the Γ-gate has not only the well known effect on the electric field distribution for the DC operation, but also improves the RF performance in terms of maximum power.

Next, we introduce an STFP and see its effect on device performance. The load-pull results depicted in Fig. 4(a) of devices with and without a STFP show an increase in the saturation power from 38.5dBm for no STFP to 39.0dBm for a 2.3μm STFP. The difference between a 1.3μm STFP and a 2.3μm STFP is within the measurement accuracy. To see how the electric field is influenced by the STFP, again device simulations were performed. The simulation result depicted in Fig. 4(b) clearly shows the spreading effect in the electric field distribution caused by the STFP. This spreading of the electric

field causes an increase in the saturation power after introducing a STFP. The peak electric field at the gate foot edge however is shielded from the effect of the STFP by the Γ-gate head. Therefore, we modified the profile of the gate foot to see if we can lower this electric field peak in order to improve the electric field distribution. These simulation results are depicted in Fig. 5. Here we have a look at the lateral part of the electric field, as this part is responsible for the breakdown. The results show a drastically lowered electric field peak in the passivation and the barrier by introducing a slanted gate foot profile, while the channel is nearly unaffected. The lowered field peak will further enhance the RF power performance of the device.

Conclusion

We conclude that device development should always consider layout aspects as equally important compared to optimization of processing steps. The significant impact of layout variations on device performance was clearly shown. Our simulation study showed that the contact resistance is a good example for a layout-dominated device parameter. The device simulations also showed that the design of the gate module has a high capability for improving the RF power performance.

Acknowledgement

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References

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Figures

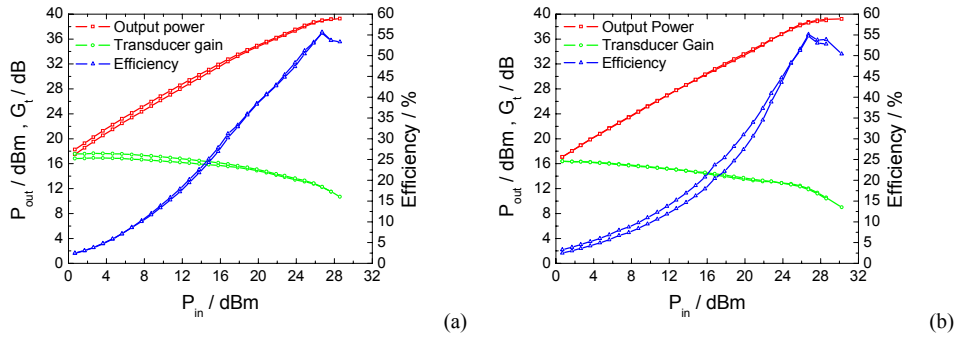

Figure 1. Load-Pull results at f = 2 GHz and deep class AB operation of two devices with a mean contact resistance of 0.25 Ωmm (a) and 1.5Ωmm (b).
Bias: V_{DS} = 50V, I_D = 50mA/mm

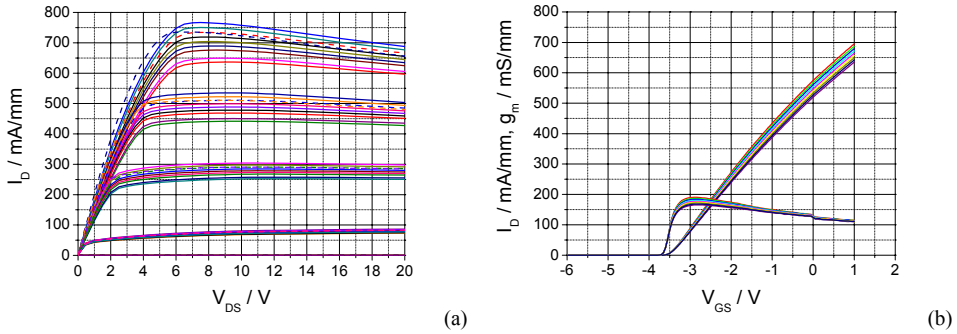

Figure 2. Simulated output characteristic (a) and transfer characteristic (b) at V_{DS} = 50V for various contact resistances. (dashed line) Simulated output characteristic for Gate-Drain distances of 3 μm and a contact resistance of 0.3 Ωmm.

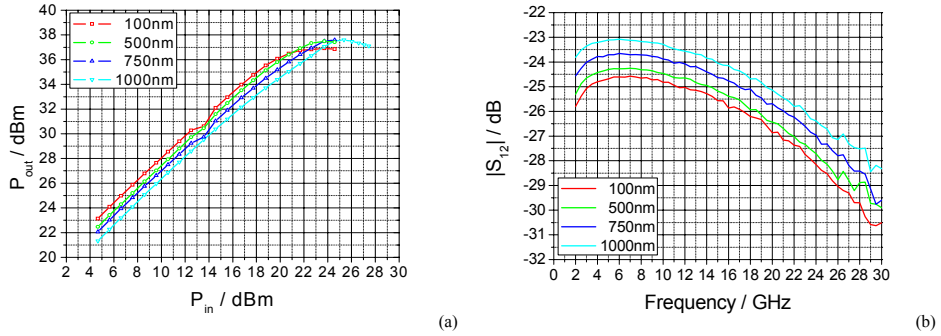

Figure 3. Output power vs. input power for four different Γ-gate configurations at f = 2 GHz and deep class AB operation (a) and related embedded S-parameters.
Bias: V_{DS} = 50V, I_D = 50mA/mm

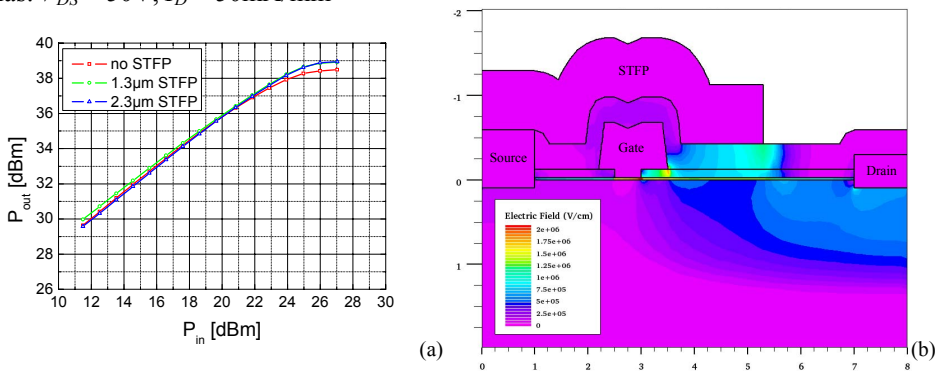

Figure 4. (a) Load-Pull results at f = 2 GHz and deep class AB operation for different STFP configurations. (b) Simulated electric field distribution with STFP and a rectangular gate foot profile. Bias: V_{DS} = 50V, I_D = 50mA/mm.

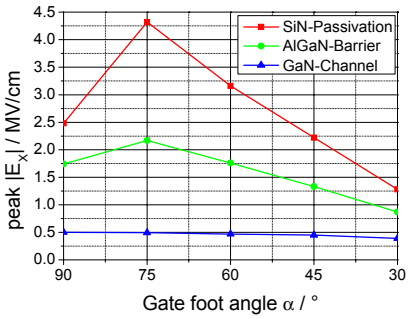

Figure 5. Simulated peak field strength of the lateral electric field at the gate foot edge vs. gate foot profile angle. Bias: V_{DS} = 50V, V_{GS} = −3V