EMMA – A Suggestion for an Embedded Multi-Precision Multiplier Array for FPGAs

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Abstract—A non-monolithic top-down reconfigurable multiplier suitable for embedding in an FPGA structure called EMMA is presented. It is constructed of four individual partitions that can operate as separate multipliers but also concatenate to form a superior multiplier with increased precision and sign handling ability. The number of possible operation modes is limited in order to keep the reconfiguration overhead low. Control signals determine behavior and mode selection, while inactive partitions are disconnected from the supply to save power. EMMA can compute signed two's complement numbers at up to 32×16-bit precision when all partitions are active and concatenated, or up to four separate 16×8-bit multiplications running simultaneously.

Introduction

- **FPGA-based DSP** designs require addition, **multiplication** and MAC
- Implementing multiplication in FPGAs using CLBs is area-inefficient and creates bottlenecks
- More and more hard-wired multipliers are embedded into FPGA structures
- However, only coarse-grain word-length steps are possible with monolithic multiplier blocks
- **Our objectives**: Run-time application-sensitive word-length decision and power trade-off with customized and configurable embedded multiplier blocks
- **EMMA** is a non-monolithic multiplier array with four independent and combinable partitions, reconfigurable multi-precision and sign handling

Basic Multiplication Scheme

$$
\begin{array}{cccccccccc}
 & & & & & \times & a_3 & a_2 & a_1 & a_0 \\
 & & & & & & b_3 & b_2 & b_1 & b_0 \\
\hline
 & & & & & & \overline{a_3b_0} & a_2b_0 & a_1b_0 & a_0b_0 \\
+ & & & & \overline{a_3b_1} & & a_2b_1 & a_1b_1 & a_0b_1 & \\
+ & & & \overline{a_3b_2} & & a_2b_2 & a_1b_2 & a_0b_2 & & \\
+ & & a_3b_3 & \overline{a_2b_3} & \overline{a_1b_3} & & \overline{a_0b_3} & & & \\
+ & 1 & 0 & 0 & 1 & 0 & & & & \\
\hline
 & p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0 &
\end{array}
$$

Fig. 1: Partial products scheme with partial product inversion and correction term, shown for 4×4-bit numbers

- **Modified Baugh-Wooley** scheme for two's complement fixed-point signed numbers
- Parallel/parallel building blocks
- Multiplexer-based exchange of intermediate data
- Sign extension column replaced by partial product negation in perimeter cells and correction term
- Grey shaded areas in Fig. 2 indicate overhead over conventional implementation (Multiplexers, XOR gates and controllable inverters)
- Blocks can be configured to handle **unsigned or signed numbers**
- **Concatenation** to form superior multiplier arrays is possible
- Easy **run-time reconfiguration** with control signals only

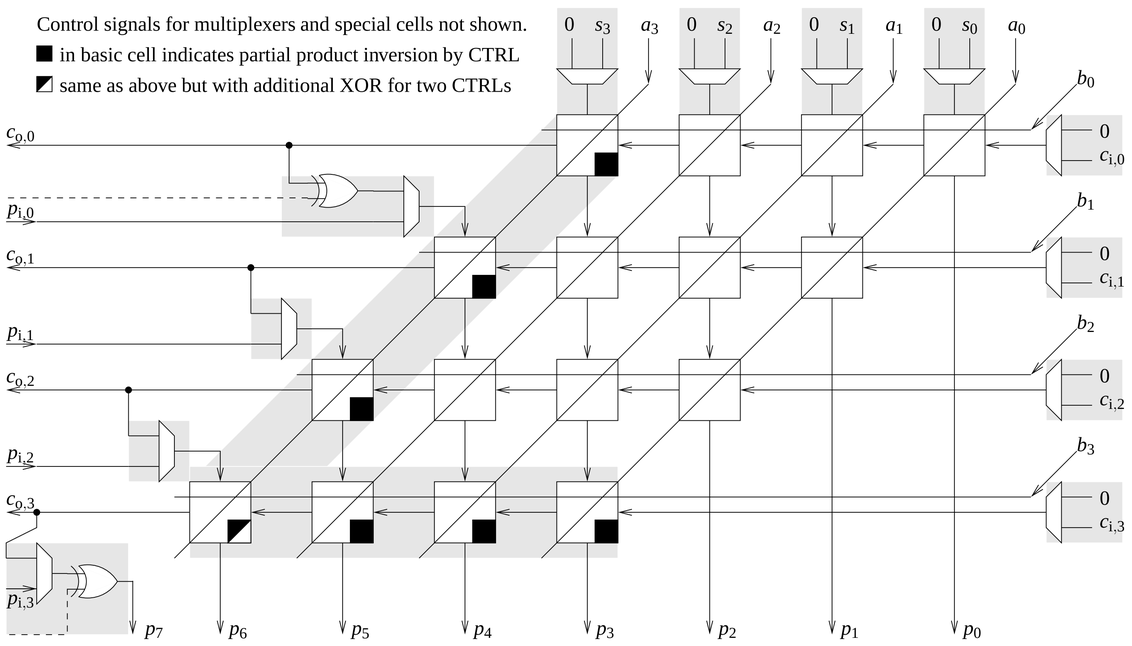


Fig. 2: Modified Baugh-Wooley two's complement multiplier structure

Input Interface

- Input operands A and B split up in MSB and LSB sub-words

$$
\left.\begin{array}{l} A_\mathrm{M} \rightarrow 16\,\mathrm{bit} \\ A_\mathrm{L} \rightarrow 16\,\mathrm{bit} \end{array}\right\} \rightarrow 32\,\mathrm{bit}
\qquad
\left.\begin{array}{l} B_\mathrm{M} \rightarrow 8\,\mathrm{bit} \\ B_\mathrm{L} \rightarrow 8\,\mathrm{bit} \end{array}\right\} \rightarrow 16\,\mathrm{bit}
$$

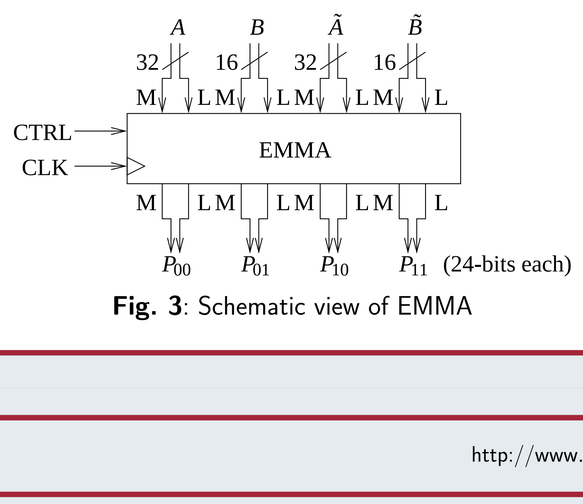


Fig. 3: Schematic view of EMMA

Partitioning Concept

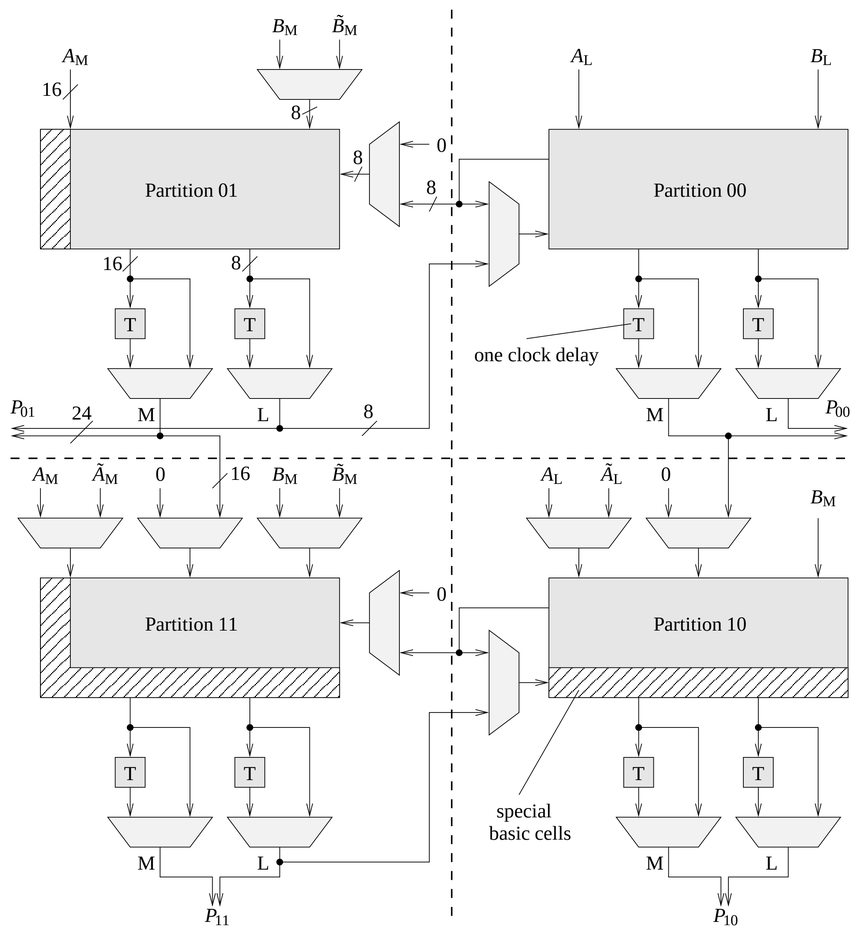


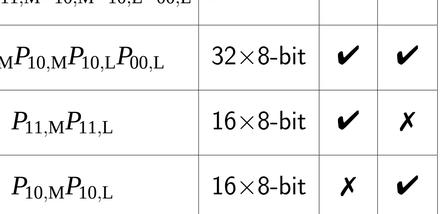
Fig. 4: EMMA is constructed from **four individual partitions**

Mode	Active Partition(s)	Input Words	Result	Precision	Sign	Reg.
A	●● ●● ⟺ 00,01,10,11	$A_\mathrm{M}A_\mathrm{L} \times B_\mathrm{M}B_\mathrm{L}$	$P_{01,\mathrm{M}}P_{11,\mathrm{M}}P_{10,\mathrm{M}}P_{10,\mathrm{L}}P_{00,\mathrm{L}}$	32×16-bit	✔	✔
B	○○ ●● ⟺ 10,11	$\tilde{A}_\mathrm{M}\tilde{A}_\mathrm{L} \times B_\mathrm{M}$	$P_{11,\mathrm{M}}P_{10,\mathrm{M}}P_{10,\mathrm{L}}P_{00,\mathrm{L}}$	32×8-bit	✔	✔
C	○○ ●○ ⟺ 11	$\tilde{A}_\mathrm{M} \times \tilde{B}_\mathrm{M}$	$P_{11,\mathrm{M}}P_{11,\mathrm{L}}$	16×8-bit	✔	✗
D	○○ ○● ⟺ 10	$\tilde{A}_\mathrm{L} \times B_\mathrm{M}$	$P_{10,\mathrm{M}}P_{10,\mathrm{L}}$	16×8-bit	✗	✔
E	●● ○○ ⟺ 00,01	$A_\mathrm{M}A_\mathrm{L} \times B_\mathrm{L}$	$P_{01,\mathrm{M}}P_{00,\mathrm{M}}P_{00,\mathrm{L}}$	32×8-bit	✗	✔
F	●○ ○○ ⟺ 01	$A_\mathrm{M} \times \tilde{B}_\mathrm{L}$	$P_{01,\mathrm{M}}P_{01,\mathrm{L}}$	16×8-bit	✗	✗
G	○● ○○ ⟺ 00	$A_\mathrm{L} \times B_\mathrm{L}$	$P_{00,\mathrm{M}}P_{00,\mathrm{L}}$	16×8-bit	✗	✔
H	●○ ●○ ⟺ 01,11	$A_\mathrm{M} \times B_\mathrm{M}B_\mathrm{L}$	$P_{11,\mathrm{M}}P_{11,\mathrm{L}}P_{01,\mathrm{L}}$	16×16-bit	✔	✗
I	○● ○● ⟺ 00,10	$A_\mathrm{L} \times B_\mathrm{M}B_\mathrm{L}$	$P_{10,\mathrm{M}}P_{10,\mathrm{L}}P_{00,\mathrm{L}}$	16×16-bit	✗	✔

Table 1: Configuration modes for EMMA with respective precision and features. Partitions active: ●; inactive: ○

Upgrades – Outlook

- Adder expansion for **complex multiplication**
- **Radix-4 Booth**-encoded multiplier scheme
- Expand multiplexers to accept **fixed input values** from look-up table
- Include one-hot encoder for **shift operations**



Conclusion

Compared to previous bottom-up reconfigurable multiplier arrays, our new approach called **EMMA** is a **medium-grain embedded multiplier block for FPGAs** that can be partitioned in four separate sub-blocks that are fully functional multipliers themselves. These partitions form various **superior multipliers in different configurations** using a small set of control signals, providing two's complement sign handling and output buffering, respectively. Thus, EMMA can help to realize **multi-precision multiplication** with parallel operation, and power can be saved by turning off unused partitions. Potential applications that can benefit from this reconfigurable embedded multi-precision multiplier array include complex multiplication.

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