Millimeter-Wave Si/SiGe HBT Frequency Divider Using Dynamic and Static Division Stages

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***Abstract*—In this paper, the authors present a fully integrated frequency divider with a divide ratio of 32, using a 0.8 μm Si/SiGe HBT technology. The divider operates at least up to 40 GHz and shows outstanding performance such as broad frequency of operation, compact die area (1130 x 460 μm^2), reasonable power consumption (150 mA at 5 V supply voltage or 110 mA at 4 V with slightly degraded performance) and excellent sensitivity. The integrated circuit combines the advantages of the dynamic topology (first two stages) which includes an additional transimpedance stage and the static topology (last three stages) in order to reach these excellent results.**

I. Introduction

Until recently, millimeter-wave applications were mostly based on III-V technology such GaAs HEMTs. However, the use of such high performance components implies a high cost which makes it incompatible with large-volume production. Since several years, many publications have proved that Si-based technologies such as Si/SiGe HBT were capable of competing with compound semiconductors. However, the improvement of Si/SiGe HBT technologies leads inevitably to a cost increase as well as a decrease of power capability due to a lower breakdown voltage. On the other hand, if appropriate design topologies are chosen, excellent performance can be reached using a technology with reasonable transit frequency (f_T), therefore resulting in a low cost integrated circuit (IC). In this work, a frequency divider with a high divide ratio of 32 operating in the millimeter-wave domain is presented. The IC consumes 150 mA at 5 V supply voltage (or 110 mA at 4 V at the cost of a lower performance) and has a die area of 1130 x 460 μm^2. The circuit uses two dynamic (also called analog or regenerative) frequency dividers with additional transimpedance amplifiers for the first stages. This allows to reach higher maximum frequency of operation. In order to divide the lower frequencies (below 20 GHz), a static frequency divider topology (also called digital) was preferred.

II. The SiGe HBT technology

The circuits use the second generation of the commercially available Si/SiGe HBT process of Atmel GmbH (SiGe2RF) [1]. This technology offers transistors with a $0.5\,\mu$m effective emitter width. A selective collector implant technique improves the RF performance of the transistors and offers devices with f_T = 80 GHz and BV_{CEo} = 2.5 V. Three aluminium metal layers, Metal-Insulator-Metal (MIM) and nitride capacitors are available as well as four types of resistors. The dividers presented here were realized on a $20\,\Omega$cm substrate.

III. Design Philosophy

A. Dynamic Frequency Divider

1) Basic Theory of the Dynamic Frequency Divider: As explained in section I, the first two stages of the 32:1 frequency divider are using a dynamic topology. A block diagram of its basic principle is shown in Fig. 1.

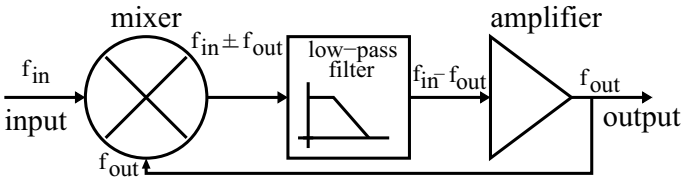

Fig. 1. Principle diagram of the dynamic frequency divider

As it can be seen, the output signal is fed back to one of the two inputs of the mixer in order to generate a division by two. In the block diagram f_{in} and f_{out} are the input and output frequencies, respectively. The mixer output contains signal at the second-order mixing products $f_{in} \pm f_{out}$. Because of the low-pass filter placed within the feedback loop, only the difference f_{in}-f_{out} is amplified and fed back to the mixer input node. Therefore the relation f_{out}=f_{in}-f_{out} is obtained, resulting in f_{out}=f_{in}/2.

2) Dynamic Divider Based on Bipolar Transistors: By using bipolar transistor technologies, it is possible to design the previously described dynamic divider in a single and compact integrated circuit.
The mixing and amplifying functions are both realized using a double-balanced Gilbert cell mixer (see Fig. 2). The input signal drives the lower differential common-emitter pair. The feedback is applied to the upper stage of the mixer via two stages of emitter followers. Because of the inherent

low-pass filter behaviour of the loop, no additional filtering is necessary. In order to obtain the division, all necessary requirements are fulfilled only by using the Gilbert cell mixer and the emitter follower stages. To reach the best RF performance, the transistors are biased at the optimum current with respect to maximum f_T.

Regenerative frequency dividers have higher maximum frequency of operation compared with the digital architecture. However, they suffer from a significantly lower operational bandwidth. In order to improve the bandwidth and the sensitivity of the analog divider, a differential common-emitter transimpedance amplifier stage is added at the outputs of the switching quad. The operational bandwidth is strongly improved due to the generated mismatch within the loop (as demanded by the broadband amplifier theory) and improves the sensitivity as well, due to its additional gain [2].

The common-collector output buffer was designed to drive the input of the next divider stage (or the 2 x $50\ \Omega$ loads during measurement procedure). It receives its input signal from the output of the first common-collector stage, improving the isolation between the output and the feedback loop. The use of simple emitter followers was preferred in order to strongly reduce the chip area and the power consumption [3]. Simulation showed that this topology was perfectly adequate in terms of output power, sensitivity and bandwidth of operation, when combined with the transimpedance amplifier stage in the loop.

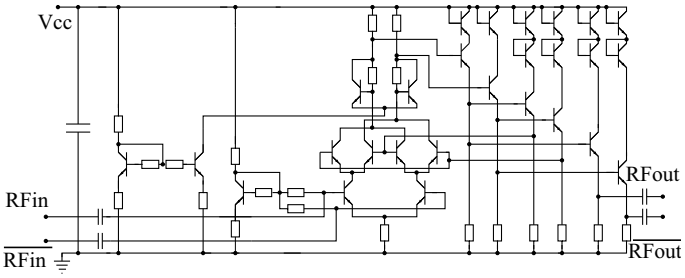

Fig. 2. Complete schematic of the regenerative dynamic frequency divider with transimpedance topology.

3) Layout and Measurements: A picture of the resulting layout is presented in Fig. 3. The chip of the standalone dynamic divider consumes a die area of only 435 x 400 μm^2, mostly dominated by the ground-signal-signal-ground (GSSG) bonding pads.

In order to characterize the 2:1 differential dynamic frequency divider, half of the circuit was connected to external $50\ \Omega$ terminations. The remaining input node was driven with a signal source while the output was detected with a spectrum analyzer. The resulting sensitivity measurements are presented in Fig. 4. The IC consumes only 36 mA at 5 V supply voltage. The measurements could only be performed up to 40 GHz (limit of the signal source). However, the outstanding sensitivity performance at 40 GHz shows that the dynamic frequency divider can operate far beyond this point (simulation predicts a maximum operation frequency of 60 GHz).

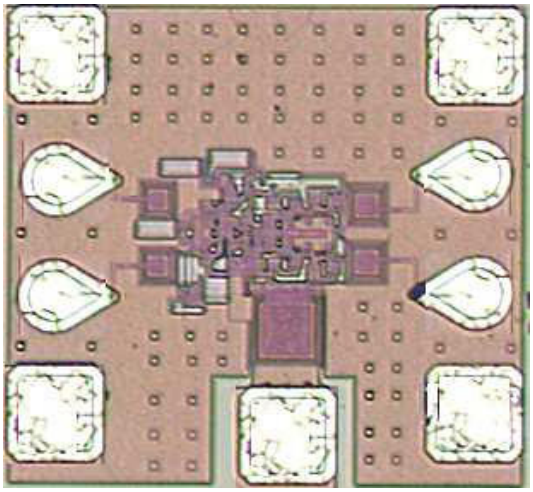

Fig. 3. Chip photography of the 2:1 regenerative frequency divider with transimpedance topology (435 x 400 μm^2)

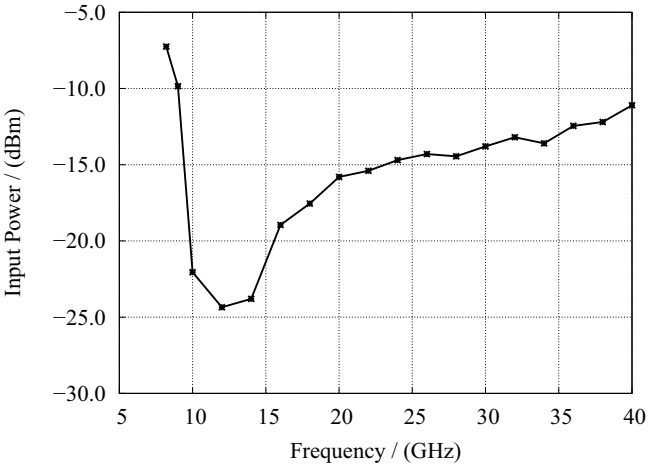

Fig. 4. Sensitivity measurements of the analog frequency divider driven single-ended at a supply voltage level of 5 V

B. Static Frequency Divider

1) Topology of the Static Frequency Divider: In this work, the topology utilized to design the digital frequency divider is the Master-Slave Toggle Flip-Flop (MS-TFF) circuit. The MS-TFF consists of two D-latches, implemented in a standard Emitter-Coupled-Logic (ECL). The ECL is presented in Fig. 5. In order to save a consequent amount of current, a single differential emitter follower stage was used instead of two or more, like widely used in literature [4]. The block diagram of the 2:1 static frequency divider is presented in Fig. 6. From [5] it can be summarized that the smallest available transistor is optimal for high speed operation. Therefore, a transistor with an emitter length of only $1.4\,\mu$m

was chosen. This also allows a low power consumption.

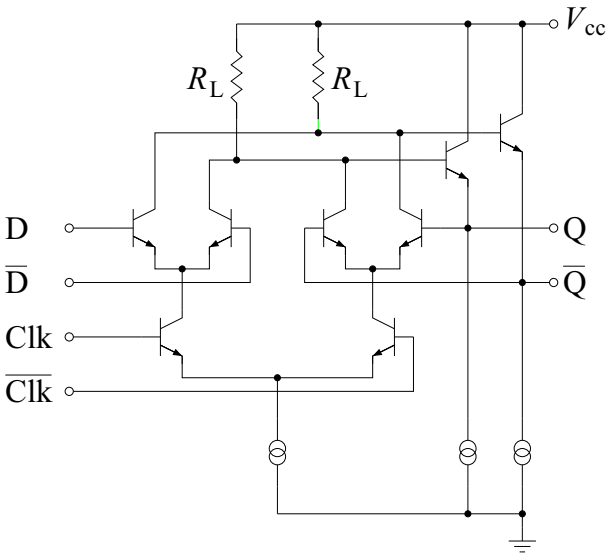

Fig. 5. Emitter-Coupled-Logic schematic

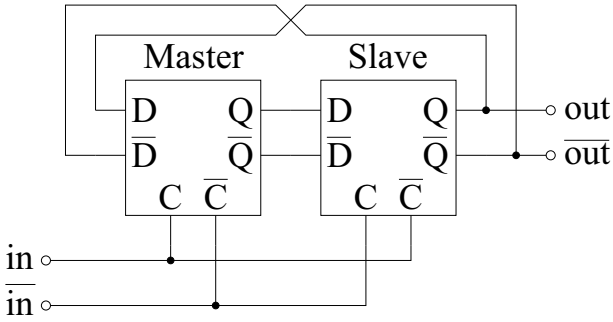

Fig. 6. Block diagram of the 2:1 static frequency divider

The complete circuit schematic of the static frequency divider is depicted in Fig. 7.

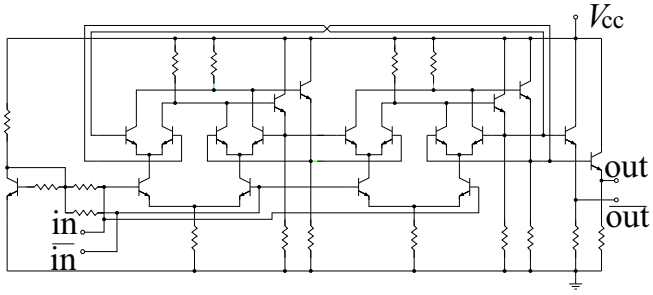

Fig. 7. Schematic of the complete 2:1 static frequency divider

2) Layout and Measurements: A chip photography of the complete 2:1 static frequency divider is shown in Fig. 8.

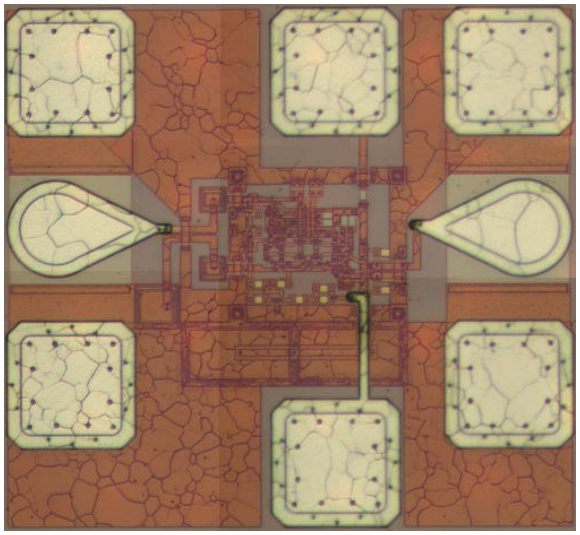

Fig. 8. Chip photography of the 2:1 static frequency divider

In order to ease the characterization of the circuit, a single-ended on-wafer measurement setup was used. This was mediated in the layout by connecting the complementary input port to ground via a capacitor. The inverted output port was left floating. The divider core itself needs a chip-area of only 95 x 73 μm^2. The overall chip size is 360 x 330 μm^2, including the bonding pads. The sensitivity measurements were performed at a supply voltage level of 5 V which is corresponding to the supply voltage of the divider by 32. However, as described in [6], the static frequency divider can operate at 4 V. The IC consumes 26 mA at 5 V supply voltage. The measured sensitivity is presented in Fig. 9.

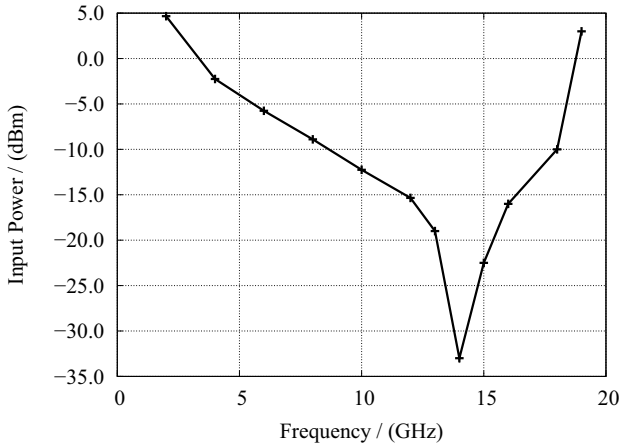

Fig. 9. Sensitivity measurements of the 2:1 static frequency divider driven single-ended

C. 32:1 Frequency Divider

The complete 32:1 frequency divider was simply designed by gathering two dynamic dividers with three static dividers in order to obtain the division ratio of 32. A single supply voltage pad was used to feed the subcells of the divider. A picture of the frequency divider is presented in Fig. 10 in which the single 2:1 dynamic and static frequency dividers can be seen. The circuit has a compact chip area of 1130 x 460 μm^2.

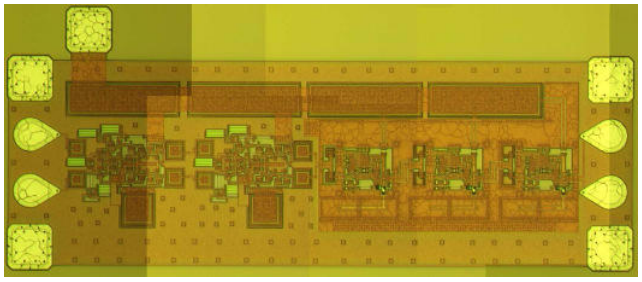

Fig. 10. Chip photography of the 32:1 frequency divider (1130 x 460 μm^2)

The IC consumes 150 mA at 5 V supply voltage. The on-chip sensitivity of the divider is shown in Fig. 11. The measurements were performed in the same way than the standalone 2:1 dynamic frequency divider. The circuit shows excellent performance over a wide bandwidth. The divider was also measured at lower supply voltage in order to improve the ratio $f_{max,op}/P_{DC}$ (where $f_{max,op}$ is the maximum frequency of operation and P_{DC} is the power consumption). At 4 V, the IC consumes 110 mA and still shows excellent performance.

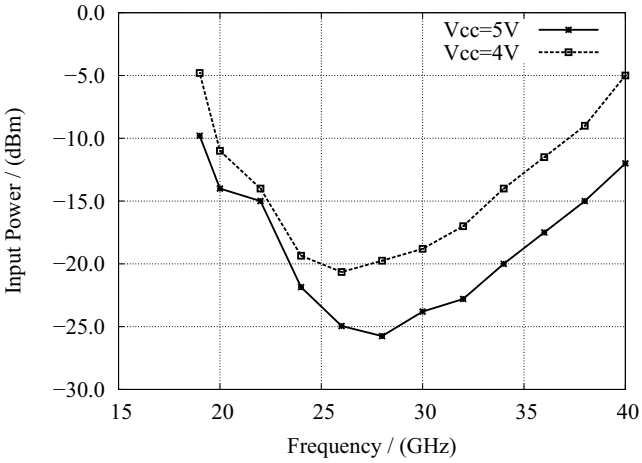

Fig. 11. Sensitivity of the frequency divider with a supply voltage level of 4 V and 5 V

The time domain measurement of the divider with a 40 GHz input signal and a -10 dBm input power in a 50 Ω environment is presented in Fig. 12.

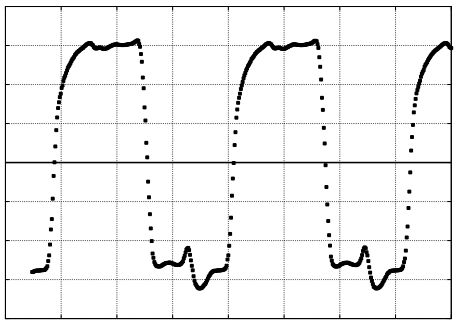

Fig. 12. Time domain measurement of the frequency divider by 32 with an input signal of -10 dBm at 40 GHz. Scale: X:250ps/div, Y:50mV/div

IV. Conclusion

A 32:1 frequency divider using a low-cost Si/SiGe HBT technology was presented. The IC consumes 150 mA at 5 V supply voltage (or 110 mA at 4 V with slightly lower performance) and has a compact die area of 1130 x 460 μm^2. The divider is made of two dynamic frequency dividers with transimpedance amplifier stages and three low power static frequency dividers. The circuit was measured single-ended on-chip and operates at least up to 40 GHz with outstanding sensitivity behaviour and excellent broadband performance. This makes this topology perfectly suited for millimeter-wave applications such as 24 GHz ISM band or Local Multipoint Distribution Services.

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