Improved SQNR and MSA in Incremental $\Delta\Sigma$ Modulators by using a Recuperation Phase

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Abstract—This paper presents a system-level technique that is capable of enhancing the efficiency of high-resolution incremental delta sigma ($I-\Delta\Sigma$) modulators. With little additional effort in circuitry it is possible to make use of a recuperation phase, in which the $I-\Delta\Sigma$ modulator's input is periodically tied to a defined reference. In these phases, the modulator is given time to adjust its residual error to a minimum. This method is capable of increasing the maximum stable amplitude (MSA) as well as the signal-to-quantization-noise ratio (SQNR). Thus, this technique is especially valuable for high-resolution ADCs employing higher order modulators as an increase in these measures directly affects power requirements. The method is analytically derived and exemplarily simulated. Furthermore, a circuit-level simulation in a 180 nm CMOS technology is presented to validate the results.

Index Terms—Incremental $\Delta\Sigma$, Recuperation Phase

I. INTRODUCTION

$\Delta\Sigma$ ADCs are preferred candidates for high-resolution analog-to-digital converters for low to medium speed signals due to their inherent properties like oversampling and noise shaping, which trade speed for accuracy. Nevertheless, these ADCs can not be used in multiplexed environments due to their memory, which is inherent to the system. Incremental $\Delta\Sigma$ ($I-\Delta\Sigma$) ADCs are able to close this gap. These ADCs are operated like their freely running counterparts, but are reset after a number of M cycles. Thus they offer true Nyquist-rate behavior that is a factor of the oversampling ratio (OSR) times lower than the internal sampling speed. Additionally, this type of ADC requires a different digital filter than freely running $\Delta\Sigma$ converters. Theoretically, a brickwall filter can be used for evaluating freely running $\Delta\Sigma$ modulators whereas a resettable reconstruction filter should be used to calculate the digital estimate of the input signal from the digital output sequence of an $I-\Delta\Sigma$ modulator [1]. Though, the efficiency of an $I-\Delta\Sigma$ ADC compared to its freely running counterpart decreases due to its operation in transient mode meaning more OSR is needed for similar SQNR. Consequently, all measures to restore the efficiency of this type of ADC are highly demanded.

In this paper, a technique is presented that makes use of the control-loop-like behavior of the $I-\Delta\Sigma$ ADC by switching off the signal input to a reference after a certain amount of cycles, such that the residual error within the system can be reduced to a minimum. Therefore, Section II introduces the measures that are necessary to evaluate the effect of signal gating and the recuperation phase (RP) method. Section III evaluates the effects of the proposed RP method for an exemplary 3rd order $I-\Delta\Sigma$ ADC designed for the multiplexed digitization of biosignals. In Section IV the circuit-level simulations are discussed and the achieved improvement in performance by

Fig. 1. Operation of a generic $I-\Delta\Sigma$ ADC during the n^{th} Nyquist-rate conversion.

making use of the RP method are shown. Section V concludes the results.

II. BASIC OPERATION OF $I-\Delta\Sigma$ ADCs

The block diagram in Fig. 1 depicts the operation principle of an $I-\Delta\Sigma$ modulator during the n^{th} Nyquist-rate conversion. In case of a discrete-time (DT) $I-\Delta\Sigma$, the continuously running input signal $u(t)$ is sampled by the switched-capacitor (SC) network of the first integrator stage of the modulator. An input sample and hold (S&H) is assumed in the subsequent derivation. Though, it can be omitted as the signal is only slowly varying as compared to the internal sampling speed f_s . Omitting the S&H leads to a modified analog input-to-digital output transfer function, which now shows lowpass characteristic with a slight signal attenuation towards the bandedge of the first Nyquist zone [2].

The $I-\Delta\Sigma$ modulator operates with an internal sampling rate of f_s that is M times higher than the filtered and decimated digital output $D_i[M]$ running at Nyquist-rate f_N . In every cycle k the modulator produces a digital output $d_n[k]$. The modulator can be regarded as an encoder that changes the analog input signal into a digital code sequence $d_n[k]$. Therefore, a digital reconstruction filter with transfer function $h[k]$ is needed to synchronously decode this sequence such that an accurate digital representation $D_n[M]$ of the input is found. Such a digital filter can be as simple as a cascade of integrators (CoI) filter of the same order as the modulator to match the integrator chain of the modulator. Other implementations like the optimal filter [3] are possible at the cost of an increased complexity. The modulator as well as the reconstruction filter are entirely reset after a number of M cycles. The n^{th} Nyquist-rate sample is taken right before the reset.

Fig. 2. 1st order incremental $\Delta\Sigma$ modulator with low-distortion path.

In the following, the basic analysis of an I- $\Delta\Sigma$ modulator is shortly reviewed, which is needed to follow the derivation of the proposed RP method. For the sake of simplicity, the equations are derived for a 1st order modulator, as depicted in Fig. 2. It is assumed that the modulator features a low-distortion path from signal input to quantizer input resulting in a unity STF for inband signals. Thus, the overall transfer function is solely defined by the digital reconstruction filter $h[k]$.

The output of the integrator $r_n[k]$ at the end of the discrete-time instant k in the n^{th} Nyquist-rate conversion cycle can be calculated as

$$r_n[k] = \sum_{m=1}^k (u_n[m] - d_n[m]). \quad (1)$$

It is assumed that the reset takes place during an infinitely small time instant at the end of the last conversion cycle. Furthermore, it is assumed that the input $u_n[k]$ is constant for a whole Nyquist-rate conversion cycle. Under this condition

$$r_n[k] = k \cdot u_n[1] - \sum_{m=1}^k d_n[m]. \quad (2)$$

Assuming stable operation, the output of the integrator is bound at any time instant m during any Nyquist-rate conversion cycle, which leads to the following inequality [4]:

$$\frac{V_{ref}}{k} \geq \left| u_n[1] - \frac{V_{ref}}{k} \sum_{m=1}^k d_n[m] \right|. \quad (3)$$

Here V_{ref} is the reference voltage. Looking at Fig. 2, the decimated and scaled digital output of the n^{th} Nyquist-rate conversion cycle at time instant k can be calculated as

$$D_n[M] = \frac{1}{M} \sum_{m=1}^M d_n[m]. \quad (4)$$

Ideally the decimated digital output sample of the n^{th} Nyquist-rate conversion $D_n[M]$ would match the input sample at the beginning of a Nyquist-rate conversion cycle. This can not be the case for a finite M at the presence of quantization errors, circuit non-idealities and noise. Nevertheless, it is desirable that the error

$$u_n[1] - D_n[M] \stackrel{!}{=} 0. \quad (5)$$

Using equation (4) in (2) matches (5) for $k = M$ and $r_n[M] = 0$. This leads to the conclusion that the quantization error of an I- $\Delta\Sigma$ modulator is visible at the output of the last integrator. Without the loss of generality, this consideration is valid for higher order systems, if the residual error is scaled accordingly by the respective integrator coefficients. This property is e.g.

Fig. 3. Block diagram of the implemented 3rd order CIFF modulator. This modulator is followed by a 3rd order, resettable CoI filter [5].

exploited in extended counting I- $\Delta\Sigma$ modulators. Referring the error voltage at the output of the last integrator to the digital output by dividing it by the respective filter weight and the integrator coefficients, this gives the remaining output-referred quantization error of the ADC.

III. PROPOSED RECUPERATION PHASE (RP) METHOD

A. Improved SQNR by the Recuperation Phase

As in any control system, the impulse response is defined as the reaction of the system's output to external impulse excitation. In the case of the I- $\Delta\Sigma$ modulator, the quantization error as a reaction of an impulse at the input is of interest. Thus, any excitation of the input will lead to a response of the loop such that the quantization error $r_n[k]$ can never reach a steady state, which should ideally become zero.

The idea of the recuperation phase is to use the last part of every conversion for modulator recuperation, during which the modulator can further reduce the remaining quantization error without input disturbance. Therefore, the input of the modulator is disconnected from the signal and tied to a defined voltage for a certain number of cycles. It can be shown that the best results are achieved by tying the input voltage to any of the thresholds of the quantizer. The optimal length of this phase depends on the selected modulator architecture, the order, as well as the aggressiveness of the scaling of the coefficients, which affect the loopfilter transfer function. In order to determine the optimal length of the recuperation phase, a particular architecture has to be chosen, simulated and analyzed.

As an example, we have chosen an I- $\Delta\Sigma$ ADC which is suitable for the processing of biosignals with large dynamic range. An SNR ≥ 94 dB is targeted. Moreover, the ADC should be able to be multiplexed between exemplarily 10 electrodes, each having a signal bandwidth of 10 kHz, which leads to a Nyquist-rate $f_N=200$ kS/s. A 3rd order CIFF $\Delta\Sigma$ architecture including a low-distortion path is chosen using a single-bit quantizer for inherent DAC linearity [5]. The resulting exemplary modulator is shown in Fig. 3. The order of the CoI reconstruction filter matches the order of the modulator. The coefficients are derived with the help of a genetic algorithm as used on www.sigma-delta.de [6]. The used scaling coefficients are shown in Table I. Simulations of this I- $\Delta\Sigma$ show that an OSR of 160 is required to obtain an SQNR of ≥ 100 dB, which is necessary to achieve a circuit noise

TABLE I
SCALING COEFFICIENTS OF THE PRESENTED MODULATOR

a1	b1	b4	c1	c2	d13	d23
0.2393	0.2393	1.0000	0.4309	0.9169	9.7523	8.9423

Fig. 4. RMS error calculated for a sweep across different amplitudes from 0 to the MSA at each cycle for different lengths R of the recuperation phase.

dominated $\text{SNR} \geq 94$ dB. This results in an internal sampling frequency of $f_s = 32$ MHz.

Simulations for 3 distinct values of the RP, where the RP starts R clock cycles prior to the end of every single Nyquist-rate conversion, are performed to see how the output referred quantization error behaves during a single Nyquist-rate conversion cycle. This error is calculated by sweeping the input signal amplitude from 0 to the MSA and calculating the rms value of the output of the last integrator individually (i.e. a representative value of the remaining quantization error) for every time instant $k=40\dots M$, with $M=160$ during every Nyquist-rate conversion cycle. To refer this error to the digital output, it is furthermore divided by a factor $F[k]$ for every individual time instant k to account for the scaling in the CoI Filter. This factor $F[k]$ is only valid for $k > 3$ due to the delay within the filter. It can be calculated for the exemplary modulator as:

$$F[k] = \frac{1}{b_1 \cdot c_1 \cdot c_2} \cdot \frac{6}{(k-1) \cdot (k-2) \cdot (k-3)}. \quad (6)$$

The results are shown in Fig. 4. It can be seen that for the common operation without RP, the quantization error steadily decreases over operation time until the final cycle. Interestingly, the quantization error rapidly drops at the beginning of an RP and then steadily decreases again towards the end of a conversion.

For the three shown distinct RPs with length R as shown in Fig. 4, it should be noted that the new trendline for the quantization error is the same irrespective of the start of the RP. The steady decrease after the sudden drop in the quantization noise shortly after the start of the RP goes along with the modulator running again into limit cycles, after which no dramatic decrease in quantization noise is visible.

To select the optimal time instant for the start of the RP, another disadvantageous effect of this method has to be taken into account, namely the attenuation of the signal power. By tying the input to zero, no signal is fed to the modulator and digital filter during the RP. This means that the effective output

Fig. 5. Effective signal gain α for different RP lengths R .

Fig. 6. Maximum achieved SQNR for different RP lengths R .

signal amplitude is attenuated by

$$\alpha = 1 - \frac{(R-1) \cdot (R-2) \cdot (R-3)}{(M-1) \cdot (M-2) \cdot (M-3)} \quad (7)$$

due to the RP, where R denotes the length of the RP with $R=3\dots M$. Fig. 5 shows the attenuation α of the output signal amplitude due to (7) for different RP lengths. Obviously, the RP length should be kept small to limit its influence on the signal amplitude as circuit noise is not attenuated during the RP in contrast to the quantization noise.

B. Increased MSA by the Recuperation Phase

The MSA of any $\Delta\Sigma$ modulator gives an upper limit for the maximum amplitude of the input signal that can be applied to the modulator before it starts to overload, which leads to a drop in SQNR. Generally, a large MSA is important since for a required SNR, the MSA defines the allowable input referred noise, and the latter sets the requirements on sampling capacitor size, input stage thermal and $1/f$ noise, etc.. Consequently, increasing the MSA directly yields smaller size and power consumption of any I- $\Delta\Sigma$ modulator. By switching off the input signal, the modulator is given time to stabilize as no additional signal power is injected into the system anymore. Therefore, it seems reasonably conclusive that a larger amplitude for the cycles before the RP can be tolerated without driving the modulator into overload towards the end of the Nyquist-rate conversion cycle. Fig. 6 shows the simulated SQNR for different RP lengths. It can be seen that, by allowing an RP, the amplitude for the peak SQNR of the exemplary 3rd order, single-bit I- $\Delta\Sigma$ modulator can be extended by around 2 dB while, as was shown in Fig. 4, also the peak SQNR is simultaneously increased.

Fig. 7. Signal swing of the first integrator at an arbitrarily chosen time instant during conversion

Fig. 8. Signal swing of the first integrator a) without using RP, b) using an RP length of $R=25$, c) using the configuration of b) with the rescaled coefficients shown in II.

C. Increased Signal Swings by the Recuperation Phase

Disadvantageously, the usage of an RP and thus the potential increase of the MSA may result in an increased swing at the output of the first integrator. This integrator swing is transiently illustrated in Fig. 7. As a reference, the output swing without the usage of an RP (blue curve) is depicted. Before the RP starts, both curves are identical. It can be seen that after the the RP starts, overshoots at the output of the first integrator occur (orange curve). Since the RP is again a perturbation at the $I-\Delta\Sigma$ input, the system must respond with its own step response and overshooting. A more precise evaluation by means of a histogram of the integrator swing is depicted in Fig. 8. It should be noted, that an increase in the MSA has already been taken into account in these simulations where no RP is simulated with a normalized amplitude of 0.67,

TABLE II
RESCALED COEFFICIENTS FOR REDUCED INTEGRATOR SWING

a1	b1	b4	c1	c2	d13	d23
0.1197	0.1197	1.0000	0.8618	0.9169	19.5046	8.9423

whereas RP simulations are done with an amplitude of 0.83. The additional swing could cause serious problems like saturation of the integrator Opamps, which may result in a significant drop in performance. Therefore, countermeasures should be considered to reduce the overshoots. An obvious solution is to modify the modulator scaling such that the old swings are restored. The new scaling coefficients and the resulting histogram are shown in table II and Fig. 8c. This can be achieved by increasing the feedback integration capacitor of the first integrator. Thereby, the RP firstly allows to reduce the sampling capacitor and the integration capacitor by approximately 40% due to the increased MSA, as will be outlined in Section IV, but the increased swing requires the integration capacitor to be doubled again. Consequently, the integration capacitor is almost the original size, while the sampling capacitor is still reduced. It should be noted that the load seen by the amplifier is mainly determined by the input sampling capacitor. Therefore, rescaling does not affect power or noise requirements on the OTA to a first order approximation.

D. Multibit Quantization during the Recuperation Phase

Another advantage of the RP is that a multibit quantizer can be beneficially used during the RP. Thereby, the operation during only the RP greatly relaxes the required relative element matching of the DAC elements as compared to conventional multibit designs. First of all this is due to the fact that quantizer decisions towards the end of a Nyquist-rate conversion are less weighted due to the reconstruction filter [5]. Secondly, no signal content is present at the input during the RP. Only a small, signal dependend error is stored at the output of the last integrator, which contributes less harmonic distortion. Therefore it is possible to switch to a multi-bit quantizer during the RP, which leads to an enhanced SQNR as well as to a slight reduction of the overshoots in the first integrator. Table III shows the achievable SQNR by making use of a 4b quantizer, with different relative mismatch values of the multibit DAC unit elements. For comparability, the amplitude was set to -3.5 dBFS for all simulation. By choosing a 4b

TABLE III
SQNR DEGRADATION DUE TO DAC MISMATCH

RP length	0	25	50	75
Mismatch [%]	SQNR[dB]	SQNR[dB]	SQNR[dB]	SQNR[dB]
5.0	100.3	86.0	81.0	76.3
1.0	100.3	108.8	94.4	90.6
0.5	100.3	110.8	106.5	98.7
0.1	100.3	117.8	113.3	103.1
0.0	100.3	117.9	126.4	126.3

quantizer with a relative mismatch as large as 0.5% for an RP of $R=25$ yields an achievable SQNR of 110.8 dB, which is approximately 10.5 dB higher than by just making use of a single-bit quantizer and RP. This could then be used to reduce the required OSR for the target resolution and it mitigates the overshoot issue at the same time while merely increasing the need for more power.

A typical spectrum with and without the use of the RP technique can be seen in Fig. 9. In this spectrum, a 4b

Fig. 9. 4096-point FFT of the decimated output of the I- $\Delta\Sigma$ ADC with and without the use of the RP for an input signal at -3.5 dBFS with a frequency of 20 kHz.

quantizer with a mismatch of 0.5% has been used during the RP to decrease the quantization noise and reduce the overall swing. Note, harmonic distortion is seen due to the operation at the MSA of the modulators.

IV. CIRCUIT DESIGN AND SIMULATION RESULTS

The circuit design for this exemplary modulator was carried out in a 180 nm CMOS technology with a supply voltage of $V_{DD} = 3\text{ V}$ and a common-mode voltage of $V_{CM} = 1.5\text{ V}$, respectively. A slew-rate enhanced folded cascode amplifier in the first integrator stage as well as telescopic amplifiers for the 2nd and 3rd integrator have been used as in [5]. Bootstrapped switches for high-linearity had to be used in the sampling network of the first integrator. The SNR of the circuit-level modulator is mainly determined by the input sampling capacitor C_s , which due to the oversampling nature can be approximated by

$$P_{noise} \propto \frac{k_b T}{C_s \cdot M} \quad (8)$$

according to [7], where k_b is the Boltzmann constant and T is the temperature. For the exemplary design, C_s has been chosen 300 fF to meet the target of $\text{SNR} \geq 94\text{ dB}$, while all other noise sources have been excluded from simulation. By using the proposed RP for a length of 25 cycles and increasing the amplitude by approximately 2 dB, the sampling capacitor size could theoretically be reduced by 37% if only the thermal noise contribution of the input SC network is considered. Consequently, also the integration capacitor of the first stage can be reduced by the same amount. Simulating the fully differential circuit-level implementation of the modulator for a sinusoidal input signal with an input amplitude of $V_{in,diff} = 2.0\text{ V}$ ($\approx -3.5\text{ dBFS}$) at a frequency of 10 kHz using the previously described parameters and coefficients but without the RP method, leads to an SNR of 95.6 dB. Making use of the proposed RP method and switching the input to VCM for the last 25 cycles of each Nyquist-rate conversion allows to increase the input amplitude to $V_{in,diff} = 2.5\text{ V}$ ($\approx -1.5\text{ dBFS}$). This leads to an SNR of around 97.5 dB. This makes it possible to reduce the sampling capacitor C_s by 36% as confirmed by a simulation shown in Fig. 10. This decrease in C_s directly leads to power savings in the first, power hungry integrator and is therefore a great measure of improving the

Fig. 10. Possible reduction of the sampling capacitor C_s due to the RP method.

efficiency of the modulator, which validates the usefulness of this easy to use technique of RPs in I- $\Delta\Sigma$ modulators.

V. CONCLUSION

In this paper, a new system-level technique especially suited for high-resolution, low power I- $\Delta\Sigma$ is presented. The novelty in this design is the RP method that allows to reduce the internal quantization error and increase the MSA at the same time, thereby increasing the efficiency and resolution of a system without excessive circuit effort and without the need for more power in the OTAs. Furthermore, the usage of a multibit quantizer during a recuperation phase is possible which further enhances the efficiency of the modulator and reduces integrator swing. Another benefit for the usage of an I- $\Delta\Sigma$ employing this technique is the fact that preceding circuitry driving the modulator can be deactivated during the RP thereby further reducing the power consumption of a system that integrates such an ADC. Regarding the simulation results including the RP method, the proposed ADC is able to reduce the input sampling capacitor by 36% which directly leads to tremendous power savings in the first integrator and therefore of the whole ADC.

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