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Towards a Highly Flexible Spectrum Sensing Platform for Cognitive Radio Networks

Peter Lohmiller, Ahmed Elsokary, Václav Valenta,
Xiaolei Gai, Andreas Trasser and Hermann
Schumacher
Institute of Electron Devices and Circuits
Albert-Einstein-Allee 45, 89081 Ulm, Germany
{peter.lohmiller, ahmed.elsokary, vaclav.valenta,
xiaolei.gai, andreas.trasser, hermann.schumacher}@uni-
ulm.de

Sébastien Chartier
Cassidian
T/R Modules and MMICs - COEER2
Wörthstraße 85, 89077 Ulm, Germany
sebastien.chartier@cassidian.com

Abstract— Multi-nodal spectrum sensing is a promising approach to robust cognitive radio networks, which provides increased adaptability to database-anchored sharing approaches. Yet its commercially viable implementation requires compact, low-cost, flexible sensing receivers. This paper describes an implementation approach relying on a fully differential 0.25 μm SiGe:C BiCMOS low-noise down-converter RFIC in the front-end, which covers 0.3-6 GHz. Its quadrature outputs are processed in a commercially available baseband processor that combines dual channel 14-bit, 250 MS/s analog to digital converters (ADC) with a Virtex 6 FPGA. The design and implementation status of the system will be described, as well as its validation under realistic noise and interference conditions, sensing white spaces in the UHF TV band.

Keywords—cognitive radio; dynamic spectrum access; reconfigurable RFIC, RF front-end; spectrum sensing

I. INTRODUCTION

Dynamic spectrum access and interference-free use of temporarily and spatially underutilized or unused portions of the radio spectrum are the main features of the Cognitive Radio (CR) network. Compared to traditional fixed radio resource allocation, CR technology represents a radical approach to radio resource management and is often claimed to be the most effective solution to the spectrum scarcity problem. However, besides certain political issues, there are many technical obstacles on the way towards robust cognitive wireless communications [1] [2]. The most challenging issues and key problems are related to a reliable determination of the vacant spectrum (sensing of spectrum holes, white spaces) and to the hardware implementation of a wideband, flexible and highly linear RF front-end. These two issues are addressed in this paper.

Spectrum opportunities perceived by cognitive users vary significantly across different locations and environments [3] [4]. As a result, novel spectrum access strategies based on a geo-location and database access became a very active research topic. Moreover, it has also been shown that the spectrum sensing reliability can be significantly enhanced by a collaborative spectrum sensing [5] [6]. This approach refers to a network, where spatially distributed CR sensing nodes (either mobile or fixed) under different channel conditions achieve higher primary user detection probability by exchanging

localized sensing information via network cooperation. Additionally, spatial diversity and parallel processing of the collaborative spectrum sensing information can, to some extent, mitigate strict and sometimes contradictory sensing requirements on the RF front-end [5].

The lack of experimental studies focusing on an interactive development of both flexible RF front-end architectures and spectrum sensing algorithms under real noise and interference conditions often leads to very optimistic results and unrealistic scenarios. Therefore, development of a usable CR network should always take into account real conditions and limitations of RF and baseband entities. This paper describes the initial stage of the development of an extremely wideband down-converter RFIC and baseband components of the sensing platform as well as development of a spectrum sensing algorithm that are to be employed in a single sensing unit in a multi-nodal spectrum sensing network.

This paper is organized as follows: Section II reviews spectrum sensing requirements and trade-offs, derives limitations and introduces the overall architecture of the proposed sensing platform. Section III describes the different entities of the proposed platform: in detail the fully differential 0.25 μm SiGe:C BiCMOS low-noise down-converter RFIC and the baseband hardware processing unit as well as the developed sensing algorithm. Results of experimental field measurements are given in Section IV. A summary and outlook can be found in Section V.

II. SPECTRUM SENSING REQUIREMENTS AND SYSTEM DESCRIPTION

The overall performance of a sensing unit is a tough compromise between several conflicting system requirements, such as spectrum sensing time, detection probability of primary users, power consumption or size. Such system requirements are application specific (e.g. static spectrum monitoring with no constraints on size and computational power vs. spectrum sensing integrated into a handheld device with limited resources). Therefore, to investigate these performance factors from the point of view of the RF front-end as well as the baseband processing, a very flexible wideband sensing platform has been developed. The overall block diagram of the platform is shown in Fig. 1.

Figure 1. Block diagram of the developed spectrum sensing platform.

The RF front-end is a fully differential direct conversion receiver module followed by a dual (ADC). The I/Q quadrature signals are sampled by 14-bit, 250 MS/s ADCs and are further processed in a Virtex 6 FPGA that performs all baseband operations.

An advantage of the direct conversion receiver module is the simplicity. It is based on only one mixing stage, thus keeping the overall complexity and the power consumption low. Filtering is only necessary before the ADC to prevent aliasing. Hence, a tunable image reject bandpass filter is avoided, which in turn simplifies the highly broadband operation. The RF bandwidth is mainly determined by the antenna, low noise amplifier (LNA) and mixers. By using a current low-cost SiGe technology, low-noise and broadband circuits can be realized, which helps to keep additional costs low, while achieving good RF performance. The RF front-end developed here for the spectrum sensing unit achieves an extremely wide RF bandwidth of up to 10 GHz. This is more than sufficient for the typically observed frequency range in the context of CR, expected to operate below 6 GHz in the future [7]. This wide frequency range makes the designed front-end very suitable for spectrum sensing over a wide frequency range. This is the main difference compared to other reported works, focused on test beds mainly for the TV spectrum or e.g. the 2.4 GHz ISM band [8]. Nevertheless, as the concept of CR is not limited to this frequency range and future standards for other regions might be defined for other parts of the spectrum, the RF front-end designed here can be used also in the IEEE 802.22 radio band, but is not limited to it, which makes it a very versatile test bed.

Since the sensing speed is also an important issue, the RF front-end has to provide a wide IF bandwidth, as this will determine the number of steps needed for analyzing given frequency bands. The designed front-end provides an IF bandwidth of 300 MHz. For initial measurement purposes, the IF bandwidth has been reduced by external low pass filters (LPFs) to 50 MHz in order to reduce the necessary sampling rate. However, this is of course a self-made limitation, which will become unnecessary when using higher sampling rates.

There are further benefits of the direct conversion architecture even from the baseband processing point of view. For instance, as the Nyquist bandwidth of a complex I/Q signal is more than twice that of a real signal, only half of the sampling rate in I/Q branches can be used. However, this is just a relative advantage, given by the need for two ADCs. Moreover, several issues related to DC offset and sideband

images may appear as a result of phase and gain mismatch between I/Q channels. This problem can be eliminated by baseband I/Q correction processing.

Another important issue in wideband direct conversion architectures is the linearity of the LNA, which may become the bottleneck of the whole wideband sensing unit. This is due to the fact that the effect of intermodulation (IM) distortion becomes much more serious than in narrowband radios, since the IM products generated by the LNA may fall into the required band, thereby corrupting the signal of interest even before the down-conversion [2].

III. HARDWARE DESCRIPTION

A. RF-Subsystem

The analog RF hardware consists of an omnidirectional antenna, one RF and two intermediate frequency (IF) baluns, two anti-aliasing LPFs and the RFIC itself (see Fig. 1). With the transformers and IF filters as off-chip components, the system stays highly flexible. As the corner frequency of LPFs is related to the sampling rate of the ADC, different baseband sampling rates can easily be assured by using different filters. On the other hand, this flexibility has negative impact on the overall size of the platform, which is considered to be less important at this development stage than the required flexibility.

As the concept of traditional spectrum sensing implies the lack of local information about the primary users, an omnidirectional behavior of the antenna is important. As a result, a broadband omnidirectional discone antenna covering 0.3-3 GHz was chosen for our platform [9]. On the other hand, this is at the expense of a low, 0 dBi gain.

The unbalanced signal from the antenna is converted to a differential signal by an RF transformer [10] and is then fed to the differential input of the LNA. At the output of the RFIC, two baluns are used to feed the single-ended inputs of ADCs [11]. As the transformers are embedded in a surface mount package, Rogers 4003 printed circuit boards (PCB) were developed and equipped with SMA connectors in order to match them with the coaxial measurement environment.

For the initial measurements, a sampling rate of 100 MS/s was chosen. With an expected IF bandwidth of 300 MHz, an anti-aliasing LPF is needed at the inputs of both ADCs. For this purpose, two ZX75LP-40-s+ LPFs with a bandwidth of 40 MHz were used [12].

The developed RFIC was realized in a 0.25 μm SiGe:C BiCMOS technology from IHP [13]. This technology offers three different modules (SG25H1/H2/H3). Due to the relatively low upper frequency limit of our system (below 6 GHz), the SG25H3 technology has been found a good compromise between the f_t/f_{max} of 110 GHz/180 GHz and the collector-emitter breakdown voltage BV_{CE0} of 2.3 V.

As described, the RFIC should provide a direct down-conversion reception (or a homodyne reception). In the first step, the RF signal is amplified through a broadband LNA, which is based on a fully differential cascode topology with resistive feedback. As the detection of very weak signals is a

key requirement in spectrum sensing, a low overall noise figure is one of the main requirements for the RFIC. A noise figure lower than 2.1 dB together with a gain of 15 dB below 6 GHz have been achieved and are excellent values to attain superior system noise performance. A more detailed description of the LNA as well as detailed measurement results can be found in [14].

Since the spectrum sensing unit has no information about the nature of the signal, it has to be designed for real and complex input signals. Two mixers working in quadrature perform the necessary complex down-conversion. Each mixer is based on a double balanced Gilbert cell, followed by emitter followers acting as buffer stages for a broadband impedance match. The circuit schematic of the designed mixer is shown in Fig. 2.

Figure 2. Circuit schematic of the designed double balanced Gilbert cell mixer.

At an earlier stage of the development, a single standalone mixer was fabricated and characterized. On-wafer measurements have confirmed that the 3 dB RF bandwidth of 10 GHz and the IF bandwidth of 350 MHz can be reached. Within the required frequency range below 6 GHz, the mixer achieves a conversion gain of more than 7 dB. The input-referred 1 dB compression point P_{1dB} was determined at -5.5 dBm.

A complex down-conversion stage requires a precise quadrature local oscillator (LO) signal. In our design, the quadrature signal is generated through a static frequency divider by four, using two D-flip-flops. The D-flip-flop is based on an emitter-coupled logic (ECL), which is in principle a differential current steering-logic using bipolar transistors. The circuit schematic and the block diagram of the divider are depicted in Fig. 3 and Fig. 4 respectively. The outputs of the divider are labeled with small letters, where i_+ and i_- are the in-phase components of the divided LO signal, whereas q_+ and q_- are the 90° out-of-phase signals respectively. This nomenclature is meant to prevent any confusion with the typical naming of digital building blocks in which the output signals are usually named Q_+ and Q_- .

Thanks to the ECL topology, the output power is almost independent of the input power as long as the power of the input signal is high enough to switch currents between transistors. Measurements have shown that the divider can

divide even very low LO signals down to -7 dBm. The output power of the divider is then already sufficient to achieve a conversion gain of the mixers larger than 7 dB.

Figure 3. Circuit schematic of the ECL T-flip-flop divider.

Figure 4. Block diagram of the divider by 4 where q_+ , q_- , i_+ and i_- are the quadrature and in-phase components of the divided LO signal.

The LNA, mixers and divider were finally merged together into a single chip and mounted in a Quad Flat No leads (QFN) package. Afterwards, the QFN chip was soldered on a Rogers 4003 substrate and installed in a metal housing. Pictures of the final module as well as a close-up view of the chip in the QFN package are shown in Fig. 5.

Figure 5. RFIC module and close-up picture of the chip mounted in a QFN package using the chip wire bonding technique.

B. Characterization of the RFIC module

Before performing field measurements, the RFIC module was tested and characterized separately to guarantee a proper function in the later steps. The time domain measurement setup looked very similar to Fig.1. Instead of the antenna, a standard signal generator was connected at the input. Instead of the IF balun, LPF and ADCs, a four channel oscilloscope, which can perform these tasks digitally, was used to observe each output

individually. As the LO generation is not implemented on-chip, a signal source at the LO port was also necessary. For characterization of the amplitude and phase imbalance, I+/I- and Q+/Q- channels were subtracted respectively and plotted against each other. Considering the effect of the analog LPF, a 40 MHz low pass digital filtering was enabled in the oscilloscope. The measurement results are shown in Fig. 6. It can be seen that excellent phase accuracy is achieved. The deviation from the desired 90° is only 0.08° at 20 MHz. At the same time, the difference between peak to peak voltages $V_{pp}(I)$ and $V_{pp}(Q)$ is only 0.19 mV, which is less than 0.2 %.

Figure 6. Output I/Q waveforms showing the amplitude and phase imbalance. $f_{LO}=2.48$ GHz, $f_{RF}=600$ MHz.

After characterizing the module in the time domain, the measurement setup was modified to measure the frequency behavior. The IF bandwidth was determined by sweeping the RF frequency from 100 MHz to 900 MHz and keeping the LO frequency fixed at 2 GHz. Fig. 7 shows the result.

Figure 7. Frequency response of the designed RFIC module.

The designed RFIC module achieves a 3 dB bandwidth of 300 MHz. Sampling such a high bandwidth with a very high resolution at once already requires a high performance ADC, thus preventing the RFIC from being the bottleneck of the whole system in terms of sensing speed. As the LO frequency is in the center of the desired RF signal, a highly symmetric conversion gain is desired for high- and low-side LO injection. Assuming a spectrum analyzer's measurement inaccuracy of ± 1 dB, the RFIC's conversion gain is considered symmetric within the whole 3 dB bandwidth.

Furthermore, since it is very difficult to implement a wideband tunable preselection RF filter, a lot of strong interferers are expected at the input. As a result, high linearity of the RF front-end is required. Measurements of the input referred 1 dB compression point P_{1dB} reveal a value of -24 dBm. By cascading P_{1dB} of the mixer and the LNA, (P_{1dB} of -5.5 dBm and -18.5 dBm respectively) a theoretical P_{1dB} value of -22.5 dBm can be expected. This is very close to our measurement results and it shows that to get better overall P_{1dB} performance, both components would need to be improved. A more meaningful parameter for practical sensing applications is the third order intercept point (IP3) as it determines the Spurious Free Dynamic Range (SFDR). IP3 measurements will be carried out during the next validation step in the future.

C. Baseband Subsystem

Another crucial challenge in CR networks is a continuous monitoring and real-time baseband processing of very wide frequency bands. In our platform, an IF wideband signal of up to 300 MHz can be delivered by the RFIC down-converter. It is obvious that analyzing such a wideband signal requires fast and high resolution ADCs. The ADC used in our platform offers a dual channel sampling speed of up to 250 MS/s with a resolution of 14 bits. Therefore, complex IF I/Q signals of up to 250 MHz can be analyzed and hence, for example, the whole UHF TV band can theoretically be analyzed in only two iteration steps.

Having such flexible system, different spectrum sensing approaches will be evaluated on the designed platform in the future. However, to validate the sensing platform at the beginning of the development, IF I/Q bandwidths have been limited to 50 MHz. The sampled I/Q signals were fed to the FPGA Virtex 6 platform, where a spectrum sensing algorithm based on the energy detection was implemented. The following baseband operations have been designed: Serial Fast Fourier Transformation (FFT), averaging, and decision execution. A block diagram of these baseband operations is depicted in Fig. 8. Corresponding baseband parameters are summarized in Tab. I.

Figure 8. Block diagram of baseband processing steps.

TABLE I. SUMMARY OF BASEBAND PARAMETERS

Parameter	Value
IF bandwidth	61.44 MHz
I/Q sampling rate	61.44 MHz
FFT size	256
Averaging	Variable
Time per sweep	Variable (depends on averaging)

The I and Q channels are processed by a 256 point FFT, which results in the frequency resolution of 240 kHz. A radix-4 Single-path Delay Commutator (SDC) pipelined FFT was used,

known to utilize less multipliers, with the drawback of occupying more memory on the FPGA. This approach is comparable to other FFT implementations in [15].

The FFT was optimized for a high clock frequency by further pipelining of all adders and complex multipliers. Twiddle factor calculation was done beforehand and stored in block ROMs prior to the synthesis, so as to save the calculation time by only reading twiddle factors from a memory. Progressive FFT bit-width was used to reduce the size of adders and multipliers, while keeping the accuracy (SQNR) minimally affected. The algorithm has been optimized for the 14-bit input of the ADC. The design is fully pipelined, capable of a streaming input. The FFT was followed by a bit reversal circuit implementation similar to [16]. Averaging was done on two levels: average of M bins, followed by spectral averaging over N spectra for the whole 256-point transforms, as shown in Fig. 9., where the input is given to a shifting unit, which does a logic shift right of the input (equivalent to division by powers of 2) by a number of bits given by the control unit. This scheme of averaging eliminates the usage of a divider, which significantly saves computational resources. The averaging is flexible to accommodate any number of spectral averages giving the user the options for trading off detection time versus detection capability.

Figure 9. Accumulator based spectral averaging.

The number of segments is always preferred to be in the power of two, which reduces the division by N to a simple bit shifting operation, thus saving hardware costs.

The energy detection problem was modeled as a testing problem of hypothesis H_0 and H_1 :

$$y = \begin{cases} w(t), & H_0 \\ s(t) + w(t), & H_1 \end{cases}$$

where $w(t)$ is the Additive White Gaussian Noise (AWGN), $s(t)$ the detected signal, and $y(t)$ the received signal. Evaluation of this hypothesis is done by comparing the averaged RX power level with a predefined threshold. The value of the threshold is determined by the noise level in the AWGN channel.

IV. EXPERIMENTAL FIELD MEASUREMENTS

Fig. 10 shows the final spectrum as a function of time obtained during an experimental measurement trial under indoor environment. The LO input frequency was chosen as 2.552 GHz, so that the IF bandwidth shown in the spectrogram corresponds to the RF bandwidth 607-668 MHz. Two DVB-T channels with center frequencies at 626 MHz and 650 MHz, can be clearly identified.

Figure 10. Spectrogram depicting the activity in the down-converted UHF band over 260 iterations (corresponding to 140 ms), $N=128$.

An instantaneous measurement result is depicted in Fig. 11, showing the noise floor of -77 dBm. As a result, the DVB signals can be clearly distinguished. The number of spectral averages selected is 128, bin averaging is varied for $M=0,4,8$ bins. A smoother measurement can be observed by increasing the number of bins.

Figure 11. Influence of the bin averaging for $M=0,4,8$ bins.

In the last validation step of the sensing platform, a theoretical evaluation of the probability of false alarm and detection was carried out for a 5 MHz QPSK modulated signal. This scenario enables to evaluate the designed algorithm in a more general case, regardless of RF front-end performance. For this purpose, a 5 MHz QPSK modulated signal processed by an AWGN Simulink channel model has been used to model different SNR values. This signal was analyzed by the proposed algorithm running on the FPGA and the output was recorded and processed by Matlab to calculate individual probabilities. 1550 frames have been analyzed for each SNR value. The threshold value has been determined as the optimum tradeoff between the probability of false alarm and detection for the individual SNR value. Corresponding results are depicted in Fig. 12.

It is evident that this evaluation approach, where the whole 50 MHz channel is assumed, has certain limitations and cannot be directly applied to the evaluation of detection and false alarm probabilities of 8 MHz DVB-T channels, however, it provides a clear performance advantage of two different averaging modes of the designed detector.

Figure 12. Probability of detection and false alarm as a function of SNR (with and without the proposed averaging method).

As shown in the FPGA utilization summary in Tab. II, the algorithm can be implemented on a much smaller FPGA. However, the operating clock frequency may vary.

TABLE II. FPGA UTILIZATION SUMMARY

Element	Number	Virtex-6 Utilization
Slices Occupied	1264	3.00%
Max. clock freq.	180 MHz	--
DSP48 units	40	5.00%
LUTs	3396	1.00%

V. CONCLUSION

In this paper, we present the current development status of a novel spectrum sensing platform, recently implemented at Ulm University. For the sake of demonstration, the experimental implementation of an energy detector was carried out and validated under realistic conditions. Main trade-offs between the achievable probability of detection and sensing time were discussed here along with limitations and possible improvements of this approach.

It has been shown that the designed platform offers an extremely high degree of flexibility in the RF front-end as well as in the baseband processing unit, which makes it very attractive for practical evaluation of different types of spectrum sensing algorithms in a very broad frequency range. The latter is the main focus of future research, which is oriented on the development of a wideband multi-nodal distributed sensing network with different algorithms running at individual sensing nodes.

From the RF front-end point of view, future development directions will be dealing with linearization, which was identified as the most critical issue in wideband receivers, with

a tremendous impact on the system performance. The latter includes not only the linearization of for example individual receiver building blocks, such as LNA or mixers, but also a re-evaluation of the whole receiver architecture. An up-down-conversion approach, using real up-conversion to a high IF followed by a complex down-conversion may provide better performance at the cost of complexity. To facilitate future field tests, integration of the LO generation unit is envisioned as well.

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