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*IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM),
30. September – 3. Oktober
2012 in Portland, Oregon*

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MEMS Module Integration into SiGe BiCMOS Technology for Embedded System Applications

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Abstract — The introduction of radio frequency micro-electro-mechanical systems (RFMEMS) as a monolithic option into state-of-the-art Si/SiGe BiCMOS foundry processes has paved the way for single chip radio frequency microsystems at millimeter wave frequencies. Deep silicon substrate etch techniques have also been developed to prevent high substrate losses which help in achieving high performance passive components at mm-wave frequencies. Using the same process techniques, realization of highly efficient on-chip antennas has become feasible, which in the millimeter-wave range no longer come with a hefty chip real estate penalty.

In this paper, the current status of embedded BiCMOS+MEMS technology development is presented. Reconfigurable circuits using embedded RFMEMS switches and mm-wave transceivers with on-chip antennas are also discussed as application examples.

Index Terms — Silicon bipolar/BiCMOS process technology, RFMEMS, RFMEMS switch, On-Chip antennas, mm-wave ICs, reconfigurable ICs.

I. INTRODUCTION

The combination of MEMS and semiconductor technologies has been a very attractive research topic for the last decades. Several methods in literature have been suggested to integrate MEMS components into semiconductor die using hybrid and monolithic processing techniques [1-5]. The processing techniques in MEMS and semiconductor industry are similar but low throughput, repeatability issues and low yield of MEMS processes makes this combination very difficult. Moreover, the high yield requirement which allows for decreasing cost in semiconductor technologies is highly threatened by integrated MEMS devices. All these bottlenecks force the semiconductor industry to find an intermediate solution, such as heterogeneous integration. In the last few years, chip stacking using Through-Silicon-Vias (TSVs) and interposer techniques has become popular to combine different substrates. By

using these methods, different products which include several MEMS components are already on the market. Although the interconnect losses from these integration methods are acceptable for frequencies below 40GHz, the interconnect losses become much more important for 60GHz and above, and can define the overall system performance. Due to the significant effect of interconnect losses in interposer or chip stacking techniques, embedded integration of RF-MEMS components into semiconductor technologies is necessary especially in 60GHz or higher frequency applications. Such fully embedded solutions at higher mm-wave frequencies become attractive as applications with substantial market volume, such as personal area networks at 60GHz, automotive radars and E-band communication circuits in the 76-81GHz range, or security radar/imaging at 94, 120 and 140 GHz.

In the realm of group III-V semiconductor technologies, monolithic inclusion of RFMEMS is also not particularly new, but again met a slow uptake. An MMIC combining two GaAs HEMTs with two Ohmic contact RFMEMS switches was previously reported in 2001 [6]. More recently, the European MEMS-4-MMIC project conducted a comprehensive research on the monolithic integration of RFMEMS components into a commercially available GaAs MMIC technology [7]. More commonly, however, adaptive and reconfigurable microsystems involving RFMEMS have been implemented using a multi-chip approach see e.g. [8].

Latest developments in SiGe technologies provide heterojunction bipolar transistors (HBTs) for aforementioned mm-wave applications with an f_{max} of up to 500GHz [9]. Next generation high frequency systems also need to fulfill special requirements such as multi-band/wide-band operation and phased-array antennas. These smart systems can be made feasible by the extension of BiCMOS processes with different additional MEMS modules, which is extensively studied in this paper.

II. RFMEMS SWITCH INTEGRATION

The IHP 250 nm Si/SiGe:C BiCMOS technology SG25H1 offers HBTs with $f_T=180$ GHz and $f_{max}=220$ GHz, and a five-layer metallization stack with 3 thin and 2 thick metals. The full technology specification is available at [10, 11].

The IHP RFMEMS integration combines RFMEMS functionality with the performance and circuit complexity of a Si/SiGe BiCMOS process. It relies on layers and processes already available in the baseline technology, adding little overhead. The bottom three metallization layers of the layer stack are used to implement the monolithically integrated RFMEMS switches. The capacitive switch is built between the Metal 2 (M2) and Metal 3 (M3) layers, while high-voltage electrodes are formed using Metal 1 (M1). The schematic cross-section is shown in Fig. 1. The movable membrane uses a stress-controlled variant of the M3 layer - stress control is very important in RFMEMS membranes as a warping membrane will modify switching voltages as well as capacitances in the up- and down-states.

Fig. 1. Schematic cross-section of the RFMEMS capacitive switch in IHP SG25H1 technology.

A thin $\text{Si}_3\text{N}_4/\text{TiN}$ stack, part of the BiCMOS metal-insulator-metal (MIM) capacitor, forms the switch contact region. This configuration creates a height difference between the high-voltage electrode and the signal line. The latter acts as a mechanical stop for the membrane, it will not touch the high-voltage electrodes, eliminating the need for another dielectric layer there, and avoiding the risk of dielectric charging of the actuation electrode dielectric, which is the leading cause for premature failure in electrostatically actuated RFMEMS [12].

To investigate the reliability of the manufactured switches, both mechanical displacement (via Laser Doppler Vibrometry) and switch-off times were assessed. Twelve switches were actuated in parallel by

an actuation voltage of 45 V, with a symmetric rectangular waveform of $f_{rep}=33.3$ kHz. Measurements were performed every 10 minutes, or 20 million cycles. The measurements were stopped after 50 billion cycles without failures, and with very stable displacement and switching time [13].

The high-frequency switch performance is assessed using vector network analysis on-wafer up to 110 GHz. As the equivalent circuit of a capacitive shunt switch is approximately a series-resonant LC combination, the series inductance can be conveniently used to tune the isolation behavior (switch in the down-state) for best performance in a particular frequency band. The main parts of the series inductance come from the movable membrane itself and the additional series inductance to tune the resonance frequency. Every change on the movable membrane also changes the mechanic behavior of the switch. Therefore, only the additional inductance, which has no effect on mechanics of the system, is tuned for the maximum frequency at the desired frequency. This is shown in Fig. 2, which compares the isolation and insertion loss of switches optimized for 30, 50, 80, and 100 GHz operation. Such tuning allows using the same mechanics for all different frequency bands. The switches provide an insertion loss better than 0.3 dB and isolation in excess of 25 dB even at 100 GHz [14].

Fig. 2. Measurement results of insertion loss and isolation as a function of frequency for four designed variants of the RFMEMS switch [14].

a) RFMEMS Switch driver

One of the main issues in using electrostatically actuated MEMS in high-frequency ICs is the rather high actuation voltage, which, at the typical 25-50 V, far surpasses the breakdown voltages of active devices (BJTs or FETs) in the signal path. External voltage supplies add cost, and may not be possible for space

reasons in the first place. Fully embedding the DC-to-DC converter in the RFIC is preferred. The most critical parameter for such circuits is the well-to-substrate breakdown voltage. Several studies were published describing high-voltage driver circuits using DMOS or other dedicated high-voltage MOS transistors [15, 16] typically not available in an RF-BiCMOS process.

Here, a high voltage (HV) PMOS transistor was created from the standard 2.5V PMOS cell by increasing the lateral distance between the n-well and the surrounding p-well regions, enhancing the n-well to substrate breakdown voltage from 11 to more than 50 V. A Dickson type, 20 stage charge pump (CP) circuit was then realized to create the on-chip excitation pulse. The charge pump is driven at 2.5 V with an optimum clock frequency of 20 MHz, generated on-chip using a ring oscillator.

Fig. 3. Annotated chip micrograph of the integrated high voltage driver unit, along with the RFMEMS switch (upper right). Measurement results (bottom) of the switching time of RFMEMS switch using on-chip high voltage driver.

Fig. 3 shows the micrograph of the realized driver unit along with an RFMEMS switch. The rather large footprint of the charge transfer block will be reduced by more than a factor of 10 in an upcoming re-design. Fig. 3 (bottom) also shows the switching performance of the switch for different supply voltages applied to the V_{dd} of the oscillator. The switch can be actuated using the HV generation circuit with a switch-on time less than 6 μs at 40 V V_{out} . For the same actuation voltage applied from a pulse generator (rise time < 10 ns), the switch-on time is around 4 μs . It is obvious that the rise time of the charge pump has no significant effect on switch-on time of the RF-MEMS switch.

b) Packaging

As the RFMEMS switches operate reliably even in an ambient environment, a specific environment was not considered (i.e. low-pressure or hermetic) and a non-hermetic packaging solution was developed. Such non-hermetic packages don't degrade the RF performance as high as the hermetic ones, therefore provide better RF performance. The package can encapsulate an individual switch, or also a complete circuit. The packaging process starts with bonding a silicon and a glass wafer. The silicon wafer is etched to create frames which define the inside cavity, with the glass wafer forming the lid. The individual packages are then separated and put in place, using Benzo-cyclo-butene (BCB) as an adhesive. BCB allows a curing temperature below 300 °C, without adverse effects on the BiCMOS or RFMEMS components [14]. Fig. 4 shows the result of a packaging process, both for an individual switch and a packaged reconfigurable voltage-controlled oscillator (described further down).

Fig. 4. Micrographs of a packaged single RFMEMS switch (left) and a packaged reconfigurable voltage controlled oscillator (VCO) with two RFMEMS switches (bottom right). The picture at the top right shows an SEM micrograph of the unpackaged VCO.

c) Reconfigurable millimeter-wave circuits

Reconfigurability may allow a mm-wave system to assume different functions. For instance, a system could work as a car-to-infrastructure transceiver at 60 GHz while a vehicle is in motion, but act as a close range radar system at 79 GHz when slow-moving or parking. Likewise, a system could be optimized to work in both bands of the E-band “wireless fiber” allocation now becoming increasingly popular for LTE base station backbone links. Or, reconfigurability could result in commodity building blocks for mm-wave systems, addressing a wide spectrum of frequencies or applications. Up to 60 GHz, CMOS switches are still

provide enough performance and reconfigurability using high-end CMOS technologies [17]. At higher frequencies, however, RFMEMS switches become much more attractive, as we have seen.

The circuits described in the following use an RFMEMS switch to modify the electrical length of a transmission line, depending on the state of the switch capacitance. In the examples below, the capacitance changes between 22 fF (up-state) and 220 fF (down-state), while the series inductance in the down-state is approximately 21 pH.

The first example is a Colpitts-type differential VCO [18]. As Fig. 5 (left) shows, it includes a differential common base buffer stage and a divide-by-64 block on chip, facilitating measurements of phase noise as well as transient frequency switching behavior. The base inductors are modified by the introduction of the two RFMEMS switches.

Fig. 5. Left - schematic diagram of the mm-wave Colpitts oscillator, including RFMEMS switches. Right - chip micrograph.

In the absence of a design kit, the switch parameters were obtained by electromagnetic simulation. Fig. 5 (right) exhibits a chip micrograph, emphasizing the large size of the RFMEMS, posing a layout challenge. The overall chip dimensions, however, are still reasonable.

Fig. 6 shows the VCO tuning characteristics. The left hand picture was measured in the lower band, with the RFMEMS switch in the up-state, while the right hand graph shows the upper band, with the switch in the down-state.

Fig. 6. Tuning ranges of the band-switchable VCO in simulation and measurement: left - RFMEMS switches in the up-state; right - switches in the down-state.

Compared to simulations, the tuning range in each band is shifted downward, a result of additional switch parasitics not yet accounted for (e.g. via inductances). This can be easily remedied. The output power at mid-band is 4 dBm for the lower, and 5 dBm at the upper band. Phase noise was assessed at the divide-by-64 port, and determined to be -82 dBc/Hz at 1 MHz offset in the low band, and -84 dBc/Hz in the high band, after correcting the shift introduced by the divider (36 dB). Output power and phase noise are very comparable to the original design without band switching. The switching speed is a strong function of the applied actuation voltage. At 40 V, the oscillator reaches its steady state in less than 5 μ s.

Circuits can also be reconfigured between bands with a significant frequency offset. This is shown in the next example. It is motivated by the fact that short range radars for automotive applications now employ two different bands – around 24 and 79 GHz. The low-noise amplifier shall address both bands, using a switched resonant load [19].

Fig. 7. 24/77 GHz band-switched low noise amplifier. Left - schematic diagram, Right - chip micrograph [19].

The LNA has a two-stage cascode topology, see Fig. 7 (left). The input circuit has been chosen such that it provides reasonable power and noise match both at 24 and 79 GHz. Thus, only the loads have to be switched. The loads are resonant circuits formed by thin-film microstrip transmission lines.

The fabricated circuit (Fig. 7, right) showed experimental results quite close to simulation, and featured 25 dB gain with 4.3 dB noise figure at 24 GHz, and 18 dB gain with 8.3 dB noise figure at 77 GHz (accounting for a 2 GHz shift in the passband to lower frequencies) [19].

III. LOCALIZED BACKSIDE ETCH (LBE) MODULE

In the last decades, substrate etching technique has been investigated as a promising technique for achieving high performance passives at mm-wave frequencies. Performance analyses have been done to reveal the effect of the substrate [20 – 22]. Related works show that using substrate etching technique, quality factor of inductors can be improved and self-

resonance frequencies can be shifted to higher frequencies [23].

In IHP's LBE module, silicon back-side etching process was performed with an additional mask layer and the module is now available in all IHP technologies.

Si substrate was removed by deep silicon plasma etching from the backside of the wafer until the process reaches the first Pre-Metal-Dielectric SiO₂ (PMD) layer. A generic cross-section of the proposed process is given in Fig. 8 [24].

Fig. 8. Illustration of substrate etch process [24].

a) LBE processed inductors

Prototype inductors are realized using IHP's 0.25 μm SG25H1 process to demonstrate the performance improvement of substrate etch technique. The process has 5 layer aluminum metallization with a substrate resistivity of 50 Ωcm . The top-aluminum layer has a thickness of 3 μm which is suitable for inductor structuring.

Cross-section views of the inductor after etching of the silicon and a diced inductor after backside etching are given in Fig. 9. Silicon under the inductor was etched up to the back-end oxide layer. The observations on the remaining 10 μm back-end oxide proved that the deep-silicon etching process does not cause any stress problems on the remaining membrane. Several types of inductors are designed to compare the substrate effects. Single turn low-value inductors are the most important types due to their very low inter-winding capacitance which limits the series self-resonance frequency of inductors. Fig. 10 shows the quality factor curve of 1.9 nH and 10 nH inductors respectively for both with and without silicon [24]. The performance improvement after substrate etching can be obviously seen in Fig. 10. The simulation/modeling data of the silicon etched inductors are also given in the same figure.

Fig. 9. SEM Cross-Section (Left) and the diced view (Right) of silicon etched inductors.

Fig. 10. Quality factor curves of inductors with and without silicon [24].

b) On-chip antennas and THz resonators

As the frequency of operation increases, interconnects between board (or package) and chip are increasingly difficult to realize. On the other hand, the geometric dimensions decrease, which makes realizing radiating structures directly on-chip increasingly attractive. Beyond 100 GHz, it rapidly becomes the most viable option for getting signals off chip [25].

The substrate etch module provides not only low-loss interconnects but also mm-wave on-chip antennas and resonators/transducers for many applications. Fig. 11 shows different examples which were realized by using the backside silicon etch module. Using this module, realization of high-gain mm-wave on-chip antennas and different types of transducers/resonators are possible. Fig. 11 also demonstrates that the dicing procedure of the substrate etched dies is reliable and handling of the diced chips is possible after the dicing process.

Fig. 11. 120 GHz on-chip antenna (backside silicon is removed). 120 – 240 GHz transducers using backside etch technique.

The combination of complex Si/SiGe microwave circuits with on-chip antenna structures had been investigated earlier (e.g. [26]) and proven to be entirely feasible, with low cross-talk between the antenna and susceptible structures on the same die (especially spiral inductors). The referenced work, however, relied on high-resistivity Si substrate for antenna performance. Fabrication of antennas on micromachined membranes [27] reduce loss further and present the antenna with a much reduced effective dielectric constant.

In the technology described here, removal of the silicon substrate in proximity to the antennas can be performed using a standard Bosch process from the backside of the substrate. The concept is illustrated in Fig. 12. The plane view shows the layout of two folded dipoles fed in phase by a common feedline, while the cross-section visualizes the metallization system and the etching scheme. The top metal layer, TM2, and the bottom metallization, M1, form a thin-film microstrip line feeding the antenna. A prototype antenna consisting of two folded dipoles fed in phase [28] achieved 8.4 dBi gain at 130 GHz, and a radiation efficiency of 60%.

Fig. 12. Fabrication of an on-chip 122-140 GHz dipole array using bulk micromachining [28]. Left: plane view; right: cross-section. Note that cross-section is not to scale. Units are in μm .

c) 122 GHz transceiver with on-chip antennas

A 122 GHz FMCW/CW radar transceiver has been designed and successfully fabricated for short-range distance and speed sensing, as shown in Fig. 13, combining a harmonic transmitter [29] and a receiver with subharmonically pumped mixers [30], driven by a 60 GHz Colpitts VCO whose output is split into two paths. The receiver front-end includes an LNA, a 90 degree coupler and two sub-harmonic pumped passive mixers, and the transmitter front-end comprises a frequency doubler and a power detector, which is used as a millimeter wave built-in-self-test (BIST). The use of serial peripheral interface (SPI) significantly reduces the number of bond pads and facilitates the communication between analog front-end (AFE) and digital processor. Two on-chip antennas with localized back-etch (LBE) process have been designed and integrated into a single chip. Each antenna is a two-

element folded-dipole array. One input of the folded-dipole array is fed by a single-ended microstrip transmission line and the other one is floating as a virtual ground, which forms a single-ended to differential transformation. The integration of an on-chip antenna and the use of millimeter wave BIST drastically reduce the high frequency packaging and testing cost, and thus the overall radar system cost.

Fig. 13. Chip micrograph of a 120 GHz transceiver IC using four on-chip dipole antennas (before membrane etch).

IV. CONCLUSION

This article presented the possibilities of making microwave and millimeter-wave ICs more intelligent through a combination of established Si/SiGe BiCMOS technologies, which allow for complex ICs combining a multitude of high-speed analog and digital functions, and RFMEMS processing tightly integrated with the baseline BiCMOS technology. The addition of RFMEMS switches and integrated antennas enhanced by micromachining especially pays off at millimeter waves, where chip-to-board interconnects become increasingly cumbersome, and RFMEMS reconfiguration switches offer unparalleled low loss, high isolation and high linearity.

The technology will see increasing use in complex millimeter-wave phased array sensors, such as enhanced automotive radars, or handheld radar scanners for security applications operating at 94 GHz and beyond.

ACKNOWLEDGEMENT

Part of this work was financed by the European Commission in the FP7 FLEXWIN research project, and the German Ministry of Education and Research (BMBF) in the NANETT project.

The valuable input by Dr. Tatyana Purtova, Gang Liu, A. Cagrı Ulusoy, Matthias Wietstruck, Wogong Zhang, Ruoyu Wang and Yaoming Sun is gratefully acknowledged.

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