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Performance Evaluation of a Class E Power Amplifier Loaded by a High-Isolation Duplexer

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Abstract—This paper presents a performance evaluation of a class-E switched-mode power amplifier, designed in pHEMT GaAs technology, loaded by a high-isolation and low-Insertion Loss (IL) duplexer. This duplexer is based on Surface Acoustic Wave (SAW) technology. Measurements of the duplexer and layout of the class E PA are simulated under Agilent-ADS with a Wideband Code Division Multiple Access signal (WCDMA) in the 1.92 – 1.98 GHz band, for transmission scenario. In this band the amplifier alone achieved 75% to 82% efficiency and 23.5dBm to 24.2dBm output power. The association of the amplifier and the duplexer permitted to reach a drain efficiency of 78% while the output power is 22.7dBm at the central frequency, in the WCDMA band a minimum of 60% efficiency and 21dBm output power is maintained.

Keywords- Class E, Power amplifier, FBAR, duplexer

I. INTRODUCTION

Wireless communication and connectivity systems in the 1 to 6 GHz band have recently evolved towards flexible radio devices. It is potentially of great interest to use switched based amplitude coded architectures [1][2]. Consequently, it has to comply with different standard specifications while keeping high performances such as efficiency and linearity for high data rate signals. Instead of including an independent architecture for each standard, universal transmitter architecture, capable of generating all different standard waveforms seems to be the best solution, especially in terms of consumed power.

To further reduce the complexity of individual RF front-ends and thus drive the total implementation costs down, novel RF front-end architectures that don't require bulky external SAW filters have been proposed for WCDMA transceivers. However, since the transmitter (TX) and receiver (RX) paths are active in WCDMA transceivers at the same time, the inter-stage SAW filter plays an important role as it reduces the out-of-band spurious emission, intermodulation products and cross-compression due to TX leakage and strong out-of-band blockers. Therefore, if we want to avoid using external SAW filters, other solutions need to be conceived to prevent the TX to RX desensitization. This might be achieved, for example, by improving the isolation between TX and RX or by increasing the dynamic range of the RX section. A solution implemented by the authors of [3] uses an FBAR based antenna duplexer with very high isolation between the TX and RX ports, which in turn relaxes the linearity requirements for the RF IC.

Another challenge in the conception of radio transceivers is related to the efficient and distortion-less high power amplification of different types of signals. A solution may be offered through constant envelope architectures. In these architectures, the input of the power amplifier (PA) is a constant envelope signal even if the useful signals at the input and output of the transmitter have a time varying envelope. The potential interest of such architectures is to allow the use of high efficiency power amplifiers such as switched-mode PAs.

In this article we deeply analyze and simulate with measurements and layout consideration the influence of loading a class-E switched mode PA with a prototype of the super-isolation SAW antenna duplexer. Since the antenna duplexer is designed for the WCDMA band, the associated PA is also optimized for 1950 MHz.

Figure 1. Class E Power amplifier topology

II. CLASS E POWER AMPLIFIER DESIGN

The theory of a class E PA has been studied in [4]; [5] and [6]. Class E PA uses an inductor and a shunt capacitor to balance the parasitic output capacitance of the transistor and present an inductive load at the switching frequency. Several classical topologies of class E PA exists, the topology used in this paper is described in fig. 1, and is named “parallel inductor” with a finite feed inductor.

The class E PA circuit consists of a parallel inductance $L2$ supplying the dc current, a parallel capacitor $C2$ shunting the transistor and a resonating impedance $L0-C0$, blocking unwanted harmonics from reaching the load $Rload$. The shunt capacitor can absorb the intrinsic device output capacitance. The transistor is considered as an ideal switch to provide instantaneous device switching between its on-state and off-

state. For this study we will work with 0.15 μ m pHEMT D-Mode transistors, TQP15 technology from TriQuint Semiconductor.

At 1.95GHz the theoretical load impedance value needed in order to obtain the maximum output power is 50 ohms, fortunately the input impedance of the duplexer between 1.92GHz to 1.98GHz is around 50 ohms. Thus, a lossy output matching network is not necessary. An additional parallel capacitor was added between the capacitor $C0$ and the load, when the ideal lumped elements were replaced by the elements of the TQP15 technology. We found that the transistor was presenting an input instability at our frequency in the saturated state. In order to stabilize the transistor and also to make an input adaptation, we chose to use a resistive feedback between the gate and the source of the transistor, and we also optimized the value of the inductor that deliver the gate biasing current. It's principally the feedback technique that made the structure stable while the inductor improved the input adaptation. In the class E PA the input impedance varies while the transistor is switching between off state to on state, for that reason it is not possible to use a conventional adaptation technique. By the examination of the time repartition of the drain current and voltage, we noticed that the PA is most of the time in saturated stated. We made a trade-off in the adaptation between on to off state while prioritizing the on state.

In order to optimize the performances of the amplifier layout to electrical schematic and electrical schematic to layout simulations have been made, it results in a modification of the values of the elements of the layout. The layout is reported in fig. 2.

Figure 2. Class E power amplifier layout in TQP15

TABLE I. VALUES OF THE ELEMENTS OF THE LAYOUT

	Values of the elements		
Capacitors	2.10 pF	3.06 pF	2.1 pF
inductors	1.2 nH	3.45 nH	3.7 nH
Resistor	150 ohms		

The table I. presents the values of the lumped elements of the layout. The values of the inductor being not very important we chose to put the layout in the smallest available surface, which is 1000 μ m per 1500 μ m.

In order to analyze the potential performances of this amplifier we chose to use the drain efficiency and the output power as figures of merit. The drain efficiency is calculated as the ratio between the RF output power and the DC power provided trough the drain of the transistor.

In the theory, the excitation signal of a class E power amplifier should be a rectangular signal, evolving between the gate to source voltage that provides the maximum current and the pinch voltage. Due to the input network and the frequency operation, the signal will be filtered, and thus will be sinusoidal instead of rectangular. Using this signal will decrease the performances because the transition time between the off state and the saturated state will longer. In order to reduce the transition time and to approach a rectangular signal while using a sinusoidal one, the signal will evolve between the gate to source voltage that provides the maximum current and two times the pinch voltage. Any value under the pinch value will not be taken into account; it implies that the signal will be down clipped, it will decrease the transition time and approach a rectangular signal.

Using this technique we obtain 10% more efficiency while maintaining almost the same output power.

Fig. 3 and fig. 4 present the simulated performances in terms of efficiency and output power, in the band of the duplexer. We respectively obtained 75% to 82.5% efficiency while the output power is between 23.5dBm to 24.2dBm.

Figure 3. Efficiency vs frequency

Figure 4. Output power vs frequency

III. HIGH-ISOLATION FBAR DUPLEXER

Fig. 5 depicts the duplexer mounted on a test fixture as well as a detailed close-up of the chip and additional external components (matching SMD inductors). Since we are dealing with transmitter design, the main focus of this section is oriented on performance analysis of the transmitting path of the duplexer. Therefore, the following characterizations and analyses will be related to the “TX to antenna” signal path of the duplexer.

Figure 5. Super-isolation duplexer mounted in a test fixture (a). The right-hand plot shows a detailed close-up of the chip and external passive components (b).

The S parameters had been measured using an input power between 0dBm to 15dBm in the 500MHz to 6GHz band, using a S-parameter network analyzer 8753ES from Agilent.

De-embedded S11 and S21 parameters of the TX to antenna path are depicted in Fig. 6. and Fig. 7. The insertion loss S21 is varying in the range of 0.7 – 1.3 dB. The reflection coefficient S11 at the input of the duplexer varies in the range from 11.5 dB (at the central frequency) to at least 20 dB (at the borders of the allocated band). Attenuation of the TX signal in the downlink RX WCDMA band (2110 – 2170 MHz, not depicted in the figure) is more than 40 dB.

To estimate the level of non-linear phase degradations introduced by the duplexer, argument of the S21 has been analyzed. Fig. 8 demonstrates the nearly linear course of the phase around the central frequency and a non-linear course at higher offsets from the central frequency.

This degradation is caused by higher order phase shift components, which in turn leads to a variable group delay (negative derivative of the phase) at higher frequency offsets (green curve in Fig. 7). Variation of the group delay doesn't exceed 2.5 ns within the allocated WCDMA TX band (max. 0.08 ns/MHz) and it can be seen that a significant growth of the group delay appears at borders of the half power bandwidth.

Figure 6. S21 and S11 de-embedded measurement results

Figure 7. S21 de-embedded in the 1.9GHz-2GHz band

Figure 8. Group delay of the S21

IV. CLASS E POWER AMPLIFIER AND DUPLEXER ASSOCIATION

The measures of the duplexer were put in a file and used a load for our PA, the results presented below are simulated ones. Fig. 9 and Fig.10 present the drain efficiency and the output power of the association of the class E power amplifier and the duplexer.

At 1.95GHz we obtained a drain efficiency of 78% while the output power is 22.7dBm, in the band 1.92GHz -1.98GHz a minimum of 60% efficiency and 21dBm output power is maintained. The amplifier alone was providing 75% to 82% efficiency while the output power was between 23.4dBm to 24.4dBm. The insertion of the duplexer results in a loss of

1.5dBm output power and 3% efficiency at the central frequency.

The loss in the output power is partly explained by the insertion loss of the duplexer 0.7-1.3dBm, 1.1dBm at the central frequency. In the band of study the theoretical load impedance of the class E power amplifier is 50 ohms, the duplexer present approximately the same in-band impedance, but the out-band impedance of the duplexer is far from a 50 ohm impedance. Furthermore, the difference in the out-band impedance could also explain the efficiency drop.

Table II present a comparison of our designed class E PA with other class E PA with an output power not too far from what we achieved regardless of the technology.

TABLE II. COMPARISON OF THE PERFORMANCES WITH PUBLISHED WORK

	[7]	[8]	Our work
Frequency	2.14GHz	1.95GHz	1.95GHz
Drain efficiency	74.8%	74.5%	80.5%
Output power	33dBm	27dBm	23.9dBm

In [7] GaN transistors are used it explain the difference in output power, and in comparison with [8] we improved efficiency by 6% while decreasing output power by 3.1dBm. While designing our PA we focused on the efficiency more than on the output power, because of the trade-off between efficiency and output power we decreased the output power in order to increase efficiency.

Figure 9. Efficiency vs frequency

Figure 10. Output power vs frequency

V. CONCLUSION

In this paper, we presented the design of a class E switched mode power amplifier in pHEMT GaAs technology matched to a prototype of a high-isolation and low-Insertion Loss duplexer based on SAW technology. The proposed architecture has been validated using a signal in the WCDMA transmission band, which is allocated in 1.92 – 1.98 GHz.

The class E PA alone achieved 75% to 82% efficiency and 23.4dBm to 24.4dBm output power in this band. The association of the PA and the duplexer permitted to obtain a maximum drain efficiency that reaches 78% and a 22.5dBm output power, and in the band a minimum of 60% and 21dBm is maintained. The insertion of the duplexer results in a loss of 1.5dBm output power and 3% efficiency at the central frequency.

The insertion loss of the duplexer could explain a part of this loss but not all, the out-band impedance of the duplexer have also an effect on the performances. A way to get rid of this problem is to design an amplifier optimized for the two first harmonics, the output network of the class E PA should be made in order to match the impedance of the duplexer for those two harmonics. The classical class E PA load impedance is optimized only on the central frequency and the out-band impedance of the class E is not necessary the optimum one, with the two harmonics optimized class E better performances should be achieved.

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