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Reprinted from
2011 IEEE Semiconductor Conference Dresden, 27 – 28 September 2011

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U- and V-band Signal Sources in Si/SiGe Technology

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Abstract—A U-band VCO and a V-band push-push frequency doubler are designed in a $0.25\ \mu\text{m}$ SiGe:C BiCMOS technology. The VCO oscillates from 48 GHz to 55 GHz, with an output power of around -1 dBm and a phase noise of -84 dBc/Hz at 1 MHz offset. The push-push frequency doubler has a minimum loss of 12 dB at 50 GHz for an input power of 6 dBm. It achieves an output power of -2.4 dBm at 50 GHz and -5.8 dBm at 75 GHz for an input power of 10 dBm. The VCO is biased at 4 V consuming 36 mA, and the push-push doubler draws 9.4 mA from a 2 V supply.

I. INTRODUCTION

Millimeter-wave signal sources are key components of modern communication and radar systems. Wireless systems at high frequencies attract much attention due to their wider bandwidths which enable much higher transmission rates [1]. Frequency doublers are widely combined with VCOs to generate signals at high frequencies, because the VCOs at low frequencies usually have better phase noise. Gilbert-cell and class-B topologies usually suffer from a low output power or a limited bandwidth. Therefore a push-push topology was used here which combines efficient frequency doubling with a simple topology.

This paper presents a VCO covering a frequency range from 48 GHz to 55 GHz and a push-push doubler which works in V-band at a supply voltage of 2 V with a current consumption of 9.4 mA.

II. TECHNOLOGY OVERVIEW

The IHP technologies SG25H3 $0.25\ \mu\text{m}$ SiGe:C BiCMOS process was used in the design. The technology offers npn transistors with an f_T of 110 GHz, an f_{max} of 125 GHz, and BV_{ceo} of 2.3 V. It also offers four types of resistors, metal-insulator-metal capacitors, scalable MOS varactors and so on. There are five metal layers: 3 thin metal layers and 2 TopMetal layers.

III. VCO

A. Circuit Design

The schematic of the VCO is shown in Figure 1. The VCO core is based on a negative-resistance configuration, which is realized by capacitive degeneration in the emitter. MOS

Fig. 1. Schematic of the VCO with cascode-amplifying output buffer.

varactors were used to tune the oscillation frequency. The output buffer is a cascode-amplifying stage, in order to achieve a higher output power.

The inductors in the circuit are realized by Thin Film Microstrip Lines (TFMSLs) which is shown in Figure 2(a). The top metal is TopMetal 2, with a thickness of $3\ \mu\text{m}$. The

Fig. 2. (a) Structure of Thin Film Microstrip Lines (TFMSLs). (b) Quality factor of a $300\ \mu\text{m}$ TFMSL used as an inductor.

bottom metal is Metal 1, with a thickness of $0.58\ \mu\text{m}$. The distance between them is $9.16\ \mu\text{m}$. As the TFMSL is to be used as an inductance, its characteristic impedance should be high to decrease the necessary geometric length, resulting in a narrow signal line width. It was chosen to be $3\ \mu\text{m}$ and

the simulated characteristic impedance of the line is about $82\ \Omega$. The quality factor of a $300\ \mu\text{m}$ line used as an inductor was simulated and the result is shown in Figure 2(b). It was above 9 from 40 GHz to 75 GHz. To speed up the design process, a scalable TFMSL model [2] was established based on Momentum simulations.

To determine the oscillation frequency of the VCO, small signal S-parameter simulation was performed for the start-up condition. Figure 3 shows the results of the input impedance simulation. The oscillation starts where X_1 and X_2 cancel out

Fig. 3. (a) Simulation of the input impedance, seeing into the base of T_1 and the base inductor L_B . (b) Simulated imaginary part of Z_1 and Z_2 . At 46 GHz the sum of X_1 and X_2 equals zero, indicating the start-up oscillation. (c) Simulated real part of Z_1 and Z_2 . At 46 GHz, $|R_1| > 1.2R_2$.

each other while R_1 is negative and $|R_1| > 1.2R_2$ [3]. It will finally sustain at the frequency where $Z_1 + Z_2 = 0$. Figure 3 shows the oscillation starts at 46 GHz (V_{tune} is 3 V).

B. Measurement

The chip photo of the VCO is shown in Figure 4. The chip

Fig. 4. Chip photo of the VCO shown in Figure 1. The chip size is $450\ \mu\text{m} \times 770\ \mu\text{m}$, including bond pads.

occupies an area of $450 \times 770\ \mu\text{m}^2$ including bond pads. To measure the VCO on wafer, a 67 GHz differential probe, a V-band sub-harmonic mixer (Agilent 11970V) and a spectrum analyzer (HP 8563E (30 Hz-26.5 GHz)) were used. One of the differential output was connected to the spectrum analyzer and

the other was terminated by a $50\ \Omega$ load. The VCO was biased at 4 V and consumed 36 mA.

The measured oscillation frequency and output power are shown in Figure 5. The VCO oscillates from 48 to 55 GHz and

Fig. 5. Measured oscillation frequency and single-ended output power of the VCO.

the output power is around -1 dBm. To compare the measurement with the simulation, Figure 6 shows the measured and the simulated results with the TFMSL model and Momentum. Figure 6 shows that below V_{tune} of 1 V the measured oscil-

Fig. 6. (a) Measured and simulated oscillation frequency of the VCO. (b) Measured and simulated single-ended output power of the VCO.

lation frequency agrees quite well with the simulation with Momentum, while the measured output power of the VCO differs by around 7 dB. Compared to the simulation with the

TFMSL model, the measured frequency was higher by about 5 GHz and the measured output power was lower by around 4 dB. The difference of the output power may be due to the shift in the oscillation frequency, the simulation deviation of the transmission lines and the models of other components. For the future design, such deviation must be taken into consideration during simulation, and in order to establish a more precise TFMSL model based upon measurements, a line must be characterized on wafer.

The output spectrum of the VCO is shown in Figure 7. The phase noise at 1 MHz offset is -84 dBc/Hz, compared to

Fig. 7. Measured output spectrum of the VCO at the oscillation frequency of 48 GHz (single-ended).

-88 dBc/Hz in simulation. The deviation may result from the noise induced by the tuning voltage supply [4]. Figure 7 shows the single-ended output power with the losses. To get the real output power, the losses from the cables, probes and other measurement setup should be compensated. In addition, due to the differential output, 3 dB must be added.

The phase noise of the VCO was also measured using the Phase Noise Utility of the Agilent 8565EC, which is a built-in software specialized to measure the phase noise of an oscillator at different offset frequencies or to continuously measure the phase noise at one spot offset frequency [4]. It was measured from 500 kHz to 100 MHz. The measurement result is shown in Figure 8. The phase noise at 1 MHz offset is -85 dBc/Hz, which agrees quite well with the first measurement.

IV. PUSH-PUSH DOUBLER

A. Circuit Design

The schematic of the push-push Doubler is shown in Figure 9. It is based on the common-collector push-push topology, i.e., the output is taken from the emitter. The common-collector configuration reduces the effect of the base-emitter junction capacitors at high frequencies thus increases the bandwidth [5].

Fig. 8. Measured phase noise of the VCO 500 kHz to 100 MHz at the oscillation frequency of 48 GHz, using the Phase Noise Utility of the Agilent 8565EC.

Fig. 9. Schematic of the push-push doubler.

B. Measurement

The chip photo of the frequency doubler is shown in Figure 10. The area of the chip is $345 \times 485 \mu\text{m}^2$ including

Fig. 10. Chip photo of the push-push doubler shown in Figure 9. The chip size is $345 \mu\text{m} \times 485 \mu\text{m}$, including bond pads.

bond pads. For the characterization on wafer, a signal source (Agilent E8254A (250 kHz-40 GHz)) was used to generate signals with a maximum power of 10 dBm. A 25-37.5 GHz signal was then fed single-endedly to the input, while the other input end was connected to a 50-Ohm terminator. The output of the doubler was connected through a 110 GHz GSG probe to the V-band sub-harmonic mixer (Agilent 11970V) and the

spectrum analyzer (HP 8563E). The doubler was biased at 2 V and consumed 9.4 mA.

Figure 11 shows the measured and simulated output power vs. output frequency for an input power of 5 dBm. The

Fig. 11. Measured and simulated output power of the push-push doubler vs. output frequency, the input was driven single-endedly.

measured output power generally decreases with increasing frequency. At this input power, the measured maximum output power is -6.7 dBm at 52 GHz. The output power decreases to -9.6 dBm at 64 GHz, by about 3 dB. The simulated output power is relatively constant, around -6.5 dBm.

Figure 12 shows output power vs. input power for different input frequencies: 25 GHz, 30 GHz, 35 GHz and 37.5 GHz. When an input power of 10 dBm was applied, it achieves an

Fig. 12. Output power of the push-push doubler vs. input power for different input frequencies, the input was driven single-endedly.

output power of -2.4 dBm at 50 GHz (for fundamental frequency of 25 GHz) and -5.8 dBm at 75 GHz (for fundamental frequency of 37.5 GHz). The output power does not saturate yet for 10 dBm input power, because large transistors were used in the circuit.

Figure 13 shows conversion gain as a function of the input power for different input frequencies. The frequency doubler

Fig. 13. Conversion gain of the push-push doubler vs. input power for different input frequencies, the input was driven single-endedly.

has a minimum loss of 12 dB at 50 GHz (for fundamental frequency of 25 GHz) with an input power of 6 dBm. For a 37.5 GHz input signal the gain saturates to -16 dB at the input power of 5 dBm.

Besides, because the doubler was driven single-endedly, the fundamental suppression could not be precisely measured. In future measurement a balun needs to be designed to differentially feed the input of the doubler.

V. CONCLUSION

Using a 0.25 μm SiGe:C BiCMOS technology from IHP, a 48 GHz - 55 GHz VCO was fabricated. The measured results were compared with the simulation. The deviation between them will have to be improved through a more precise TFMSL model based upon measurements. A push-push frequency doubler was also designed. It achieves an output power of -2.4 dBm at 50 GHz and -5.8 dBm at 75 GHz for an input power of 10 dBm. The doubler consumes 9.4 mA from a 2 V bias.

ACKNOWLEDGMENT

The first author gratefully acknowledges the support of the Carl-Zeiss-Stiftung. The authors are also grateful to IHP microelectronics, Frankfurt (Oder), Germany, for the fabrication of the ICs.

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