Comparison of Direct Digitization Current Sensing Circuits for EIS

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Abstract—In this work, a qualitative comparison between state of the art current recorders for biomedical applications is presented. Prior work showed that direct digitizing frontends outweigh their analog counterparts. This work performs a comparison between the direct digitization frontends, namely time-based and current-input CT $\Sigma\Delta$ frontends. It is shown that time-based converters - due to usage of current conveyors to generate a low impedance node - suffer from inferior linearity. Also the trade-off between SNR versus conversion time limits their achievable SNR and the maximum input signal frequency. On the other hand, with the usage of a FIR-DAC within a current-input CT $\Sigma\Delta$, the requirements of the critical first amplifier are highly relaxed. In addition, the FIR-DAC reduces the influence of clock jitter and allows the current-input CT $\Sigma\Delta$ to achieve a higher SNR and linearity compared to the time-based converters.

I. INTRODUCTION

Potentiostatic applications such as electrochemical impedance spectroscopy (EIS), cyclic voltammetry (CV), chronoamperometry (CA), or scanning ion-conductance microscopy (SICM) are in need of a current recording block to record the signal currents from a voltage excitation signal. Fig. 1 shows a typical system configuration for such application. The resulting signal currents, which can vary from pA to μ A in a frequency range from DC to the MHz range, need to be recorded by a current input stage and finally digitized and sent to a processing unit in order to evaluate the sample under test (SUT) [1]. Recent state of the art (SoA) reported on developing less noisy or higher linear, faster or higher power and area efficient circuitry for this recording. Thus, a comparison between the published SoA can facilitate the choice of a suitable architecture for a given application.

The SoA for the current recorders can be divided to two main categories: firstly, architectures which perform an input signal current to voltage conversion, such as resistive and capacitive transimpedance amplifiers (R-TIA/C-TIA), whereafter the voltage is digitized with an arbitrarily chosen analog to digital converter (ADC) [1]. Secondly, there are architectures which directly convert the signal current into the digital domain within the front-end, such as current to frequency converters (C-FC) [2] and current-input continuous-time sigma-delta modulators (Current-CT $\Sigma\Delta$) [1].

This paper intends to compare those architectures with the goal to highlight their pros and cons. First, a short recap of our prior comparison on the SoA is presented, which is followed by introducing the SoA of time-based current to digital converters and Current-CT $\Sigma\Delta$. It is then proposed to utilize a finite impulse response (FIR) filter in the Current-CT $\Sigma\Delta$ to relax its requirements on the first integrator and to reduce their jitter sensitivity. The comparison between C-FC and Current-CT $\Sigma\Delta$ is then carried out concerning linearity, noise, jitter sensitivity and input impedance.

Fig. 1. Typical set-up of an biochemical experiment, such as EIS and SICM.

II. PREVIOUS WORK

The previously published work [1] gave a detailed description and comparison of R-TIA, C-TIA, and Current-CT $\Sigma\Delta$. It was shown that the R-TIA suffers from a trade-off between speed and transimpedance. This is solved by the C-TIA utilizing a combination of an integrating and differentiating stage. However, other trade-offs as different signal transfer characteristics for low and high frequency signals and a frequency dependent dynamic range are seen in the C-TIA, reducing its possible performance and attractiveness. The third investigated architecture was a Current-CT $\Sigma\Delta$, which seems to solve all of those trade-offs, comes with the additional advantage of direct digitization, but achieves this at the cost of basically one drawback. High sampling frequencies and single-bit operation for good linearity heavily increase the requirements of the input stage of the $\Sigma\Delta$ s. Moreover, CT $\Sigma\Delta$ are highly sensitive to clock jitter, which is critical for low noise-applications.

The previous study [1] compared analog output approaches (R-TIA and C-TIA) with a digital output approach (Current-CT $\Sigma\Delta$). With an implementation example, it was argued that the Current-CT $\Sigma\Delta$ with its inherent digitization outweighs the analog frontends. However, still a comparison with other direct digitization architectures was missing. Therefore, in this paper time-based current digitizers and Current-CT $\Sigma\Delta$ are analyzed and compared.

III. TIME-BASED CURRENT DIGITIZER

One of the most important issues that current recorders need to deal with is generating a virtual ground for the signal currents. The reason for a low impedance node is to ensure the input current (I_{in}) is only proportional to the device under test rather than the input impedance of the current recorder [3]. A structure, which can be used for this purpose, is a current conveyor. Many current conveyors have been proposed in literature [2][3][4] to generate this low ohmic current input node. In this work the principle of a very simple current conveyor is shortly described with its pros and cons.

A. Current conveyor

Fig. 2.a shows a current conveyor. An operational amplifier (OA) is configured in a negative feedback with use of transistor M1. This negative feedback fixes the input node voltage to the positive input voltage of the OA (V_{ref}) and results in an input

Fig. 2. a) A typical current conveyor b) conveyed current integrated on a capacitor c) or translated to voltage with a transistor in diode configuration.

impedance Z_{in} of [3]:

$$Z_{in} = \frac{1}{g_{m1} A(j\omega)} \parallel \frac{1}{j\omega C_P}, \quad (1)$$

where g_{m1} is the transconductance of the transistor M1, $A(j\omega)$ is the open loop gain of the utilized amplifier, and C_P is the parasitic capacitance at the input node.

The OA enforces a virtual ground at the input node (Fig. 2.a), therefore it can be assumed that the signal current I_{in} flows towards the output node. In [4], I_{out} has been integrated into a capacitor C_{int} (Fig. 2.b). The drawback of this method is the big non-linearity that is introduced by transistor M1. As reported in [4], for small input currents M1 goes into sub-threshold region, which has the worst linearity. By increasing I_{in} , the output voltage V_{out} increases and thereby the V_{DS} of M1 increases and pushes it into strong inversion, which yields improved linearity. Another approach was reported in [3], where the voltage conversion was done by use of diode connected transistor M2 (Fig. 2.c). Thereby, I_{out} can be mirrored to several branches, however the previously outlined non-linearity is still present, as the diode configured transistor M2 introduces non-linearity as well.

One method to increase the linearity of M1 is to bias it with a constant current source [3]. As shown in Fig. 3, transistor M2 acts as a constant current source (I_{DC}). In this way, the difference $|I_{DC} - I_{in}|$ passes through the transistor M1. Therefore, for small I_{in} , transistor M1 is in saturation region and for large values of I_{in} , I_{DC} can be chosen to keep M1 in the saturation region as well. Though, a drawback of this method is that the power consumption increases and another noise source is introduced at the input node [3].

Next, the noise properties of the current conveyor are discussed. Since transistor M1 (Fig. 2.a) is configured as common gate and for practical values of g_{m1} , $A(j\omega)$, and C_P , the input referred current noise $\overline{I_{n,in}^2}$ of the circuit can be calculated as [4]:

$$\overline{I_{n,in}^2} \approx \overline{V_{n,OP}^2} (2\pi f C_P)^2, \quad (2)$$

where $\overline{V_{n,OP}^2}$ is the OTA input referred noise. Using the DC current source to increase the linearity of the current conveyor (Fig. 3), this increases the $\overline{I_{n,in}^2}$ to:

$$\overline{I_{n,in}^2} \approx \overline{V_{n,OP}^2} (2\pi f C_P)^2 + 4k_B T g_{m3}, \quad (3)$$

where k_B is the Boltzmann constant, T is the temperature, and g_{m3} is the transconductance of transistor M3. Eq. 3 depicts the trade-off between noise and linearity of the system. In order to increase the linearity of the current conveyor, I_{DC} (Fig. 3)

Fig. 3. A current conveyor with enhanced linearity.

Fig. 4. Current to frequency converter (adapted from [2]).

must be increased, which means higher g_{m3} and higher g_{m3} yields to a larger input referred current noise.

B. Current to Frequency Converters

In this section, three time-based ADCs, utilized in the SoA, are shortly reviewed and their pros and cons are compared. Fig. 4 shows a current to frequency converter that is proposed in [2]. The input current (I_{in}) is mirrored by M2 and integrated on C_{int} , while assuming that the flip-flop (FF) output (Q) is zero. When V_{int} exceeds V_{th1} , the FF output is set and M3 turns off while M4 turns on. Then C_{int} starts to discharge by a constant current source of I_{ref} . Discharging continues until V_{int} crosses V_{th2} , and by that the FF output resets and again I_{in} is integrated on C_{int} . The output data Q consequently shows a period of $(T + D)$ and a pulse width D [2]:

$$T = \frac{V_{dd} C_{int}}{2I_{in}}, \quad D = \frac{V_{dd} C_{int}}{2I_{ref}}. \quad (4)$$

Eq. 4 indicates that I_{in} is inversely proportional to T , which means for small I_{in} a very long time is needed to charge C_{int} . This is a very important trade-off of the time-based digitizers, since the minimum detectable input is proportional to the conversion time of the ADC and the maximum input frequency is inversely proportional to that conversion time.

Another current to frequency converter is the dual-mode ADC proposed by [4]. The conveyed input current (I_{in}) is integrated on a capacitor (C_{int}) and results in V_{out} (Fig. 3.b). The integrated voltage is then converted to the digital domain in two steps. In the first phase the most significant bits (MSB) are extracted. This process takes a very long conversion time for small inputs. In order to mitigate this trade-off, in the second phase a single-slop ADC is used to calculate the least significant bits (LSB). More detailed description can be found in [4]. The proposed architecture partially solves the long conversion time of [2], however it suffers from a bad linearity due to the usage of the current conveyor.

Current controlled ring oscillators (CCRO) are also proposed to digitize currents [5]. Fig. 5.a shows a CCRO with improved matching. The operation frequency of the CCRO (f_{osc}) is

Fig. 5. a) current controlled ring oscillator (CCRO) with enhanced matching b) CCRO with enhanced linearity with use of a CCII+ (adapted from [5]).

proportional to [5]:

$$f_{osc} \propto \frac{I_{in}}{C_L V_{osc}}, \quad (5)$$

where C_L is the load of each stage and V_{osc} is the rail voltage of the ring oscillator. Deriving the dependency of f_{osc} to V_{osc} as done in [5], it can be concluded that this dependency results in strong non-linearity. [5] reduces this dependency by utilizing a second generation current conveyor (CCII+) as shown in Fig. 5.b to fix the V_{osc} to a known potential regardless of I_{in} . With this modification the dependency of f_{osc} to V_{osc} is reduced and thereby the linearity of the CCRO is increased.

The input impedance of the circuit in Fig. 5 is $Z_{in} = 1/g_{m,in} \propto 1/I_{in}$, where $g_{m,in}$ is the input transistor transconductance. Input impedance of the CCRO is inversely dependent on the input current (I_{in}). Also, the working region of M1 is defined by I_{in} . This means for small currents, M1 is in weak inversion. Thereby CCRO has a very big input impedance with big non-linearity. To remove these dependencies, and thus to generate a better virtual ground, a current conveyor must be introduced at the input node of the CCRO. This leads to a noise and linearity specifications close to the mentioned methods.

A very important noise source in current-to-digital converters (and ADCs in general) is the quality of the sampling clock, like clock jitter. Since, in time-based ADCs the data is encoded in time domain, quality of the clock has a major role [7].

IV. CURRENT-MODE CTΣΔM

CTΣΔMs can be used to digitize voltage and current inputs [1]. Fig. 6.a shows the output of a current-CTΣΔM with single-bit internal quantizer, where the output spectrum shows large high frequency quantization noise due to the noise-shaping property of the ΣΔM. The single-bit quantizer is usually employed to achieve high intrinsic linearity in the feedback DAC [6]. Though, this single-bit feedback signal is directly seen at the sensitive input node of the first integrator through the outermost digital to analog converter (DAC), which is usually realized as a resistor or a current source. As discussed in more details in [1], this puts stringent requirements to the first amplifier, such as gain-bandwidth and slew rate, to follow the dynamics of the single-bit feedback. This together with the anyhow needed inband linearity and noise performance of the input stage, is the strongest disadvantage of current-CTΣΔM, together with its known sensitivity to clock jitter.

Fig. 6. Current-CTΣΔM a) single-bit DAC b) multi-bit DAC c) FIR DAC.

To reduce this drawback two solutions are commonly employed. The first approach as shown in Fig. 6.b and uses a multi-bit quantizer. This highly relaxes the dynamic requirements on the first integrator and it reduces the jitter sensitivity [6]. Problematically, the mismatch between the multibit DAC elements introduces its non-linearity directly to the input node, which makes linearization techniques, high area and power consumption consequently necessary, and have thus to be avoided in area limited, multichannel EIS applications.

Another approach to decrease the dynamic requirements on the first amplifier in the presence of single-bit operation is to use a FIR-DAC as shown in Fig. 6.c [8]. The FIR-DAC basically acts like a low pass filter for the high-frequency quantization noise, and it smooths the DAC feedback signal seen by the first integrator. This reduces the GBW and SR requirements of the first integrator manifold, depending on the actual design. The mismatch between the individual FIR-DAC elements does not create non-linearity, but only a slight change in the filter coefficients. A further advantage of using a FIR-DAC in CTΣΔMs is the reduction of jitter sensitivity [8]. The FIR-DAC is realized by splitting the single-bit DAC into several elements (Fig. 6.a), where the number of taps can be found through simulation [8].

The Virtual ground, i.e. small input impedance, in current-CTΣΔMs is being generated by two-fold. Firstly by the negative feedback around the first integrator and secondly by the overall loop-filter ($LF(j\omega)$) as:

$$Z_{in} = \frac{1}{j\omega C_{int} A(j\omega)} \parallel \frac{r_{DAC}}{LF(j\omega)} \parallel \frac{1}{j\omega C_P}, \quad (6)$$

where r_{DAC} is the DAC's output equivalent resistance, C_{int} is the integration capacitor, and C_P is the parasitic capacitance present at the input node. Together with the FIR-DAC in the outermost feedback a compensation filter (CF) is needed in an

TABLE I. COMPARISON BETWEEN THE DIFFERENT EXCITATION SIGNAL TYPES.

	Linearity	Noise	Input Impedance	Jitter Sensitivity	Convergence Time
Current to Frequency	-	-	+	-	-
Dual mode ADC	-	-	+	-	-
Enhanced CCRO	-	-	+	-	-
$\Sigma\Delta$ Single-Bit DAC	-	+	++	-	+
$\Sigma\Delta$ Multi-Bit DAC	-	+	++	+	+
$\Sigma\Delta$ FIR DAC	+	+	++	+	+

inner feedback path to restore the original NTF. Since CF is introduced in the inner feedback path, its noise contribution is shaped by $\Delta\Sigma$ loop and is neglectable. CF compensates for the delay that FIR-DAC has introduced in the $\Delta\Sigma$ loop [8].

The Noise performance of current-CT $\Sigma\Delta$ M including the FIR-DAC is unaltered to the single-bit DAC [8]. Therefore, $\overline{I_{n,in}^2}$ of the FIR-DAC current-CT $\Sigma\Delta$ M is [1]:

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,OP}^2}}{\left(1/g_{m,cs} \| 1/j\omega C_P \| 1/j\omega C_{int}\right)^2} + 4k_B T g_{m,cs}, \quad (7)$$

where $g_{m,cs}$ is transconductance of the unit current source. For practical values of C_P , C_{int} , and $g_{m,cs}$, Eq. 7 becomes:

$$\overline{I_{n,in}^2} \approx \overline{V_{n,OP}^2} (2\pi C_P)^2 + 4k_B T g_{m,cs}, \quad (8)$$

V. DISCUSSION

Tab. I summarizes the comparison between the mentioned time-based converters and the different versions of current-CT $\Sigma\Delta$ M. In terms of linearity, all the mentioned time-based converters have inferior performance than FIR-DAC $\Delta\Sigma$ M. These non-linearities arise due to the utilization of current conveyors. The linearity in single-bit current-CT $\Sigma\Delta$ M is also highly dependent on the first amplifier, since it needs to work on the large dynamics of the single-bit feedback signal. Therefore, the first amplifier is power hungry to satisfy the required linearity. Mismatches between unit elements of a multi-bit DAC do not allow good intrinsic linearity unless area and power hungry linearization techniques are used. Employing a FIR-DAC in a current-CT $\Sigma\Delta$ M shows the best linearity with relaxed requirements on dynamics of the first integrator, whereas the additional area consumption is negligible and the additional power consumption mostly stems from the FF used in the FIR-DAC, which run at the full sampling frequency.

Another trade-off in time-based converters is their conversion time for small amplitude signals. This means for small amplitudes the architectures trade conversion speed against sensitivity. Since the Nyquist theorem needs to be fulfilled with this conversion time, the maximum detectable frequency will become limited. On the other hand, current-CT $\Sigma\Delta$ M work on their defined conversion rate given by the oversampling ratio and clock frequency.

The quality of the virtual ground node in current conveyors is only dependent on the first amplifiers open loop gain (Eq. 1). In current-CT $\Sigma\Delta$ M the $LF(j\omega)$, which is a cascade of integrators, guarantees a low impedance input (Eq. 6) within the inband of the $\Sigma\Delta$ M. Therefore, lower input impedance can

be more easily achieved by the current-CT $\Sigma\Delta$ M, especially without trading input impedance against linearity.

In terms of noise, assuming the same C_P and $\overline{V_{n,OP}^2}$ for the converters and comparing Eq. 3 and Eq. 8, the only difference is found in their respective transconductance. In current conveyors, an increasing the DC current to achieve better linearity simultaneously leads to higher g_{m3} , which means more input referred current noise. In current-CT $\Sigma\Delta$ M, thanks to their scalability, the value of $g_{m,cs}$ can be more freely chosen to satisfy the noise and linearity requirements [6]. Another noise source is the clock's quality. The clock jitter limits the performances of both converters. However, by use of FIR DAC in current-CT $\Sigma\Delta$ M this sensitivity can be largely reduced, whereas in time-based converters it remains a limiting factor. Therefore, the FIR-DAC current-CT $\Sigma\Delta$ M seems to be a superior choice in terms of noise and linearity.

VI. CONCLUSION

In this paper, time-based digitizers are introduced and compared with different current-CT $\Sigma\Delta$ M. It was shown that time-based converters are in need of current conveyors to generate a low impedance input node. However, the current conveyor limits the linearity of time-based converters. Also time-based converters suffer from limited maximum signal frequency due to their slow conversion rate for small input signals. On the other hand, since in current-CT $\Sigma\Delta$ M virtual node is generated by the loop filter, there is no need of a current conveyor. With the use of a single-bit quantizer, intrinsically linear DACs are achievable. Introducing the FIR-DAC the high frequency quantization noise is low pass filtered and thereby the usually high dynamic requirements of the first amplifier are relaxed. Also the FIR-DAC reduces the jitter sensitivity of the ADC and allows the current-CT $\Sigma\Delta$ M to achieve higher SNR in comparison with time-based converters.

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