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79 GHz Fully Integrated Fully Differential Si/SiGe HBT Amplifier for Automotive Radar Applications

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Abstract—In this work, the authors present a fully integrated, fully differential amplifier operating at 79 GHz using a high-speed Si/SiGe hetero-bipolar technology. This amplifier needs a single supply voltage and shows high performance such as high gain, excellent reverse isolation and low power consumption (90 mW at 3 V supply voltage). This result was achieved by using multi-stage cascode topology and a thin-film microstrip line based design. In addition, the frequency of operation can be easily adjusted within a wide range by changing the length of the matching network (by using focused ion beam or ultrasonic manipulator). A simple but efficient layout technique was used to easily measure single-endedly the differential integrated circuit, also at these high frequencies.

I. INTRODUCTION

The suitability of Si/SiGe hetero-bipolar transistors (HBTs) for applications beyond 70 GHz has already been proven e.g. in [1-5]. However, amplifiers at these frequencies use single-ended or double-balanced design architectures making the packaging highly critical. In this work, we present a fully integrated, fully differential compact Si/SiGe HBT amplifier operating at 79 GHz for automotive radar applications. The amplifier exhibits high performance obtained by using appropriate design techniques which will be highlighted here.

II. TECHNOLOGY OVERVIEW

The technology used for this design is the SiGe BiCMOS process SG25H1 of IHP. It is a self-aligned single-polysilicon technology with 0.25 μm minimum lithographic emitter width, 4 resistor types, metal-insulator-metal (MIM) capacitors and 4 aluminium metal layers for reactive elements such as inductors and microstrip lines (an optional 5th metal layer is also available but is not used here). The transistors reach a peak f_T and f_{max} of 190 GHz with a collector-emitter breakdown voltage (BV_{CEo}) of 2 V.

III. DESIGN PHILOSOPHY

A. Basic design topology

In order to reach a competitive gain, three stages with appropriate input, output as well as interstage matching were necessary. For each stage, the cascode topology was chosen for its high performance such as high gain and excellent reverse

Fig. 1. Simplified schematic of the cascode topology

isolation. A simplified schematic of a single stage is shown in Fig. 1.

In order to increase the impedance of the current source, an LC resonator was preferred to standard topologies such as transistor or resistor based current sources. In addition, the resonator allows a lower supply voltage level because of its negligible resistance. A differential topology was preferred to single-ended architecture. Differential designs have major advantages:

- Maximum voltage swing is double compared with a single-ended design operation (at a given supply voltage level).
- Even-order harmonics (which appear in common-mode) are suppressed.
- Packaging is less critical because supply voltage and ground connections are located on an on-chip virtual ground.

However, differential designs need a more complex measurement setup. Here, a simple and efficient technique was used and is presented in section III-C.

B. Thin film microstrip lines

Several types of lines can be used for circuit design. However, due to the high frequency, the lossy substrate (Si)

and the lack of backside metallization, many line topologies had to be excluded for this work. In [6], it was shown that a coplanar waveguide (CPW) based topology is not possible on low-resistivity silicon substrate due to the extremely high losses (a CPW was already presented in [7] but using a high-resistivity silicon substrate. High-resistivity silicon substrate are somewhat more expensive and are prone to parasitic inversion channels at the Si/SiO₂ interface below the CPW). A conductor backed CPW is also difficult to realize using standard metal systems (the thin oxide layer separating ground plane from signal line would lead to an extremely narrow center conductor resulting again in unwanted losses). In [8], it was demonstrated that for inverted microstrip lines higher modes appear and coupling between them occurs. This proves that embedded inverted microstrip lines are not suitable for high frequency RFICs as well. Therefore, a thin-film microstrip line (TFMSL) based IC was preferred. TFMSL based designs have already been successfully realized e.g. in [9]. For this work, the bottom-most available metal layer was used as ground plane and the top-most as signal line. A simplified cross-section of a TFMSL is depicted in Fig. 2.

Fig. 2. Simplified cross-section of a TFMSL (not to scale)

The main advantages of TFMSL are a better accuracy of electromagnetic field (EMF) simulator compared with lumped elements, simplicity of the resulting layout (compared for instance with CPW based design), a similar quality factor compared with spiral inductors on silicon substrate and moreover the possibility to tune the inductance to lower or higher values by cutting them (see section III-C). The S-parameters of the TFMSL were simulated by using Momentum (by Agilent), Sonnet and Microwave Studio (by CST). The main parameters (impedance Z , effective permittivity $\epsilon_{r,eff}$, attenuation and phase velocity) were extracted. In order to perform efficient and accurate simulations, an equivalent-circuit model describing the TFMSL behaviour was built. This model is only scalable in length but was perfectly sufficient for this work. Indeed, in order to reduce their length all the lines of the IC have the same high impedance (approximately 70 Ω) and consequently the same width (defined by the current flowing and the metal system characteristics). A schematic of the equivalent-circuit model is presented in Fig.3.

Fig. 3. Schematic of the TFMSL model

$$Z_S = \frac{R_s + j\omega L_s}{N}$$

$$Y_P = \frac{j\omega C_p}{N}$$

Where N (integer) is the amount of cascaded single cells necessary to simulate the distributed nature of the line ($N=10$ in this work).

$$R_S = (R_0 \times \sqrt{1 + \frac{f}{f_c}}) \times L$$

$$L_S = (L_0 - L'_v \times f) \times L$$

$$C_P = (C_0 + C'_v \times f) \times L$$

Where L is the length of the TFMSL. The different parameters of the model (R_0 , f_c , L_0 , L'_v , C_0 and C'_v) are then determined by fitting the TFMSL parameters extracted from the EMF simulations to the parameters extracted from the equivalent-circuit model.

C. Layout

In order to easily correct possible inaccuracy during the simulation, a line tuning technique is used. The TFMSL length at the collector of each common base of the cascode topology can be modified by cutting shorting bars using focused ion beam (FIB) or ultrasonic manipulator in order to tune the amplifier to various operating frequencies. This technique was already presented in [10]. However, the major drawback of this topology is the important increase of access line length between the different stages of the IC resulting in an unwanted loss. Therefore, a different topology was preferred. In Fig. 4, the left hand side picture describes the topology used in [10]. The right hand side picture shows the modified topology. It can be easily seen that the modified design decreases strongly the distance between two stages. However, the location of the shorting bars that should be cut is no longer in the virtual ground node of the differential design. Consequently, several more cuts had to be performed in order to avoid

further parasitics which would lead to a decrease of circuit performance.

Fig. 4. Topology of [10] (left) compared with modified topology (right)

One critical issue of differential designs is their measurement. Four ports measurements imply a cost increase that however can be mediated by simple design techniques. For on-wafer measurements, the connection of one half of the design to a $50\ \Omega$ load is the most usual technique. However, external $50\ \Omega$ terminations of unused probe ports operating at this frequency range are expensive. Therefore, an on-chip $50\ \Omega$ resistor was used. This element was placed behind the pads and could therefore be easily disconnected by FIB technique or ultrasonic manipulator to allow mounting on an appropriate substrate. The overall size of the IC is $530 \times 690\ \mu\text{m}^2$, including bonding pads.

D. Isolation techniques

Isolation in ICs operating at millimeter-wave using technology with low resistivity silicon substrate is highly critical. Therefore, special emphasis has to be placed on reducing the cross-talk within the circuit.

1) *Differential design*: As highlighted in section III-A, an essential design technique to improve the isolation is the use of a differential architecture. A fully differential circuit design approach allows rejecting common-mode effects such as supply and substrate noise [11].

2) *DC filtering network*: The supply voltage port of each single stage of the entire amplifier is blocked by an efficient DC filter made by several capacitors placed in parallel (see

Fig. 5). In order to minimize the interconnection parasitics, the capacitors are placed in close vicinity of the amplifier core [12].

Fig. 5. Schematic of the DC filtering network (the capacitors C1 and C2 are describing the distributed concept of the architecture)

3) *Signal grounding path*: For high frequency applications like 79 GHz automotive radar, signal grounding techniques are essential requirements for optimum isolation [13]. To prevent cross-talk between stages through the substrate path, the individual stages are isolated from each other by controlling the substrate potential at their boundaries. To provide this function, substrate contacts are distributed at the periphery of each sub-circuit. By this action, the substrate coupling takes place mainly between components within a stage.

4) *pad shield*: The isolation is an issue at the interfaces of an integrated circuit. Indeed, at the input and output of an IC, the large area consumed by a signal bond pad has to be considered as a receiver of substrate noise. To reduce the parasitics caused by the pads, the bottom-most metal layer can be placed under the signal pads, providing a pad shield [14].

IV. MEASUREMENTS

As explained in the previous section, the amplifier was measured single-ended using on-chip $50\ \Omega$ terminations. Because the S-parameters of the IC driven single-ended or differential are different, it was necessary to resimulate the circuit to reproduce the measurement conditions. The measurements were performed on-wafer using ground-signal-ground probes (GSG) with $100\ \mu\text{m}$ pitch. The S-parameters were measured by using a 110 GHz network analyzer. A picture of the amplifier is depicted in Fig.6.

The IC driven single-ended exhibits a gain of 10 dB (see Fig.7), corresponding to a simulated gain (differential) of 16 dB.

By using a cascode differential topology, a strong DC filtering network, bond pad shielding technique and a tight network of substrate contacts spread at the periphery and in between each stage of the amplifier, an excellent reverse isolation of -50 dB was obtained at the frequency of operation of the IC. The input matching shows a shift to lower frequencies. This could unfortunately not be corrected by using the line tuning technique (a new version is currently being realized). However, because of the excellent output and interstage matching, the overall gain is still very good.

Fig. 6. Picture of the 79 GHz amplifier

Fig. 7. Measured S parameters of the 79 GHz amplifier

V. CONCLUSION

An amplifier with high performance such as high gain, excellent reverse isolation and low power consumption (90mW at 3 V supply voltage) was presented. The IC uses a fully differential multi-stage cascode topology, a strong DC filtering, substrate contacts tightly placed along the circuit and tunable thin-film microstrip line technique. The IC was measured single-endedly using on-chip $50\ \Omega$ terminations and exhibits a single-ended gain of 10 dB corresponding to a (simulated) differential gain of 16 dB. By using all the previously stated design techniques, an excellent wide-band reverse isolation was obtained at the design frequency.

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