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24 and 36 GHz SiGe HBT Power Amplifiers

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Abstract—We present in this paper two amplifiers using the SiGe HBT technology, operating at 24 GHz and 36 GHz, respectively. The first amplifier was designed to operate in the 24 GHz ISM band, especially for traffic and automotive applications. In the next step, this amplifier was improved to reach higher frequencies. Both amplifiers show a gain higher than 20 dB, a good matching as well as a high output linearity.

I. INTRODUCTION

The increasing demand for low-cost technology capable of high performance, such as low noise, high gain and high linearity led to the emergence of SiGe Heterojunction Bipolar Transistors (HBTs). SiGe HBTs have already demonstrated their power application capabilities at low frequencies [1]. In this paper, we present two MMIC amplifiers, operating at 24 GHz and 36 GHz, respectively, with output powers exceeding 10 mW at both frequencies, sufficient in many short- and medium-range applications, even with low-gain antennas.

II. THE SiGe HBT TECHNOLOGY

The technology used to design these amplifiers is the second generation of the commercially available Si/SiGe HBT process of Atmel GmbH (Germany) [2]. The technology offers transistors with an effective emitter width of $0.5 \mu\text{m}$. Selective collector implants provide devices with $f_T=50 \text{ GHz}$, or $f_T=80 \text{ GHz}$ with reduced breakdown voltage.

Both amplifiers are realized on a wafer with a resistivity of $20 \Omega\text{cm}$.

The standard transistor cell has single collector, emitter, and base contact areas (ceb). By using a different transistor configuration, the parasitics of the access contact can be decreased. The influence of the various transistor configurations on the rf performance has been analyzed. The addition of an extra base electrode (cbeb configuration) decreases by two the base access resistance. It allows to reach a f_{max} of 70 GHz. Due to the parasitic capacitance associated with the lateral contact topology, the f_T drops by 5 GHz. An additional collector electrode (cbebc configuration) allows to reach a f_{max} of 75 GHz. A basic schematic of the transistor is shown in Figure 1.

Fig. 1. Schematic of transistor with a cbebc configuration

III. CIRCUIT DESIGN

A first step in the design of these amplifiers was to choose an appropriate transistor configuration. As pointed out, a transistor with 2 electrodes to connect the intrinsic collector was selected due to its excellent rf performance ($f_T=75 \text{ GHz}$, $f_{\text{max}}=75 \text{ GHz}$), with an effective area of $0.5 \times 19.7 \mu\text{m}^2$ for each finger. The optimum gain is obtained at a current density of $1.6 \text{ mA}/\mu\text{m}^2$. The transistors with this given topology have been modeled using the compact MEXTRAM model [3].

A. 24 GHz amplifier

In order to obtain a high gain, as well as a better bandwidth and stability, a cascode topology was used. Three stages and an appropriate reactive interstage matching were needed to reach the targeted gain (in excess of 20 dB) and bandwidth. The stages have been designed to operate at a supply voltage level of 3 V. The circuit schematic of an individual stage is shown in Figure 2.

Fig. 2. Circuit schematic of one stage of the amplifier

For increased linearity and input matching purposes, a reactive emitter degeneration has been added to the common-emitter transistor of the standard cascode circuit topology. At a current level with a reasonable gain for the three stage amplifier, the circuit has shown an instability tendency at the design frequencies, due to a positive feedback on the supply voltage line. Therefore, an RLC filter network has been used to efficiently suppress cross coupling between individual stages. A schematic of this filter is shown in Figure 3.

Fig. 3. RLC filter network schematic

The three depicted capacitors which are connected to a single node are indicating the distributed placement of the capacitors in the layout which can be seen in Figure 4. Here, the complete chip, pads included, has a size of $380 \times 655 \mu\text{m}^2$.

Fig. 4. Layout of the 24 GHz amplifier

B. 36 GHz amplifier

The 36 GHz amplifier basically uses the same topology. The LC matching network has been modified for the higher operation frequency. To additionally improve the interstage matching, a spiral inductor has been added to the base of each transistor in common emitter configuration. Due to the placement of these lumped components, the layout of the 36 GHz amplifier is slightly larger ($380 \times 822 \mu\text{m}^2$). The complete chip is shown in Figure 5.

Fig. 5. Layout of the 36 GHz amplifier

the linearity of the amplifiers, a signal generator and a spectrum analyzer were used. The losses of the whole setup (8 dB at 36 GHz) were measured in a first step, in order to obtain the corrected input and output powers.

A. Small signal measurements

The 24 GHz amplifier reaches a gain of 22 dB at the operation frequency, with a 3 dB bandwidth of 6 GHz. The overall current drain is about 48 mA at a supply voltage of 3 V. The gain of the amplifier as well as the input and output reflection coefficients are shown in Figure 6 and Figure 7, respectively.

Fig. 6. Gain of the 24 GHz amplifier in a 50Ω test environment

Fig. 7. Input and output reflection coefficients of the 24 GHz amplifier

IV. MEASUREMENTS

S-parameters and large signal measurements were performed on wafer in a 50Ω test environment. To characterize

The 36 GHz version reaches a gain of 20.7 dB, with a 3 dB bandwidth of equally 6 GHz. The overall current drain is about 46 mA at a supply voltage of 3 V. The gain of the amplifier in a 50 Ω test environment as well as the input and output reflection coefficients are shown in Figure 8 and Figure 9, respectively.

Fig. 8. Gain of the 36 GHz amplifier in a 50 Ω test environment

Fig. 9. Input and output reflection coefficients of the 36 GHz amplifier

Both amplifiers show a return loss better than -10 dB for the input and the output, at the operating frequency. In particular due to the RLC filter network, the reverse isolation is higher than 40 dB, as can be expected for a cascode type amplifier.

B. Large signal measurements

The 1 dB output compression point of the 24 GHz amplifier is +4.1 dBm at a supply voltage level of 3 V. The output linearity is limited by the applied supply voltage and the current level in the transistors. By increasing the supply voltage ($V_{cc}=7$ V), an output power of +12 dBm was obtained. Due to the fact that the transistors were not operating at the optimum current density anymore, the gain has dropped by 4.3 dB to the value of 17.7 dB. The DC current drain corresponding to this bias point is 85 mA. The measured linearity of the 24 GHz amplifier is presented in Figure 10.

The 1 dB output compression point of the 36 GHz amplifier is +4.4 dBm when biased at 3 V. By increasing the

Fig. 10. Gain of the 24 GHz amplifier in a 50 Ω test environment as a function of the input power level

supply voltage ($V_{cc}=7$ V), +10 dBm were reached. Like for the 24 GHz amplifier, the corresponding gain is lower for this bias point and reaches 15.3 dB. The DC current drain corresponding to this supply voltage level is 94 mA. The measured linearity of the 36 GHz amplifier is presented in Figure 11.

Fig. 11. Gain of the 36 GHz amplifier in a 50 Ω test environment as a function of the input power level

With the 7 V supply voltage, both transistors of the cascode cell operate beyond the BV_{CEO} of the transistors ($BV_{CEO} = 2.5$ V). The common-emitter transistor has a collector-emitter voltage of 3.5 V, the common-base transistor of 3.1 V. This is admissible because of the relatively low equivalent input resistance of the base bias sources (approximately 5 k Ω and 1.5 k Ω for the common-emitter and common-base transistors, respectively).

V. CONCLUSION

Two integrated power amplifiers with 3 stages were simulated and measured. The measured linear gain at the operating frequency is 22 dB and 20.7 dB, for the 24 GHz and the 36 GHz amplifier, respectively. The 1 dB output compression points are +4.1 dBm and +4.4 dBm at a supply voltage level of 3 V. By applying a higher voltage level, to reach the highest available output power, +12 dBm and +10 dBm were measured for the 1 dB output compression

points, respectively. This shows that SiGe HBTs are good candidates for power applications also at high frequencies.

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