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SiGe Millimeter-Wave Dynamic Frequency Divider with Enhanced Sensitivity Incorporating a Transimpedance Stage

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Abstract—A Si/SiGe bipolar dynamic frequency divider designed for 77GHz/79GHz automotive radar is presented, which uses a transimpedance amplifier topology to improve sensitivity and operational bandwidth. Capable of operation for input frequencies from 25 GHz up to 93 GHz, the divider consumes only 35 mA at 5 V supply voltage and has a very compact die area of 295 x 475 μm^2 . In addition, measurements show that the divider operates in the full radar frequency band (76 GHz-81 GHz) up to a temperature of 100°C.

I. INTRODUCTION

Consumer electronics is about to enter the millimeter-wave range on a broad scale, as evidenced by plans to implement wireless local area networks in the 60 GHz range, or the increasing use of the 76-81 GHz band for automotive long-range and short-range radar (LRR and SRR, respectively) systems. The significant cost of current front-end implementations, however, is still a problematic obstacle, which may be overcome by switching to Si-based technologies. Si-based technology offer, most importantly, the potential for highly multi-functional monolithic integration, reducing assembly cost, and an unproblematic scale-up to large-volume production. Si/SiGe heterojunction bipolar transistor (HBT) technology is at the forefront of this development. Especially for 77 GHz automotive radar applications, outstanding IC implementations [1]–[3] clearly demonstrated the potential of SiGe HBTs.

An important task is now to assemble the necessary building blocks for multi-functional ICs, which may finally comprise a complete radar sensor, for example. Special emphasis has to be paid to high area efficiency and low power consumption. In this spirit, the authors present a 1:2 dynamic frequency divider block, which derives its excellent performance in terms of power consumption, high input sensitivity, and broad operational bandwidth from the inclusion of a transimpedance stage in the loop amplifier, while consuming a die area of only 295 x 475 μm^2 . Because operation at elevated temperature is a critical issue in many applications (e.g. automotive), operation of the divider has been validated up to 100°C.

II. SiGe:C TECHNOLOGY AND DEVICES

This circuit was designed on a 0.25 μm SiGe:C BiC-MOS technology [4]. In this process the HBT module is introduced after gate spacer formation and before CMOS source/drain implantation. The bipolar module is constructed without an epitaxially buried subcollector and deep trenches. Particularly, its key device features are the formation of the whole HBT structure in one active area without shallow trench isolation (STI) between emitter and collector contacts and the complete lateral enclosure of the highly doped collector wells by STI side walls. This design reduced device dimension, collector resistance, and parasitic capacitances significantly. The standard HBTs have a drawn emitter width of 0.21 μm , and feature f_T/f_{max} values of 190 / 190 GHz (at $V_{CE} = 1.5$ V), and a breakdown voltage $BV_{CEO} = 1.9$ V.

III. DESIGN PHILOSOPHY

A. Basic principle

The circuit is based on a regenerative dynamic frequency divider topology. A block diagram of the basic principle is shown in Fig. 1.

Fig. 1. Principle diagram of the dynamic frequency divider.

By feeding back the output signal to one of the two inputs of the mixer a division by two can be generated. Let f_{in} be the input and f_{out} be the output frequency. The mixer output then contains spectral components at the second-order mixing products $f_{in} \pm f_{out}$. Because of the deliberate low-pass filter characteristic built into the feedback loop, only the difference $f_{in} - f_{out}$ is amplified and fed back to the mixer input node. Higher-order spectral components are naturally rejected and no extra filtering is required. Because we have $f_{out} = f_{in} - f_{out}$, we get $f_{out} = f_{in}/2$.

Fig. 2. Complete schematic of the regenerative dynamic frequency divider with transimpedance topology.

B. Circuit description

The core of the IC is based on a double-balanced Gilbert cell mixer topology.

As an important modification to the original concept, a differential common-emitter transimpedance amplifier stage [5] is cascaded with the outputs of the switching quad, whose bias current is set by an extra current mirror. The transimpedance amplifier improves greatly the operational bandwidth due to the generated mismatch within the loop (as demanded by the broadband amplifier theory) and improves the sensitivity as well, due to its additional gain.

The output of the transimpedance stage feeds two cascaded common-collector buffer stages, which simultaneously act as level shifters. The differential output of the second stage is then directly coupled to the Gilbert cell mixer's switching quad. The common-collector output buffer, which is designed to drive the $2 \times 50 \Omega$ output load directly, receives its input signal from the output of the first common-collector stage, improving the isolation between the output and the feedback loop. The use of simple emitter followers was preferred over more complicated topologies found in some other published designs, because it reduces the chip area and the power consumptions, and because simulations suggested that it was perfectly adequate in terms of output power, sensitivity and bandwidth of operation for the intended application (especially the 76-81 GHz automotive radar band), when combined with the transimpedance amplifier stage in the loop.

In order to reach the optimum speed, the transistors are biased at the optimum current in respect to f_T , which coincides with the current for optimum f_{max} in

this technology. Additional transistors connected as level-shifting diodes reduce the maximum V_{CE} in the emitter followers to safe levels.

The divider was designed with a differential architecture to facilitate packaging later on, but the prototype can be characterized single-ended as well due to an on-chip termination of the unused port. A detailed schematic of the divider is presented in Fig. 2.

IV. LAYOUT

The layout of millimeter-wave ICs is always critical. For the dynamic divider, the most critical element is the feedback path which has to be optimized to decrease the parasitics created by the interconnect lines. A die photo of the circuit is depicted in Fig. 3. The chip consumes a die area of $295 \times 475 \mu\text{m}^2$ mostly dominated by the ground-signal-ground-signal-ground (GSGSG) bonding pads.

For measurements, the divider is driven by a capacitively coupled single-ended signal at one of the input nodes (the upper input port in Fig. 3), while the unused input node is connected to an on-chip 50Ω polysilicon resistor. Likewise, one of the output ports (the lower one in Fig. 3) is terminated on chip. The resistors are placed at the outside of the GSGSG pad arrangement. Hence, these elements can be easily removed after on-chip measurements to allow mounting on an appropriate substrate. Because of this technique, GSG wafer probes can be used instead of a GSGSG configuration.

Fig. 3. Picture of the dynamic frequency divider.

V. MEASUREMENTS

A. Sensitivity measurements

Measurement of ICs beyond 50 GHz are always challenging. In this chapter, the measurement procedure is described. The values of sensitivity also include best-effort estimates of losses.

The dynamic frequency divider was measured in a first step up to 70 GHz. The signal is generated by the Agilent E8257D signal generator, whose waveguide output is converted to coaxial by a waveguide-to-coaxial transformer. This element is then connected to 110 GHz GS 100 μm Picoprobe probes via a 1 mm coaxial cable. The output signal was detected by using the Agilent E2448A spectrum analyzer. As explained in section IV, by using on-chip 50 Ω polysilicon resistors, single-ended probes can be used instead of differential ones. The resulting measured sensitivity is represented in Fig. 4.

Fig. 4. Sensitivity measurements of the frequency divider up to 70 GHz (including estimate of losses).

Measurements were taken in 5 GHz increments. The

lowest frequency of operation appears to be between 20 GHz and 25 GHz.

The measurements of the divider for W band were performed using the Agilent E8257D signal source and the Millimeter Wave Source Module S10MS-AG to reach the 75 GHz-110 GHz region. The measured sensitivity of the circuit in the W band region is depicted in Fig. 5. The IC divides input frequencies up to 93 GHz.

Fig. 5. Sensitivity measurements of the frequency divider up to 95 GHz (including estimate of losses).

B. High temperature measurements

Because this IC is intended for use in automotive applications, the divider was also measured at higher temperatures. The performance of the circuit was assessed on-chip with a heatable chuck in the W band range. The temperature was increased from 25°C up to 100°C. The resulting performance are displayed in Fig. 6.

Fig. 6. Sensitivity of the dynamic frequency divider over temperature in $^{\circ}\text{C}$ (including estimate of losses).

As it can be seen, the sensitivity decreased with increased temperature (expected). However, up to 100°C, the divider operates over the complete automotive radar frequency range (76-81 GHz). Therefore this circuit appears well suited for these applications.

TABLE 1

Performance comparison with published Silicon based frequency dividers

	unit	[6]	[7]	[7]	[8]	[9]	This work
Topology		static	dynamic	static	dynamic	dynamic	dynamic
f_{max}	GHz	96	103.16	71.5	110	100	93
Power Consumption	mW	770	205.4	140	310	285	175
Technology	μm	0.13	0.25	0.25	0.15	0.12	0.25
Die area	$\mu\text{m} \times \mu\text{m}$		1000 x 500	1000 x 500	550 x 450		295 x 475
Speed/power	GHz/mW	0.13	0.50	0.51	0.35	0.35	0.53

VI. CONCLUSION

A regenerative dynamic frequency divider with transimpedance amplifier topology was presented. The divider operates over a wide frequency range (from 25 GHz to 93 GHz) with good sensitivity. In order to save a large amount of power the output buffer was extremely simplified. This simplification of the circuit architecture leads to a power consumption of only 35 mW at a supply voltage of 5 V and a compact die area of $295 \times 475 \mu\text{m}^2$. Because the divider was designed to be implemented in a 77 GHz LRR / 79 GHz SRR system, the temperature behavior was verified from room temperature to 100°C. The divider still shows good performance also in such a critical environment.

Table I shows an overview of previously published millimeter-wave frequency dividers. The presented design has the smallest chip area as well as the best ratio of highest operating speed vs. power consumption.

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