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A Fully Integrated Fully Differential Low-Noise Amplifier for Short Range Automotive Radar Using a SiGe:C BiCMOS Technology

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Abstract—A fully integrated fully differential low-noise amplifier for 79 GHz short range radar applications using a high-speed SiGe:C BiCMOS technology is presented. The integrated circuit uses thin-film microstrip lines and exhibits compact design ($530 \times 690 \mu\text{m}^2$), low power consumption (90 mW at 3 V supply voltage), high gain (13 dB gain at 81 GHz), good linearity and reverse isolation. In order to ease the measurements of the circuit, a simple technique was used to measure single-ended the differential amplifier. To overcome possible inaccuracy of the line model, shorting bars are placed along these elements to allow easy correction and to avoid redesign.

Index Terms—Millimeter wave bipolar transistor amplifiers, heterojunction bipolar transistors.

I. INTRODUCTION

Until recently, millimeter wave applications were the field of III-V technologies such as GaAs field effect transistors (FETs). However for several years outstanding integrated circuits (ICs) using Si/SiGe heterojunction bipolar transistor (HBT) technologies have been demonstrated [1]–[4]. 79 GHz short range radar (SRR) and 77 GHz long range radar (LRR) are attractive applications for silicon based technologies. Indeed, up to now, such radars uses GaAs technologies, making an increase in circuit complexity and mass market scale-up a difficult challenge. Therefore, Si based technology would be more appropriate. At this frequency range, packaging becomes highly critical due to the thick substrate and the lack of backside metallization. Most of the published amplifiers designed for SRR/LRR are using single-ended or two symmetrical single-ended amplifiers making the mounting of these ICs complex. In this work, a fully integrated fully differential low-noise amplifier (LNA) for SRR applications is presented. This IC shows a high gain over a wide temperature range, small die area, good linearity and reverse isolation. The circuit uses multi-stage cascode topology and thin-film microstrip lines (TFMSLs). A simple design feature was implemented in order to ease the measurements of the differential amplifier. Temperature-dependent measurements were also performed in order to show the performance of the IC under critical conditions.

II. SiGe:C TECHNOLOGY AND DEVICES

The circuit was designed in IHP's $0.25 \mu\text{m}$ SiGe:C BiCMOS technology SG25H1 which offers transit frequencies around 200 GHz [5]. In this process the HBT module is introduced after gate spacer formation and before CMOS source/drain implantation. The bipolar module is constructed without epitaxially-buried subcollector and deep trenches. Particularly, its key device features are the formation of the whole HBT structure in one active area without shallow trench isolation (STI) between emitter and collector contacts and the complete lateral enclosure of the highly doped collector wells by STI side walls. This design reduced device dimension, collector resistance, and parasitic capacitances significantly. The standard HBTs have a drawn emitter width of $0.21 \mu\text{m}$, f_T/f_{max} values of 190 / 190 GHz (at $V_{CE} = 1.5 \text{ V}$), and breakdown voltage $BV_{CEo} = 1.9 \text{ V}$. For TFMSL design, the $2 \mu\text{m}$ thick fourth Al metal layer was used as the signal line. The silicon nitride MIM capacitor has a capacitance density of $1 \text{ fF}/\mu\text{m}^2$.

III. DESIGN PHILOSOPHY

Three stages were necessary in order to reach high gain. At such high frequencies, the Miller effect is a critical issue in bipolar devices. However, by using a cascode topology, this parasitic effect can be drastically reduced. As pointed out in section I, the lack of backside metallization and the thick silicon substrate make the packaging of ICs operating in the mm-wave range highly critical. However, such issues can be easily overcome by using a differential topology. Differential ICs have major advantages:

- Due to the virtual ground node, mounting and packaging technique is drastically simplified. On- and off-chip decoupling of supply voltages is less critical. [6]
- On-chip noise generation is reduced [7].

The main drawback of differential ICs is their characterization. Four-port measurements imply a cost increase that however was mediated in this work by a very simple but efficient technique (see section VI-A). To provide good matching conditions, an LC matching network was used at the output of each stage to match the input of the

next stage or the $50\ \Omega$ output load of each half of the differential IC. As current source an LC resonator was preferred to standard transistor or resistor based topologies. Because of the low DC resistance across the resonator, the supply voltage can be strongly reduced in order to decrease the power consumption and therefore to enable a higher integration level. A schematic of a single stage of the complete LNA is depicted in Fig. 1. Because of the high operation frequency of the LNA, TFMSLs offer good performance and still allow a compact layout. Therefore, a topology based on TFMSL was investigated.

Fig. 1. Schematic of a single stage of the differential amplifier.

IV. THIN-FILM MICROSTRIP LINES

A wide variety of lines can be used for circuit design. However, for silicon based technologies, because of the lack of backside metallization, the high frequency and the lossy substrate ($50\ \Omega\cdot\text{cm}$ in this work) many line topologies are useless [8]–[10]. Here, a TFMSL based IC was preferred. The bottom-most available metal layer was used as the ground plane and the top-most as the signal line. The main advantages of TFMSL are a good accuracy of electromagnetic field (EMF) simulators, simplicity of the resulting layout (compared for instance with a CPW based design), a similar quality factor compared with spiral inductors on silicon substrate and moreover the possibility to tune the inductance to lower or higher values by cutting the lines (see section V).

V. LAYOUT

The major drawback of TFMSL is their space consumption. To correctly match the input of their respective next stage, the line connected to the collector of the first and second cascode stage had a simulated line

length of more than $200\ \mu\text{m}$. However, by folding these elements, it was possible to keep the IC compact. As it can be seen in Fig. 2, the $100\ \mu\text{m}$ ground-signal-ground (GSGSG) bonding pads are the elements requiring the biggest area. The IC has a total die area of $530 \times 690\ \mu\text{m}^2$. A strong advantage for TFMSLs is the possibility to modify their length on-chip. By creating shorting bars along a folded line, its equivalent electrical length can be modified by cutting these lines. This cuts can be performed using laser cutter (e.g. $532\ \text{nm}$ pulsed green laser), focused ion beam (FIB) or a needle connected to an ultrasonic manipulator. These bars were placed every $12.5\ \mu\text{m}$ and can be seen as well in Fig. 2. In order to ease the cutting, a narrow passivation window was opened on top of the TFMSLs. Because of the very low area uncovered and the possibility to correct easily possible inaccuracy, this minor modification was not included in the model. Only one DC needle is necessary to feed the three stages. However, if necessary, the three cells could be biased independently. Indeed, three pads connected by a removable metal lines are available on the chip.

Fig. 2. Picture of the chip.

VI. CIRCUIT PERFORMANCE

A. S-parameters measurements and simulated noise figure

As pointed out in section III, differential ICs need a complex measurement setup. For characterization of differential amplifiers, the connection of one half of the IC to $50\ \Omega$ terminations is the most usual technique. However, due to the high frequency, such elements are expensive. Hence, an on-chip $50\ \Omega$ resistor was placed behind the signal pads at the input and output on one side of the IC, therefore providing an on-chip $50\ \Omega$ termination. The measurement condition was simulated in a first step in order to anticipate possible problems generated by the parasitics created by the $50\ \Omega$ polysilicon resistors. However, such elements were found to be completely uncritical. The resistors can be easily removed after on-chip measurements in order to package the IC. The amplifier consumes 30 mA at 3 V supply voltage. The S-parameters of the IC were measured on-chip using $100\ \mu\text{m}$ Cascade Infinity i110 GSG probes with a 110 GHz network analyzer (Agilent 8510XF). The first measured IC had TFMSLs cut with lengths as simulated. Due to a slight inaccuracy, the peak of gain was located at 72 GHz. Therefore, the lines were cut with approximately 10 % smaller length. The resulting S-parameters are depicted in Fig. 3. In order to obtain the corresponding gain of the LNA driven differentially, 6 dB should be added to the gain of the amplifier driven single-ended. This was checked by both theory and simulation. The noise figure could not be measured at these frequencies. In Fig. 3, the simulated noise figure (NF) and minimum noise figure (NFmin) are displayed. At 79 GHz, the simulated amplifier NF is approximately 8.8 dB at 79 GHz.

Fig. 3. S-parameters measurements of the LNA driven single-ended (6dB should be added to the transmission to obtain the corresponding gain of the amplifier driven differential), the minimum noise figure as well as noise figure values are simulated (measurements could not be performed).

Because the frequency of optimum output matching is still located too high (84 GHz instead of 79 GHz) higher gain is still expected (a different TFMSL length configuration was investigated in simulation, at least 2 dB improvement is expected). As it can be seen, the input matching is shifted to lower frequency. Unfortunately, this could not be modified by using different line lengths. Because of excellent isolation techniques such as pad shielding, the use of the cascode topology, a tight network of substrate contact, strong DC filtering network [11]–[13], the reverse isolation is excellent over a very wide frequency range (better than 40 dB from 0.1 GHz to 110 GHz).

B. S-parameters measurements over temperature

In order to evaluate the performance of the IC under critical conditions, S-parameters were performed over a wide temperature range (between 25 °C and 85 °C). The corresponding measured transmission is displayed in Fig. 4. As it can be seen, the gain decreases by approximately 4 dB.

Fig. 4. Transmission measurements for various temperatures in °C (6dB should be added to the transmission to obtain the corresponding gain of the amplifier driven differential).

C. Large signal measurements

Because of the cross-talk between transmit and receiving path of the complete SRR, the linearity of the LNA is an important requirement. The Fig. 5 shows the large signal measurements of the amplifier driven single-ended. The IC exhibits a measured $P_{1dB,in}$ of -14 dBm and a $P_{1dB,out}$ of -8.25 dBm, 3 dB should be removed to $P_{1dB,in}$ to obtain the corresponding input compression point of the amplifier driven fully differentially. Likewise, 3 dB should be added to $P_{1dB,out}$ to obtain the corresponding output compression point (this was verified by simulation).

Fig. 5. Large signal measurements of the LNA driven single-ended. These measurements were performed with an input signal of 79 GHz.

VII. CONCLUSION

A fully integrated, fully differential LNA was presented. The IC shows very good performance such as high gain, small die area, good reverse isolation and linearity. The circuit is based on a multi-stage cascode topology and uses thin-film microstrip lines. In order to correct a possible inaccuracy of the model, shorting bars were placed along the folded microstrip lines. These bars can be removed to modify the operation frequency of the amplifier and reach the targeted frequency band.

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