Copyright © 2008 IEEE

Reprinted from

*Proc 2008 IEEE Topical Meeting on Silicon Monolithic ICs in RF Systems (SiRF),
Orlando, FL, USA, January 23-25, 2008, pp 195-198*

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Universität Ulm's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

A Compact Low-Power SiGe:C BiCMOS Amplifier for 77-81 GHz Automotive Radar

Bernd Schleicher*, Sébastien Chartier*, Gerhard Fischer[‡],
Falk Korndörfer[‡], Johannes Borngräber[‡], Till Feger* and Hermann Schumacher*

*University of Ulm, Institute of Electron Devices and Circuits, Albert-Einstein-Allee 45,
89081 Ulm, Germany, Phone: +49-731-5031593, Email: bernd.schleicher@uni-ulm.de,

[‡]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Abstract— In this paper a single-ended fully integrated Si/SiGe HBT amplifier working at a center frequency of 79 GHz is presented. The amplifier consists of three cascode stages. A trimmable line technique and an efficient DC filtering network were used. The amplifier shows a maximum measured gain of 13.2 dB at exactly 79 GHz and an excellent reverse isolation of more than 40 dB over the whole measured frequency range. Its performance was measured at different temperatures, showing a decrease of 5.3 dB in gain between room temperature and 85° C. The measured -1 dB input compression point is at -15 dBm. The power consumption is 52 mW at a supply voltage of 2.7 V. The circuit has a compact layout and consumes an area of 525 x 500 μm^2 including bonding pads.

I. INTRODUCTION

Until recently, millimeter-wave applications such as 77/79 GHz automotive radars were implemented using III-V semiconductors technologies such as GaAs field effect transistors. However, these technologies are not well suited for mass market scale-up due to their high cost and low integration density. Such issues can be mediated using Si/SiGe heterojunction bipolar transistors (HBTs). With the use of these processes, the goal for the circuit designer is to use efficient topologies to obtain high performance and compact ICs.

SiGe technology offers the possibility of monolithic integration with CMOS circuit blocks in commercially available SiGe:C BiCMOS processes to allow system-on-a-chip (SoC) solutions. With this technology, applications can be targeted such as the 60 GHz ISM-band, 77/79 GHz long range and short range automotive radar or even higher frequency bands. SiGe circuits working at millimeter wave frequencies have frequently been published, e.g. around 60 GHz in [1], [2] and around 77-81 GHz in [3], [4], [5]. A critical challenge for ICs designed for automotive applications is the necessary operation over a wide temperature range. Only a few publications on circuit performance at elevated temperature and at higher frequencies can be found in the literature, e.g. [6]. This paper presents the successful monolithic integration of an amplifier at 79 GHz in a commercially available SiGe:C BiCMOS technology, with measurements at room temperature (27° C), as well as 50° C and 85° C.

II. SiGe:C BiCMOS TECHNOLOGY

The circuits were designed in IHP's 0.25 μm SiGe:C BiCMOS technology SG25H1 which offers transit frequencies f_T around 200 GHz [7]. In this process the HBT module is introduced after the gate spacer formation and before CMOS source/drain implantation. The bipolar module is constructed without epitaxially-buried subcollector and deep trenches. Particularly, its key device features are the formation of the whole HBT structure in one active area without shallow trench isolation (STI) between emitter and collector contacts and the complete lateral enclosure of the highly doped collector wells by STI side walls. The resulting shrink in device dimensions reduces collector resistance and parasitic capacitances significantly.

Fig. 1. Cross section of the used metal system

The standard HBTs have a drawn emitter width of 0.21 μm , f_t/f_{max} values of 190/190 GHz (at $V_{\text{CE}} = 1.5 \text{ V}$) and a breakdown voltage $BV_{\text{CEO}} = 1.9 \text{ V}$. For inductors the 2 μm thick fourth aluminium metal layer can be used. The silicon nitride MIM capacitor has a capacitance density of 1 fF/ μm^2 . Four different types of resistors and a metal system of four layers (with an optional fifth layer, which was not used for this design) are available as well.

III. TRANSMISSION LINES

The metal system of the used technology consists of four aluminium layers embedded in silicon dioxide and covered by a nitride passivation. In fig. 1 a detailed cross section of the top and bottom metal can be seen. Thin-film microstrip lines (TFMSL) are used to realize transmission lines in this metal system, with the ground plane at the first metal layer and the conductor line at the fourth metal layer. The TFMSL is very similar to a conventional microstrip line (MSL), except for the far smaller dielectric spacing between the conductor metal and the ground metal layer, which brings the thickness of the conductor metal in the range of the thickness of the dielectric spacing. Another difference to MSL is the full embedding of the conductor metal in dielectric material.

Fig. 2. Characteristic impedance of a thin-film microstrip line with width $7 \mu\text{m}$ and simulated length $500 \mu\text{m}$ including simulation and modelling

To create suitable transmission line models, electromagnetic field simulations with different width and length dimensions were performed to investigate various geometries. The characteristic impedances Z and the complex propagation coefficients γ of the simulated and modelled lines were determined with the method proposed in [8]. This method uses an even-odd-mode excitation, where

$$S_e = S_{11} + S_{12} \quad (1)$$

is the even-mode S-parameter and

$$S_o = S_{11} - S_{12} \quad (2)$$

is the odd-mode S-parameter. Then the characteristic impedance

$$Z = Z_0 \cdot \sqrt{\frac{1 + S_e}{1 - S_e} \cdot \frac{1 + S_o}{1 - S_o}} \quad (3)$$

and the complex propagation constant

$$\gamma = \frac{2}{l} \cdot \text{arctanh} \left(\sqrt{\frac{1 + S_o}{1 - S_o} \cdot \frac{1 - S_e}{1 + S_e}} \right) \quad (4)$$

can be derived, where l is the length of the simulated or modelled line. With the help of $\gamma = \alpha + j\beta$ the attenuation coefficient α and the phase coefficient β can be separated. From β , the phase velocity v_{ph} follows as

$$v_{ph} = \frac{2\pi f}{\beta} = \frac{c_0}{\sqrt{\epsilon_{r,eff}}}, \quad (5)$$

where f is the frequency, c_0 is the speed of light and $\epsilon_{r,eff}$ is the effective relative dielectric constant.

Because of its similarity with standard microstrip lines, a model of the TFMSL was performed using a slight modification of the MSL model provided in the library of Advanced Design System (ADS) from Agilent. It was seen that by increasing the permittivity and the length of the given model a good agreement between EM simulation and modified model was obtained. The remaining parameters (dielectric and metal thicknesses, conductivity, conductor width, ...) did not have to be modified. Table I shows a summary of corrected values for the length and ϵ_r for a simulated reference line length of $500 \mu\text{m}$ and different widths.

TABLE I

CHANGES FOR THE USE OF THE MODIFIED MSL-MODEL WITH DIFFERENT WIDTHS AND A SIMULATED REFERENCE LENGTH OF $500 \mu\text{m}$

Width	Impedance Z_0	Length	Length increase	ϵ_r
$1.75 \mu\text{m}$	76Ω	$560 \mu\text{m}$	12 %	5.5
$7 \mu\text{m}$	47Ω	$540 \mu\text{m}$	8 %	4.7
$20 \mu\text{m}$	24Ω	$500 \mu\text{m}$	0 %	4.8

A comparison between modelled and simulated line can be seen in fig. 2 for the characteristic impedance of 47Ω on a line with $7 \mu\text{m}$ width and $500 \mu\text{m}$ length.

Fig. 3. One stage of the three-stage amplifier with additional input network of the first stage

IV. CIRCUIT TOPOLOGY AND LAYOUT

Among the different options for the gain cells, a three-stage cascode topology was chosen because of its high gain and good reverse isolation, and was biased with a current mirror structure. The schematic of the individual stage can be seen in fig. 3, where T_3 and T_4 forms the cascode and T_1 and T_2

the current mirrors of the biasing part. Current mirror biasing for both transistors was chosen, because it is more suitable for varying temperatures compared to resistor based biasing techniques. The capacitance C_1 provides an AC grounding for transistor T_3 . As load and output matching components, the TFMSL and the capacitance C_2 were used. It was found that with these two components only, a matching to 50Ω as well as between the stages could be achieved.

Fig. 4. Picture of the amplifier circuit (die area: $525 \times 500 \mu\text{m}^2$)

In addition, the capacitance C_2 galvanically separates the stages. The input matching of the first cascode stage was achieved by the input capacitance C_{in} and the transmission line TFMSL_{in}. Because of the presence of a ground shield in the lower metal below the input and output pads, they were approximated during the design using a simple parallel plate assumption

$$C_{Pad} = \frac{\epsilon_0 \epsilon_r A}{d} \approx 40 \text{ fF}, \quad (6)$$

where A is the area of the pad and d is the distance between pad and ground plane. For the output pad capacitance the matching network of the last cascode stage itself can be used. The TFMSL of the shorting network consists of an extended U-shape with crossing bars placed in between as proposed in [9]. This ladder structure can be cut on-chip by a focused ion beam, a laser cutter or a micromanipulator to give the chip a wide range of possible line lengths without further redesigns. This makes the circuit trimmable and was used to counterbalance the inaccuracy of the line models. The chip is designed for a single supply voltage, but, by cutting the connecting metal between the DC pads, each of the three stages could be supplied separately (which was not necessary here).

As proposed in [10], efficient interstage decoupling as well as DC blocking is provided on chip. Therefore large parallel blocking capacitances were placed on-chip between the power supply branches of each stage to provide a good RF isolation. Furthermore a high density of substrate contacts was placed to reduce crosstalk via the substrate path. For the same reason the pads were shielded by a ground metallization below the

pads. The circuit is fully integrated on a single chip. A picture of the amplifier can be seen in fig. 4. The chip has a die area of $525 \times 500 \mu\text{m}^2$ including the supply and measurement pads.

Fig. 5. Measured S-parameter of the amplifier at room temperature

V. MEASUREMENT RESULTS

A. Small-Signal Measurements

The small signal measurements were performed on-wafer with a 110 GHz network analyzer using GSG-probes with a pitch of $100 \mu\text{m}$. The measured S-parameters of the amplifier at room temperature (27°C) can be seen in fig. 5. The maximum gain of the amplifier is 13.2 dB at exactly 79 GHz. Because of the cascode topology and the isolation techniques used, the amplifier shows an excellent reverse isolation of better than 40 dB over the whole frequency band. The output matching at the targeted frequency of operation is better than -10 dB, while the maximum of the input return loss shows a shift to lower frequencies. The reason for this might be explained by an underestimation of the pad capacitance and TFMSL inductance. This was mediated at the output by using a different TFMSL length, but the same technique could not be performed at the input.

Fig. 6. Measured magnitude of S_{21} at different temperatures

B. Measurements Over Temperature

To investigate the suitability of the amplifier circuit with varying temperature, the IC was measured with the same setup at 50°C and 85°C using a heatable wafer chuck. The measured transmission can be seen in fig. 6. At increasing temperature the gain at 79 GHz is decreasing from 13.2 dB at 27°C, to 11 dB at 50°C and 7.8 dB at 85°C. The temperature affects mostly the gain, the influence on the other S-parameters is comparably small. This can be seen in fig. 7 for the reflection coefficients S_{11} and S_{22} . The influence of temperature on reverse isolation S_{12} is neglectable. Because the provided biasing technique was not sufficient to compensate the influence of temperature, a different solution will have to be provided in the future.

Fig. 7. Measured reflection coefficients at different temperatures

C. Linearity Measurements

Additionally linearity measurements at 79 GHz were performed on-wafer. The -1 dB input compression point was measured at -15 dBm which can be seen in fig. 8. The circuit power consumption is 52 mW at a 2.7 V voltage supply.

Fig. 8. Measured gain versus input power to show the linearity of the circuit

VI. CONCLUSION

In this paper an amplifier operating at 77-79 GHz is presented. The amplifier consists of a three stage cascode topology and is fully integrated using a commercially available SiGe:C BiCMOS technology. The layout includes variable matching lines to allow tuning of the frequency, as well as a DC filtering and isolation network to prevent unwanted coupling between the stages. The measurements of the amplifier show a high gain of 13.2 dB at 79 GHz, an excellent reverse isolation of 40 dB over the whole measured range and an input compression point of -15 dBm. The circuit performance was measured over a wide temperature variation in order to verify the behaviour of the IC under critical environment.

ACKNOWLEDGMENT

The authors would like to acknowledge the team at IHP for the fabrication of the chip and the measurement of the S-parameters, Holger Höhnemann and the team at ATMEL for the cutting of the transmission lines and the team at Fraunhofer IAF for the linearity measurement. This work was funded by the German Ministry of Education and Research (BMBF) through the KOKON collaborative research project.

REFERENCES

- [1] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe Bipolar Transceiver Circuits Operating at 60 GHz," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 156–167, January 2005.
- [2] Y. Sun, J. Borngreber, F. Herzel, and W. Winkler, "A Fully Integrated 60 GHz LNA in SiGe:C BiCMOS Technology," in *Proceedings of the 2005 Bipolar/BiCMOS Circuits and Technology*, (Santa Barbara, CA, USA), pp. 14–17, October 2005.
- [3] B. Dehlink, H.-D. Wohlmuth, K. Aufinger, T. F. Meister, J. Böck, and A. L. Scholtz, "A Low-Noise Amplifier at 77 GHz in SiGe:C Bipolar Technology," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, (Palm Springs, CA, USA), pp. 287–290, October 2005.
- [4] U. R. Pfeiffer, S. K. Reynolds, and B. A. Floyd, "A 77 GHz SiGe Power Amplifier for Potential Applications in Automotive Radar Systems," in *IEEE Radio Frequency Integrated Circuits (RFIC) Systems. Digest of Papers*, pp. 91–94, 2004.
- [5] H. Li, H.-M. Rein, T. Suttrop, and J. Böck, "Fully Integrated SiGe VCOs With Powerful Output Buffer for 77-GHz Automotive Radar Systems and Applications Around 100 GHz," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1650–1658, October 2004.
- [6] R. Reuter and Y. Yi, "A 77 GHz (W-band) SiGe LNA with a 6.3 dB Noise Figure and Gain Adjustable to 33 dB," in *Bipolar/BiCMOS Circuits and Technology Meeting*, (Maastricht, Netherlands), October 2006.
- [7] B. Heinemann, H. Rucker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Hoppner, D. Knoll, D. Kruger, B. Kuck, R. Kurps, M. Marschmeyer, H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, D. Wolnsky, H.-E. Wulf, Y. Yamamoto, and P. Zaumseil, "Novel collector design for high-speed SiGe:C HBTs," in *International Electron Devices Meeting, IEDM Technical Digest*, (San Francisco, CA, USA), pp. 775–778, 2002.
- [8] Y.-C. Shih, "Broadband Characterization of Conductor-Backed Coplanar Waveguide Using Accurate On-Wafer Measurement Techniques," *Microwave Journal*, vol. 34, pp. 95–105, April 1991.
- [9] H. Li and H.-M. Rein, "Millimeter-Wave VCOs With Wide Tuning Range and Low Phase Noise, Fully Integrated in a SiGe Bipolar Production Technology," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 184–191, February 2003.
- [10] S. Chartier, E. Sönmez, and H. Schumacher, "Millimeter-Wave Amplifiers Using a 0.8 μm Si/SiGe HBT Technology," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, (San Diego, CA, USA), pp. 277–280, Jan. 2006.