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A 60 GHz, Multi-Gbps Down-Converter IC in an 80 GHz f_T SiGe Technology

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Abstract

This dissertation describes the design and characterization of low-cost 60 GHz down-converter ICs and modules for short-range multi-gigabit per second wireless communications. Low-cost semiconductor technology and packaging techniques are used for the IC and module design, making the module also suited for small volume production.

The down-converter IC, consisting of a down-converting mixer, a VCO plus frequency doubler and an analog PLL, is realized in an 80 GHz SiGe HBT technology. The high ratio of operating frequency to f_T/f_{max} makes the circuit design very challenging, requiring each building blocks to be optimized carefully. The design, simulation and optimization of the individual circuit blocks, as well as experimental results are discussed in detail in this dissertation. The complete IC achieves 5 dB conversion gain and more than 10 GHz IF bandwidth, covering the complete 60 GHz ISM band. The PLL achieves state-of-art tuning range and phase noise performance.

The down-converter IC is packaged in a module with coaxial input and output. Low-cost wire-bonding techniques are implement for the IC-to-board interconnect. To compensate the influence of the bondwires, an "L-C-L" compensating structure has been adopted, which shows 0.3 dB insertion loss at 60 GHz. The design, simulation and test results of the bondwire interconnect are discussed in detail in this dissertation. Different modules have been compared and the packaging related issues are discussed.

The packaged modules are successfully implemented in a 60 GHz wireless system with BPSK modulation. Error-free transmission up to 2 Gbit/s (limited by the transmitter) has been achieved for over a distance of 1 meter. The experimental test setup and measurement results are also shown in this dissertation.

This thesis work is the first reported 60 GHz receiver front-end using such low-cost semiconductor technology and packaging techniques.

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Chapter 1

Introduction

1.1 60 GHz Wireless Link

The 60 GHz ISM (industrial, scientific and medical) band has opened a new window for wireless communications. A very wide bandwidth has been allocated worldwide. Fig. 1.1 [1] shows the 60 GHz band unlicensed frequency spectrum in several countries. In Europe, a total bandwidth of 9 GHz (57 - 66 GHz) is allocated with peak EIRP (equivalent isotropically radiated power) of 40 dBm and 25 dBm for indoor and outdoor applications. Such wide bandwidth enables ultra-high-rate (multi-gigabit) wireless transmission with simpler modulation schemes (OOK, BPSK, QPSK etc.), which reduces the system complexity significantly.

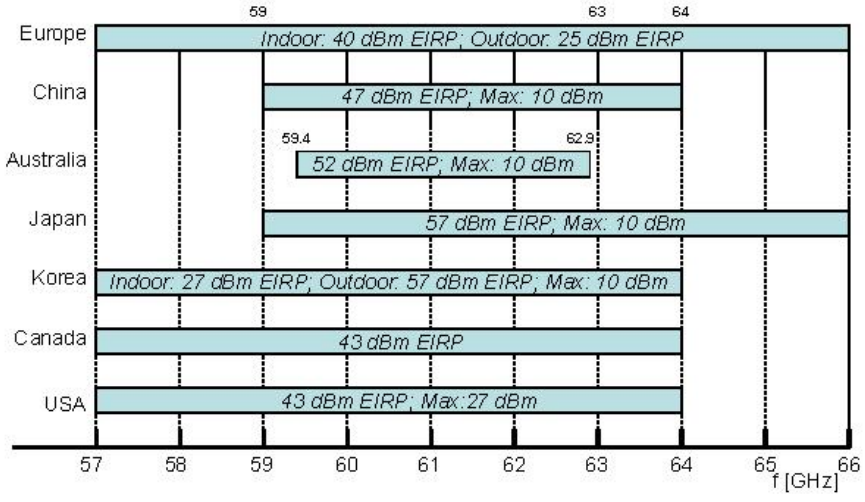


Figure 1.1: Overview of international 60 GHz ISM band frequency regulations with maximum allowed power levels.

Compared with wireless links at lower frequencies (< 10 GHz), the free space path loss at 60 GHz is much higher. Also, the atmospheric attenuation at 60 GHz is very high due to oxygen absorption, as shown in Fig. 1.2. These are drawbacks for long distance

transmissions, but are advantages for short-range (< 10 meters) communications, where interference and privacy issues are often of concern. Furthermore, high gain antennas at 60 GHz have much smaller dimensions and narrower beam widths, making high data-rate medium range (< 1 km) point-to-point links feasible.

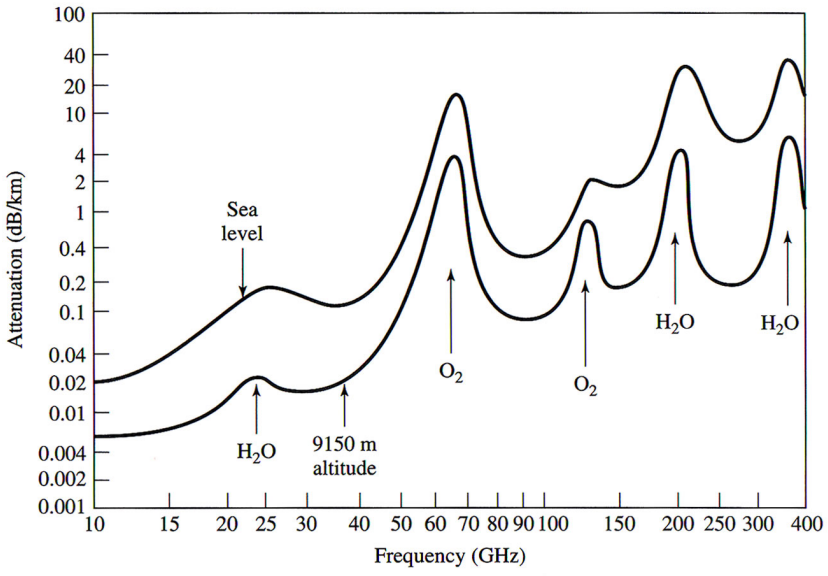


Figure 1.2: Average atmospheric attenuation versus frequency (horizontal polarization) [2].

Because of the above mentioned reasons, the 60 GHz link is very suitable for applications that requires high data-rate and operates in short-ranges, such as wireless transmission of uncompressed HDTV (high-definition television) stream, communication between PC and different peripherals, kiosk file downloading, and etc., as shown in Fig. 1.3. Therefore, wireless systems at 60 GHz have been a hot research topic in recent years.

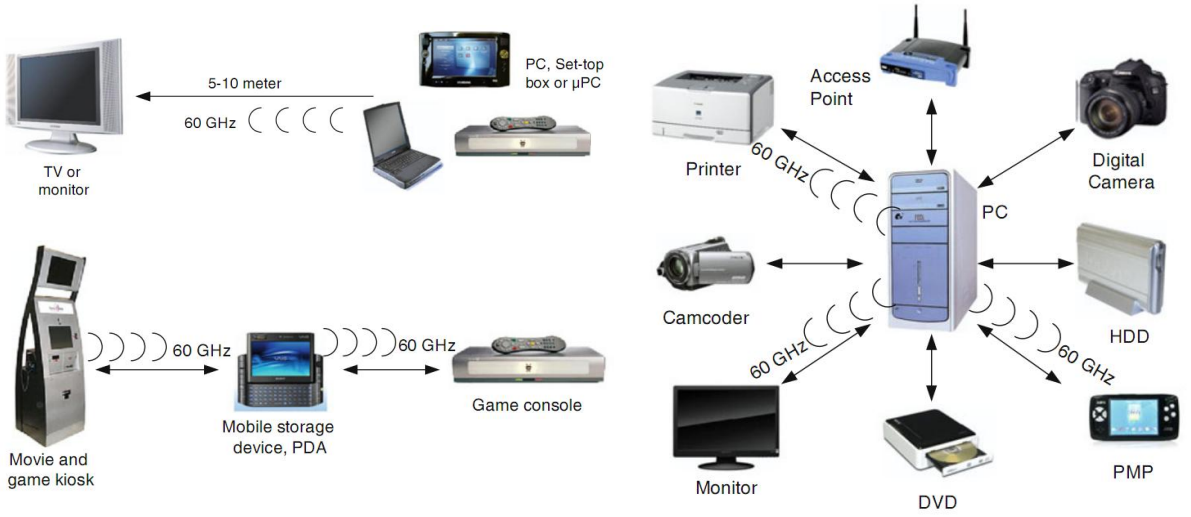


Figure 1.3: Illustration of 60 GHz applications [3].

1.2 Motivation

This thesis presents work done in the framework of the research project EASY-A (Enablers for Ambient Services and Systems - 60 GHz Broadband Links) [4], where an ultra-high data rate (10 Gbit/s) 60 GHz system for short range ($<$ 1 meter) point to point data link was to be realized. It mainly focuses on the design and characterization of the receiver front-end ICs and modules.

At the time of this thesis work, fully integrated 60 GHz front-end ICs had been reported [5–9], but all were realized in advanced semiconductor technologies (mHEMT [5, 6], SiGe BiCMOS [7, 8] and CMOS [9]). These technologies become inexpensive, only when the production volume is very high. For small volume productions, a low-cost solution is highly desirable. Therefore, this work aims to realize a 60 GHz receiver front-end by using a very cost-effective semiconductor technology (80/90 GHz f_T/f_{max}) and low-cost packaging techniques. The goal is not to achieve state-of-art performance, but rather to fully evaluate and explore the potential of the low-cost semiconductor technology and packaging techniques for millimeter-wave applications, which has been done through the following means:

- Design and optimization of 60 GHz receiver front-end building blocks and fully-integrated down-converters.
- Comparison of different circuit topologies.
- Design and characterization of bondwire interconnects for millimeter-wave packaging.
- 60 GHz receiver front-end modules fabrication, characterization and comparison.

This work is the first 60 GHz down-converter realized in such a low-cost technology. The front-end circuits achieved better performance than previously published results using the same technology. The mixer IF bandwidth, VCO tuning range, PLL locking range and phase noise are all better than or close to state-of-art results. The bondwire interconnects also show state-of-art performance and have been proved to be well suited for millimeter-wave applications. The realized receiver modules have been successfully implemented in a 60 GHz wireless system and achieved very good performance. All the details will be discussed in this thesis.

1.3 Dissertation Outline

The dissertation is organized in the following way:

Chapter 2 describes the 60 GHz wireless system and its requirements on the receiver front-end. A brief link-budget is also shown and the receiver architecture is discussed in this chapter.

Chapter 3 describes the 60 GHz down-converting mixer. An active, double-balanced mixer based on Gilbert cell topology has been realized, with a transimpedance load to extend the IF bandwidth. The design, simulation and characterization of the down-converting mixer is discussed in this chapter.

Chapter 4 discusses the LO signal generation. A VCO plus push-push frequency doubler approach has been adopted to generate the 60 GHz signal. Different versions of VCOs and frequency doublers (targeting different frequency ranges) have been realized. The design, simulation and characterization of the VCOs and frequency doublers will be discussed.

Chapter 5 describes the frequency divider design and characterization. The maximum operating frequency of static and dynamic dividers and the design guidelines are discussed. Dynamic dividers with different feedback configurations are compared in terms of maximum operating frequency, input sensitivity and output power. Multi-stage frequency dividers for different frequency division ratios (32, 64, 128) are realized, with each stage optimized individually, balancing maximum operating frequency and power consumption.

Chapter 6 describes the PLL for frequency stabilization. PLLs with different frequency division ratios have been realized, with very wide frequency locking range and low phase noise. The loop components design (PD and LF), loop simulation (loop gain, phase noise, locking time) and characterization of the PLL circuits are discussed in this chapter.

Chapter 7 shows the characterization of the complete down-converter IC and a sliding-IF receiver front-end IC.

Chapter 8 describes the packaging and module design. The ICs are packaged in a low-cost brass housing using bondwires for IC-to-board interconnect, with an "L-C-L" structure to compensate the bondwire influence. Characterizations of different compensating structures for both single-ended and differential interconnects will be shown. Design, characterization and comparison of different PLL and down-converter modules are also discussed in this chapter.

Chapter 9 shows the 60 GHz wireless transmission setup, where the down-converter module receives signals from a 60 GHz BPSK transmitter, and an analog BPSK/QPSK demodulator follows the down-converter to demodulate the data. Error-free transmission has been achieved and the experimental results are shown in detail in this chapter.

Chapter 10 summarizes this thesis work and compares it with the state-of-art results. Further improvements of this thesis work are also discussed.

Chapter 2

Design Considerations

2.1 System Requirements

The receiver is to be used in a 60 GHz wireless system targeting 10 Gbit/s data rate. The signal is D-QPSK (differential-quadrature phase shift keying) modulated and occupies a bandwidth of 4.32 GHz (59.4 - 63.72 GHz, centered at 61.56 GHz)[1]. Dual polarization MIMO[2] (multiple input multiple output) will be implemented in the system, which results in four data streams (2 × I/Q) with 3.5 Gbit/s raw data rate on each stream. Such high data rate requires at least four ADCs (analog to digital converters) with high speed and accuracy, which are very expensive and consume a lot of DC power. To overcome this problem, analog QPSK demodulation (with carrier phase and frequency recovery) will be implemented in our system, which can significantly lower the requirement of the ADCs, as only a sample and hold circuit is needed [12, 13].

One intended application of the 60 GHz system is to download data from a data-kiosk with multi-gigabit per second data rate. The user holds a mobile device in front of the Kiosk and multimedia files can be downloaded within seconds. The targeted operating range is within 1 meter. For such application scenarios, a direct LOS (line of sight) link is available and multi-path effects can be neglected. High gain patch antennas (4 × 4 patch array antennas with 15 dB gain) will be used for both the transmitter and receiver. Tab. 2.1 shows a simplified link budget calculation.

For a BER (bit error rate) of 10^{-2} (before decoding), an SNR of 10 dB is required (D-QPSK, AWGN channel). Based on the link budget calculation in Tab. 2.1, the required receiver NF (noise figure) is below 32 dB, which means that a receiver front-end without LNA is possible. On the other hand, 11 dB receiver NF is feasible, employing a state-of-art LNA (20 dB gain, 7 dB NF), allowing either the transmitter power to be significantly

[1]The ITU-R (International Telecommunication Union - Radiocommunication Sector) recommended channelization comprises four channels, each 2.16 GHz wide, centered on 58.32 GHz, 60.48 GHz, 62.64 GHz and 64.80 GHz respectively. The second and third channel are used in the system

[2]Two antennas (both at transmitter and receiver) transmit and receive in the E and H plane simultaneously.

Table 2.1: Simplified link budget calculation for 60 GHz transmission over 1 meter distance.

Tx power (P_{tx})	10 dBm
Tx antenna gain (G_{tx})	15 dB
Path loss @ 1 meter (L_{path})	67 dB
Rx antenna gain (G_{rx})	15 dB
Polarization mismatch & misalignment loss (L_{mis})*	3 dB
Analog front end implementation loss (L_{AFE})*	6 dB
Signal bandwidth (BW)	4.32 GB
Noise power at Rx (P_{noise})	-78 dBm
Receiver noise figure ($NF_{receiver}$)	?
Signal to noise ratio (SNR)	42 - $NF_{receiver}$ dB

* For both transmitter and receiver.

reduced or the transmission distance to be significantly increased. In this thesis, both receiver options (with and without LNA) have been realized and the results will be shown in Chapter 8 and 9.

2.2 Receiver Architecture

The receiver is a superheterodyne receiver, as shown in Fig. 2.1. The received signal is first down-converted to an IF (intermediate frequency), and then demodulated by the following analog demodulator [13]. This thesis mainly focuses on the down-converter module.

As indicated in Fig. 2.1, the down-converter module consists of a fully-integrated down-converter IC and a separate LNA[3]. Both ICs are packaged in a brass housing with a V-connector at the input to connect the antenna. The circuits are all differential, so a ratrace balun has been realized on the carrier substrate to convert the single-ended signal from the antenna to a differential signal.

The down-converter IC, consisting of a down-converting mixer, a VCO plus frequency doubler, and an analog PLL (phase locked loop), is realized using a low-cost SiGe HBT

[3]A second version consists of only the down-converter IC.

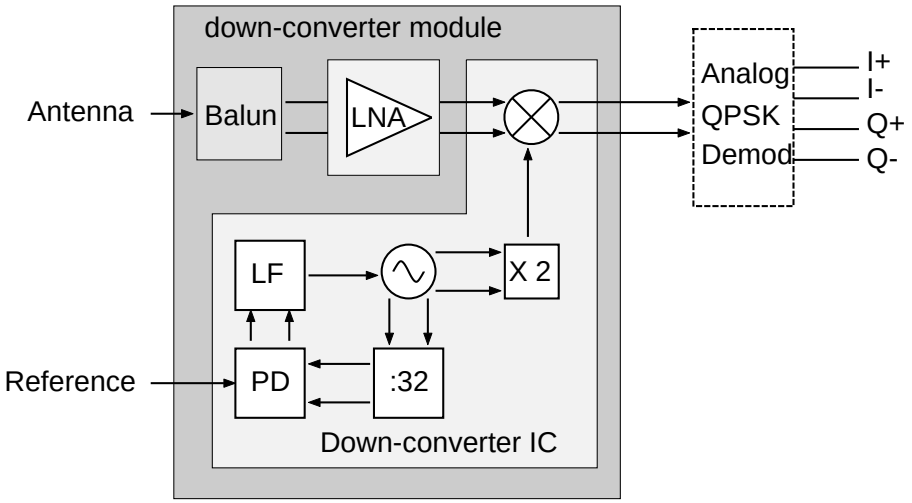


Figure 2.1: 60 GHz receiver front-end architecture.

technology, which is introduced in detail in Section 2.3 (page 8). Due to the relatively low f_T/f_{max} (80/90 GHz) of the technology, realizing an LNA at 60 GHz is not possible. Therefore, a separate LNA, realized in a 0.25 μm SiGe BiCMOS technology [14] is used in the module.

The main task of the receiver front-end (frequency down-conversion) is performed at the down-converting mixer. Besides the conversion gain and noise figure, which are two important figures of merit for down-converting mixers, the IF bandwidth is also an important requirement in this work, as the IF signal has a very wide bandwidth (4.32 GHz). Therefore, a Gilbert cell mixer with a tranimpedance load is used to achieve a wide IF bandwidth.

To drive the down-converting mixer, an LO signal with sufficient power is needed. Due to the relatively low f_{max} (90 GHz) of the technology, generating a 60 GHz signal with sufficient output power is challenging. It is very difficult to realize a fundamental VCO (voltage controlled oscillator) at 60 GHz. A push-push VCO can generate the 60 GHz signal but the output power is too low to drive a mixer. Therefore, in this thesis work, a VCO plus frequency doubler approach is adopted. It is shown in Chapter 4 that this approach can generate relatively high output power at frequencies close to f_{max} of a technology.

The free-running VCO is stabilized using a PLL. The PLL should have low phase noise, low reference spur and wide locking range, with low DC power consumption. To meet these requirements, an analog PLL, consisting of a frequency divider (FD), an analog phase detector (PD) and an active loop filter (LF) is used. The high operating frequency of the PD enables small frequency division ratio, and therefore better phase noise. The FD consists of dynamic and static frequency dividers that can operate over a wide frequency range, enabling a wide locking range. Furthermore, thanks to the VCO plus doubler approach, the FD only needs to operate at half the LO frequency, significantly reducing the DC power consumption of the FD.

2.3 Technology

A SiGe HBT technology [11], provided by Telefunken Semiconductors GmbH, is used to realize the down-converter IC in this thesis work. The process requires only 22 masks with 0.8 μm lithography and therefore is very cost-effective. Two types of npn transistors are available with minimum emitter size of 0.8 $\times$ 1.4 μm^2 (electrically active emitter size of 0.5 $\times$ 1.1 μm^2). One type of lateral pnp (LPNP) transistor is also available, but not suitable for RF purposes. Four types of resistors, MIM and Nitride capacitors, as well as varactor diodes are provided. Two types of silicon substrate (1000 Ωcm and 20 Ωcm) are available. The low-resistivity substrate is used for all the ICs.

The SIC-npn (selectively implanted collector) transistor features f_T/f_{max} of 80/90 GHz and BV_{CEO} (collector-emitter breakdown voltage) of 2.4 V. The non-SIC transistor has lower f_T of 50 GHz but much higher BV_{CEO} of 4.5 V. In this thesis work, the non-SIC transistors are only used in the active loop filter design, where high output voltage is desired. The SIC transistors are used in all other designs because of the higher f_T.

For each type of transistor, various sizes and configurations are available. The electrically active emitter width varies from 0.5 μm to 1.3 μm (with 0.4 μm step), while the emitter length varies from 1.1 μm to 40 μm (with 0.6 μm to 5 μm step). The transistors have three different configurations: "CBE" (collector-base-emitter), "CEB" (collector-emitter-base) and "CBEB" (collector-base-emitter-base, only for transistors with emitter length $>$ 5 μm). The "CBEB" configuration has the lowest base resistance (because of two base contacts in parallel) and therefore is used the most in this work. Transistors with "CEB" configuration are used in the static dividers, because of the smaller base-collect junction capacitance.

The transit frequency (f_T) and maximum oscillation frequency (f_{max}) of the transistor are dependent on the DC biasing conditions. Transistors with "CBEB" configuration have the highest f_T/f_{max}. Fig. 2.2 shows the simulated f_T and f_{max} versus collector current of a 0.5$\times$20 μm^2 transistor with "CBEB" configuration.

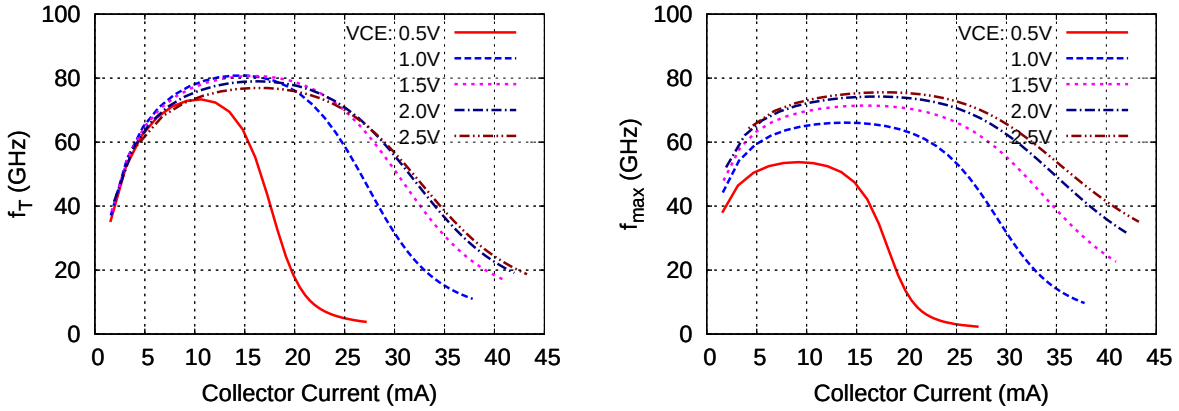


Figure 2.2: Transit frequency (f_T) and maximum oscillation frequency (f_{max}) versus collector current for different collect-emitter biasing voltage. The transistor size is 0.5$\times$20 μm^2.

The maximum f_T and f_{max} are achieved with 1.5 V VCE (collector-emitter biasing voltage) and 16 mA current (1.6 mA/μm^2). The transistor should be biased at this current and voltage level to achieve the maximum gain. However, when the collector current is reduced (by 50%) to 8 mA (0.8 mA/μm^2), the f_T and f_{max} only decrease by 5 and 3 GHz, respectively. Therefore, this biasing current level is more efficient with respect to power consumption. In this thesis work, for circuits that operate at high frequencies (VCO, doubler, mixer, divider), the transistors are biased close to this current (0.8 mA/μm^2) and voltage (1.5 V VCE) levels to have the (close to) maximum gain from the transistors while keeping the power consumption at relatively low level.

The transistors are modeled using the HICUM (HIgh-CUrrent-Model) model[4], which predicts the behavior of the transistors very well also at high VCE and with high collect current density (close to break down), making the circuit simulation more accurate.

The process offers three metal layers for passive elements and interconnections, as shown in Fig. 2.3. Thin-film microstrip lines (TFML) are built using the top and bottom metals. To have the maximum characteristic impedance and therefore maximum inductance per unit length, the minimum width of 3 μm is chosen for the top metal, corresponding to a characteristic impedance of 65 Ω. In the circuits, the TFMLs are used as inductors and matching networks. Further details of the TFMLs are provided in Appendix A (page 105).

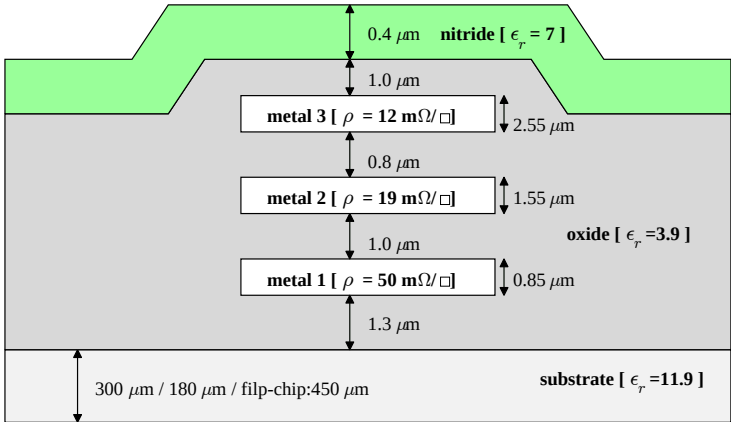


Figure 2.3: Metal layers of the SiGe2RF process.

The process is very cost-effective, making it suited for both large and small volume productions. However, the relatively low f_T/f_{max} (80/90 GHz) makes the 60 GHz receiver design very challenging. To achieve satisfactory performance while keeping the power consumption low, the circuits must be designed and optimized carefully, which will be explained in the following chapters.

[4]The HICUM model is a compact device model for homojunction bipolar transistors and heterojunction bipolar transistors, developed by the HICUM Group at CEDIC, University of Technology Dresden, Germany, and the University of California at San Diego, USA. It features a good modeling of the transistor behavior under high current densities. Details of the model is provided in [15].

Chapter 3

Down-converting Mixer

3.1 Gilbert cell Mixer

The Gilbert cell mixer [16] is very widely used in modern RF systems. It is an active, double-balanced mixer, which provides higher conversion gain than passive mixers and better port-to-port isolation than single-balanced or single-ended mixers. The core of the Gilbert cell mixer consists of three emitter-coupled pairs (ECP), as shown in Fig. 3.1 (a).

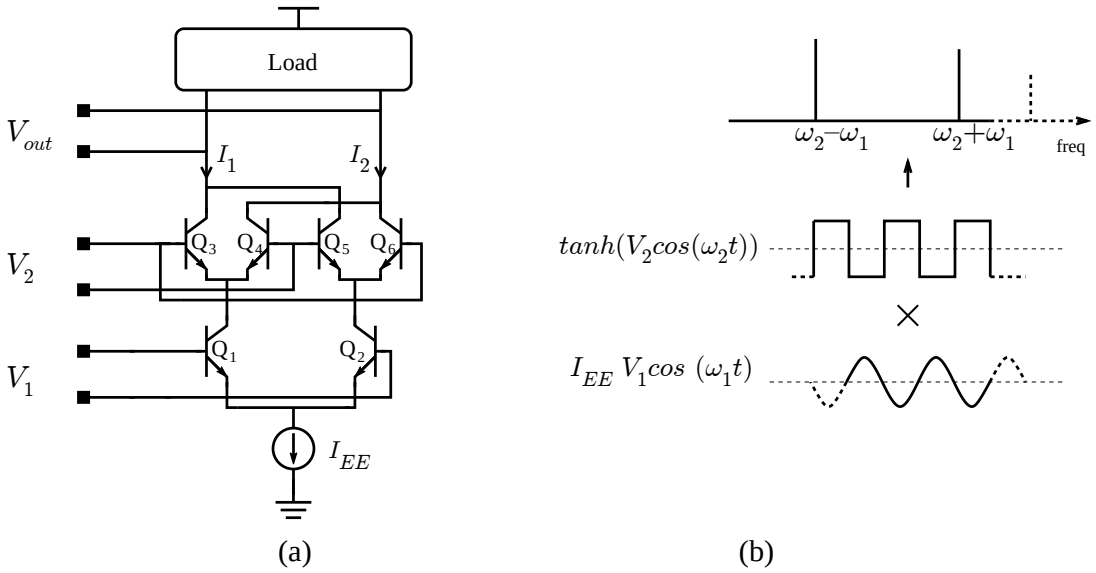


Figure 3.1: Gilbert cell mixer core.

When two input signals (V_1, V_2) are applied to the bases of the ECPs, as indicated in Fig. 3.1 (a), the output current can be calculated as [17]:

$$I_o = I_1 - I_2 = I_{EE} \cdot tanh\left(\frac{V_1}{2V_T}\right) \cdot tanh\left(\frac{V_2}{2V_T}\right), \tag{3.1}$$

where V_T is the thermal voltage[1]. If the magnitudes of V_1 and V_2 are much smaller than V_T, I_o can be approximated as $I_{EE} \cdot \frac{V_1}{2V_T} \cdot \frac{V_2}{2V_T}$. The mixer now behaves as a linear multiplier. If the magnitude of V_2 is much larger than V_T, while V_1 is small, the two ECPs (Q_3 - Q_6) behave as switches and the output current I_o can be approximated as $I_{EE} \cdot \frac{V_1}{2V_T}$ multiplies a square wave. The mixer now behaves as a modulator. When both V_1 and V_2 are much larger than V_T, all the six transistors behave as switches and the the mixer can be used as a phase detector.

To use the Gilbert cell as a mixer, it is usually operated in the modulator mode. The RF signal (at frequency f_1) is applied to the lower ECP (also called transconductance stage), which converts the RF voltage to current. The LO signal (at frequency f_2) is applied to the upper ECPs (also called switching quad) to switch polarity of the RF current. As a result, mixing products at frequencies of $m \cdot f_2 \pm f_1$, where $m = 1, 2...$, appears in the output current, as shown in Fig. 3.1 (b). The output current is then converted to voltage at the load. For Gilbert cell mixers, the fundamental mixing products ($f_2 \pm f_1$) are most important and used most frequently for up- and down-conversion, as the power levels of higher order mixing products are much smaller.

3.2 Circuit Design

Based on the Gilbert cell topology, a 60 GHz down-converting mixer has been realized. Fig. 3.2 shows the complete schematic of the realized mixer, which consists of the mixer core, the trans-impedance load stage, the emitter follower output buffer and the biasing network.

The transistors used in the mixer core (Q_1, Q_2) need to be chosen carefully. The transconductance stage (Q_1) strongly influences the conversion gain, linearity and noise performance of the mixer. In this respect, larger transistors are preferred because of the higher power handling capability (better linearity) and lower base resistance (better noise performance). However, larger transistors also consumes higher current than smaller transistors (to bias the transistor for the same f_T/f_{max}), which significantly increases the voltage drop on R_2 and R_3 and thus requires higher supply voltage. So transistors with 0.5×5 μm^2 size and "CBEB" (collector-base-emitter-base) configuration are used for the transconductance stage. The relatively small size requires less current and the "CBEB" configuration offers much lower base resistance than smaller transistors with only one base contact. The same transistor is also used in the switching quad (Q_2). The small transistor size, and therefore small junction capacitors (mainly the base-emitter capacitor), enables fast switching, which reduces the third order intermodulation products [18]. Smaller transistor also has higher output impedance, which leads to more mismatch between the mixer core and the transimpedance stage and hence wider IF bandwidth, as explained next. The transistor is also large enough to handle the RF signal from the transconductance stage.

[1]The relationship between current and voltage across a p-n junction depends on a characteristic voltage called the thermal voltage, denoted V_T. The thermal voltage depends on absolute temperature T as $V_T = \frac{kT}{q}$, where q is the magnitude of the electrical charge on the electron and k is the Boltzmann constant.

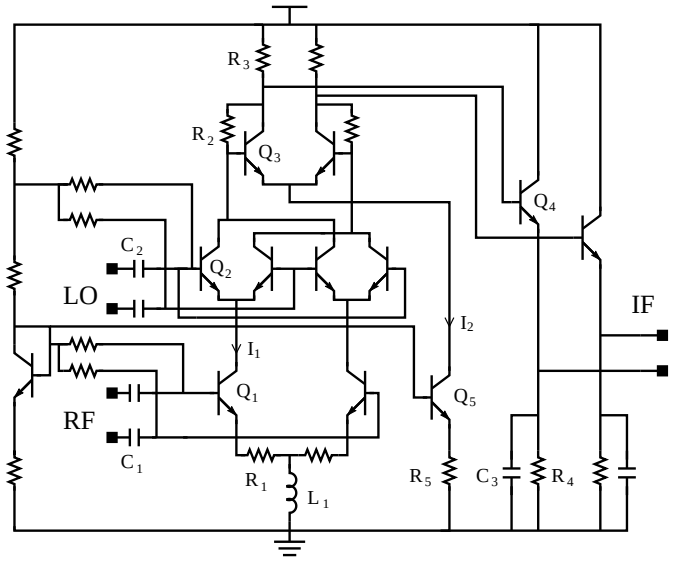


Figure 3.2: Full schematic of the 60 GHz down-converting mixer. The detailed parameters can be found in Appendix C.1 (Fig. C.1, page 113).

Emitter degeneration (R_1) is used at the transconductance stage to improve the linearity of the mixer, at the cost of reduced conversion gain. Inductor L_1 helps to suppress the unwanted common mode signal coming from the RF input.

The mixer core produces an IF current, which will be converted to a voltage at the IF load. Different types of loads can be used, leading to different mixer performance. The resistive load, as used in [7] and [8], is the most commonly used load for down-converting mixers. It is simple and easy to design, but only suited for low IF frequencies. The load resistor and the junction capacitance of transistor Q_2 and Q_4 forms a low-pass filter and the conversion gain decreases strongly as the IF frequency increases. For the superheterodyne receiver in this work, where the IF signal is centered at 5 GHz, the resistive load is not suited. Another type of load is the inductive load, which resonates with the parasitic capacitance and can achieve higher conversion gain at higher frequencies. However, as the IF frequency is 5 GHz, the required inductor is around 2 nH (to have the resonance frequency at 5 GHz), which is very large for on-chip realization. Moreover, the bandpass behavior of the inductive load makes the bandwidth very small. Decreasing the quality factor (Q) of the inductor by connecting a small resistor in series can help to increase the bandwidth, but the gain also drops significantly. A third type of load is the transimpedance load, as shown in Fig. 3.2. The IF current is converted to voltage by a feedback amplifier (R_2, R_3 and Q_3). As a comparison, Fig. 3.3 shows the simulated conversion gain versus RF frequency (LO fixed at 55 GHz, 0 dBm) for mixers with different loads. The conversion gain with transimpedance load is higher than the resistive and inductive (Q of 0.5) load. Furthermore, the IF bandwidth of the transimpedance load is much wider than the other two types of loads.

The mixer is designed to drive a 50 Ω (100 Ω differentially) load. This low impedance will reduce the conversion gain of the mixer if it is directly connected to the output of the transimpedance stage. Therefore, an emitter follower is added as an output buffer,

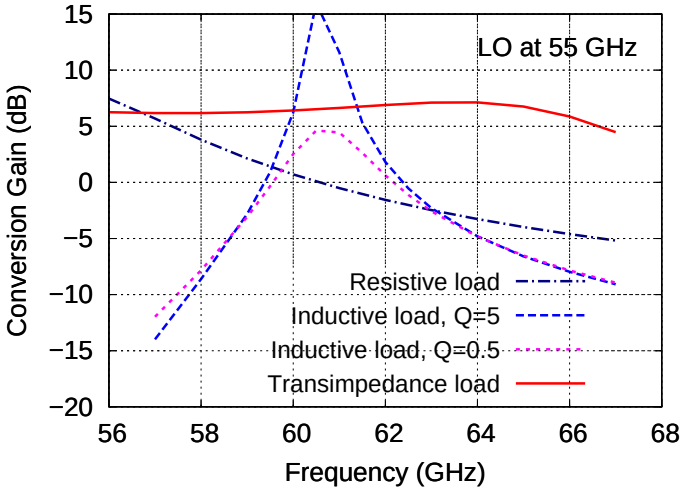


Figure 3.3: Simulated conversion gain versus RF frequency of mixers with resistive (400 Ω), inductive (L of 2 nH, Q of 5 and 0.5, which forms a series resonance at 5 GHz with the output capacitance of the Gilbert cell core) and transimpedance load. LO is at 55 GHz with 0 dBm power.

which provides a high impedance to the transimpedance stage and a low impedance to the load. Capacitor C_3 further peaks the gain at high IF frequency and increases the IF bandwidth. Biasing of the circuit is done using resistive voltage dividers. To isolate the RF and LO signal from the biasing network, large resistors (2.5 $k\Omega$) are used, instead of inductors or quarter wavelength transformers, to save chip area. The complete schematic of the mixer with component parameters can be found in Appendix C.1 (Fig. C.1, page 113).

Transimpedance load

As explained in Chapter 2, the received RF signal has a very wide bandwidth (RF signal 59.4 - 63.72 GHz), leading to a very wide IF bandwidth (IF signal 2.84 - 7.16 GHz). For better performance, the mixer should have a flat (ideally) frequency response over the entire RF frequency range. Therefore, the transimpedance load is implemented in the final mixer design. The wide bandwidth is achieved mainly through the shunt feedback resistor (R_2 in Fig. 3.2). Fig. 3.4 shows a simplified model of the transimpedance amplifier, where R_F is the shunt feedback resistor. The following discussion follows [19].

The open-loop amplifier is assumed to have an infinite input impedance and a voltage gain of $A(j\omega)$, which has a single-pole roll-off and can be expressed as

$$A(j\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_0}}, \tag{3.2}$$

where A_0 is the open-loop DC voltage gain and $\frac{\omega_0}{2\pi}$ is the 3-dB cutoff frequency set by the dominant pole in the transfer characteristic.

The closed-loop voltage of the amplifier can be approximated as

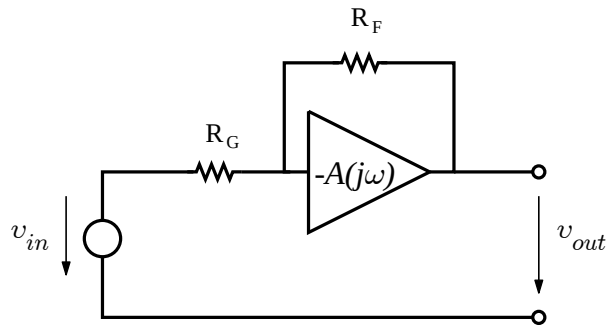


Figure 3.4: Simplified model of transimpedance amplifier.

$$\frac{\upsilon_{out}}{\upsilon_{in}} = -\frac{A_0 \cdot R_F}{R_F + (A_0+1)\cdot R_G} \cdot \frac{1}{1 + j\frac{\omega}{\omega_0{}'}} = -(1 - \frac{(A_0+1)\cdot R_G}{R_F + (A_0+1)\cdot R_G}) \cdot \frac{A_0}{1 + j\frac{\omega}{\omega_0{}'}}, \quad (3.3)$$

where $\frac{\omega_0{}'}{2\pi}$ is the new 3-dB cutoff frequency, with

$$\omega_0{}' = \omega_0(1 + \frac{A_0 \cdot R_G}{R_G + R_F}) \quad (3.4)$$

The input resistance for frequencies approaching zero is calculated as

$$Z_{in} = \frac{R_F}{1 + A_0} \quad (3.5)$$

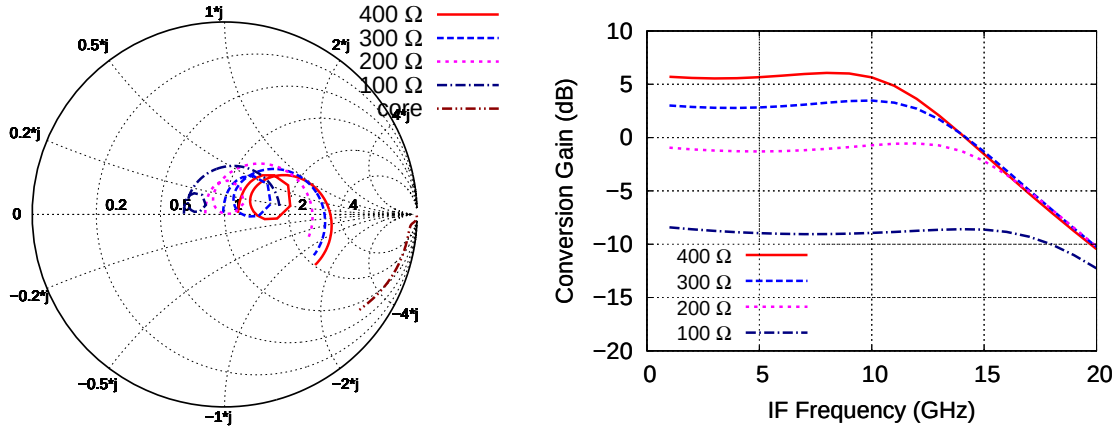
Equation 3.3 and 3.4 show that the bandwidth of the amplifier is increased and the gain is decreased because of the shunt feedback resistor. The input resistance also becomes smaller, mainly determined by the feedback resistor and the open-loop gain of the amplifier, as shown in Equation 3.5.

The Gilbert cell core plus transimpedance load follows the principle of strong impedance mismatch between succeeding stages to extend the IF bandwidth [20, 21]. The output impedance of the mixer core is very large (small capacitance) and the input impedance of the transimpedance load is small, leading to a higher cutoff frequency (RC cutoff frequency). The bandwidth is mainly determined by the feedback resistor R_2. Fig. 3.5 shows the simulated input impedances looking into the mixer core and the transimpedance stage for different R_2, as well as the corresponding conversion gain. As R_2 decreases, the input impedance of the transimpedance decreases and the bandwidth increases. However, the conversion gain also decreases, due to less gain from the transimpedance stage. In this design, R_2 is chosen to have a 10 GHz IF bandwidth. R_3 is maximized to have higher conversion gain.

Fig. 3.6 shows the simulated conversion gain of the mixer core, the gain of the transimpedance stage and the total conversion gain, with sweeping IF frequency. The conversion gain of the mixer core has a wide bandwidth and slightly peaks and the gain of the

transimpedance stage decreases with increasing IF frequency. The total conversion gain is flat for the upper band (LO frequency < RF frequency) and slightly peaks for the lower band (LO frequency > RF frequency), which is a superposition of the gain of the mixer core and transimpedance stage.

One drawback of the transimpedance load is that it significantly raises the necessary supply voltage of the mixer, due to the voltage drop on R_2 and R_3. Thus for a fixed supply voltage, the choice of R_2, R_3 and the biasing current (I_1 and I_2) is limited, which then limits the maximum achievable gain for this design, where relatively large resistor and current are needed for higher conversion gain. The mixer is designed for a 4 V supply, in consistence with the voltage supplies used in other front-end circuits. To achieve the optimum performance, the voltage drops on Q_1 and Q_2 are minimized (without going into saturation) to gain more voltage headroom for the transimpedance stage. R_2 and R_3 are chosen to be 400 Ω and 300 Ω, as a compromise between conversion gain and IF bandwidth. The current through Q_1 and Q_3 are all set to 2 mA, which is mainly limited by the available voltage drop on the transimpedance load. Therefore, small transistors are used for Q_1 and Q_3 to have higher gain at this current level (compared with larger transistors).



(a) (b)

Figure 3.5: (a) Simulated reflection coefficients looking to the mixer core and the transimpedance load (for different feedback resistor R_2). The frequency range is from 1 GHz to 20 GHz. (b) Simulated conversion gain versus IF frequency. The LO is fixed at 55 GHz with 0 dBm power.

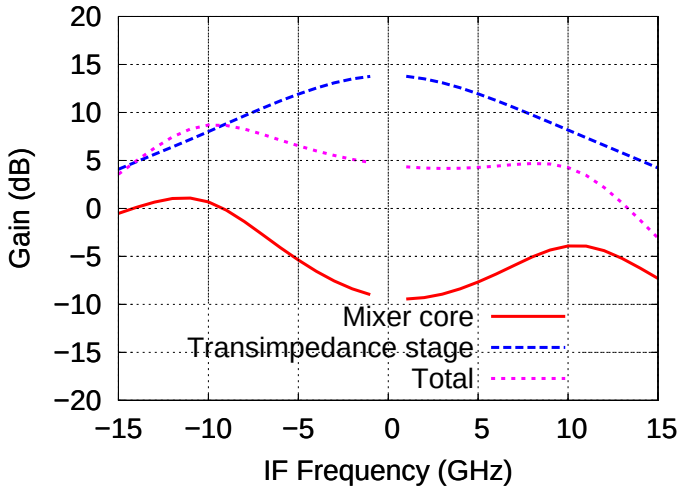


Figure 3.6: Simulated conversion gain of the mixer core, gain of the transimpedance stage and the total conversion gain. The LO frequency is fixed at 55 GHz. RF frequency is LO frequency + IF frequency.

3.3 Performance

The mixer is simulated in Agilent ADS, using harmonic balance simulation. Layout is performed in Cadence. The circuit layout is kept as symmetric and compact as possible. "GSSG" (ground-signal-signal-ground) pads with 100 μm pitch are used to connect the differential input and output. Fig. 3.7 (a) shows a photo of the realized mixer chip.

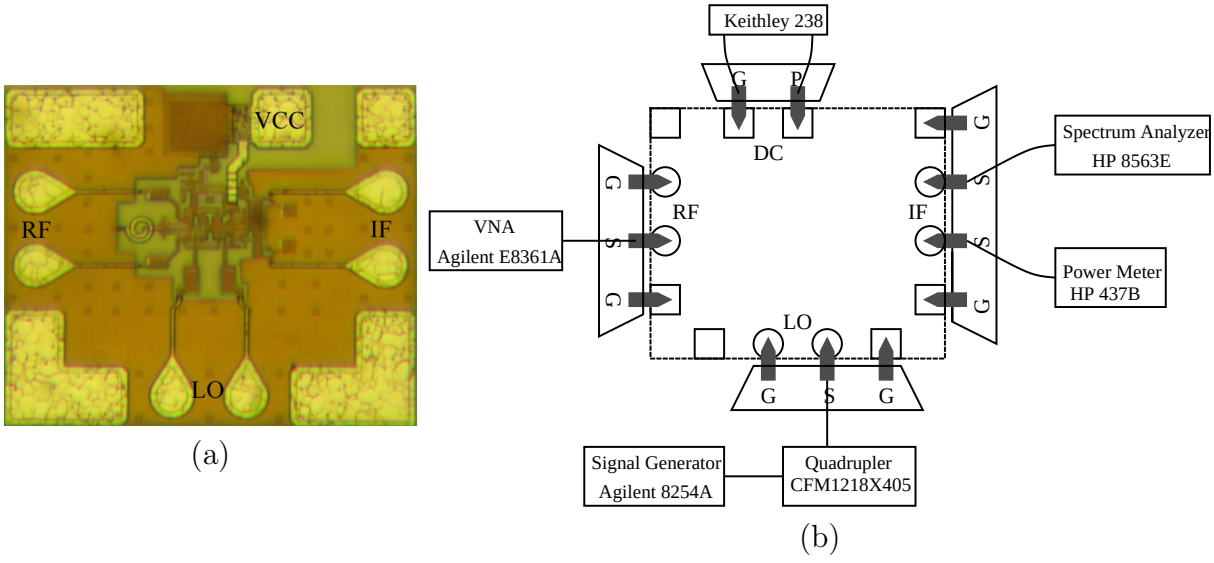


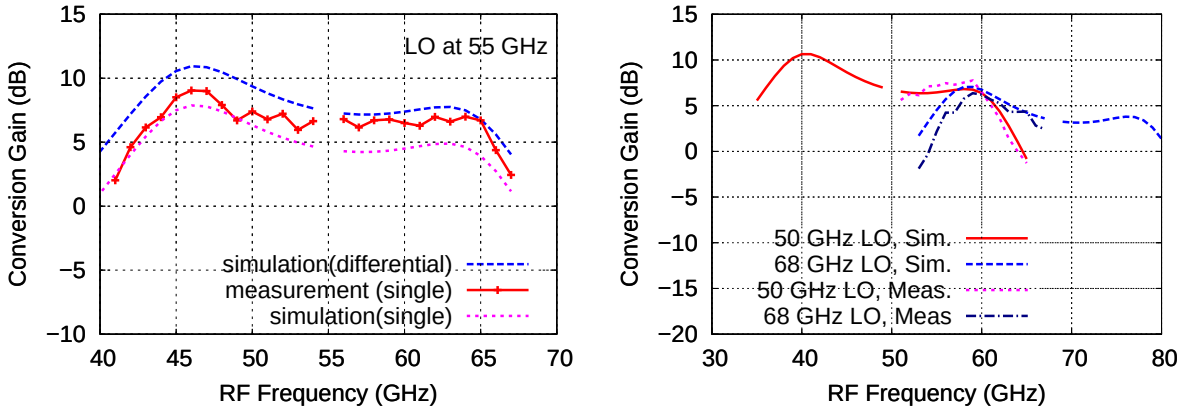
Figure 3.7: (a) Photo of the realized mixer chip. The size is 550 × 450 μm^2, including the bonding pads. The die area is only 250 × 200 μm^2. (b) Mixer measurement setup.

The mixer was characterized on wafer. Due to the lack of differential signal sources, the RF and LO input were fed single-endedly using "GSG" probes. The positive and negative input were connected to the "S" and "G" of the probe, respectively. Compared with

fully differential operation, this will lead to lower conversion gain and higher port-to-port leakage, but it is sufficient for characterization purpose. A 67 GHz VNA (Agilent E8361A) was used to generate the RF signal. The LO signal was generated by using a 40 GHz signal generator (Agilent e8254A) and a V-band frequency quadrupler (CERNEX CFM1218X405). The positive and negative IF output were connected through a 40 GHz "GSSG" probe to a spectrum analyzer (HP 8563E) and a power meter (HP 437B) simultaneously, so that they could be monitored at the same time. The mixer needs only one 4 V supply and draws 17.4 mA current. Fig. 3.7 (b) shows the measurement setup.

Gain and bandwidth

To characterize the conversion gain and bandwidth of the mixer, the LO was fixed and the RF signal was swept. Fig. 3.8 (a) shows the measured conversion gain versus RF frequency, when the LO was fixed at 55 GHz.



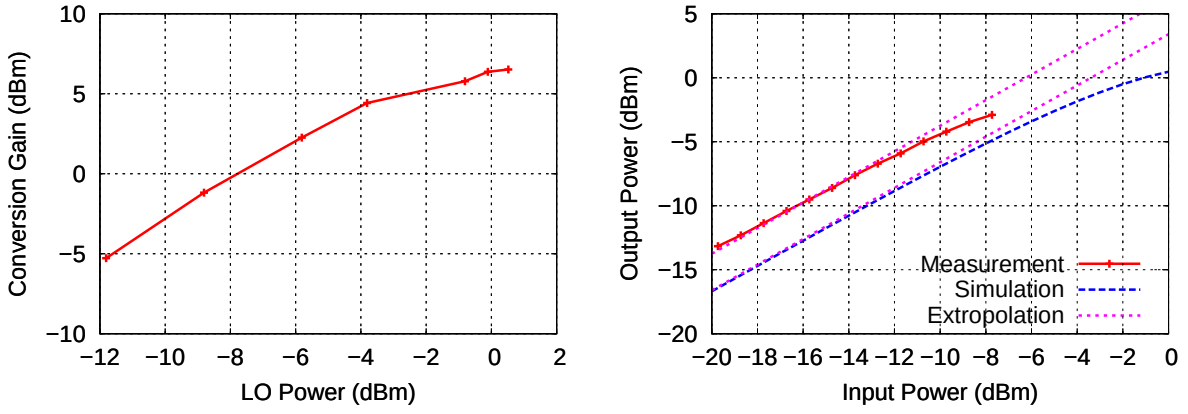
(a) (b)

Figure 3.8: (a) Simulated (differential and single-ended) and measured conversion gain versus RF frequency with 55 GHz LO signal. (b) Simulated conversion gain versus RF frequency for 50 GHz and 68 GHz LO signal and measured conversion gain for 50 GHz and 68 GHz LO. LO power is 0 dBm for all cases.

The RF was swept from 40 to 67 GHz, covering both the lower (RF frequency $<$ LO frequency) and upper (RF frequency $>$ LO frequency) bands. The measured conversion gain is about 6.6 dB ($\pm$ 0.4 dB) for the upper band and 7.5 dB ($\pm$ 1.5 dB) for the lower band (for IF frequencies below 10 GHz). The 3 dB bandwidth for both bands is above 10 GHz. For comparison, the simulation results for both differential and single-ended feeding are also plotted. The measured conversion gain is about 2 dB higher than simulated gain. One possible reason for this is that the input power is handled differently in the simulation tool compared with the real measurement setup due to the mismatch at the RF input. Small errors can also come from the error in the power calibration (cable and probe losses etc.) and process variations. But the measured frequency response agrees well with the simulation. When driven fully differentially, 3 dB more conversion gain can be expected, as predicted by the simulation. The power unbalance between the two IF outputs is less than 0.7 dB, which is within the accuracy tolerance of the measurement setup ($\pm$ 1dB).

As there is no specific matching network at the input and output, the mixer is also very broadband in terms of LO and RF frequencies. Fig. 3.8 (b) shows the simulated conversion gain versus RF frequency for 50 GHz and 68 GHz LO signals. For all the LO frequencies, the RF frequency is swept from (f_{LO}-15) GHz to (f_{LO}+15) GHz. As the LO frequency increases, the conversion gain slowly decreases, due to the lower gain in the transconductance stage. However, the IF bandwidth remains the same. As a verification, two measurements were done for 50 GHz LO (upper band) and 68 GHz LO (lower band), the measured conversion gain is very close to simulation results, as shown in Fig. 3.8 (b). Simulations indicate that 2 dB conversion gain at 90 GHz can be expected, with an 80 GHz LO signal. Combining with the 80 GHz VCO, as will be shown in Chapter 4, a frequency down-converting stage with at least unity gain for RF frequency up to 90 GHz is thus feasible in a low-cost technology with 80/90 GHz f_T/f_{max}.

The conversion gain of the Gilbert cell mixer is also a function of the LO power. If the LO power is low, the switching quad will not fully switch, which will lead to less conversion efficiency, and thus less conversion gain. The conversion gain increases with increasing LO power until the LO power is large enough to fully switch the switching quad, then it starts to saturate. Fig. 3.9 (a) shows the measured conversion gain versus LO power for this mixer. The optimum LO power for driving this mixer is about 0 dBm, where the switching quad of the mixer is switched almost fully on and off and the conversion gain starts to saturate. However, as the technology has limited gain at 60 GHz, the output power generated by the VCO circuit is around -4 dBm, where the conversion gain is about 4 dB.



(a) (b)

Figure 3.9: (a) Measured output power versus input power. LO was fixed at 55 GHz, 0 dBm. (b) Measured conversion gain versus LO power. RF was fixed at 61 GHz, -20 dBm.

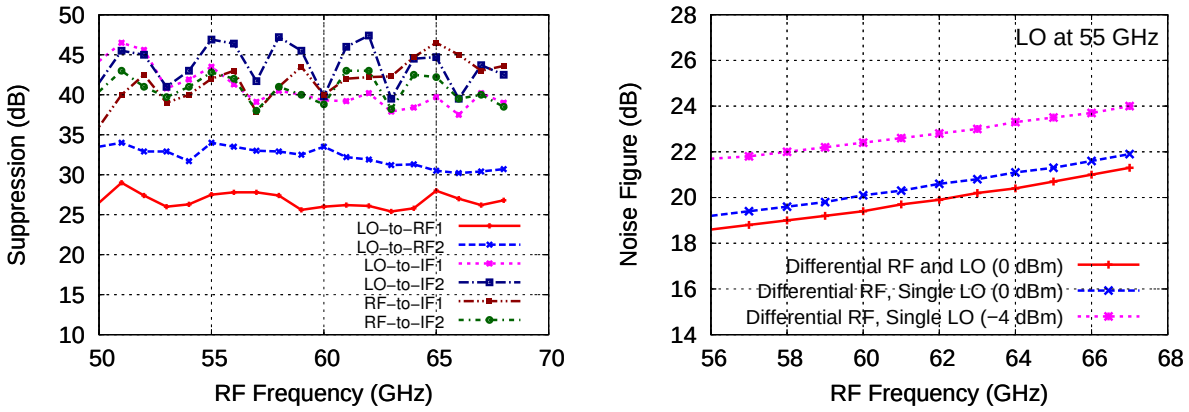
Linearity

The linearity of the mixer was checked by sweeping the RF input power. Fig. 3.9 (b) shows the measured results, as well as simulation results for comparison. The measured conversion gain is higher than simulation, thus the measured output power is also higher than simulation. But the measured output 1 dB compression point, which is -4.5 dBm, agrees well with simulation. This is because the linearity of the mixer is mainly determined by the emitter follower buffer stage. Increasing the current flow in the emitter follower

can further increase the output 1 dB compression point. For this work, -5 dBm output power is considered sufficient, so the current in the emitter follower is reduced to save power consumption.

Port-to-port isolation

Gilbert cell topology is a double balanced topology, therefore has very good port-to-port isolation. Ideally, there should be no leakage from one port to another. However, in reality, certain mismatch in the layout is unavoidable, which will lead to port-to-port leakage. Such leakage, especially the LO-to-RF leakage, can cause problem for the system and should be avoided. To check the port-to-port leakage of the mixer, 50 GHz to 67 GHz signals were applied to the RF and LO port, and the leakage signal was measured at the RF port (for LO-to-RF leakage) and IF port (for RF-to-IF and LO-to-IF leakage). Fig. 3.10 (a) shows the measurement results. The suppression is calculated by taking the LO (0 dBm) and RF(-20dBm) power and subtracting the measured leakage signal power. Although the RF and LO was driven single-endedly during the measurement, the RF-to-IF and LO-to-IF suppression is better than 37 dB, because the leaked RF or LO signal is further attenuated by the transimpedance stage. The leakages of the LO signal to the two RF ports are different, due to the fact that LO was driven single-endedly. But the suppression is still better than 25 dB.



(a) (b)

Figure 3.10: (a) Measured port-to-port suppression of the mixer. (b) Measured SSB NF. RF was fixed at 61 GHz, -20 dBm.

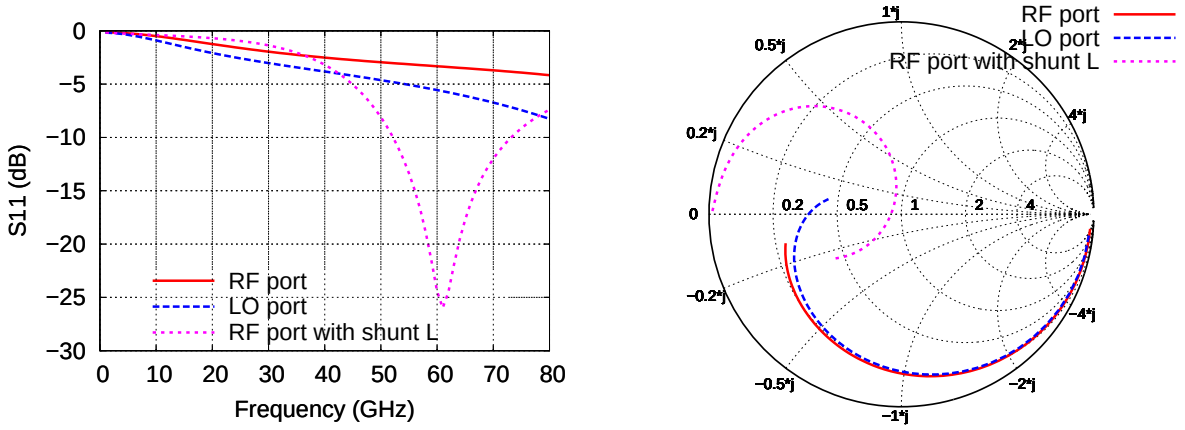
Noise figure

Simulation shows that the noise figure of the mixer is mainly determined by the transconductance stage and the switching quad. In this design, the noise figure is high, because of the semiconductor technology. Due to the relatively low f_T/f_{max}, the transistors have poor noise performance (minimum NF of 8 dB) and very low gain (-1 dB associated power gain for minimum NF) at 60 GHz. Therefore, the noise from the switching quad and transimpedance stage are not sufficiently suppressed by the transconductance stage. Fig. 3.10 (b) shows the simulated SSB (single-side-band) noise figure versus RF frequency, when LO is fixed at 55 GHz. For fully differential operation, the SSB NF is about 20 dB. For the real application, the mixer will be driven by a single-ended LO with -4 dBm

power, the simulated NF under this condition is about 3 dB worse, which is also shown in Fig. 3.10 (b). However, as discussed in Chapter 2, for short range communications, the requirement of NF is very relaxed for this work (<32 dB), so the noise figure of the mixer is still acceptable. The NF of packaged down-converter has been measured, which is about 26 dB. The calculated NF of the down-converter IC is about 24 dB, which is slightly higher than simulation. The details of the NF measurement will be shown in Chapter 8 (Fig. 8.22, page 94).

Input/output matching

The input and output of the mixer is not well matched to 50 Ω. Fig. 3.11 shows the simulated reflection coefficients from the RF, LO and IF ports. With this mismatch, the mixer can operate over a very wide frequency range, as shown in Fig. 3.8 (b). Besides this, the output impedance of the LNA was also unknown. Therefore, no specific matching was done for this design. However, the RF port can be well matched to 50 Ω by connecting a shunt transmission line (125 μm) at the input, as shown in Fig. 3.11 (b).



(a) (b)

Figure 3.11: Simulated reflection coefficient of the RF and LO port. RF port can be matched using a shunt transmission line at the input.

3.4 Summary and Comparison

A 60 GHz down-converting mixer has been successfully realized using an 80 GHz technology. A transimpedance load is used to achieve a wide IF bandwidth. The conversion gain and noise figure are not state-of-art results (mainly limited by the semiconductor technology), but are sufficient for the intended application. Compared with the mixers reported in [5–9], this mixer achieves much wider IF bandwidth and covers the complete 60 ISM band, which makes it suited for wideband applications.

Chapter 4

VCO and Frequency Doubler

This chapter describes the LO signal generation for driving the mixer. Due to the relatively low f_T/f_{max} of the technology, realizing a fundamental VCO at 60 GHz is not possible. Therefore, a VCO plus doubler approach is used. Different versions of VCOs and frequency doublers have been realized. The design, simulation and measurement details of the VCO and frequency doubler are discussed in this chapter.

4.1 VCO

VCO is a crucial component in most wireless systems, as it provides the LO signal to drive the up-converting or down-converting mixer. For this thesis work, the basic requirement of the VCO is having sufficient output power to drive the following frequency doubler. Phase noise is not very critical, as the VCO will be stabilized in a PLL. Wide tuning range is preferred, which gives more flexibility in the frequency plan and enables reuse of the VCO for other applications.

Different VCO topologies have been reported in literature. For integrated VCO design, the Colpitts topology 4.1 (a) and the cross-coupled topology 4.1 (b) are the most commonly used topologies. The cross-coupled VCO relies only on the positive feed back between the two transistors to generate the negative impedance and therefore is very compact. However, the equivalent capacitance from the negative resistance cell is directly in parallel with the LC tank, which reduces the frequency tuning range. Furthermore, the VCO core must be well buffered, because the output node is directly connected to the LC tank. These characteristics make the cross-coupled topology more suited for low frequency oscillators. For millimeter-wave frequencies, the Colpitts topology is more often used, because it has a wider tuning range and provides better isolation between the VCO core and the load.

In the Colpitts VCO, the feedback through the two capacitors (C_1 and C_2) generates a negative resistance and an equivalent capacitance at the base of transistor Q_1. Taking the simplified small signal equivalent circuit model of the transistor (neglecting the base-collector capacitance), as shown in Fig. 4.1 (c), the input impedance looking into the base

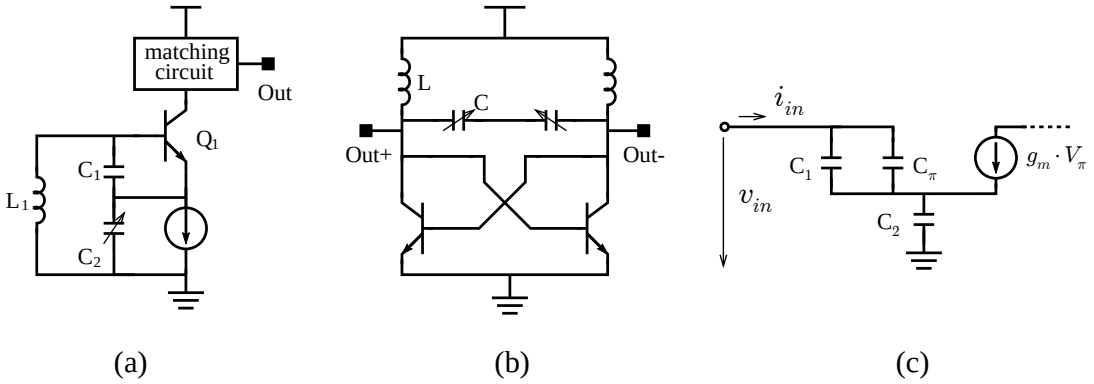


Figure 4.1: (a) Colpitts VCO topology. (b) Cross-coupled VCO topology. (c) Simplified small signal equivalent circuit model of the Colpitts VCO core (without inductor).

of Q_1 can be calculated as [22]

$$Z_{in} = \frac{v_{in}}{i_{in}} = -\frac{g_m}{\omega^2 C_2(C_1 + C_\pi)} + \frac{1}{j\omega}\frac{C_2(C_1 + C_\pi)}{C_1 + C_2 + C_\pi} \tag{4.1}$$

The final oscillation frequency is then

$$f_{osc} = \frac{1}{2\pi\sqrt{L_1 C_{eq}}}, \tag{4.2}$$

where C_{eq} is the equivalent capacitance ($\frac{C_1+C_2+C_\pi}{C_2(C_1+C_\pi)}$), which is ($C_1$+$C_\pi$) in series with C_2. The oscillation frequency can be changed by tuning the capacitor C_1 or C_2. C_1 is directly in parallel with C_π or sometimes, as in this work, directly replaced by C_π). So tuning C_2 is a better choice. To have a wide tuning range, the tuning capacitor should be much smaller than the other capacitor.

4.1.1 VCO Design

Fig. 4.2 shows the schematic of the realized VCO. The VCO core consists of transistor Q_1, varactor diode C_{VAR} and inductors L_B, L_E. Capacitor C_1 in Fig. 4.1 (a) is omitted, because the base-emitter capacitance of Q_1 alone is sufficient. The inductor L_E is in parallel with the varactor diode. The resonance frequency of L_E and C_{VAR} is chosen to be much lower than the oscillation frequency, so that the combination of them still behave capacitively within the whole tuning range of the VCO. A common base stage (Q_2) is cascaded to the VCO core to provide power amplification and further isolate the VCO core from the load. Transmission line (L_M) improves the matching between the VCO core and common-base buffer. The output matching network consists of three transmission lines (L_{C1}, L_{C2} and L_{C3}). L_{C1} increases the bandwidth of the matching network, compared to a single load line (L_{C2} only). The circuit is fully differential, so biasing and later packaging of the circuit is greatly simplified, because of the virtual

ground on the symmetry line. Two differential outputs are provided, so that the VCO can drive the frequency doubler and divider simultaneously[1].

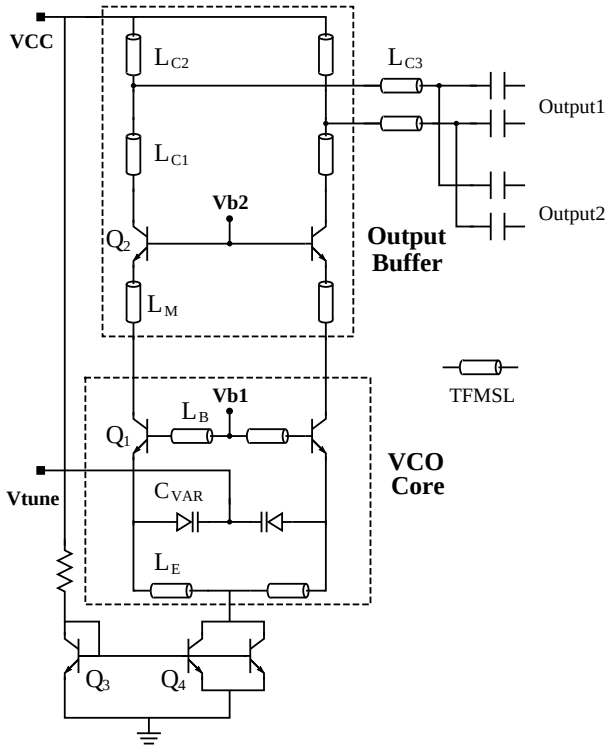


Figure 4.2: Simplified schematic of VCO.

Large transistors with emitter length of 30 μm are used for Q_1 and Q_2, because of the following reasons:

1. Large transistors can provide more output power, which is difficult to achieve with smaller transistors, as the oscillation frequency is relatively high compared to f_{max}.

2. The base resistance of the transistor decreases with increasing emitter length. This is beneficial for oscillator designs because more negative resistance can be achieved at the base. Low base resistance also helps for achieving low phase noise [24].

3. The base-emitter capacitance is more suited for the targeted frequency. A very large L_B will be needed when using smaller transistors, which takes more area and makes layout more difficult.

The inductors (L_B and L_E) and matching networks (L_M, L_{C1}, L_{C2} and L_{C3}) are all realized with Thin-Film-Microstrip-Lines (TFML), which are formed by the top and bottom metal layers. To have a larger unit inductance, the minimum allowed width of 3 μm is chosen for the top metal. The line is first simulated using a EM simulation tool (ADS Momentum)

[1]For stand-alone VCOs, the two output branches are the identical, providing the same output power. For the final ICs, the two outputs are designed differently so that less power goes to the frequency divider, while most of the output power goes to the frequency doubler.

and then modeled using a lumped element Π model that is scalable in length. Very good agreement between the model and the EM simulation results have been achieved. Compared with spiral inductors, the TFML gives more flexibility in the design, as the length can be chosen freely. The characteristic impedance of the line is 62 Ω. A 200 μm line gives an inductance of 94 pH at 30 GHz, with a Q (quality factor) of 6.5. Details of the transmission line model are provided in Appendix A (page 105).

Biasing of the circuit is done using resistive voltage dividers and current sources. The transistors are biased close to I_{max} (current for maximum f_T/f_{max}) to have maximum gain, as explained in Chapter 2 (Fig. 2.2, page 8). The complete schematic with parameter details of all the components are provided in Appendix C.2 (Fig. C.2, page 114).

Frequency and Tuning Range

The oscillation frequency is tuned by changing the voltage across the varactor diode (C_{VAR}). The tuning range of the VCO is directly related to the capacitance ratio of the varactor (C_{max}/C_{min}). In this thesis work, the smallest varactor diode (20 μm stripe length and 1.8 μm stripe width) is used[1]. The capacitance of a single varactor changes from 43 fF to 107 fF, when the DC voltage across the varactor varies from 4 V to 0 V and the quality factor changes from 20 to 10, as shown in Fig. 4.3. The capacitance can be further increased to 158 fF with slight forward biasing (- 0.4 V), but the quality factor drops to 7. This is helpful to achieve wider tuning range, especially when the free-running phase noise of the VCO is not very critical, as in this thesis work.

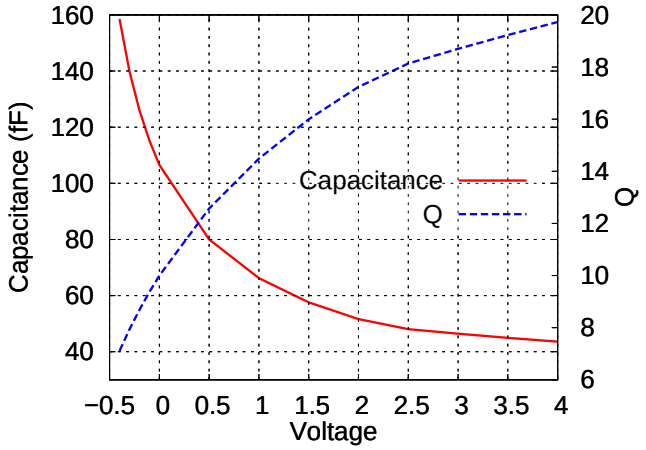
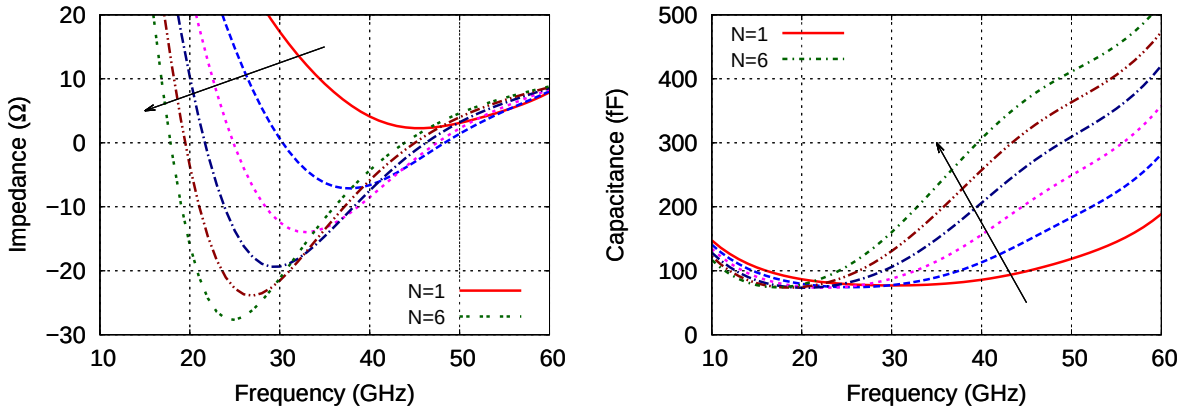


Figure 4.3: Capacitance and quality factor of a single varactor (at 30 GHz).

The oscillation frequency is determined by the base inductor and the equivalent capacitance looking into the base (Equation 4.2), which is the base-emitter capacitance (C_π) in series with the varactor capacitance (C_{VAR}). To have a wide tuning range, C_{VAR} should be much smaller than C_π. However, the negative resistance is also dependent on C_{VAR}, which must be taken into consideration. Fig. 4.4 (a) shows the simulated negative resistance with increasing number of parallel varactor diodes (from 1 to 6).

[1]Larger capacitance is realized by connecting several small diodes in parallel. This gives higher Q compared to using a large diode.



(a) (b)

Figure 4.4: Simulated resistance (a) and equivalent capacitance (b) looking into the base of Q_1 with increasing number (N) of parallel varactors diodes. V_{tune} is 2 V, corresponding to 1 V across the diode.

With a certain C_{VAR}, the resistance becomes positive below the resonance frequency of L_E and C_{VAR}, because the combination of L_E and C_{VAR} is not capacitive anymore. At higher frequencies, the resistance also becomes positive, due to the feedback from the base-collector capacitance[2]. As C_{VAR} decreases, the negative resistance decreases[3], leading to less voltage swing or no oscillation at all. Also, smaller C_{VAR} requires larger L_1 for the same oscillation frequency, which then increases the chip area and makes layout more difficult. In this design, the number of parallel diodes is chosen to be three, which provides sufficient negative resistance without sacrificing the tuning range too much[4].

S-parameter simulation has been used to determine the oscillation frequency. The oscillation starts at the frequency where the imaginary part of the two impedances (looking into L_B and base of Q_1) cancel out. Since the varactor number has been fixed, the base inductor L_B is tuned to shift the oscillation frequency to the designed frequency range. Fig. 4.5 (a) shows the simulated imaginary part of the impedances looking into the transistor and the base inductor at different tuning voltages (0.5 V to 4.5 V in 1 V steps). Fig. 4.5 (a) shows the sum of the imaginary part of both impedances, which becomes zero at the frequency of oscillation.

[2]Verification by simulation is provided in Appendix B on page 109.

[3]The decrease of the negative resistance is also due to the base-collector capacitance. This can not be seen from the Equation 4.1 because the base-collector capacitance is not included in the model. Verification by simulation is provided in Appendix B on page 109.

[4]The total capacitance of three varactors in parallel is about 120 fF to 480 fF, which is in the same range as C_π (about 300 fF).

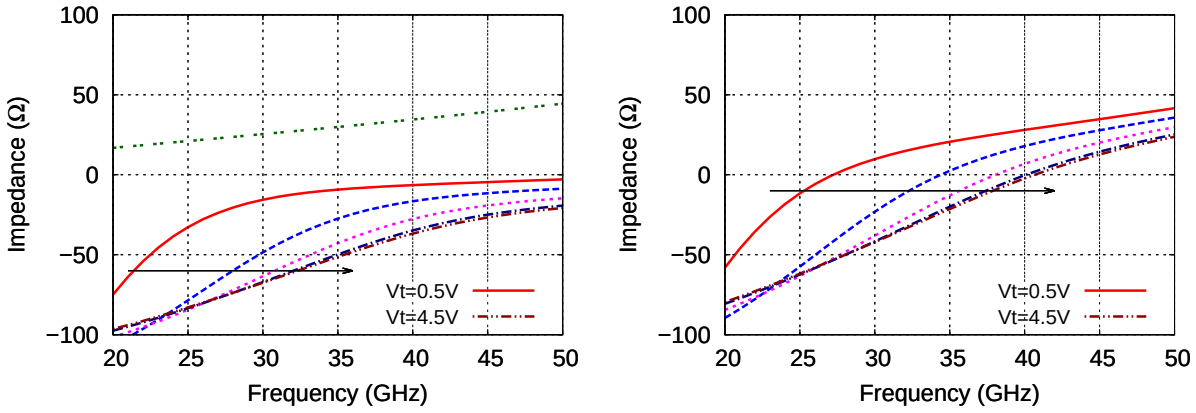


Figure 4.5: (a) Simulated imaginary part of the impedance looking into the base of Q_1 and L_B at different tuning voltages (0.5 V to 4.5 V in 1 V steps) . (b) Sum of the imaginary part of the two impedances.

Phase Noise

The phase noise of the VCO can be divided into conversion noise and modulation noise [25]. The conversion noise is the low-frequency noise generated in the transistor and LC resonator, that is up converted to the side of the carrier frequency. In SiGe HBTs, the main contributions to this noise are thermal noise (from the base resistance), shot noise (at the collector current) and low-frequency noise[5] [24]. The conversion noise can be expressed using a semi-empirical formula, proposed by Leeson [22, 26]:

$$L(\Delta\omega) = \frac{2FKTB}{P_s}\left[1+\left(\frac{\omega_o}{2\Delta\omega Q}\right)^2\right]\left(1+\frac{2\pi f_c}{|\Delta\omega|}\right), \tag{4.3}$$

where P_s is the output signal power, F is the noise factor, accounting for the additional noise in the oscillator core and f_c is the cutoff frequency for low-frequency "$1/f$" noise. From this aspect, to achieve lower phase noise, large output power, large transistor (small base resistance), low collector current and high Q passive elements are preferred.

The modulation noise comes from the frequency modulation, caused by the noise voltage that is generated across the tuning capacitor. It is directly proportional to the equivalent noise resistance (R_e) of the diode and the gain (K_0, Hz/V) of the VCO[6], which can be expresses as $\frac{2KTR_eK_0^2}{f_m^2}$ [25]. When the VCO has very high gain and the diode has large equivalent noise resistance, the modulation noise can dominate in the total phase noise. Therefore, from this aspect, VCO with low gain is preferred for better phase noise.

[5]The low-frequency noise is due to interaction with impurities or dislocations which create energy levels inside of the forbidden gap of semiconductor materials. These traps may locally lead to enhanced scattering of charge carriers (mobility fluctuation noise) or modify the number of charge carriers through trapping and release, with a characteristic time constant τ (number fluctuation noise) [22]. The low-frequency noise has a "$1/f$" frequency dependence, therefore it is also called "$1/f$" noise.

[6]The VCO gain is expressed as frequency change per unit voltage change (the slope of the tuning characteristic), which reflects the tuning sensitivity of the VCO.

In this thesis work, phase noise is not optimized, as there isn't much freedom for optimization. Large transistors are used and the Q of the varactors are improved by connecting several varactors in parallel, which are good for achieving low phase noise. However, a large collector current has to be used to have sufficient gain and output power, and the targeted wide tuning range will lead to a large gain of the VCO, tending to increase the phase noise. The simulated and measured phase noise are described in the following section.

Output Power

The output power of the VCO (Fig. 4.2) is mainly determined by the voltage swing in the VCO core and the output matching network (L_{C1}, L_{C2} and L_{C3}) of the output buffer. The voltage swing in the VCO core is already maximized, since large transistors are used in the VCO core and the current is set to I_{max}. Therefore, only the output matching network is tuned to have a constant output power over the complete tuning range. The total output power is about 7 dBm, limited mainly by the output buffer.

To have higher output power, a second VCO is designed, where cascode amplifiers are used as output buffers. Fig. 4.6 shows the schematic of the VCO. It has a slightly different VCO core (higher operating frequency), which is directly connected to two cascode amplifiers. Large transistors ($20 \times 0.5\ \mu\text{m}^2$) are used in the amplifier to have more output power (Q_2, Q_3). The output matching network of the amplifier consists of L_{C3}, L_{C4} and L_{C5}, which match the output impedance of the cascode core to 50 Ω. Together with the VCO core, more than 10 dBm output power can be provided. However, the DC power consumption is also quite high (96 mA at 4 V), due to the buffer amplifiers. Detailed schematic of this VCO is provided in Appendix C.2 (Fig. C.3, page 115).

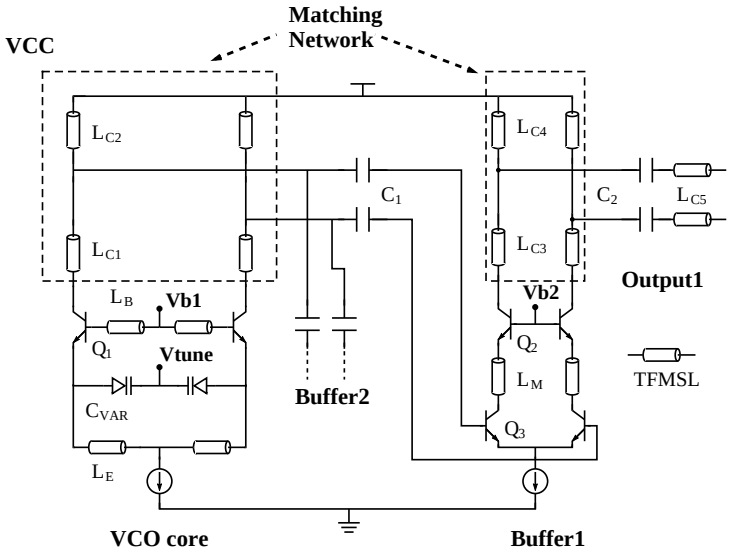
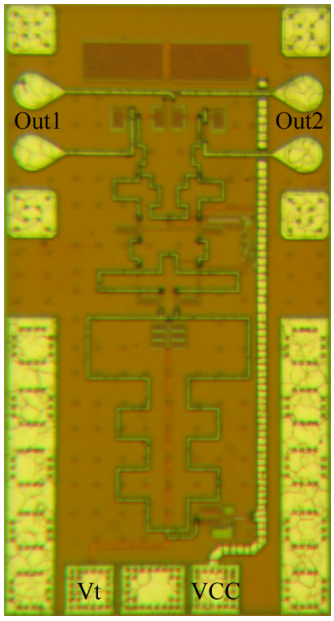


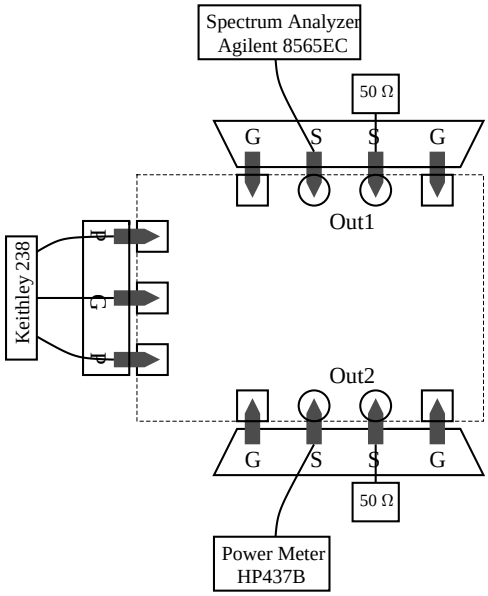
Figure 4.6: Simplified schematic of the VCO with separate cascode amplifier as output buffer.

4.1.2 Performance

The realized VCO chip is shown in Fig. 4.7 (a). The TFMLs are folded to save chip area, so the IC is still very compact and takes about 0.5 mm^2 area. The circuit has been characterized on wafer. Fig. 4.7 (b) shows the measurement setup. The two outputs are monitored simultaneously using a spectrum analyzer and a power meter.



(a)

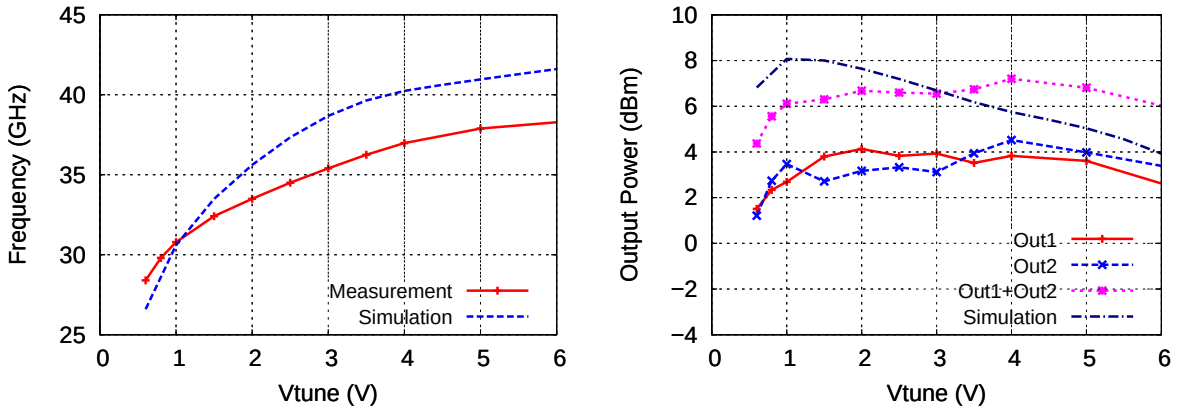


(b)

Figure 4.7: (a) Photo of the realized VCO chip. The size is 0.53 × 1 mm^2, including the bonding pads. (b) VCO measurement setup.

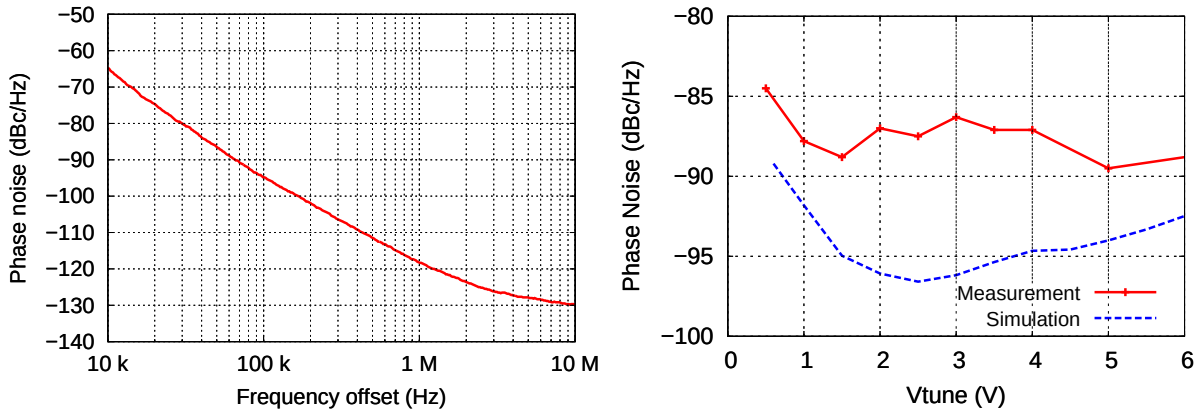
The VCO is biased under 4 V supply and consumes 37.7 mA current. By changing the tuning voltage from 0.6 V to 6 V, the VCO frequency can be tuned continuously from 28.4 GHz to 38.3 GHz (30%), as shown in Fig. 4.8 (a), and the output power from the two outputs are quite similar with less than 1 dB difference, leading to more than 6.5 dBm total output power, as shown in Fig. 4.8 (b), which is close to the simulation results. The difference is mainly due to the following reasons: model accuracy (TFML, varactor, transistor), parasitics (vias, interconnects), coupling between TFMLs and other layout effects (TFML crossing etc.).

The phase noise of the free running VCO is difficult to measure because the frequency change due to the noise picked up at the tuning node is too much for the instrument to follow. To overcome this problem and measure the phase noise of the VCO, a divide-by-32 frequency divider is integrated with another VCO. After frequency division by 32, the phase noise can be improved by 30 dB ($20 \cdot log(32)$) and the frequency change is small enough to be measured using the instrument. Fig. 4.9 (a) shows the measured phase noise of the divided signal (6 V tuning voltage). The same measurement was repeated for different tuning voltage. The calculated VCO phase noise at 1 MHz offset is shown in Fig. 4.9 (b). The reason for the difference between the measurement and simulation is not clear at the moment.



(a) (b)

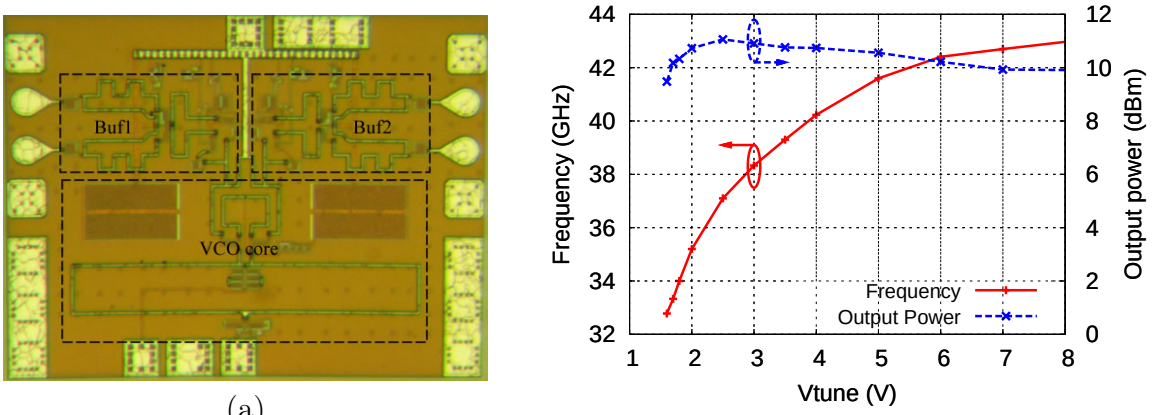
Figure 4.8: (a) Frequency and output power (b) versus tuning voltage. 3 dB has been added to "Out1" and "Out2" to represent the differential output power.



(a) (b)

Figure 4.9: (a) Measured phase noise (10 kHz to 10 MHz offset) of the divide-by-32 signal (b) Calculated phase noise (at 1 MHz offset) of the VCO versus tuning voltage.

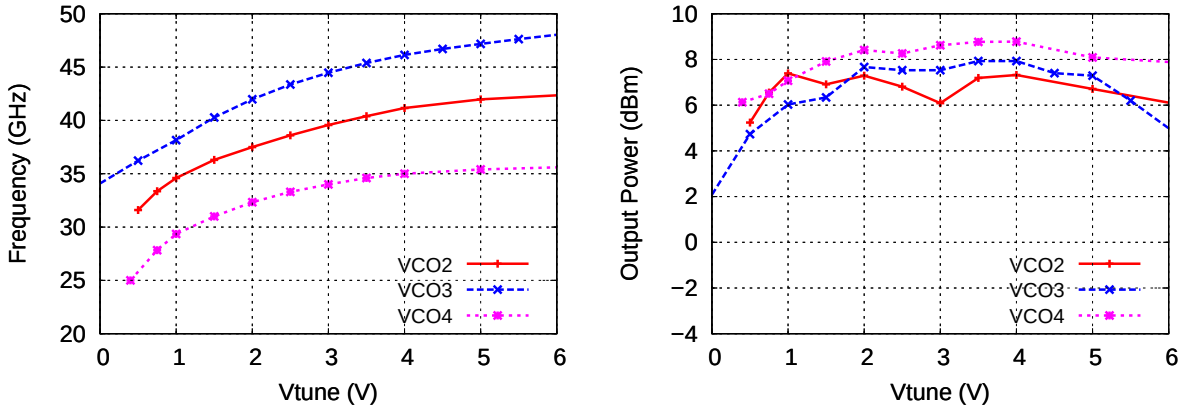
The VCO with separate buffer amplifiers (4.6) has also been realized and characterized. Fig. 4.10 (a) shows the chip photo of the realized VCO. The frequency can be tuned from 33 GHz to 43 GHz, as shown Fig. 4.10 (b), with more than 10 dBm output power, and the DC power consumption is 376 mW (4 V, 96 mA). Further measurement details of the VCO can be found in [27].



(a) (b)

Figure 4.10: (a) Photo of the VCO with separate buffer amplifier at the output. The size is 1×0.75 mm^2, including the bonding pads. (b) Measured frequency and output power.

One advantage of using TFMLs in the design is that the circuit can be easily modified. Different VCOs have been realized for different frequency ranges, by adjusting the length of L_B (in Fig. 4.2) and the number of varactors (C_{VAR}) that is connected in parallel. Fig. 4.11 shows the measured frequency and output power of three different VCOs. They cover a frequency range from 25 GHz to 48 GHz, with about 6 dBm output power, which is sufficient to drive a frequency doubler (described in the following subsection). Therefore, with slight modification of the VCO and a frequency doubler, signal generation from 25 GHz to 96 GHz can be easily realized.



(a) (b)

Figure 4.11: Frequency (a) and output power (b) versus tuning voltage of different VCOs.

4.2 Frequency Doubler

Conversion gain, maximum output power and suppression of unwanted harmonics are important characteristics of frequency doublers. In this thesis work, the output signal of the frequency doubler will drive the switching quad of the down-converting mixer. Therefore, the main design goal is to have high conversion gain and output power. Meanwhile, a wide band frequency doubler is preferred, since the VCO has a very wide tuning range, as described in Section 4.1.2.

A frequency doubler based on the push-push topology has been realized. The doubler mainly consists of a emitter-coupled-pair (ECP), as shown in Fig. 4.12 (a). When there is a differential signal applied to the bases of the two transistors of the ECP, the current that flows through the emitter node (where the two emitters are connected) contains a strong second harmonic, which is then converted to a voltage by the inductor at the emitter. This type of frequency doubler can provide higher conversion gain, compared to passive frequency doublers based on diodes, as in [28], and it requires less chip area than the non-linearity type of frequency doublers[7], because no specific filter and matching networks is needed at the input and output. Frequency doublers based on the push-push topology have been reported [30–32], but they all operate at relatively low frequencies (compared to f_{max}). In this thesis work, the frequency doubler is operated at frequencies close to f_{max}. Therefore, the circuit is modified to have better performance in the designed frequency range.

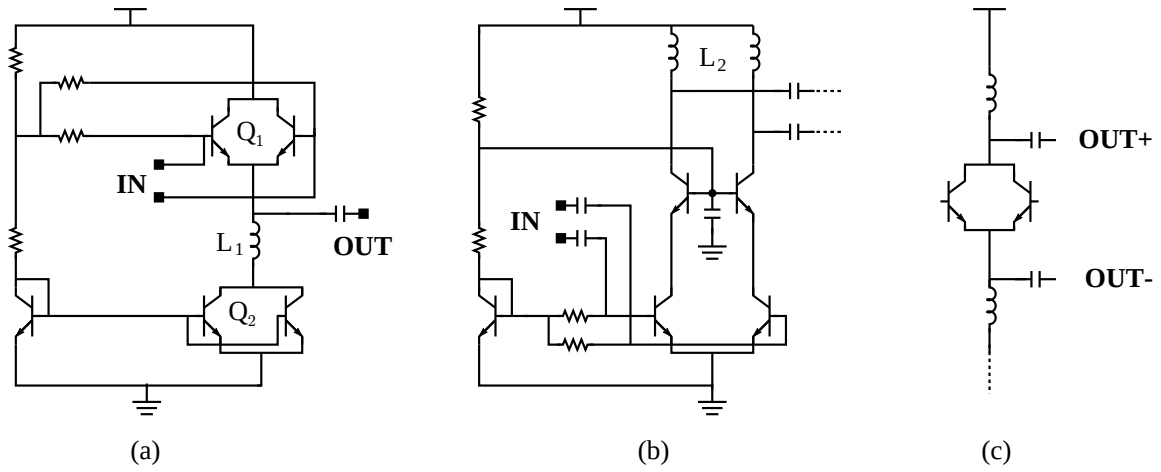


Figure 4.12: (a) Push-push frequency doubler core. (b) Driver amplifier. (c) Push-Push core with differential output.

4.2.1 Doubler Design

The push-push frequency doubler is shown in Fig. 4.12 (a). The core of the doubler is the CEP (Q_1 and Q_2). The transistors are biased using voltage divider and current sources

[7]By driving the transistors into saturation and filter out the second harmonic, as in [29].

(Q_3 and Q_4). The output current is converted to voltage using an inductor (L_1) at the emitter node. The circuit can also provide a second output by using another inductor at the common collector to form a differential output, as shown in Fig. 4.12 (c). However, the phase difference between the two outputs is near 180 degrees only over a very narrow bandwidth, because of the inductive loading. Therefore, only one output is taken from the common emitter in this thesis work.

Transistor Q_1 and Q_2 have large sizes (20 μm emitter length), so that they can handle more current. One design choice is the biasing condition of the transistors. Fig. 4.13 shows the simulated output power and conversion gain versus frequency at different input power levels for class-A and class-B operation. For low input power levels, class-B operation shows higher conversion gain and consumes less DC power, leading to better efficiency. However, the DC current increases and the conversion gain decreases with increasing input power, leading to lower output power at high input levels, compared to the class-A operation. Therefore, in this thesis work, the transistors are biased under class-A operation, for higher output power.

The load inductor L_1 is also important for achieving higher conversion gain and output power. In this design, a 0.28 nH spiral inductor is used for L_1, which provides sufficient conversion gain and occupies not too much area. A TFML can also be used to realize L_1 but requires more chip area.

The frequency doubler requires differential input signals. An input with common mode component will reduce the conversion gain and increase the fundamental leakage at the output. In this thesis work, the frequency doubler is driven by the VCO, which directly provides the differential signal. However, to characterize the frequency doubler, a balun is needed, since a differential signal source is not available. Therefore, a separate frequency doubler with integrated driver amplifier at the input has been realized. The amplifier is a cascode amplifier tuned at 30 GHz with a peak gain of 7 dB, as shown in Fig. 4.12 (b), which serves as an active balun[8] and amplifies the input signal. The detailed schematic of the push-push doubler with driver amplifier is provided in Appendix C.2 (Fig. C.4, page 115)

4.2.2 Performance

The frequency doubler with integrated driver amplifiers was characterized on-wafer.
Fig. 4.14 (a) shows the photo of the realized circuit. The doubler is biased at 4V and consumes 39 mA current in total (18.8 mA from the doubler core). The input signal was applied through a "GSG" probe, as shown in Fig. 4.14 (b). The output was connected to a V-band harmonic mixer, which extends the frequency range of the spectrum analyzer.

The input signal was swept from 20 GHz to 40 GHz, with fixed power of 0 dBm. This leads to about 7 dBm at the output of the driver amplifier, which is comparable to the VCO output power. The measured power of the frequency-doubled signal and the leaked fundamental signal is shown in Fig. 4.15. The measured output power peaks at

[8]The second input of the amplifier is grounded so the differential amplifier serves as an active balun.

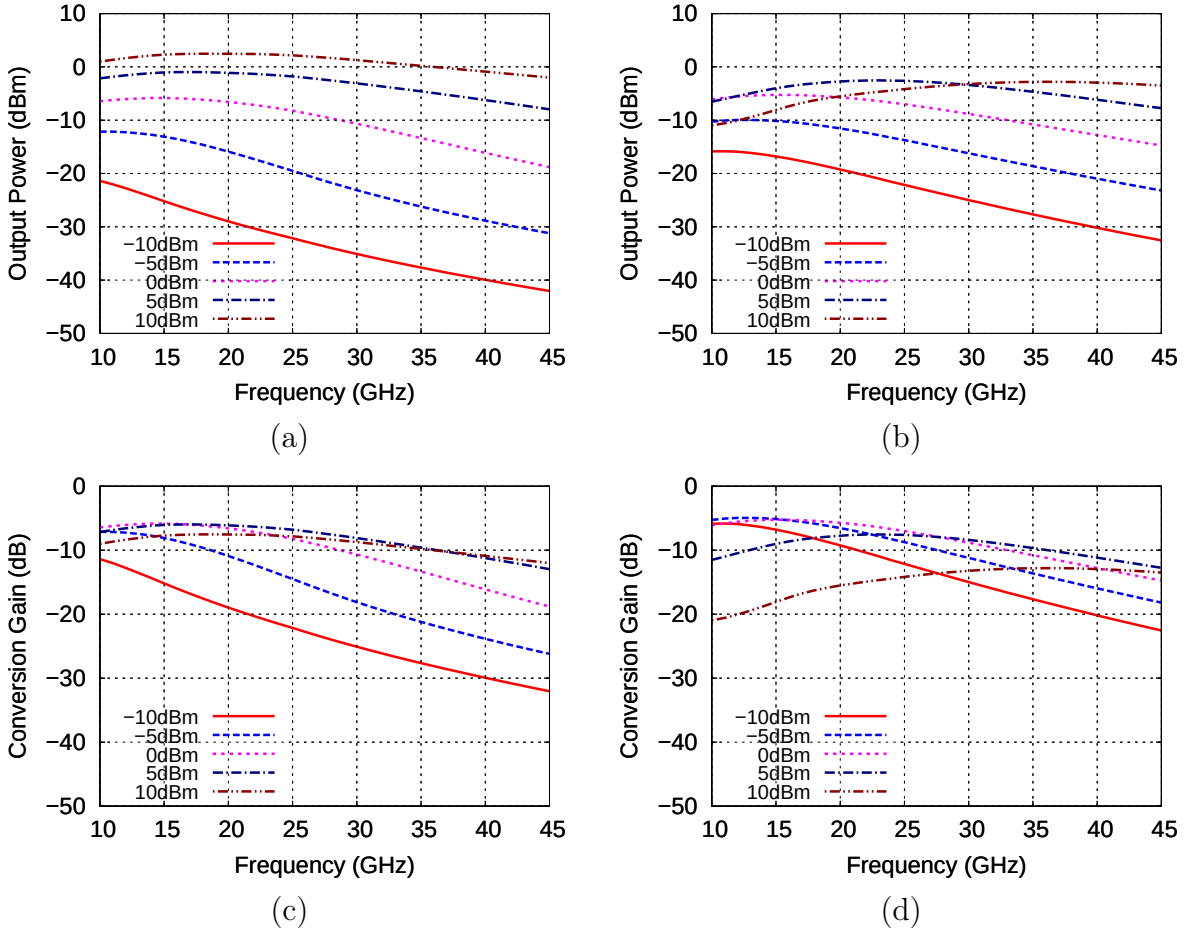


Figure 4.13: Simulated output power and conversion gain versus frequency for class-A operation ((a), (c)) and class-B operation ((b), (d).)

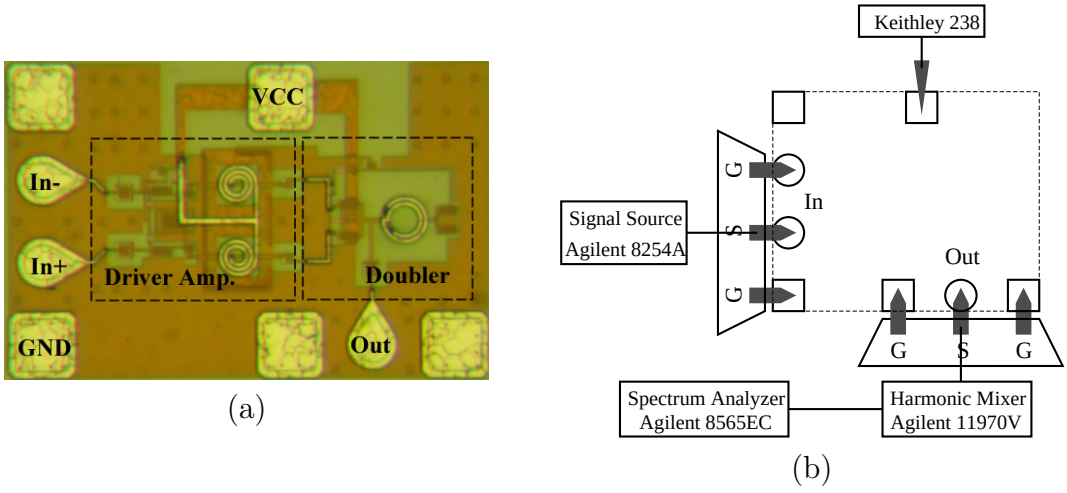


Figure 4.14: (a) Photo of the realized frequency doubler with driver amplifier. The size is 0.58×0.38 mm^2, including the bonding pads. The doubler core is only 0.17×0.17 mm^2 (b) Measurement setup.

60 GHz (-1.6 dBm), and slowly decreases to -4.4 dBm at 50 GHz and 68 GHz (30% 3-dB bandwidth). The bandwidth is mainly limited by the driver amplifier. The simulated output power under ideal differential driving condition is also shown in Fig. 4.15 for comparison. Due to the non-ideal input signal, the measured output power is lower than simulation and the leakage of the fundamental signal at the output is relatively high. When the input is fed differentially, the leakage is much lower, as shown later in Fig. 4.18. The frequency doubler was characterized further, by sweeping the input power for different output frequencies. The measured output power and calculated conversion gain are shown in Fig. 4.16. A maximum converion gain of 1.5 dB is achived at 60 GHz output with -6 dBm input power. The saturated output power is about -1.5 dBm at 60 GHz and -3.5 dBm at 50 and 70 GHz.

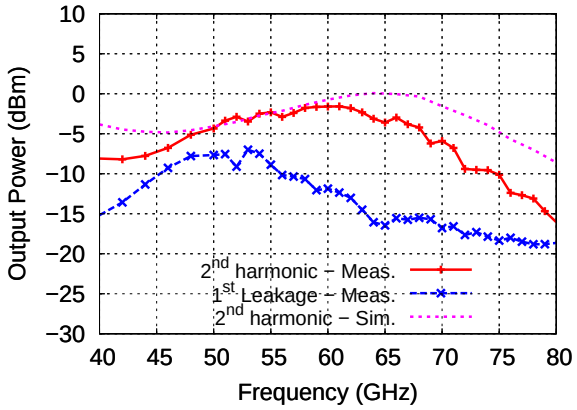
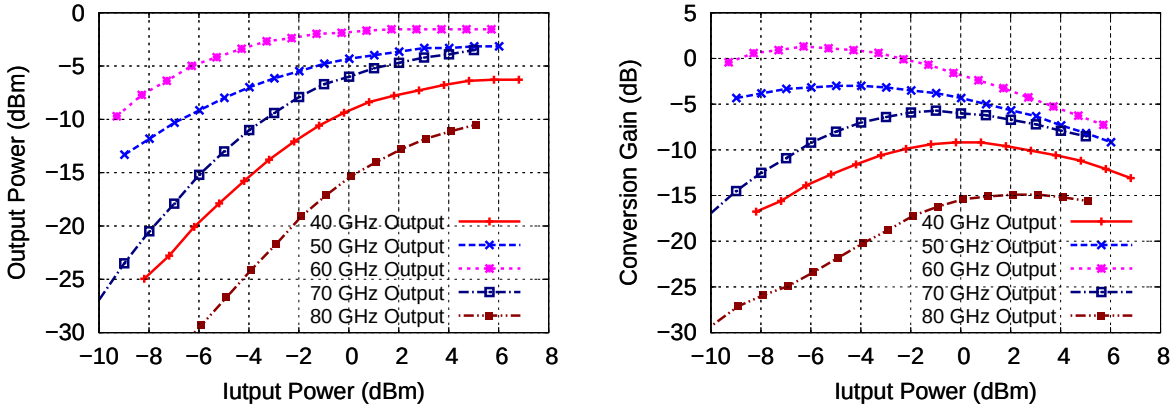


Figure 4.15: Measured output power versus frequency.

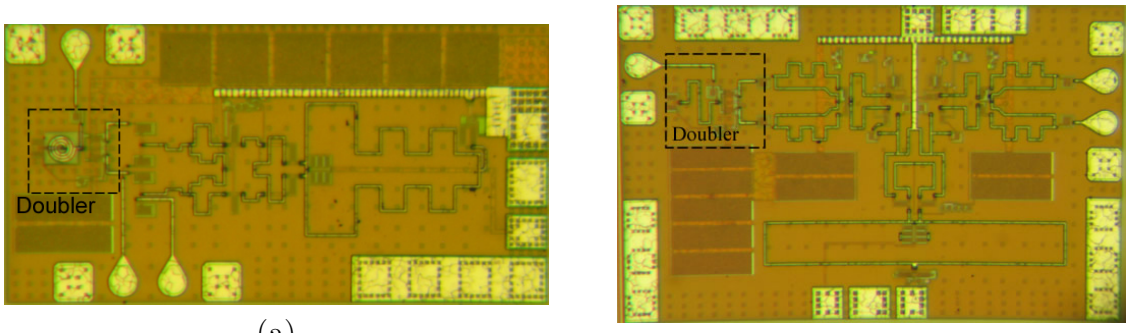


(a) (b)

Figure 4.16: Measured output power (a) and calculated conversion gain (b) versus input power at different output frequencies.

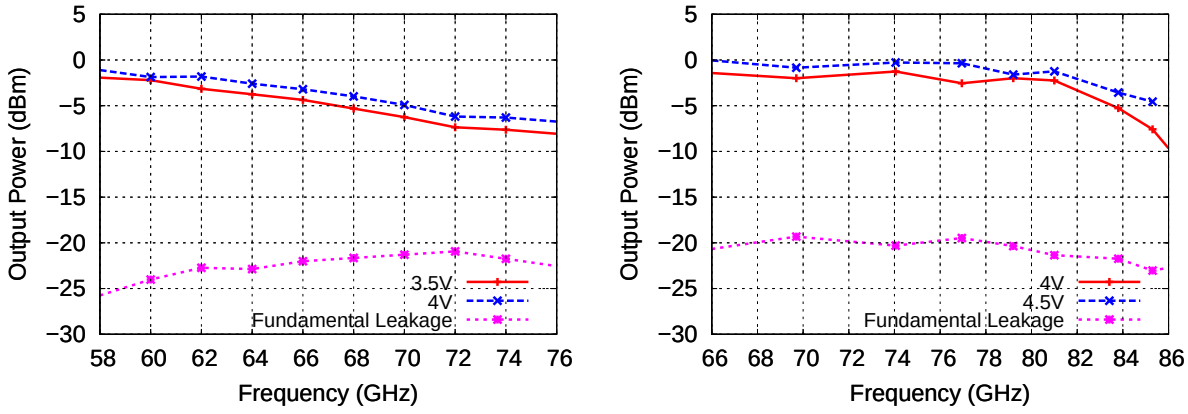
In the final circuit, the doubler core will be directly integrated with the VCO. Two different VCOs with different frequency tuning ranges and output power have been integrated with the doubler for characterization. Fig. 4.17 (a) shows a photo of the fist IC. The circuit is characterized on-wafer, biased at 3.5 V and consumes 170 mW DC power. The measured output power, as shown in Fig. 4.18 (a)., decreases slowly from -1.9 dBm (at 58 GHz)

to -8 dBm (at 76 GHz). The fundamental leakage at the output is below -21 dBm over the complete frequency range. At 66 GHz, which is the intended LO frequency for the down-converter, the output power is -4 dBm and the leakage of the fundamental signal is below -22 dBm (18 dB suppression). The output power of the doubled signal can be increased by increasing the supply voltage to 4V (58.5 mA current). Fig. 4.17 (b) shows the second IC, targeting higher output power and frequency. It consists of a push-push doubler (inductor L_1 realized with TFML) and the high output power VCO with separate buffer amplifiers (Fig. 4.10 (a)). The circuit operates under 4 V supply (99 mA current). Fig. 4.18 (b) shows the measured output power at the doubler output. The power peaks at 74 GHz (-1.1 dBm) and decreases to -2.4 dBm at 81 GHz. The fundamental leakage is below -20 dBm. By increasing the supply to 4.5 V (112 mA current), 0 dBm output power can be achieved up to 77 GHz. The second buffer amplifier of the VCO provides a direct output of the fundamental signal. The current in this amplifier is reduced to save DC power. The power of the fundamental output is -1±1 dBm, which is sufficient to drive frequency dividers.



(a) (b)

Figure 4.17: (a) Photo of IC1, including frequency doubler and VCO1 (Fig. 4.7). The chip size is 1.1 × 0.56 mm^2. (b) Photo of IC2, including frequency doubler and the VCO with high output power (Fig. 4.10). The chip size is 1.2 × 0.75 mm^2.



(a) (b)

Figure 4.18: Measured output power (frequency-doubled output and fundamental leakage) of the VCO and doubler ICs (Fig. 4.17 (a) and Fig. 4.17 (b)).

4.3 Summary and Comparison

VCOs with high output power and wide tuning range are described in this chapter. The 30% tuning range is comparable to the state-of-art results reported in [33] (30%) and [23] (26%). With slight modification, different VCOs have been realized, which cover a complete frequency range from 25 GHz to 48 GHz.

Push-push frequency doublers are also described in this chapter. The doubler operates over a very wide bandwidth and is capable of generating high output power. By combining the VCO and frequency doubler, signal generation from 58 GHz to 86 GHz with relatively high output power has been demonstrated, using a SiGe HBT technology with 80/90 GHz f_T/f_{max}. Tab. 4.1 compares this work with other signal generation circuits that operate at frequencies close to f_{max}.

Table 4.1: Comparison of Signal Generation Circuits Operating at Frequencies Close to f_{max}

Ref	**Technology** f_T/f_{max} **(GHz)**	f_{osc}	f_{osc}/f_{max}	**Tuning Range**	**Pwr dBm**	**PN** @1MHz	**Fundamental Output**	**DC mW**	**Topology**
[34]	InGaP HBT 50 / -	60	1.2 (f_{osc}/f_T)	2.3%	-14	-77.5	Yes	-	VCO+doubler
[35]	0.14μm SiGe:C HBT 200 / 275	278	1.01	1.5%	-20	-	No	132	Push-push
[36]	0.5μm InP D-HBT 405 / 335	287	0.85	4%	-3	-	No	-	Push-push
[37]	0.14μm SiGe:C HBT 200 / 275	190	0.69	3.9%	-4.5	-73	No	215	Push-push
[38]	0.13μm CMOS - / -	192	>1	0.7%	-20	-100 at 10MHz	No	16.5	Push-push
[39]	90nm CMOS - / 160	324	2	1.2%	-46	-78	No	12	Linear superposition
This	**0.8μm SiGe HBT 80 / 90**	**86**	**0.96**	**26.3%**	**-2.5**	**-83**	**Yes**	**392**	**VCO+doubler**

Chapter 5

Frequency Divider

Frequency dividers are important building blocks in modern PLLs and synthesizers. In this thesis work, frequency dividers are used in the PLL to lower the VCO frequency. Two types of single-stage frequency dividers (static and dynamic) are realized and multi-stage frequency dividers with different division ratio are built by cascading the two types of single-stage dividers. The design, simulation and characterization of the frequency dividers are described in this chapter.

5.1 Static Divider

Static frequency dividers are the most commonly used frequency dividers nowadays. The most basic one is a divide-by-2 frequency divider based on master-slave D flip-flops (MS-DFF), as shown in Fig.5.1 (a). The first DFF (master) is clocked by the input signal, while the second DFF (slave) is clocked by the inverted input signal. When there is a input clock, as shown in Fig.5.1 (b), the output node holds the polarity for one period of the input clock and inverts for the next period. Therefore, the output clock period is doubled.

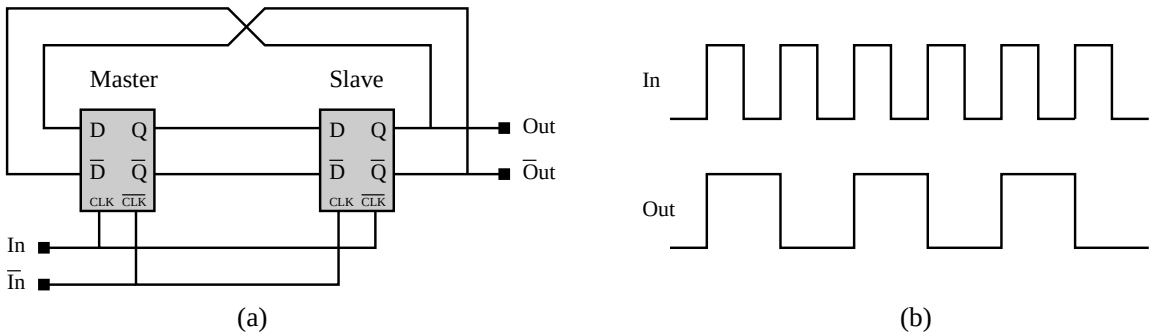


Figure 5.1: (a) Block diagram of the static frequency divider based on master-slave D flip-flops. (b) Illustrative input and output wave forms of the static frequency divider.

The most important characteristics of frequency dividers are speed (maximum operating

frequency), required input power, output power and DC power consumption. These characteristics can not be achieved at the same time. Therefore, different trade-offs must be considered for different requirements. In this thesis work, different static frequency dividers are designed and optimized for different purposes (maximum speed, low power consumption, etc.). This section describes the static frequency divider for maximum speed, other dividers are described in Section 5.3 (page 52).

Circuit Design

Fig. 5.2 shows the schematic of the static divider realized according to the block diagram of Fig. 5.1 (a). The DFFs are built using ECLs (Emitter-Coupled-Logic). The emitter follower (Q_4) provides the DC level shift and improves the speed. More stages of emitter followers can be used to further improve the speed, as widely used in reported frequency dividers [40, 41], but this requires higher supply voltage and more current, which significantly increases power consumption, while the increase of speed is not significant. Therefore, only one stage of emitter followers is implemented. The output is buffered by another emitter follower stage (Q_5) to reduce the loading to the divider core and provides higher output power.

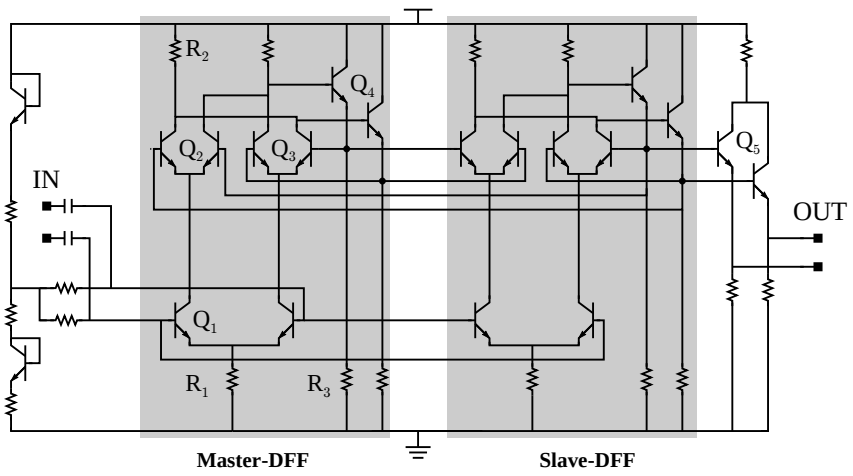


Figure 5.2: Schematic of the static frequency dividers.

The maximum operating frequency of the MS-DFF divider has been studied in [42,43]. It is approximately given by $1/(2\tau_D)$, where τ_D is the propagation delay time of the critical path in the circuit (upper ECLs (Q_2, Q_3) and emitter followers (Q_4)). It is shown in [42,43] that τ_D can be expressed as the linear weighed sum of different time constants, which are determined by the load resistor and the transistor junction resistances and capacitances, as shown in Equation 5.1.

$$\begin{aligned}\tau_D = {} & K_{01}\tau_F + R_2(K_{02}C_{JC} + K_{03}C_{JS} + K_{04}C_{JE}) \\ & + R_B(K_{05}C_{JE} + K_{06}C_D + K_{07}C_{JC} + K_{08}C_{JS}) \\ & + R_C(K_{09}C_{JE} + K_{10}C_D + K_{11}C_{JC} + K_{12}C_{JS}) \\ & + R_E(K_{13}C_{JE} + K_{14}C_D + K_{15}C_{JC} + K_{16}C_{JS}),\end{aligned} \tag{5.1}$$

where K_{01}-K_{16} are the weighting factors, R_B, R_C, R_E are the transistor base, collector and emitter parasitic resistances, C_{JC}, C_{JS}, C_{JE}, C_D are the base-collector, collector-substrate, base-emitter depletion and base-emitter diffusion capacitances. The weighting factors can be calculated using the sensitivity analysis introduced in [44]. According to [42], the main contributions to τ_D in HBTs are: τ_F (transistor forward transit time), R_2C_{JC}, R_BC_D, R_BC_{JE}, R_2C_{JS}. Therefore, to have small τ_D, the load resistor (R_2) should be small. However, τ_D increases when R_2 is below an optimum value, due to the increase of C_D (calculated as $2\tau_F/R_2$) [43]. The transistor in the upper ECLs should also be small to minimize the junction capacitance, but the base resistance also increases as the transistor gets smaller, which could prevent using the smallest transistor.

The static frequency divider is designed based on the above mentioned guidelines. Transistors with "CEB" configuration are used for Q_1, Q_2 and Q_3, because of the lower base-collector junction capacitance, compared to the "CBE" configuration. The emitter finger size is 2.0×0.5 μm^2, which is the third smallest size available in the technology. Compared with smaller transistors, this gives better compromise between base resistance and junction capacitance, which leads to higher maximum operating frequency[1]. The transistors are biased at I_{max}, to have the highest f_T and therefore lowest τ_F. The feedback transistor Q_4 has "CBEB" configuration, with emitter size of 5.0×0.5 μm^2 to have small base and emitter resistance, which also reduces the total propagation delay.

According to [42], an optimum load resistor exists for minimum τ_D. Calculating the optimum load resistor (R_2) based on the method described in [42] is very time-consuming and not practical for this thesis work [2]. Instead, R_2 is determined by decreasing its value step by step until the maximum operating frequency stops increasing. It is found that 100 Ω is an optimum value for achieving the highest operating frequency.

To provide sufficient output power and reduce the loading of the MS-DFF divider core, an emitter-follower (Q_5) is added at the output. The detailed parameters of the frequency divider can be found in Appendix C.3 (Fig. C.5, page 116).

When there is no input signal applied, the divider maintains a self-oscillation (output frequency f_{osc}), due to the polarity inversion in the DFFs. The self-oscillation frequency is a measure of the speed of the static divider, since it is directly related to the delay in the loop. Higher self-oscillation frequency gives higher maximum operating frequency. Therefore, the self-oscillation frequency is maximized in the design to have the highest operating frequency. The dividers are simulated in ADS, using transient simulation. The self-oscillation frequency can be easily calculated using Fast-Fourier-Transform (FFT).

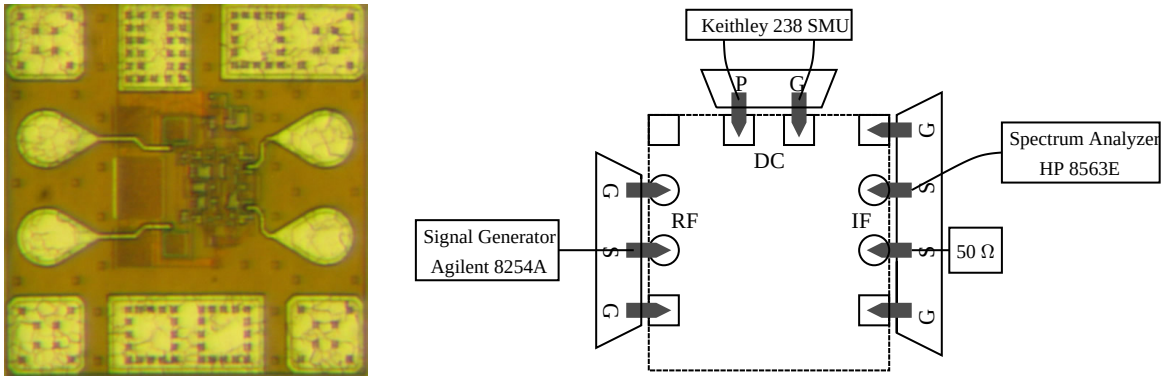
Optimized for maximum speed, the static divider consumes 26.5 mA current from a 4 V supply. When the required operating frequency of the divider is lower, the speed can be traded for less power consumption, by decreasing the current in the ECLs and increasing the load resistors. A second divider has been realized for comparison, with 150 Ω load resistor and 18 mA total current.

[1] Static dividers using the smallest transistors has been reported in [45], where the maximum operating frequency is 6 GHz (20%) lower than this design

[2] K_{01}-K_{16} need to be calculated, each requiring changes of two parameters in Equation 5.1 and calculation of τ_D. Further details is provided in [44]

Characterization

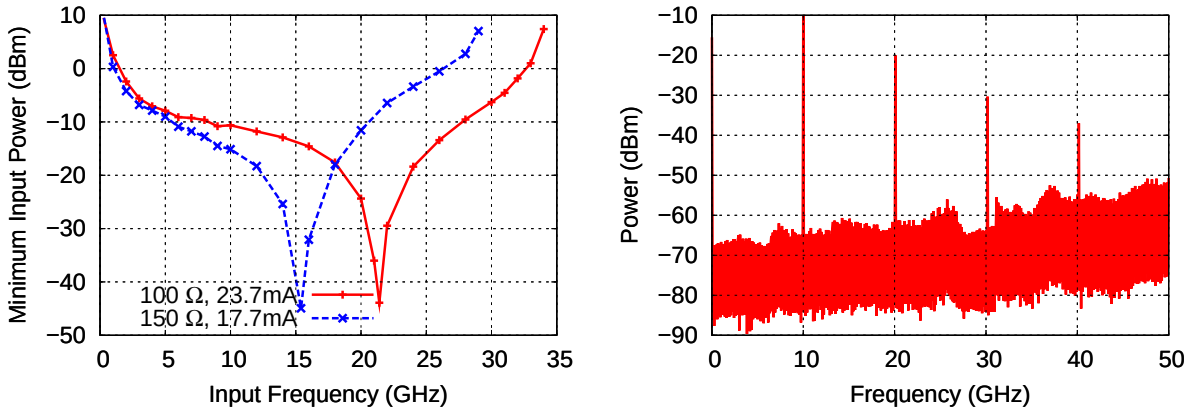
Fig. 5.3 (a) shows a photo of the realized static frequency divider. The circuit was characterized on wafer. Fig. 5.3 (b) shows the measurement setup. Due to the lack of differential signal source, the input was fed single-endedly.



(a) (b)

Figure 5.3: (a) Photo of the realized static frequency divider. The size is 0.36 × 0.38 mm^2, including the bonding pads. (b) Divider measurement setup.

To determine the input sensitivity curve, the input power was reduced at each input frequency until the divider stopped dividing. The measured input sensitivity curves for the two versions of static dividers are shown in Fig. 5.4 (a). The self-oscillation frequencies of the two dividers differ by 3 GHz. The one optimized for highest speed can divide up to 34 GHz, while the other can divider up to 29 GHz. At frequencies (input) close to the self-oscillation frequency, the required input power is very low, as shown in Fig. 5.4 (a). As the frequency gets far from the self-oscillation frequency, the required input power increases. For the high-speed divider, the required input power is below -10 dBm from 8 GHz to 28 GHz.



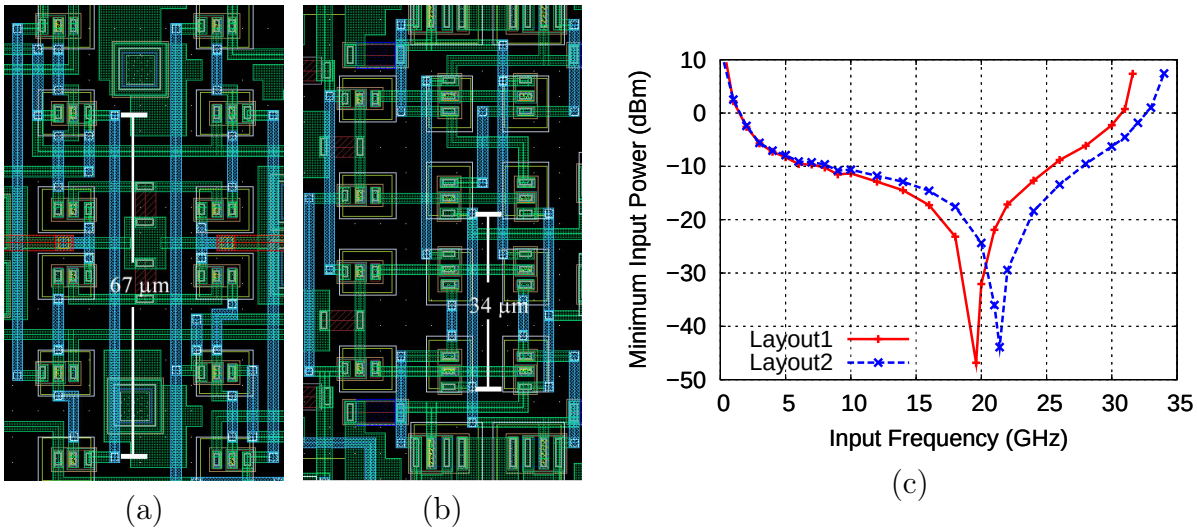
(a) (b)

Figure 5.4: (a) Input sensitivity curve of the two static dividers (b) Output spectrum of the divider with 20 GHz input signal.

In principle, the static divider can operate down to DC. However, due to the small on-chip DC-blocking capacitance (500 fF) at the input, the dividers can divide only down

to 270 MHz. The output power remains constant when the input signal power increases. Both dividers can deliver -5 dBm total output power, which is sufficient to drive a second divider. Fig. 5.4 (b) shows the measured single-ended output spectrum with a 20 GHz input signal.

Layout of the MS-DFF divider is very critical for the maximum operating frequency. To minimize the propagation delay, the interconnect between transistors should be as short as possible. For the same divider design, two different layout configurations have been realized with different emphasis. The symmetry of the circuit is kept as much as possible in the first layout (Fig. 5.5 (a)), leading to a longer interconnect (67 μm) between the master and slave DFFs. The second layout (Fig. 5.5 (b)) has shorter interconnect (34 μm) between the master and slave DFFs but also has slight asymmetry. The input sensitivity of the two dividers are shown in Fig. 5.5 (c). At frequencies below 8 GHz, the measured sensitivity curves of the two dividers overlap with each other. However, as the input frequency increases, the performance of the two dividers starts to deviate and the maximum operating frequency of "layout1" is about 3 GHz (almost 10%) lower than "layout2". This difference is only caused by longer interconnects, which clearly shows the importance of layout optimization for millimeter-wave circuits.



(a) (b) (c)

Figure 5.5: (a) Layout1 of the divider with emphasis on the symmetry. The longest interconnect is 67 μm. (b) Layout2 of the same divider, with emphasis on shorter interconnect. The longest interconnect is 34 μm. (c) Measured sensitivity curve of the same divider design with two different layouts.

Higher Operating Frequency

The maximum operating frequency of the static frequency divider based on the MS-DFFs (Fig. 5.2) has been analyzed. It is still possible to improve the maximum operating frequency, with modification of the circuit topology. One method is to separate the load resistors of the reading (Q_2) and latching (Q_3) ECL [46], as shown in Fig. 5.6 (a). Therefore, the latching ECL can have a small load resistor to reduce the RC delay in the latching ECL and improve the speed of the static divider. An extreme case is to completely remove the latching ECL. The maximum operating frequency can be increased

to 46 GHz (in simulation) without the latching ECL. However, the operating frequency range becomes much narrower.

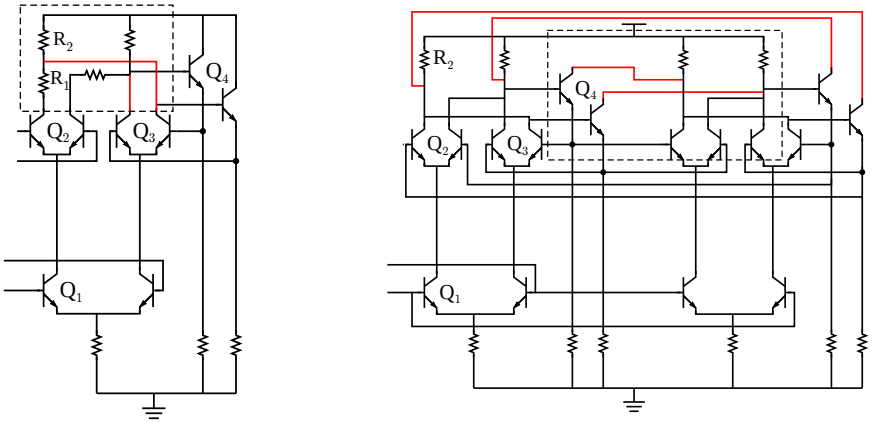


Figure 5.6: (a) DFF with separate load resistors for the reading and latching ECL. (b) Modified static frequency divider, with collector of Q_4 in the master DFF connected to the load resistor of the slave DFF.

Another method is to connect the collector of Q_4 in the master DFF to the load resistor of the slave DFF [46], as shown in Fig. 5.6 (b). By doing this, the current flowing through the load resistor can be switched faster and the speed of the divider can be improved to 42 GHz (in simulation). Since higher current is flowing through the load resistor, the required supply voltage is higher.

A third method is to insert an inductor in series with the load resistor to increase the gain at higher frequencies. This is especially useful for high frequency dividers, as the required inductor is small. For the design in this thesis work, the speed improvement is not much (up to 38 GHz) but very large inductors (0.4 nH) are required, which significantly increases the circuit size and make the layout more difficult.

Therefore, none of the above mentioned methods for speed improvement was adopted. Instead, higher operating frequency has been achieved by using dynamic frequency dividers, which can operate up to much higher frequencies and consume less power (for the same speed). The design and characterization of the dynamic dividers are introduced in the following section.

5.2 Dynamic Divider

As shown in the last section, the maximum operating frequency of the static frequency divider is 34 GHz, which is not sufficient to cover the entire tuning range of the VCO described in Chapter 4. Therefore, dynamic dividers that can operate at much higher frequencies are realized. The dynamic frequency divider is base on the regenerative concept [47], as shown in Fig. 5.7. It consists of a mixer, a low-pass filter and an amplifier, which form a feedback loop. The output of the mixer, after passing the low-pass filter

and amplifier, is fed back to one input of the mixer. When an input signal at frequency f_{in} with a certain power is applied to the other input of the mixer, the divider will sustain an oscillation within the loop at frequency $\frac{f_{in}}{2}$, provided that the higher mixing products ($\frac{3f_{in}}{2}$, $\frac{5f_{in}}{2}$, etc.) are filtered out by the low-pass filter. When further frequency multiplication or division is introduced in the loop, different frequency division ratios ($\frac{1}{3}$, $\frac{1}{5}$ etc.) can also be realized.

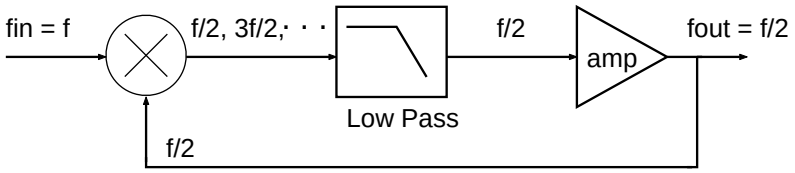


Figure 5.7: Regenerative frequency divider principle.

Circuit Design and Simulation

Fig. 5.8 shows a general schematic of the dynamic divider. The mixer is based on the Gilbert cell topology with a trans-impedance amplifier (TIA) as the load. The TIA increases the mismatch in the loop, leading to wider bandwidth (similar to the transimpedance load in the down-converting mixer, Chapter 3), and much better performance (with respect to maximum operating frequency, safe broadband operation and high sensitivity), compared with a single resistor as the load [48]. The feedback is done through emitter followers (EFs), which perform both current amplification and DC level shift. Also, because of the inherent low-pass characteristic of the loop response, no additional low-pass filter is needed. Another EF is used as the output buffer to reduce the loading of the divider core and increases the output power.

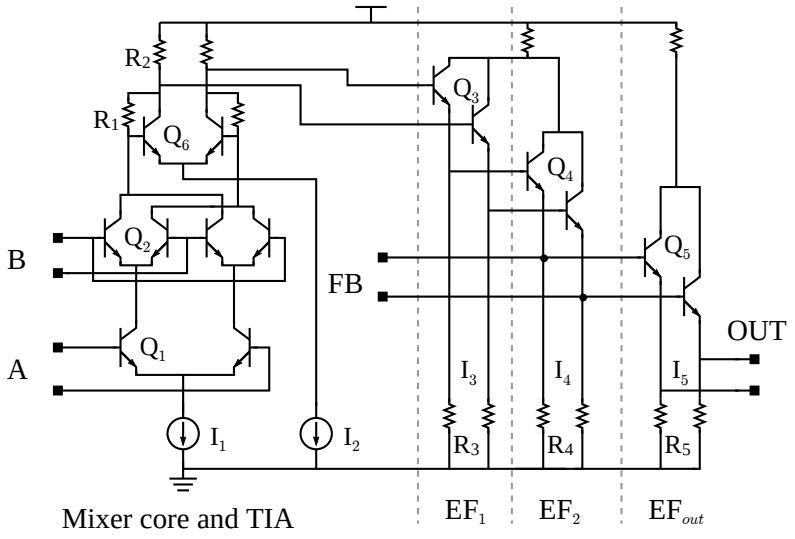


Figure 5.8: General schematic of the dynamic frequency divider.

The schematic in Fig. 5.8 is not complete and can lead to two different configurations. The feedback from the EF (indicated as "FB"), can be connected to either the transconductance stage (indicated as "A") or the switching quad (indicated as "B") of the mixer,

while the divider input signal is applied to "B" or "A" of the mixer. Dynamic dividers based on these two types of configurations have been reported [49, 50], but the difference between the two configurations has rarely been discussed and a direct comparison of the two configurations has not been reported at the time of the thesis work. Therefore, different dividers based on the two configurations have been realized and compared in this thesis work.

The first divider uses the "B" port of the mixer as divider input, while the feedback is connected to the "A" port of the mixer, as shown in Fig. 5.9 (a). Two EFs are inserted in the feedback path. The circuit is optimized for maximum operating frequency with a 4 V supply. The second divider uses the same topology ("B" port as divider input), but operates at lower frequencies with reduced current. The output EF (Q_5) is connected to the base of Q_4, due to the low DC potential at the emitter of Q_4. The third divider uses the "A" port of the mixer as the divider input, but only one EF is inserted in the feedback path, because of the low DC voltage drop in the path, as shown in Fig. 5.9 (b). This reduces the maximum operating frequency of the divider. So a fourth divider was designed, which also uses the "A" port as the divider input but the supply voltage is increased to 5 V and two EFs are inserted in the feedback path to achieve higher operating frequency.

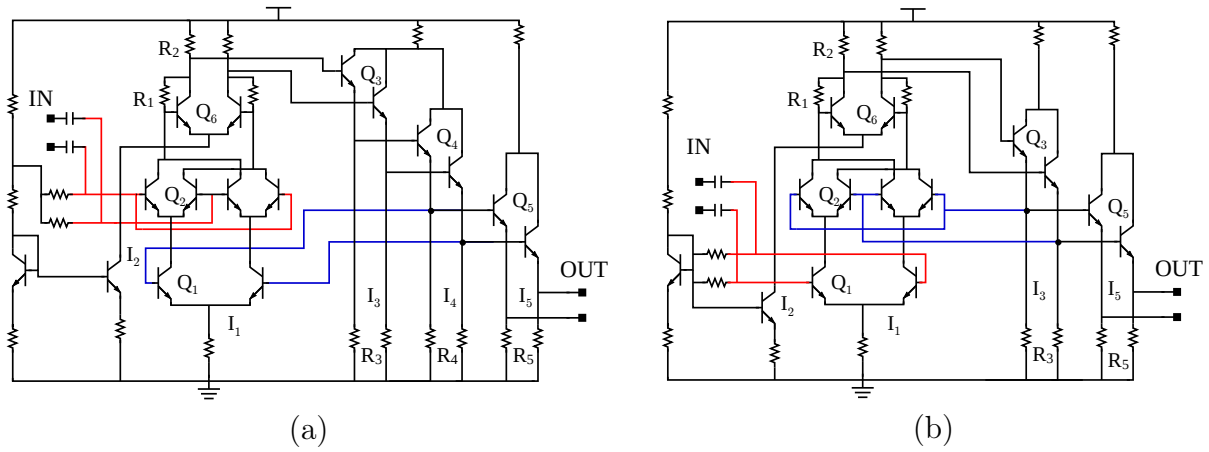


Figure 5.9: (a) Schematic of dynamic frequency divider I (b) Schematic of dynamic frequency divider III.

Small transistors ($5 \times 0.5\ \mu m^2$ emitter finger size, "CBEB" configuration) are used in the mixer core and TIA, which provide sufficient gain with small current consumption. The four dividers have the same mixer core (slightly different current) and differ mainly in the TIA (R_1, R_2) and EFs (transistor and current). The detailed summary of the four dynamic dividers are shown in Tab. 5.1, Tab. 5.2 and Tab. 5.3.

The dynamic dividers usually operate at higher frequencies, where the static dividers can not operate. Therefore, the maximum operating frequency is an important characteristic of the dynamic dividers. In the regenerative topology (Fig. 5.7), the maximum operating frequency is determined by the open-loop gain (referred to later as loop gain) bandwidth (where the open-loop gain drops to 1). When the loop gain is smaller than 1, the oscillation in the loop will not sustain and the divider can not divide properly. Since the signal that travels in the loop is at half the input frequency, the maximum operating frequency is

about twice the frequency, where the loop gain drops to 1[3].

Table 5.1: Summary of the dynamic dividers

Circuit ID	**Divider Input**	**V_{supply}** (V)	**Current** (mA)	**EFs in the feedback path**
I	"LO"	4	28.5	2
II	"LO"	4	17.2	2
III	"RF"	4	28	1
IV	"RF"	5	38.3	2

Table 5.2: Biasing current and resistors of the dynamic dividers

Circuit ID	**I_1** (mA)	**I_2** (mA)	**R_1** (Ω)	**R_2** (Ω)	**I_3** (mA)	**R_3** (Ω)	**I_4** (mA)	**R_4** (Ω)	**I_5** (mA)	**R_5** (Ω)
I	3	4.8	300	250	3.3	650	4.4	300	2.5	200
II	3	4.4	300	350	1.3	1.5k	1.3	800	2.1	500
III	3.7	4.4	250	300	4.3	450	-	-	5.4	200
IV	3.6	4.4	350	300	3.9	750	5.1	400	5.3	220

Table 5.3: Transistors of the dynamic dividers

Circuit ID	**Q_3**	**Q_4**	**Q_5**
I	0.5×5 μm^2	0.5×10 μm^2	0.5×10 μm^2
II	0.5×5 μm^2	0.5×5 μm^2	0.5×5 μm^2
III	0.5×10 μm^2	-	0.5×10 μm^2
IV	0.5×5 μm^2	0.5×10 μm^2	0.5×10 μm^2

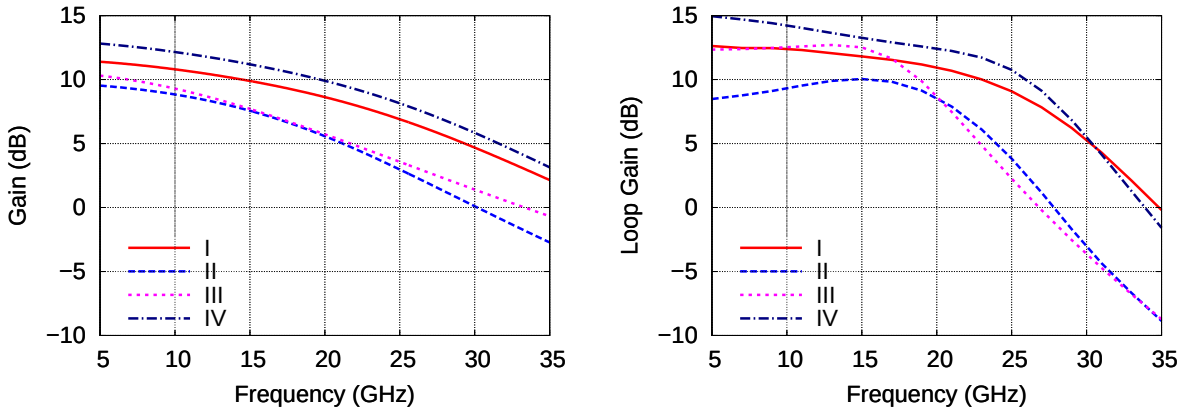
The loop gain is simulated in ADS using harmonic-balance simulation. To determine the loop gain, the dividers are cut at the feedback point "FB", as shown in Fig. 5.8. For divider I and II, input signal at frequency f_{in} is applied to the "B" port and another signal at frequency $\frac{f_{in}}{2}$ is applied to the "A" port. The loop gain is just the conversion gain of the mixer with TIA and feedback EFs. A dummy mixer core is terminated at "FB", and the gain is calculated as the power gain from "A" to "FB". For divider III and IV, input signal at frequency f_{in} is applied at the "A" port and another signal at frequency $\frac{f_{in}}{2}$ is

[3]The phase of the loop gain is not a concern, because the phase of the output signal will adjust itself and settle at a state so that the total phase delay in the loop is a multiple of 2π [51]

applied to the "B" port. The loop gain is calculated as the the power gain from "B" to "FB" (at frequency $\frac{f_{in}}{2}$).

To achieve the highest operating frequency, the loop gain bandwidth must be maximized. Since the four dividers have the same mixer core, only the TIA and feedback EFs are optimized for higher bandwidth, by adjusting the resistors (R_1 and R_2) and currents in the TIA and EFs. Fig. 5.10 (a) shows the simulated gain of the TIA and EF chain of the four dividers. Divider IV has the highest gain in the TIA and EF chain, followed by divider I. Divider III consumes the same current as divider I, but has lower gain in the TIA and EF chain, because it has only one EF in the feedback loop. Divider II has similar gain as Divider III, but with less current consumption.

The simulated loop gain (with 0 dBm input power) is shown in Fig. 5.10 (b). Divider I has the highest bandwidth. Although divider IV has the highest loop gain, the gain drops faster as the frequency increases, compared with divider I, which leads to less gain bandwidth. This is because the trans-conductance stage (Q_1) of divider I operates only at half the input frequency and hence has higher gain than divider IV, where (Q_1) operates at the input frequency. When "FB" is connected to the "A" port (as in divider I and II), there are more voltage drop in the feedback loop, which allows more EFs in the feedback loop with a fixed supply voltage, so divider II can achieve similar loop gain bandwidth as divider III with much less power consumption.



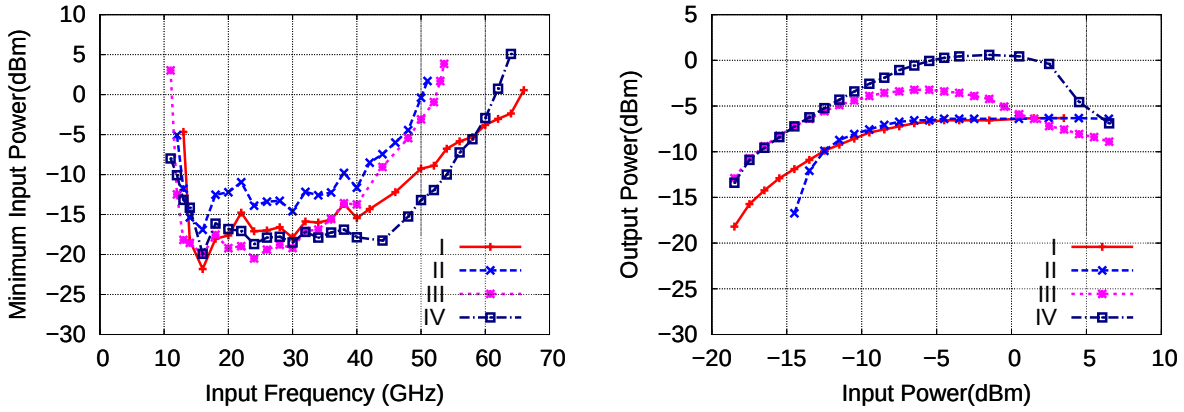
(a) (b)

Figure 5.10: (a) Simulated gain of the TIA and EF chain. (b) Simulated loop gain of the dividers with 0 dBm input power.

Characterization

The four dividers were characterized on wafer, using the same setup as the static dividers (Fig. 5.3 (b)). The measured input sensitivity curves are shown in Fig. 5.11 (a). Divider I has the highest operating frequency of 67 GHz (limited by the measurement setup). Divider IV can operate up to 64 GHz, while divider II and III can operate slightly above 50 GHz. The measured maximum operating frequency agrees quite well with the expectation base on the loop gain simulation (Fig. 5.10 (b)). At frequencies below 14 GHz, the dividers cannot divide properly, due to the not sufficiently suppressed higher mixing

harmonics[4].



(a) (b)

Figure 5.11: (a) Measured input sensitivity curve of the four dynamic dividers. (b) Measured output power versus input power with 30 GHz input signal.

The loop gain of the dynamic divider decreases as the input signal power decreases. When the gain is less than 1, the divider stops operating. Therefore, the required minimum input power of the dynamic divider is mainly determined by the loop gain. As shown in Fig. 5.11 (a), the required minimum input power for the four dividers are different. Divider II requires the highest input power due to the lowest loop gain. Generally, divider I and II ("B" as input) requires higher input power than divider III and IV, because the loop gain drops faster as the input power decreases.

The output power of the dynamic divider is determined by the steady-state power in the loop (as in an oscillator) and the output EF buffer. The power in the loop starts from noise level and increases until the gain decreases to 1. Then it remains constant. Fig. 5.11 (b) shows the measured output power of the four dividers with increasing input signal power. At low input levels, the loop gain increases as the input signal power increases, leading to an increasing output power. At high input levels, the loop gain starts to saturate, due to the non-linearity of the circuit, especially in the trans-conductance stage, and the output power stops increasing. For divider III and IV, the feedback is connected to the switching quad of the mixer and the trans-conductance stage is not in the feedback loop, so the loop gain decreases (due to gain suppression in the TIA and EFs) to 1 at higher power level, compared to divider I and II. Therefore, the steady-state signal power in the loop in divider III and IV are higher than in divider I and II. This leads to higher output power in divider III and IV[5]. It should also be noted that the output power of III and IV starts to decrease when the input power is too high, as shown in Fig. 5.11 (b). This is because less "LO" power is needed to maintain the oscillation in the loop, due to the large input

[4]At the lower edge of the operating frequency range, the divider operation is not stable. The divider operates either in synchronous mode (normal divide-by-two), or asynchronous mode (two output frequencies that are not equal), depending on the input signal power and the phase shift of the loop. Detailed explanation is provided in [51].

[5]By increasing the current in the output EFs, the output power of divider I and II can be increased, but still less than divider III and IV.

power at the transconductance stage. Therefore, for dividers with "RF" as input, very high input power should be avoided.

The simulation and measurement results show that the configuration of divider I and II (feedback to "RF" port, "LO" port as input) should be used, when higher operating frequency and low power consumption are pursued. When the input and output power are of more concern, the configuration of divider III and IV (feedback to "LO" port, "RF" port as input) should be used.

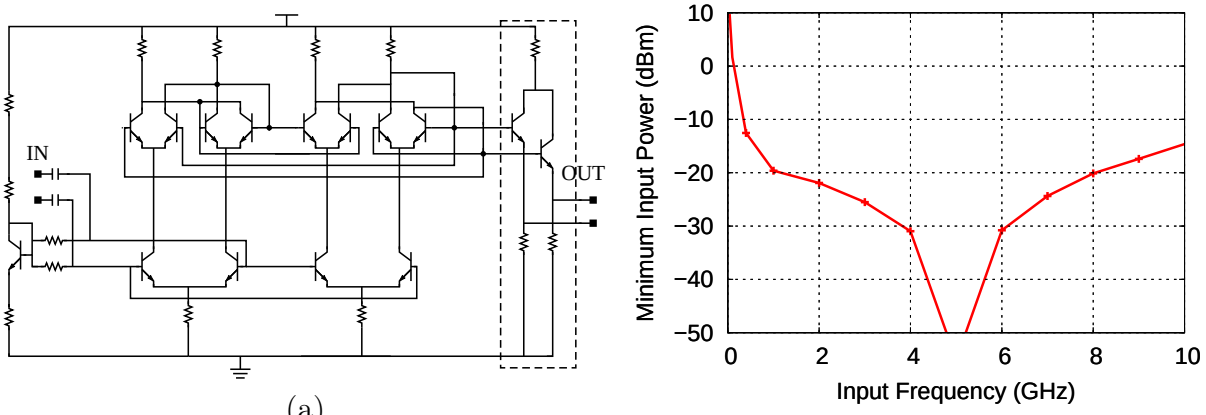
5.3 Multi-Stage Divider

Frequency dividers are usually used in the PLL to lower the VCO frequency so that the loop can be designed at much lower frequencies. Therefore, higher frequency division ratio is necessary. The most common method to get higher division ratio is to cascade several divide-by-2 dividers. However, because of the many stages, the DC power consumption of the frequency divider goes up and contributes the most to the total DC power consumption of a PLL. Therefore, the DC power consumption of the multi-stage divider should be minimized. Also, the divider chain should be able to operate properly over the complete designed frequency range, so the operating frequency range, input and output power of each individual stage must be designed carefully.

Different static and dynamic frequency dividers have been described in Section 5.1 and 5.2, but those dividers are optimized for higher operating frequency, thus consume more DC power. In a multi-stage divider, only the first one or two stages need to operate at high frequencies, the following stages all operate at much lower frequencies. Therefore, the maximum operating frequency of those stages should be reduced to lower the DC power consumption.

For the low frequency stages, static dividers are more suited because they can operate down to very low frequencies (MHz range, limited by the on-chip capacitor). In the static divider shown in Fig. 5.2, the current in the ECLs can be reduced to save DC power. The load resistor R_2 should be increased to compensate the drop of output voltage swing due to less current flow through the load resistors. Furthermore, the emitter followers (Q_4), which consume quite high current, can be omitted, as shown in Fig. 5.12 (a). The output EF buffer (in the dashed box) is only needed at the last output stage. By these means, the DC current is reduced from 23.7 mA to 5 mA for the inter-stage divider (without EF) and 9.7 mA for the last-stage divider (with EF). The inter-stage dividers can operate up to 16 GHz, while the output stage can divide from 40 MHz to 10 GHz. Fig. 5.12 (b) shows the measured input sensitivity curve of the last output stage.

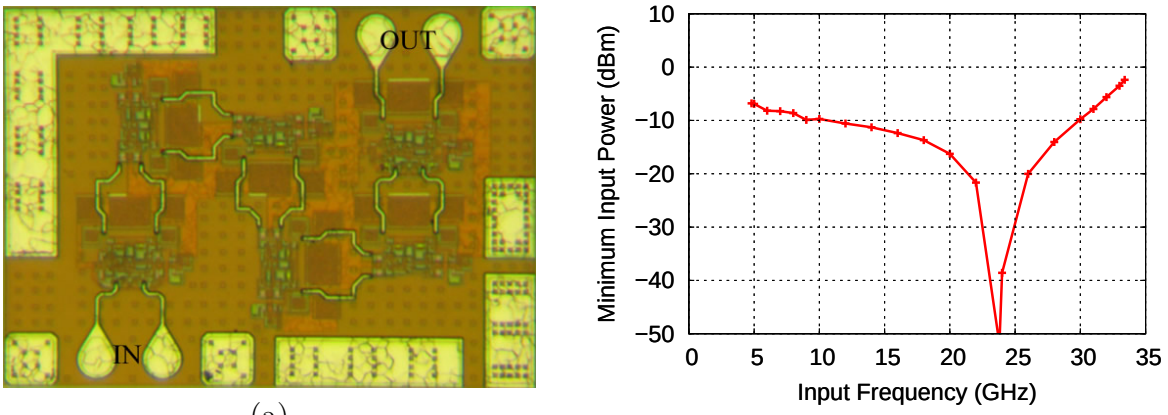
To test the performance of the inter-stage divider and output-stage divider, an all static, divide-by-64 frequency divider was realized, as shown in Fig. 5.13 (a). The high-speed divider (described in Section 5.1) is used as the first stage, followed by four inter-stage dividers and one output stage. The total DC power consumption is 200 mW (4 V, 50 mA). The measured input sensitivity is shown in Fig. 5.13 (b). It can divide from 5 GHz to



(a) (b)

Figure 5.12: (a) Schematic of the static frequency dividers for lower operating frequency. (b) Measured input sensitivity curve of the last output stage.

33 GHz with -1 dBm output power, which proves that the inter-stages and output stage operate quite well. The required input power is below -10 dBm from 10 GHz to 30 GHz.



(a) (b)

Figure 5.13: (a) Chip photo of the all static, divide-by-64 frequency divider. Chip size is 0.8 $\times$0.58 mm^2. (b) Measured input sensitivity curve of the divide-by-64 divider.

For higher operating frequencies, dynamic dividers are used for the first one or two stages. Fig. 5.14 shows the block diagram and chip photo of a divide-by-32 divider, designed for high operating frequency.

To achieve the highest operating frequency, the dynamic divider with "LO" as input (divider I), which operates up to 67 GHz, is used as the first stage. The dynamic divider with "RF" as input (divider III), which needs less input power, is used as the second stage. The following three stages consists of two inter-stage static dividers and one output stage. The total DC power consumption is 304 mW (76 mA, 4 V). Fig. 5.15 (a) shows the measured input sensitivity and output power of this divider.

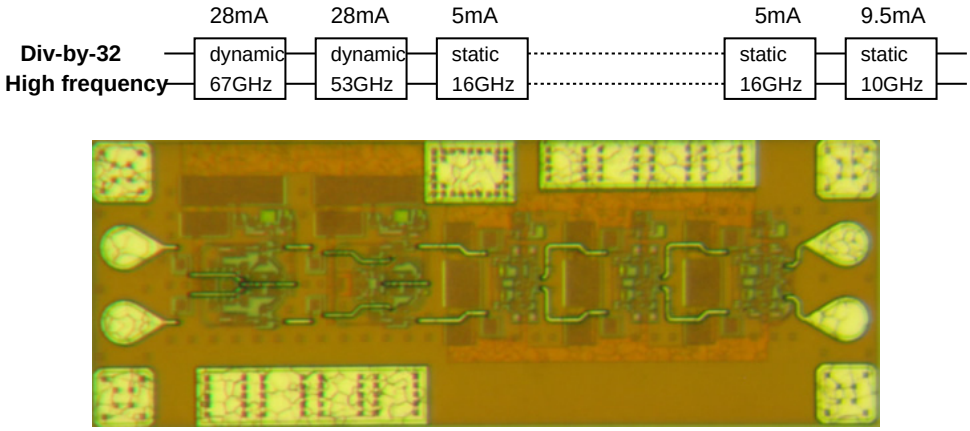


Figure 5.14: Block diagram and chip photo of the divide-by-32 frequency divider. The chip size is 1.04 ×0.38 mm^2.

It can operate from 30 GHz[6] to 60 GHz. The lowest operating frequency is limited by the second dynamic divider, which stops dividing at 15 GHz. The highest operating frequency is limited by the second and third stages, because the output power from the second stage is not sufficient to drive the third stage. The measured output spectrum and waveform are shown in Fig. 5.16 (a) and (b).

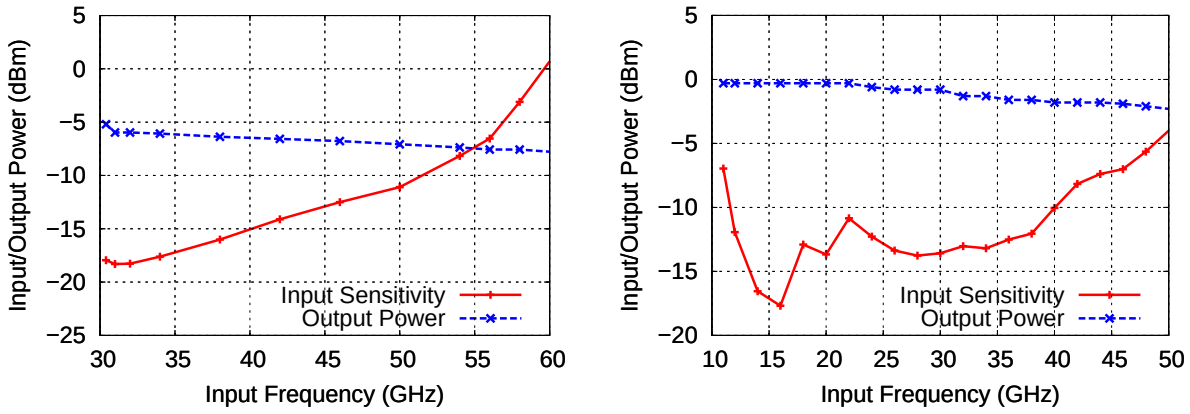
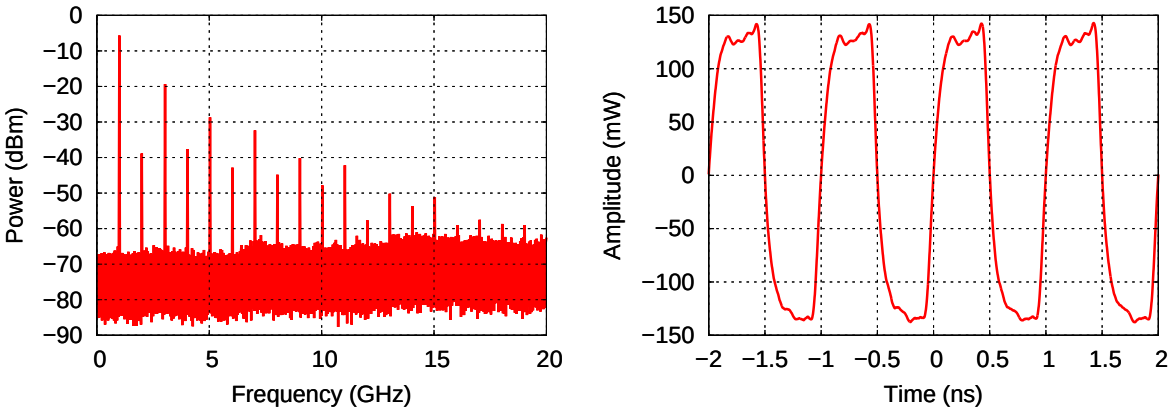


Figure 5.15: Input sensitivity and output power of the divide-by-32 divider. (b) Input sensitivity of the divide-by-128 divider .

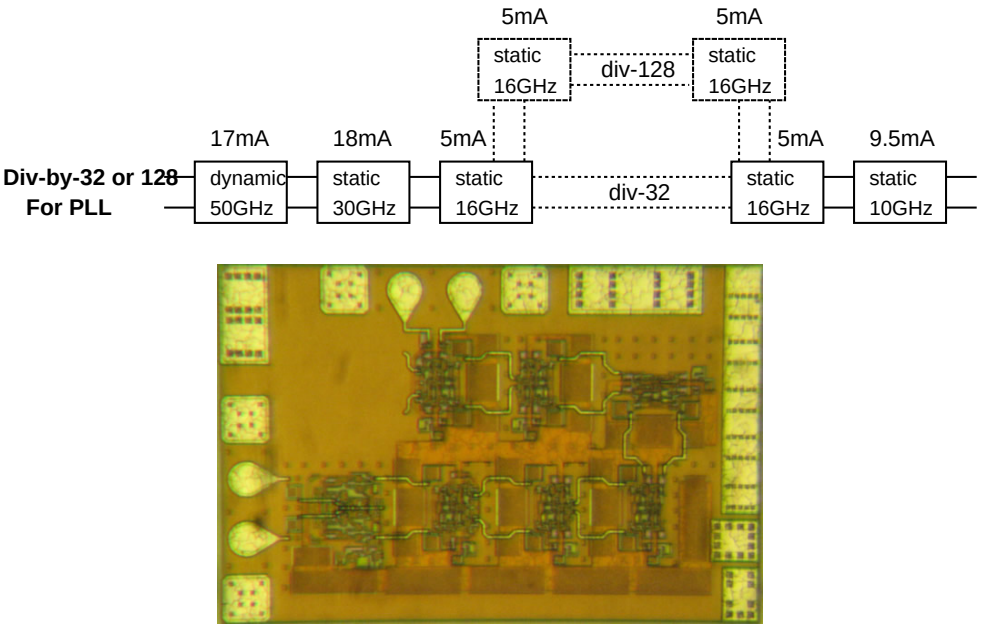
For use in the PLL, the first two stages are replaced with lower-frequency dividers to reduce the power consumption, as shown in Fig. 5.17. The division ratio can be doubled by inserting an inter-stage divider, with only 5 mA more current. Divide-by-128 dividers have also been realized for use in the PLL. Fig. 5.15 (b) shows the measured input sensitivity of the divide-by-128 divider. The operating frequency is from 11 GHz to 50 GHz, which covers the complete frequency tuning range of the VCO. The total DC power consumption is 260 mW (65 mA, 4 V).

[6]The measurement was stopped at 29 GHz, where the required input power is already above 0 dBm.



(a) (b)

Figure 5.16: (a) Output spectrum of the divide-by-32 divider with 32 GHz input. (b) Output wave form of the divide-by-32 divider with 32 GHz input.



(b)

Figure 5.17: Block diagram and chip photo of the divide-by-128 frequency divider for use in the PLL. The chip size is 0.9 ×0.6 mm^2.

5.4 Summary and Comparison

Static and dynamic frequency dividers are described in this chapter. The maximum operating frequency of static and dynamic dividers are analyzed and design guidelines for achieving higher operating frequency are discussed. Dynamic dividers with different configuration are analyzed and compared. The static dividers operate up to 34 GHz (42% of f_T) and the dynamic dividers operate up to 67 GHz (83% of f_T). The relative speed (with respect to f_T) is comparable to the state of art results [41, 50]. Multi-stage dividers with different division ratios have been realized with wide operating frequency range and low power consumption. The dividers achieve much higher operating frequency with much less power consumption than the previously reported designs using the same technology [45].

Chapter 6

Phase Locked Loop

The Phase Locked Loop (PLL) is an essential building block of the receiver. It stabilizes the free running VCO and suppresses the in-band phase noise by synchronizing the phase of the free running VCO with the phase of a stable reference signal. Analog PLLs have been realized in this thesis work. The loop component design, loop simulation and PLL IC characterization are described in detail in this chapter.

6.1 Loop Design

In modern communication systems, the most commonly used PLLs are digital PLL and analog PLL (linear PLL). The digital PLL is based on phase-frequency detector (PFD) and charge pump (CP). It can have a very wide locking range[1], but the operating frequency of the PFD is usually low, due to the delay in the Flip-Flops and power consumption limitation, which then requires higher frequency division ratio, especially for millimeter-wave PLLs. The analog PLL is based on analog phase detector (PD) and active loop filter (LF). Therefore, it can operate at very high frequencies, but usually has limited locking range, depending on the loop filter and loop bandwidth. In this thesis work, realizing a digital PLL is not possible due to the lack of high speed p-type devices, so an analog PLL has been realized for use in the receiver. The main design goal is to achieve wide locking range and low phase noise.

Fig. 6.1 shows a block diagram of the PLL. The phase detector detects the phase difference between the reference input and the frequency-divided VCO signal, and produces a control signal, which, after passing the loop filter, controls the VCO in a way that the phase of the frequency-divided VCO signal follows the phase of the reference signal. The frequency divider decreases the input frequency from the VCO, so that the PD can operate at lower frequencies. The division ratio N is an important design parameter. Small division ratio is preferred for better phase noise, because the phase noise of the reference signal will

[1]Locking range is the frequency range, in which the PLL can lock to the reference from any initial state. Definition of PLL locking range can be found in literature [52].

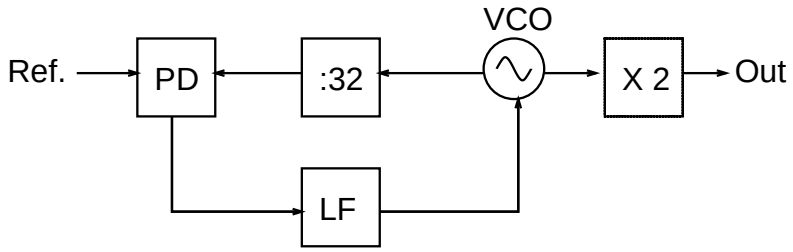


Figure 6.1: Block diagram of the analog PLL.

be raised by $20 \cdot log(N)$, as will be shown in Section 6.2 (page 61). On the other hand, a large division ratio can bring the reference signal down to very low frequencies (MHz range), where a variety of stable signal sources (crystal oscillators, synthesizers, etc.) are available. In this thesis work, PLLs with two different division ratios (/32 and /128) have been realized for comparison.

The VCO, frequency doubler and frequency divider have been described in Chapter 4 and 5. Divide-by-32 and divide-by-128 dividers with reduced power consumption are used in the PLL. The phase detector is a Gilbert cell mixer with resistive load. Compared to the phase-frequency detector used in the digital PLL, the Gilbert cell phase detector can operate at much higher frequencies, enabling lower frequency division ratio in the PLL, and therefore better phase noise. The simplified schematic of the phase detector is shown in Fig. 6.2.

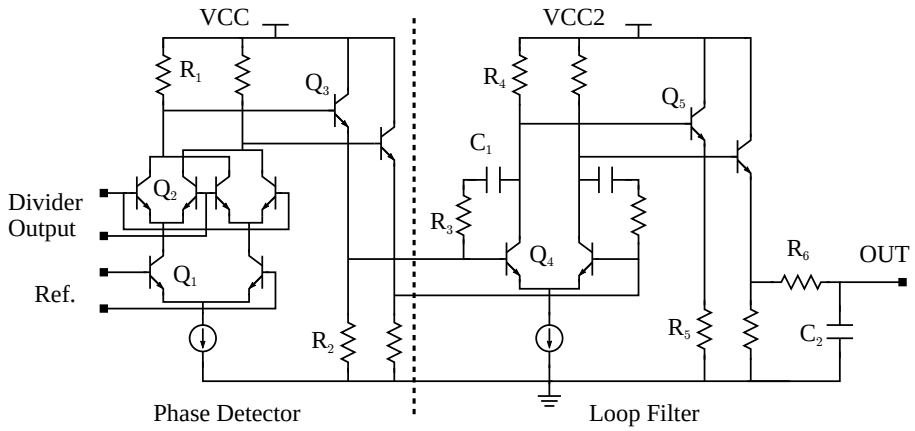


Figure 6.2: Simplified schematic of the phase detector and active loop filter.

The emitter-follower (Q_3) provides the DC level shift so that the phase detector can drive the following loop filter directly. The divider output is connected to the switching quad of the mixer core and the reference signal is connected to the trans-conductance stage.

When the two input signals are different in frequency (at the initial phase of the locking process), the PD operates as a mixer and generates a low frequency signal, which tunes the VCO frequency towards the reference frequency. When the two input signals have the same frequency but differ in phase (by $\Delta\phi$), a DC voltage shift (ΔV) is produced at the output, fixing the VCO frequency at the reference frequency (multiplied by the division

ratio N). Fig. 6.3 shows the simulated output voltage of the phase detector versus the input phase error.

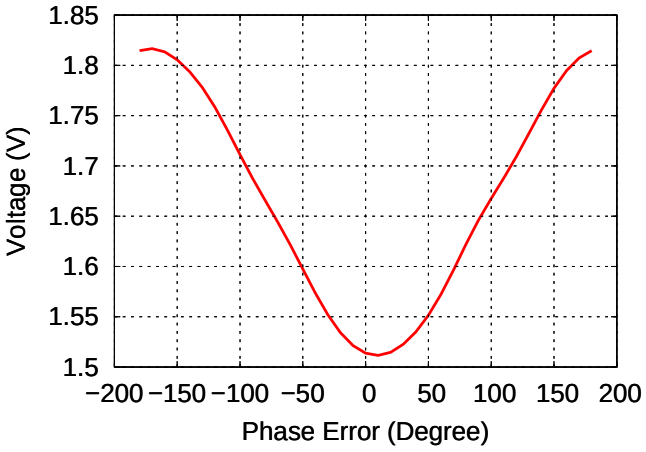


Figure 6.3: Output voltage of the phase detector versus input phase error. The input signal power is -3 dBm at the switching quad and -15 dBm at the trans-conductance stage.

The gain of the phase detector (K_D), defined as $\Delta V/\Delta\phi$, is mainly determined by the load resistor (R_1) and the reference signal power. As will be shown in Section 6.2 (page 61), K_D influences the PLL loop gain and noise contribution from the phase detector, thus needs to be chosen carefully. In the current design, the load resistor is 550 Ω and the phase detector gain is about 0.1 (with -15 dBm reference signal power).

In addition to the DC voltage shift, the output of the phase detector also contains AC signals, which are mixing products of the two input signals. These AC signals will modulate the VCO and generate spurs (reference spurs) around the locked signal, and must be sufficiently suppressed. The suppression of the AC signals on the tuning node (and hence the spur signals at the PLL output) is determined by the loop filter attenuation at the spur frequencies (harmonics of the reference frequency), which can be controlled by the loop filter bandwidth. To have high spur suppression, a small bandwidth (low cut-off frequency) is preferred. However, a small loop filter bandwidth directly leads to small loop bandwidth, and hence small frequency locking range and longer settling time of the PLL, so a compromise between spur suppression and locking range must be considered when choosing the filter bandwidth. In this thesis work, a relatively wide bandwidth was chosen, because wide locking range is the main design goal and the reference spurs are less critical since they are far from the locked signal.

The loop filter is also shown in Fig. 6.2. It is a simple design based on a feedback amplifier and passive RC filter with emitter-follower in between for DC level shift. The bandwidth is mainly determined by the feedback (R_3, C_1) and the RC filter (R_6, C_2, C_{VAR}). Fig. 6.4 shows the simulated AC power gain of the filter. It has 31 dB gain and a 3-dB bandwidth of 60 MHz. For PLL with division ratio of 128, the filter bandwidth is decreased to 20 MHz, by adding a second RC filter at the output node and a shunt capacitor at the input of Q_5. The simulated gain of this filter is also shown in Fig. 6.4.

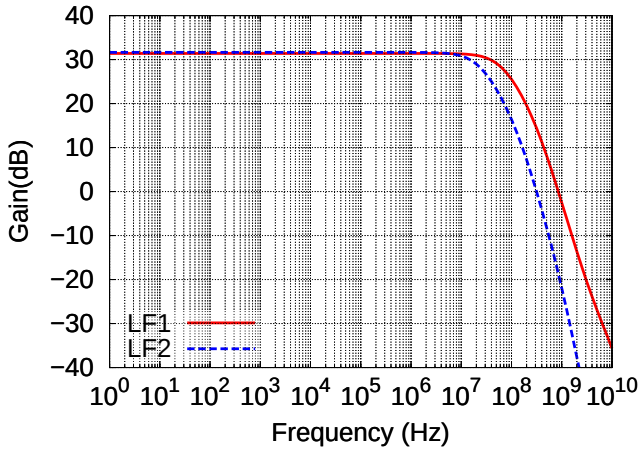


Figure 6.4: Simulated AC gain of the loop filter. "LF1" is for division ratio of 32 and "LF2" is for division ratio of 128.

The VCO tuning characteristic was shown in Fig. 4.8 (page 31). A frequency tuning from 28 GHz to 38 GHz corresponds to a voltage tuning from 0.6 V to 6 V. In order to have a wide PLL locking range, the loop filter output must be able to cover a wide voltage range. Since the output voltage swing of the phase detector is very small (0.13 V peak-to-peak, at 30 MHz), the loop filter must provide sufficient gain to have a large output voltage swing. This also increases the gain of the PD and helps to suppress the noise contribution from the PD and LF, as will be shown in Section 6.2 (page 61).

The gain of the loop filter can be easily adjusted by changing the load resistor (R_4) and biasing current. With a load of 2.5 kΩ, the loop filter has 25 dB gain and 2.3 V (peak-to-peak) output voltage swing, which guarantees that the output voltage swing does not limit the locking range[1]. Because of the high voltage swing, the non-SIC transistors (with 4.5 V BV_{CEO}) are used in the loop filter design. The circuit parameters of the phase detector and loop filters can be found in Appendix C.4 (Fig. C.6, page 116).

The locking range of the PLL is limited by the loop bandwidth and covers only a part of the VCO tuning range (about 3 GHz around the free-running frequency). Therefore, the usable frequency range of the VCO is strongly limited, although it has a very wide tuning range. To overcome this, the locking range can be shifted by tuning the supply voltage of the loop filter ($VCC2$). The biasing current of the filter is fixed, so changing the supply voltage only shifts the DC voltage level at the output node. As a result, the free-running frequency of the VCO, and hence the locking range can be shifted, while the loop response remains the same. By adjusting $VCC2$ from 2 V to 6 V, the locking range covers almost the whole tuning range of the VCO, as will be shown in Section 6.3 (page 67).

[1]The 2.3 V voltage swing allows 4 GHz tuning range, which is wider than the locking range determined by the loop bandwidth.

6.2 Loop Simulation

In order to predict the PLL performance and hence optimize the loop design, different simulations have been performed. The loop bandwidth and in-band phase noise are simulated in the frequency domain, based on linear PLL models. The transient behavior (locking time) and output spectrum are simulated in the time domain, based on behavior models and real circuit models. The simulation details are shown in the next subsection.

6.2.1 Loop Gain Simulation

In the locked state, the PLL can be modeled by a linear model in the frequency domain, as shown in Fig. 6.5, where K_D, K_V, $F(S)$ and N are phase detector gain, VCO gain, loop filter transfer function and frequency division ratio, respectively.

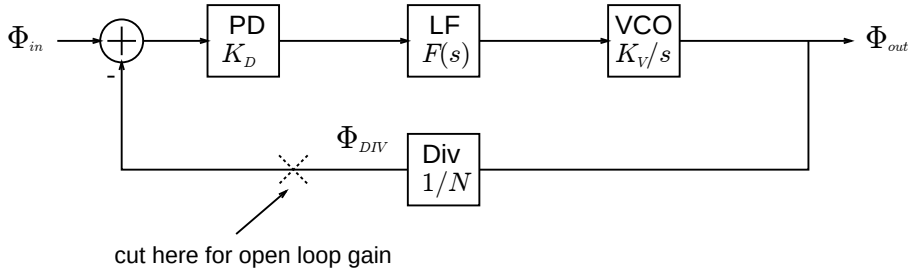


Figure 6.5: Linear model of the PLL in frequency domain.

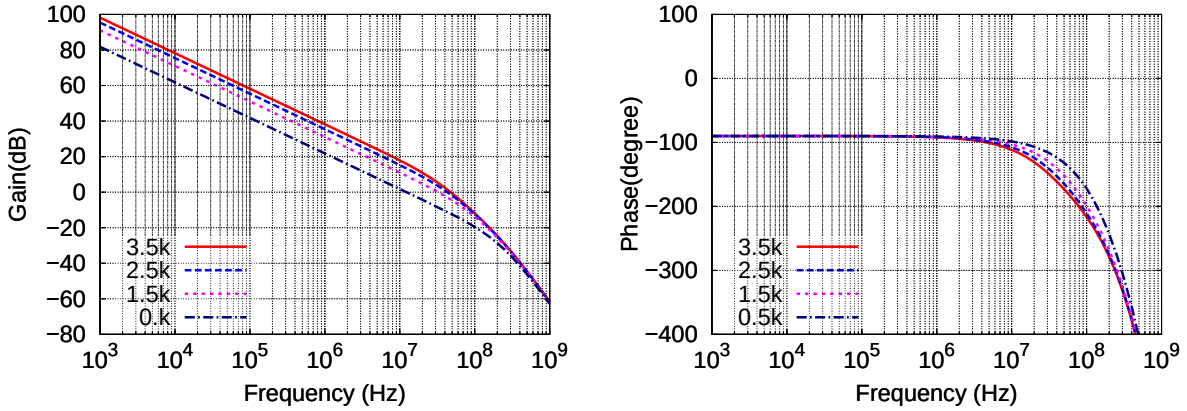
For the PLL design, the two most important parameters are the open- and closed-loop gain. To simulate the loop gains, the phase detector, VCO and frequency divider are replaced with ideal behavioral models. Due to the difficulty to extract the behavior model of the loop filter, the complete circuit model of the loop filter is use in the simulation. The simulation is performed in ADS, using AC simulation. By feeding an input signal at the input, signals at different nodes can be calculated.

The open-loop gain determines the loop bandwidth and stability. It is defined as

$$\frac{\Phi_{DIV}}{\Phi_{in}} = \frac{K_D \cdot F(s) \cdot K_V}{N \cdot s} \tag{6.1}$$

which is the product of the transfer functions of all the loop components, and can be calculated by cutting the loop after the frequency divider, as shown in Fig. 6.5. The PLL loop bandwidth is defined as the frequency where the magnitude of the open-loop gain drops to one and the stability of the PLL is usually defined by the phase margin, which is the phase difference between 180 degree and the phase of the open-loop gain at the frequency where the magnitude of the open-loop gain equals one. According to the control theory, the loop oscillates when the magnitude of the open-loop gain equals one and at the same time, the phase equals 180 degree (zero phase margin), which should be avoided in the PLL design. A small phase margin will lead to a peak in the closed-loop gain

at frequencies close to the loop bandwidth. In this PLL design, the phase margin can be well controlled by tuning the load resistor in the loop filter (R_4 in Fig. 6.2). Fig. 6.6 shows the simulated magnitude and phase of the open-loop gain for different load resistors. As the load resistor decreases, the phase margin increases and the loop becomes more stable. However, as R_4 decreases, the loop bandwidth also decreases, reducing the locking range of the PLL. In the current design, 2.5 kΩ is used, which gives a good compromise between loop bandwidth and stability. The simulated closed-loop gain for different load resistors is shown in Fig. 6.7 (a).



(a) (b)

Figure 6.6: Simulated magnitude (a) and phase (b) of the open-loop gain, with different load resistors in the loop filter (R_4 in Fig. 6.2).

The close-loop gain (also called the transfer function) can be calculated as

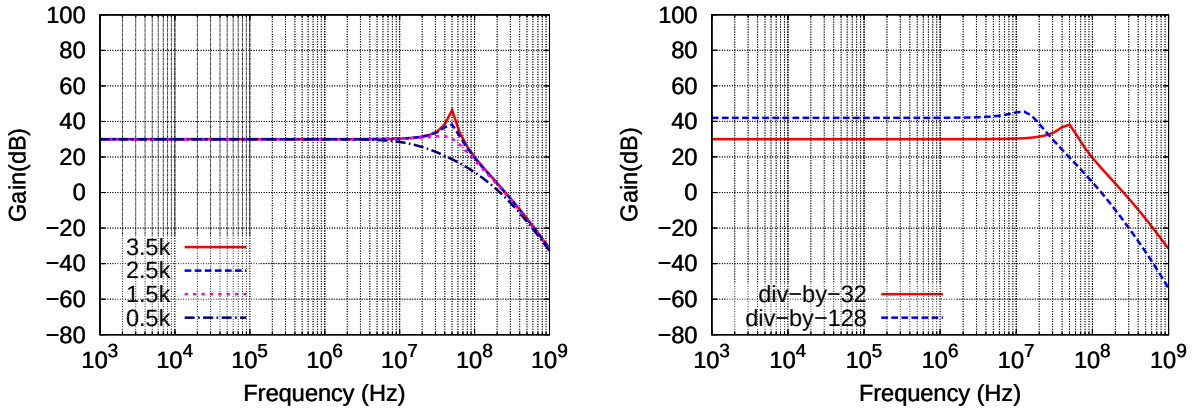
$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{N \cdot K_D \cdot F(s) \cdot K_V}{N \cdot S + K_D \cdot F(s) \cdot K_V} \tag{6.2}$$

which defines the phase relation between the input and output. The performance of the PLL (locking range, spur suppression, etc.) is mainly determined by the closed-loop gain. Fig. 6.7 (b) shows the simulated closed-loop gain of the two PLLs with different frequency division ratios.

The 3-dB loop bandwidth is about 70 MHz for the divide-by-32 PLL and 20 MHz for the divide-by-128 PLL. Within the loop bandwidth, Φ_{out} equals $N \cdot \Phi_{in}$ (in linear scale), which means that the output phase of the VCO follows the input phase with a multiplication factor of N (due to frequency division). Outside of the loop bandwidth, the close-loop gain drops, meaning that the PLL starts to loose control of the VCO and the output phase of the VCO does not follow the input phase anymore.

6.2.2 Noise Simulation

Phase noise is also an important characteristic of a PLL. Ideally, the output phase noise should be the same as the phase noise of the reference signal plus $20 \cdot log(N)$, as indicated in



(a) (b)

Figure 6.7: (a) Simulated closed-loop gain, with different load resistors in the loop filter (R_4 in Fig. 6.2). (b) Simulated closed-loop gain of the two PLLs with frequency division ratio of 32 and 128.

the closed-loop gain simulation. However, the other loop components also have individual noises, which contribute to the final output phase noise. The noise from each component is added to the loop, as shown in Fig. 6.8.

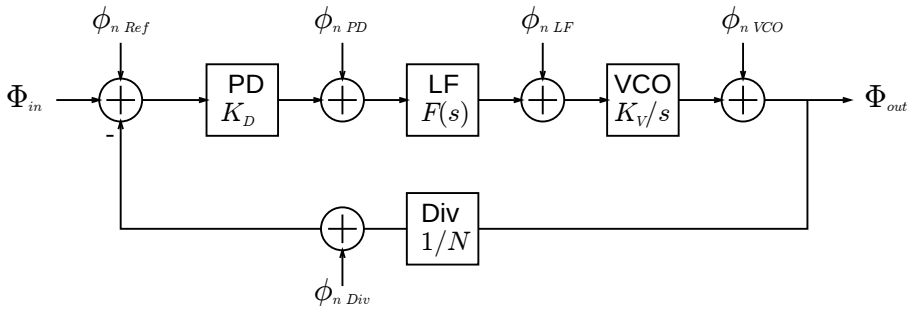


Figure 6.8: Linear model of the PLL, including noise.

Each noise component has its own transfer function, as shown in Tab. 6.1, where $H(s)$ is the closed-loop gain, defined as

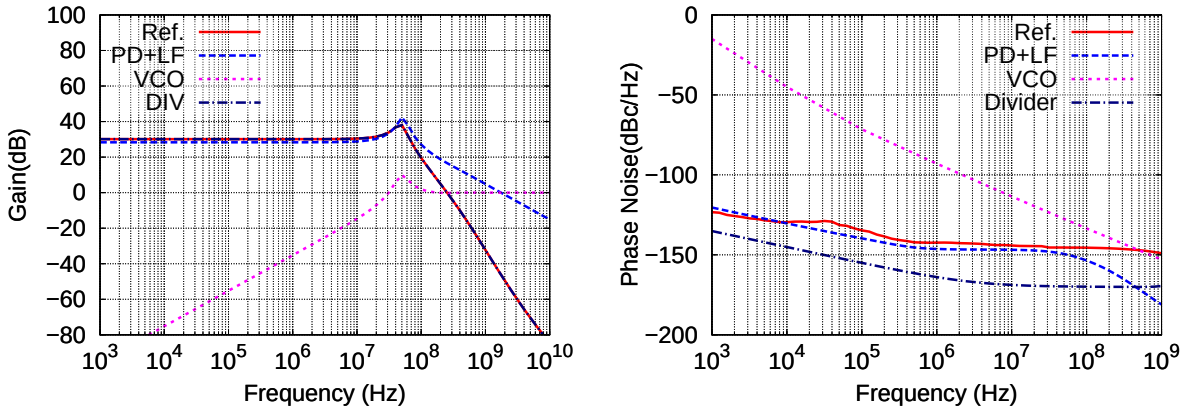
$$H(s) = \frac{\Phi_{out}}{\Phi_{in}} = \frac{N \cdot K_D \cdot F(s) \cdot K_V}{N{\cdot}S + K_D \cdot F(s) \cdot K_V} \tag{6.3}$$

The simulated transfer functions of different loop components are shown in Fig. 6.9 (a) (for the divide-by-32 PLL). The reference signal and the frequency divider has the same transfer function of $H(s)$. Within the loop bandwidth, the magnitude of the transfer function is 30 dB ($20{\cdot}log(32)$), which indicates that the noise of the reference signal and frequency divider is raised by 30 dB, due to frequency division. From this aspect, low frequency division ratio is preferred for lower phase noise. The transfer function of the PD and LF is $H(s)$ divided by K_D and $K_D{\cdot}F(s)$. Therefore, to minimize the noise contribution from the PD and LF, K_D and $F(s)$ should be large. In this design, the noise

Table 6.1: Transfer function of each loop component

Loop Component	**Transfer Function**
Reference	$H(s)$
PD	$\frac{H(s)}{K_D}$
LF	$\frac{H(s)}{K_D \cdot F(s)}$
VCO	$\frac{s \cdot H(s)}{K_D \cdot F(s) \cdot K_V}$
Divider	$H(s)$

of the PD and LF are combined and added at the output of the LF[1]. $K_D \cdot F(s)$ is about 3 within the bandwidth, so the in-band magnitude of the transfer function of PD and LF is about 6 dB lower than $H(s)$. The transfer function of the VCO is a high pass filter, indicating that the noise of the VCO is highly suppressed within the loop bandwidth.



(a) (b)

Figure 6.9: (a) Simulated magnitude of the transfer functions of the loop components. (b) Simulated and measured phase noise contributions of the loop components.

In the locked state, the PLL can be modeled as a linear system, where the total output noise is the sum of each noise component multiplying with its own transfer function, as shown in Equation 6.4.

$$\phi_{total} = (\phi_{nRef} + \phi_{nDiv}) \cdot H(s) + \frac{\phi_{nPD} \cdot H(s)}{K_D} + \frac{\phi_{nLF} \cdot H(s)}{K_D \cdot F(s)} + \frac{\phi_{nVCO} \cdot s \cdot H(s)}{K_D \cdot F(s) \cdot K_V} \tag{6.4}$$

In order to achieve the lowest possible phase noise, the noise from other loop components should be lower than the reference noise. To check this, the phase noise of the PLL and

[1]The noise of the PD is not amplified with the same gain as the differential output signal of the PD, so the PD and LF are treated as one circuit in noise simulation, as shown in Fig. 6.2.

the contributions from the loop components has been simulated using AC simulation. The noise is represented by rms noise voltage at each frequency[2]. The simulated noise data of the phase detector, loop filter, frequency divider and the measured noise data of the VCO, reference signal, as shown in Fig. 6.9 (b), are used in the simulation.

The simulated total phase noise for the two PLLs with different frequency division ratio is shown in Fig. 6.10. The contributions from the loop components are also plotted. For both PLLs, the in-band phase noise is mainly dominated by the reference signal, followed by the phase detector and loop filter. The divider phase noise is much lower and has almost no influence on the output phase noise. Because of the higher frequency division ratio, the simulated phase noise of the second PLL is about 12 dB higher.

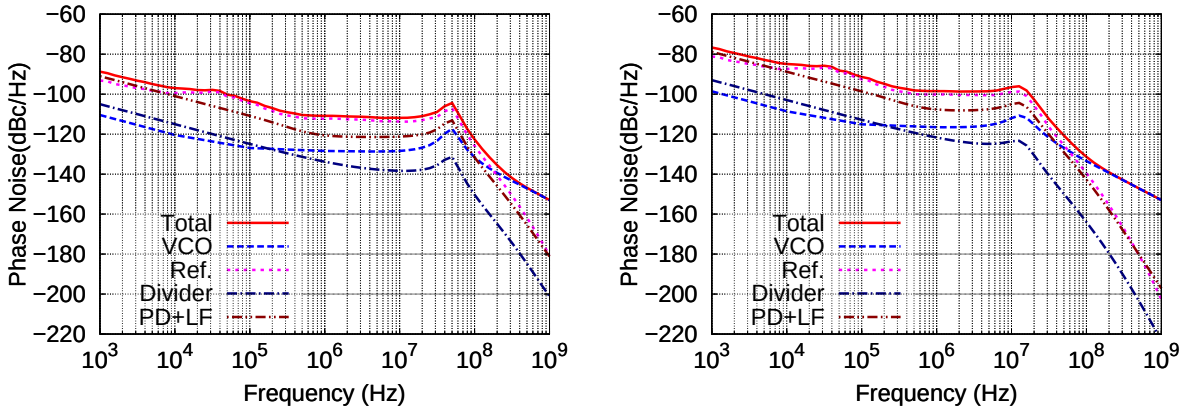


Figure 6.10: Simulated total phase noise and the contribution from the loop components for the two PLLs with division ratio of 32 (a) and 128 (b).

6.2.3 Transient Simulation

The lock-in process of the PLL is a non-linear, dynamic behavior, which cannot be modeled using the linear model in Fig. 6.5. Therefore, transient simulation was performed to check the time domain response of the PLL. Fig. 6.11 shows the simulation setup.

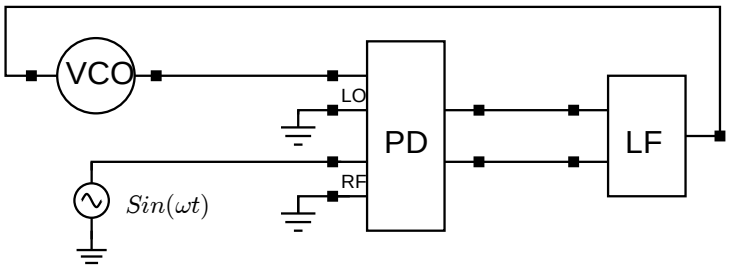


Figure 6.11: Transient simulation with ideal VCO.

[2]In simulation, the phase noise is calculated as $10 \cdot log(\frac{V^2}{2})$, where V is the rms noise voltage.

For shorter simulation time, the frequency dividers are not included and an ideal VCO is used in the simulation. The gain and frequency of the VCO is defined according to the measured characteristics of the VCO (after frequency division). An ideal signal source is used as the reference signal. Both the VCO and signal source have single-ended output, so the phase detector is fed single-endly with the second "LO" and "RF" input connected to ground. The VCO free running frequency is set to 1.05 GHz and 263 MHz, for division ratio of 32 and 128. The reference frequency is set to 1.1 GHz and 275 MHz, respectively.

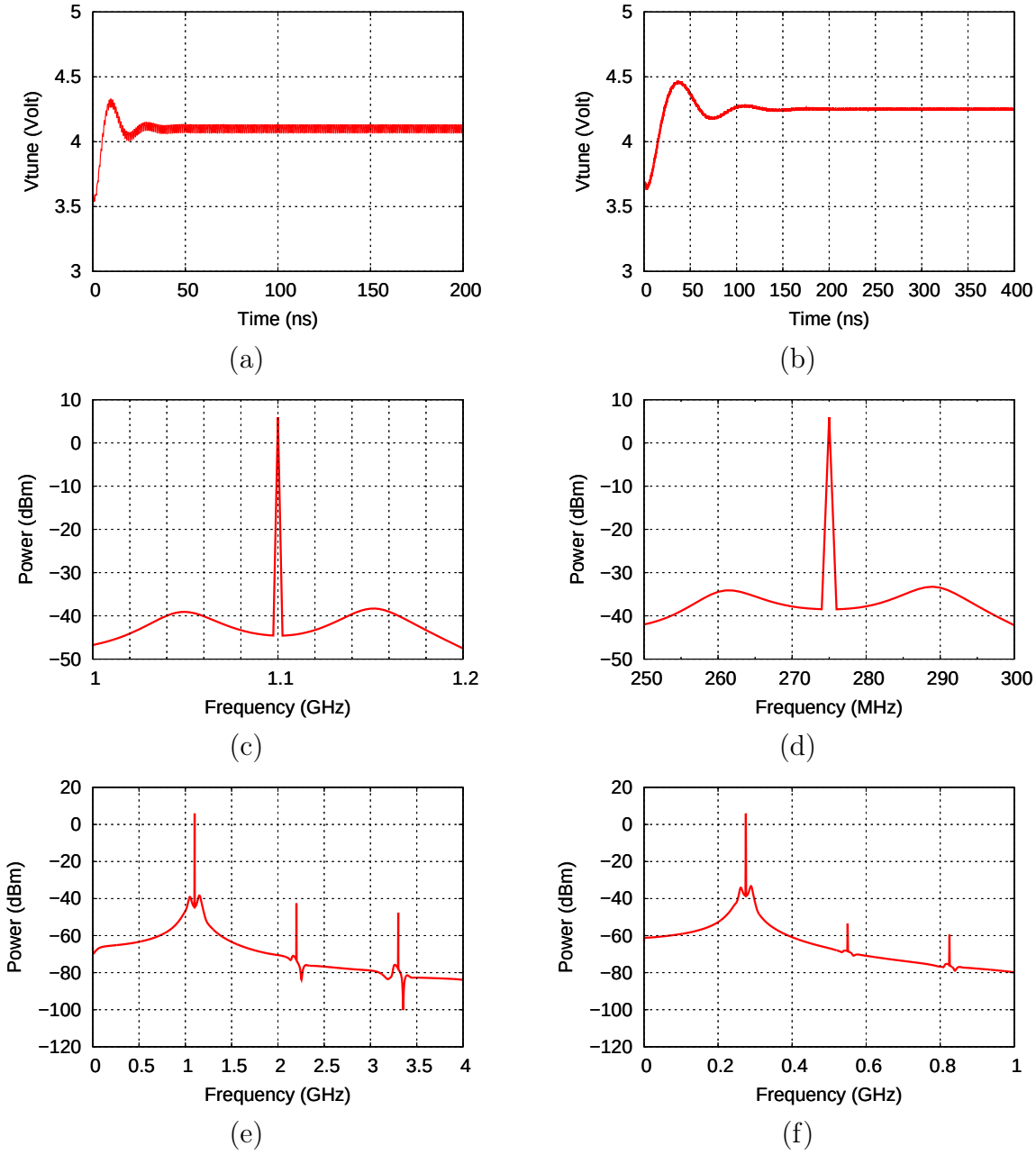


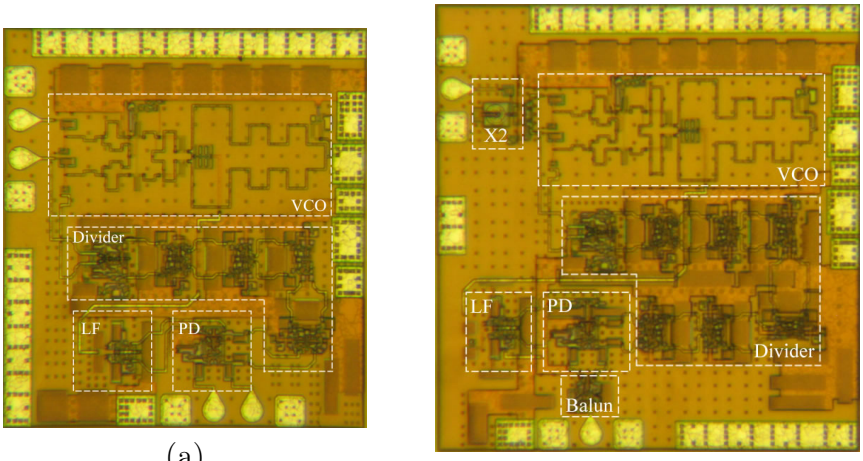
Figure 6.12: Simulated tuning voltage and spectrum of the PLL with division ratio of 32 ((a), (c), (e)) and 128 ((b), (d), (f)).

The simulated tuning voltage of the VCO is shown in Fig. 6.12 (a), (b). The VCO is locked to the reference signal after 50 ns (/32) and 200 ns (/128). Due to the narrower

loop bandwidth, the locking time of the PLL with division ratio of 128 is much longer. By doing Fast Fourier Transform, the output spectrum can be displayed. Fig. 6.12 (c), (d) shows the calculated spectrum. The spectrum agrees well with the loop gain simulation in Fig. 6.7 (a). The reference spurs, which are highly suppressed by the loop filter, are also visible, as shown in Fig. 6.7 (e), (f).

6.3 Measurement Results

Two different VCOs have been integrated with PLLs for different frequency ranges (VCO1, Fig. 4.8 on page 31 and VCO2, Fig. 4.11 on page 32). For each VCO, four versions are realized for characterization (with and without frequency doubler, division ratio of 32 and 128). For the PLL with division ratio of 128, an active balun is added at the reference input. Fig. 6.13 shows two realized PLL ICs. Both ICs are very compact and occupy only 0.95 mm^2 and 1.31 mm^2 chip area, respectively.



(a) (b)

Figure 6.13: (a) PLL with VCO2 (Fig. 4.11 on page 32) and divide-by-32 divider. Chip size is 0.95 ×1 mm^2. (b) PLL with VCO1 (Fig. 4.8 on page 31), doubler and divide-by-128 divider. Chip size is 1.12 ×1.17 mm^2.

The ICs were characterized on-wafer. For simplicity reason, the reference signal was generated by a signal generator (Agilent 8254A). The fundamental output was directly connected to the spectrum analyzer (Agilent 8563E, up to 50 GHz) via a "GSSG" probe, while the frequency-doubled output was connected via a "GSG" probe to a V-band harmonic mixer, which extends the frequency range of the spectrum analyzer. The DC power consumption for the different configurations are 320 mW (VCO, /32), 352 mW (VCO, /128), 380 mW (VCO, doubler, /32) and 401 mW (VCO, doubler, /128), respectively.

Fig. 6.14 shows the measured output spectrum. The reference is at 1 GHz for division ratio of 32 and 250 MHz for division ratio of 128, with -15 dBm power. The output is at 32 GHz. For all version of PLLs, clean locked signals were observed. The suppression of the reference spur is about 35 dB for division ratio of 32 and 45 dB for division ratio

of 128, which is quite sufficient for the intended applications. The frequency doubled spectrum is also shown in Fig. 6.14 (e) and (f) [3].

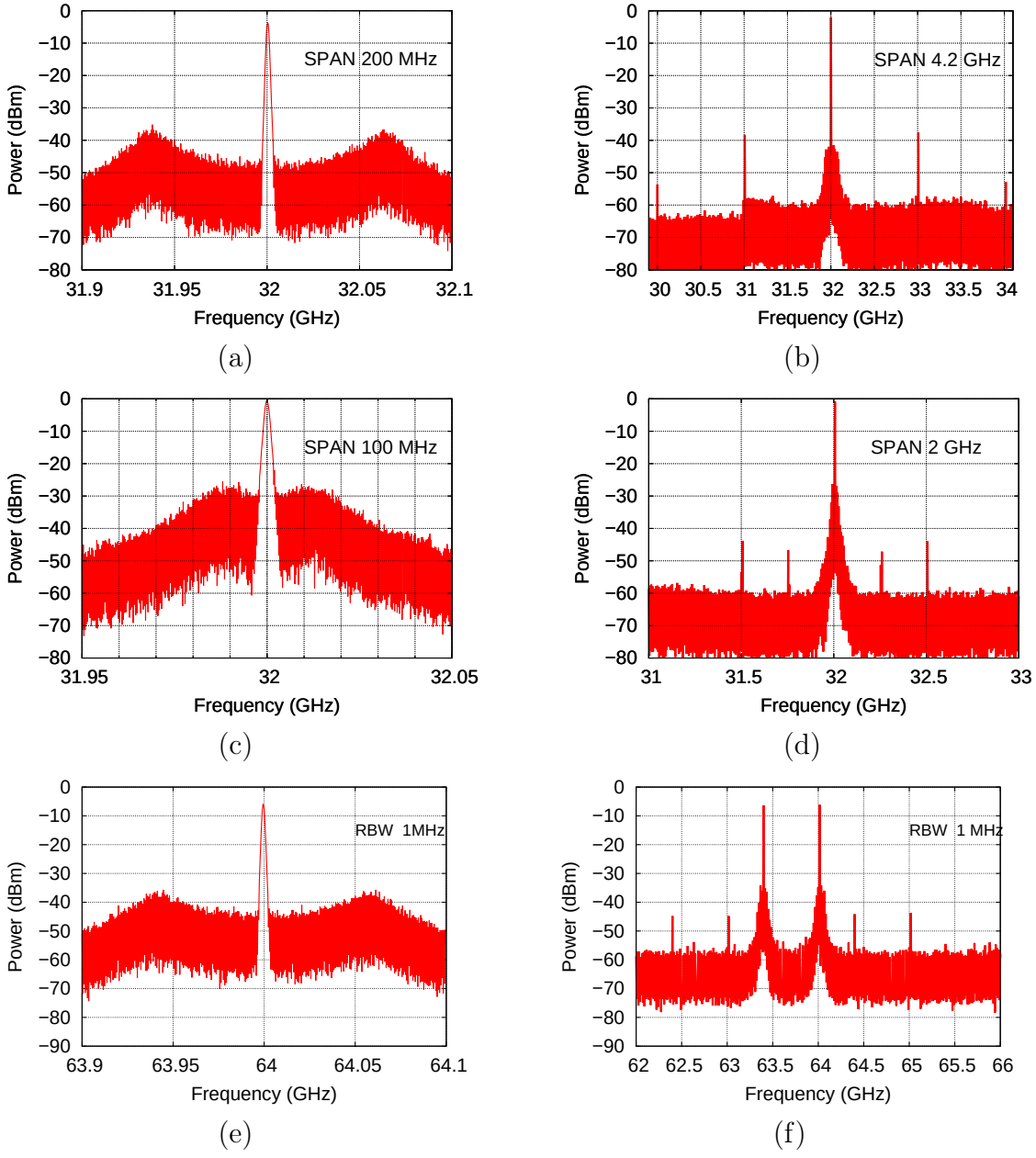


Figure 6.14: Measured output spectrum of the PLLs (at 32 GHz) with division ratio of 32 (a), (b) and 128 (c), (d). Output spectrum at 64 GHz (e), (f). The spectrum at 79.4 GHz is an artifact of the harmonic mixer.

The phase noise has been measured at both the fundamental and frequency-doubled

[3]The spectrum at 63.4 GHz in Fig. 6.14 (f) is due to the harmonic mixer (Agilent 11970V) that is used in the measurement. The IF output of a harmonic mixer contains many mixer products (frequencies of LO±source, 2LO±source, 3LO±source...nLO±source). As a result, within a single harmonic band, a single input signal can produce many responses, only one of which is valid. These responses come in pairs, where the members of the valid pair are spaced 621.4 MHz apart and the right-most member for the pair is the correct response (for this analyzer, the left member of a pair is not valid).

output. Fig. 6.15 shows the measured phase noise at 32 GHz and 64 GHz. At 32 GHz, the measured phase noise at 1 MHz offset is -112 dBc/Hz for division ratio of 32 and -99 dBc/Hz for division ratio of 128. The phase noise of the frequency-doubled output is 6 dB higher. For comparison, the simulated phase noise of the fundamental output is also shown. The measured phase noise agrees very well with the simulation results.

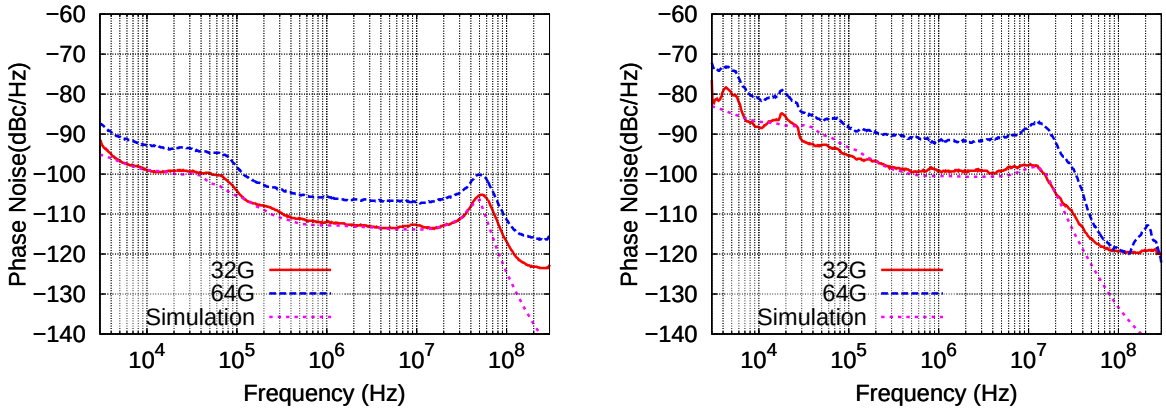


Figure 6.15: Measured phase noise of the fundamental and frequency doubled PLL output and simulated phase noise of the fundamental output. (a) division ratio of 32. (b) division ratio of 128.

In a real wireless system, the reference signal should be generated by low-cost, stable signal sources. At frequencies around 1 GHz range (for the PLL with division ratio of 32), crystal oscillators exist (for instance, a temperature compensated crystal oscillator, TCXO-S1000-LF, from KVG Quartz Crystal Technology GmbH), which can provide better phase noise (< -150 dBc/Hz at 100 kHz and 1 MHz offset) than the signal generator (-145 dBc/Hz at 1 MHz offset). According to the noise simulation (Fig. 6.10, page 65), the phase noise is mainly dominated by the reference signal and there is about 10 dB room for improvement (limited by the PD and LF), which means at least 5 dB lower phase noise can be expected, when the TCXO is used as the reference signal source. At lower frequencies (MHz range, for the PLL with division ratio of 128), many signal sources are available (crystal oscillators, synthesizers, etc.), which can provide similar or better phase noise than the signal generator. With a programmable crystal oscillator (Si 570) as reference signal, the PLL can be used as signal sources for Ka-/V-band applications. Fig. 6.16 shows the measured phase noise at 32 GHz, using the programmable crystal oscillator as reference signal source, which is very close to the performance using the Agilent signal generator as reference signal source.

The locking ranges of the PLLs were measured with different loop filter supply voltages. The measured locking range (after frequency doubling) is shown in Fig. 6.17. With a fixed supply voltage, the locking range is about 6 GHz. However, by switching the loop filter supply voltage, the VCO can be locked over a very wide frequency range (28%), which almost covers the complete tuning range of the VCO. At low and high supply voltages, the gain of the loop filter decreases, reducing the loop bandwidth and locking range. The measured output power of all the PLLs is shown in Fig. 6.18.

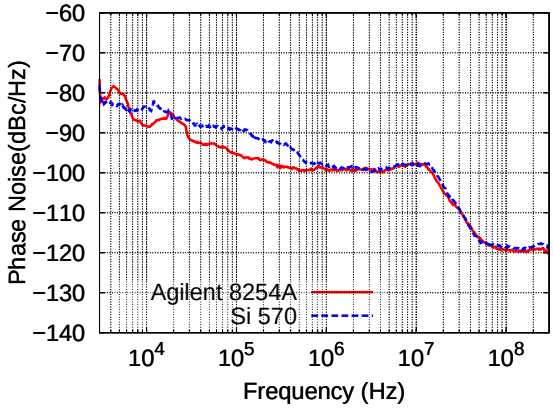
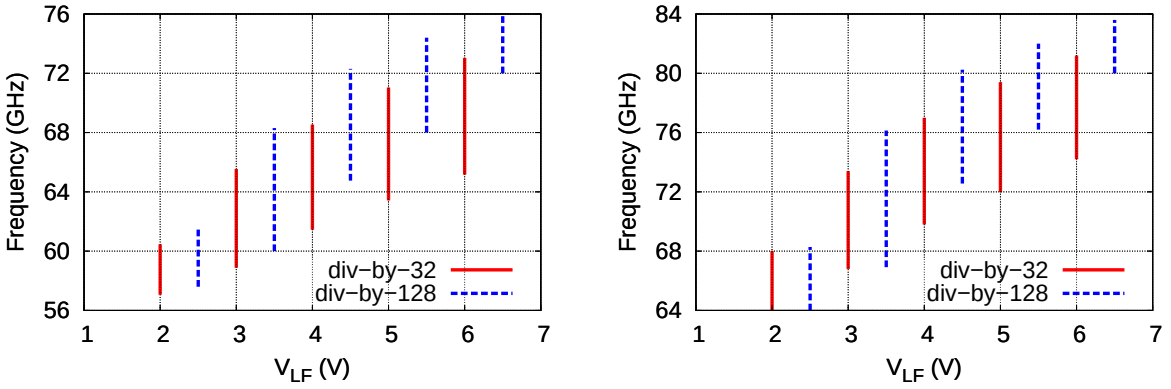


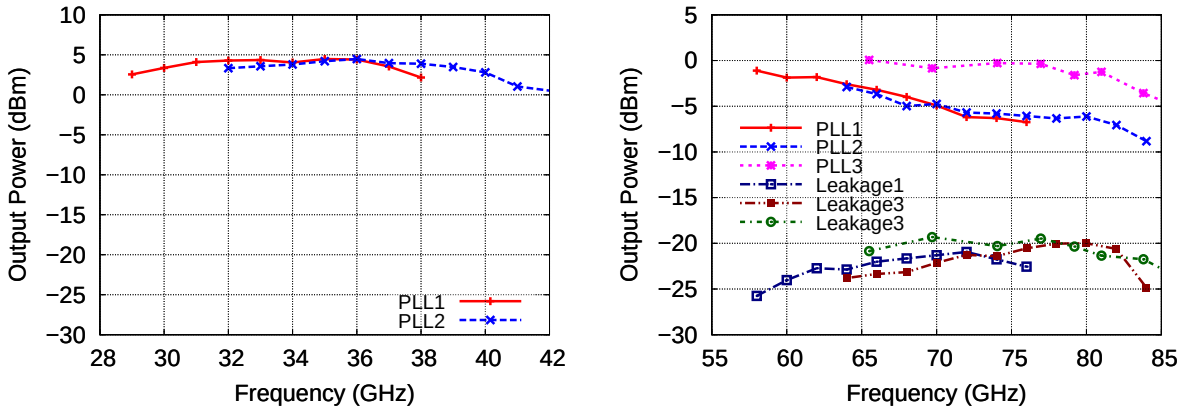
Figure 6.16: Measured phase noise at 32GHz using the Agilent 8254A and Si570 as reference signal sources



(a) (b)

Figure 6.17: Measured locking range with different loop filter supply voltage for two PLLs with VCO1 (a) and VCO2 (b).

The VCO with high output power (Fig. 4.18, page 37) has also be integrated with the PLL. Fig. 6.19 shows a chip photo of the PLL IC. The locking range is from 64.5 GHz to 85 GHz and the output power is above -1.6 dBm up to 81 GHz, as shown in Fig. 6.18 (b) (PLL3). The phase noise is -106 dBc/Hz at 1 MHz offset, similar to the phase noise of other PLLs (Fig. 6.15 (a)). The total DC power consumption is 600 mW (150 mA at 4 V).



(a) (b)

Figure 6.18: Measured output power at different frequency for PLL without (a) and with (b) doubler.

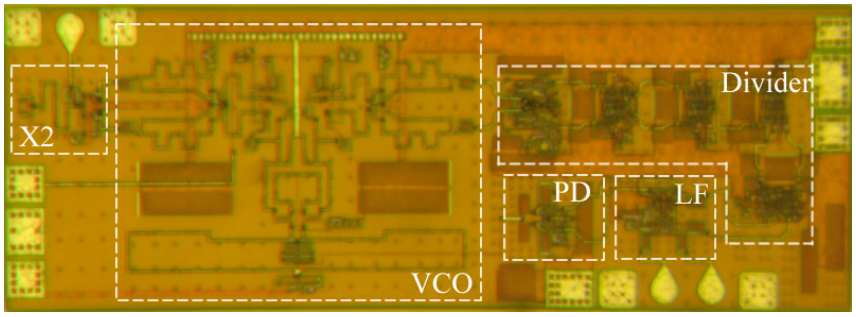


Figure 6.19: PLL with the high power VCO. The size is 1.17 mm^2(1.8 ×0.65 mm^2). DC power consumption 600mW (150mA × 4V.)

6.4 Summary and Comparison

Design, simulation and characterization of different PLLs are described in this chapter. The PLLs have been combined with different VCOs, and locked signal generation from 32 to 42 GHz and 64 to 84 GHz (after frequency doubling) have been realized. Tab. 6.2 shows a comparison of this work with state-of-art millimeter-wave PLLs. The frequency tuning range of the PLLs in this work is much wider than other PLLs, and the achieved phase noise is also comparable to the state-of-art results, despite the fact that the circuits are realized in a much cheaper technology.

Table 6.2: Comparison of Recent Millimeter-wave PLLs

Ref.	**Technology** f_T/f_{max} **(GHz)**	**Tuning Range**	**Division Ratio**	**Loop Bandwidth**	**PN @1MHz**	**Spur (dBc)**	**Output Power (dBm)**	**DC** mW	**Chip Size** mm^2
[53] *TMTT* 12	0.18μm BiCMOS 200/180	90.9 - 101.4 (10.9%)	768	4 MHz	-92	-52	-	140	1.9
[54] *TMTT* 11	65nm CMOS -/-	70 - 78 (10.8%)	1024 to 1984	100 KHz to 1 MHz	-83	-49	-	65	0.16 [1]
[55] *JSSC* 11	65nm CMOS -/-	58 - 63 (8.3%)	1620 to 1984	4 MHz	-95	-67 to -58	-10	80	-
[56] *RFIC* 11	0.13μm BiCMOS 230/-	92.7 - 100.2 (8.3%)	64	45 MHz	-102	-60	3	570	1.1 x 1.1
[57] *TMTT* 11	90nm CMOS -/-	60.2 - 62.4 (3.6%) 81.3 - 83.3 (2.4%)	768 1024	700 KHz	-70 -72.5	-36 -52	-9.5 -7.34	106.6 109.9	1.5 x 0.75
[58] *JSSC* 11	0.13μm BiCMOS 230/280	86 - 92 (6.7%) 80 - 100 (22.2%) [2]	16	1 MHz to 10 MHz	-100	-	-3	1150 to 1250 [3]	1.7 x 1.1
[59] *JSSC* 09	0.18μm BiCMOS 200/180	75.67 -78.5 (3.7%)	768	4 MHz	-103.5	-47.8	-17.8	75	1 x 0.8
[60] *ISSCC* 09	45nm CMOS -/-	57 - 66 (14.6%)	512 - 8184	1 MHz	-75	-42	-	78	0.99 x 0.83
This Work	**0.8μm SiGe HBT 80/90**	**32 - 42 (27%)**	**32 128**	**50 MHz 15 MHz**	**-112 -99**	**-35 -42**	**4 @ 36 GHz 4 @ 36 GHz**	**320 352**	**0.9 x 1 1.1 x 1.2**
This Work	**0.8μm SiGe HBT 80/90**	**64 - 84 (27%)**	**64 256**	**50 MHz 15 MHz**	**-106 -93**	**-37 -43**	**-2.4 @ 64 GHz -6 @ 81 GHz**	**380 to 517 [4]**	**1.1 x 1 1.1 x 1.2**

[1] core area, [2] total range of two VCOs under differential biasing conditions, [3] with two VCOs and programmable division ratios (/16, /32/, /64, /128), [4] depending on the loop filter supply voltage.

Chapter 7

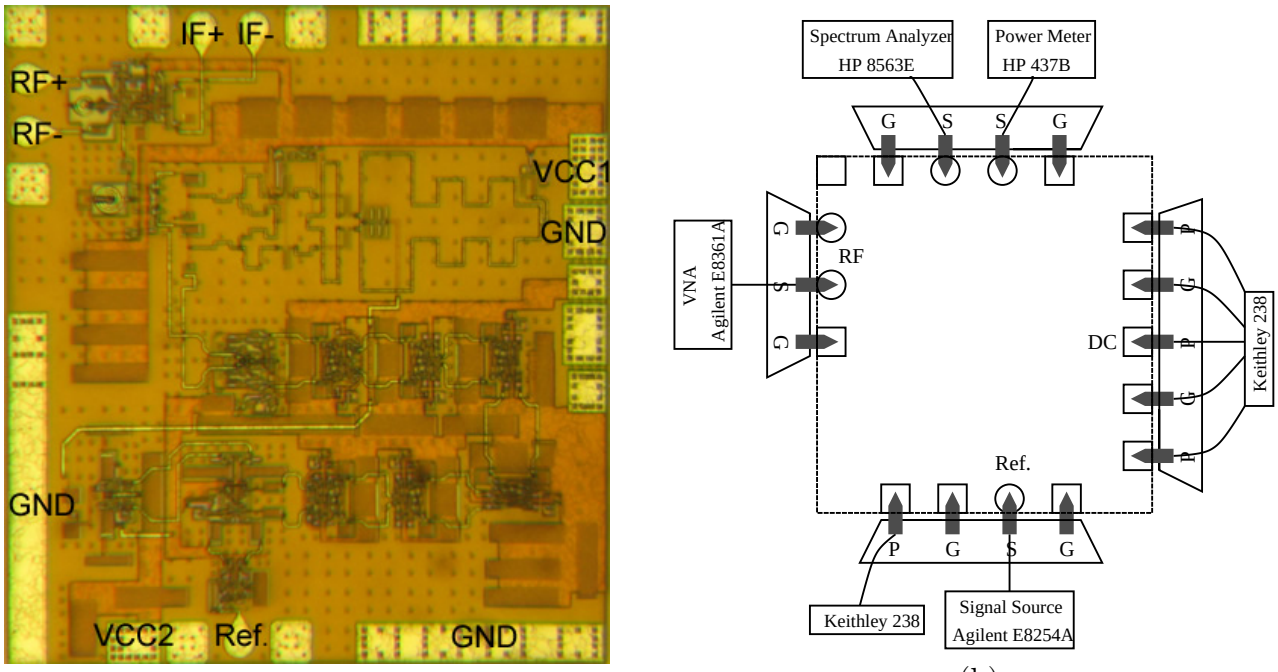
Down-converter ICs

This chapter describes fully integrated multi-functional ICs that combine the building blocks described in previous chapters. A down-converter IC (for analog oriented receiver) and a sliding-IF receiver IC (for digital oriented receiver) have been realized. Characterization of these ICs are shown in this chapter.

7.1 Down-converter IC

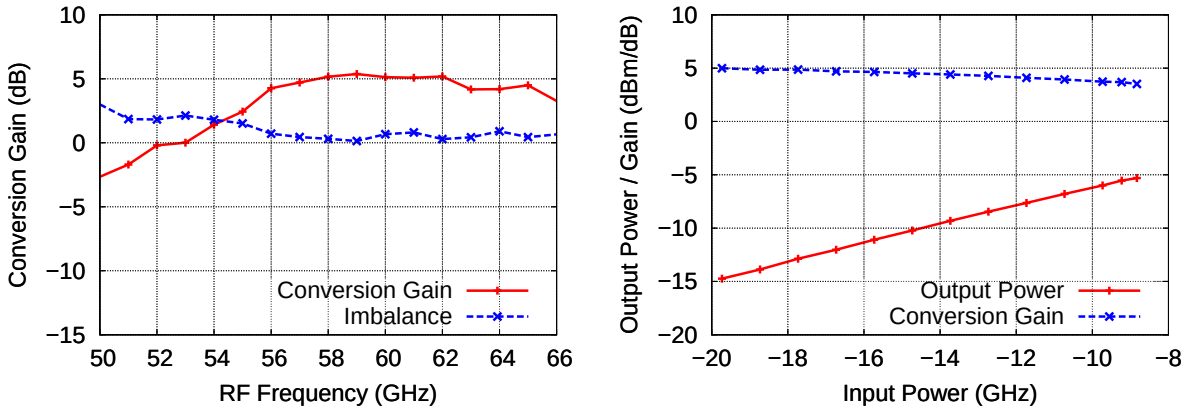
The down-converter IC consists of the down-converting mixer (Chapter 3, page 11) and the PLL circuit (Chapter 6, page 57). Since the PLL output (after frequency doubling) is single-ended, the second LO input of the mixer is directly grounded on chip via a 500 fF capacitor. Two different versions are realized with different frequency division ratios. The one with division ratio of 32 has lower LO phase noise but requires a 1.04 GHz reference signal, which is difficult to get. The one with division ratio of 128 requires only a 260 MHz reference signal, which can be taken easily from commercially available components, making the receiver easily reconfigurable (in terms of frequency). Fig. 7.1 (a) shows a photo of the realized down-converter IC.

The IC was characterized on-wafer. Due to the lack of differential signal sources, the RF input was connected single-endedly. The differential outputs were monitored simultaneously using a spectrum analyzer and power meter. Fig. 7.1 (a) shows the measurement setup. The IC consumes 130.5 mA (124 mA for /32) current from a single 3.5 V supply. The reference signal was fixed at 260 MHz (1.04 GHz for /32), which corresponds to an LO frequency of 66.56 GHz. The RF signal was swept from 50 GHz to 66 GHz, the measured conversion gain is shown in Fig. 8.18 (a), which is relatively flat from 56 GHz to 66 GHz and slowly decreases to -2.5 dB at 50 GHz. The 3dB-bandwidth is about 10 GHz, covering the complete 60 GHz ISM band. The measured amplitude imbalance between the two outputs ("IF+" and "IF-") is also shown in Fig. 8.18 (a). Within the 3dB-bandwidth, the imbalance is less than 1 dB. Fig. 8.18 shows the measured output power and conversion gain versus RF power. The conversion gain decreases from 5 dB to 4 dB when the RF power is increased to -10 dBm.



(a) (b)

Figure 7.1: (a) Chip photo of the down-converter IC. The chip size is 1.15 ×1.25 mm^2. (b) On-wafer measurement setup.



(a) (b)

Figure 7.2: (a) Measured conversion gain and amplitude imbalance between "IF+" and "IF-" versus RF frequency. (b) Measured output power and conversion gain versus input power (RF at 61 GHz).

7.2 Sliding IF Receiver

The down-converter described in section 7.1 is suited for an analog oriented receiver, in which the down-converted 5 GHz QPSK signal is processed by the following analog demodulator. A second down-converter has been realized, where the received RF signal is first down-converted to an intermediate frequency and then down-converted to DC through an I/Q demodulator. The baseband data (I/Q outputs) can then be processed directly by the baseband processor. For such a receiver structure, two LO signals are needed. One way to ease the design and save power consumption is to reuse the first LO signal (after frequency division). By choosing proper frequency division ratio and frequency of the first LO, the frequency-divided LO signal can be directly used for the I/Q demodulator. The center frequency of the received RF signal can be changed by changing the LO frequency, which also leads to a change of the intermediate frequency. Therefore, such an receiver structure is called sliding-IF structure. Fig. 7.3 shows the block diagram of the sliding-IF receiver. The frequency of the second LO is $\frac{1}{16}$ of the first LO. The frequency dividers in the PLL are reused, only one divide-by-two divider with I/Q outputs is added. An IF amplifier with 20 dB gain is inserted to amplify the IF signal. The two mixers are Gilbert cell mixers with resistive load.

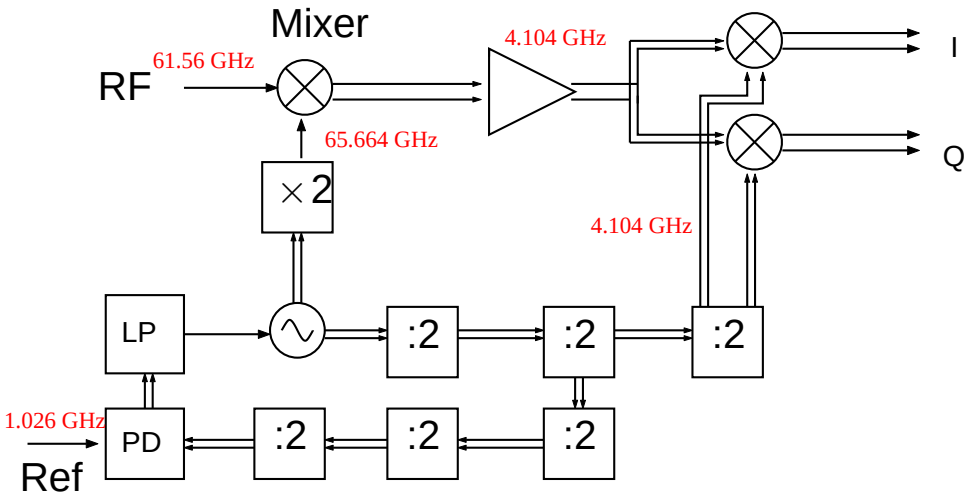


Figure 7.3: Block diagram of the sliding-IF receiver and the frequency plan for RF centered at 61.56 GHz.

As described in Chapter 2, the received RF signal is centered at 61.56 GHz. With an LO signal at 65.664 GHz, the RF signal can be down-converted to DC. The frequency plan is also shown in Fig. 7.3. The realized IC, as shown in Fig. 7.4, is very compact and occupies only 1.4 mm^2 chip area.

The IC was measured using the same setup as the down-converter. The I and Q output were connected through a "GSGSG" probe to two spectrum analyzers and measured simultaneously. The total DC power consumption is 759 mW[1]. The measured conversion

[1]The power consumption is not optimized. By optimizing the frequency divider and IF amplifier, the DC power consumption can be further reduced.

gain and linearity are shown in Fig. 7.5. The receiver has a peak gain of 24.5 dB and a 3 dB-bandwidth of 2 GHz (baseband bandwidth, DC to 2 GHz), which is sufficient for data rate up to 8 Gbit/s with QPSK modulation. The bandwidth in the current design is limited due to the small AC coupling capacitance at the IF amplifier input [2]. The input 1dB compression point is at -25 dBm, mainly limited by the IF amplifier. By setting the reference frequency to 993 MHz, 1.026 GHz and 1.059 GHz, the received RF frequency can be set to 59.58 GHz, 61.56 GHz, 63.54 GHz, respectively [3]. The measured conversion gain at these frequencies is shown in Fig. 7.5 (a). The gain and bandwidth changes only slightly for different RF frequencies, showing that the sliding-IF receiver also has a wide RF bandwidth.

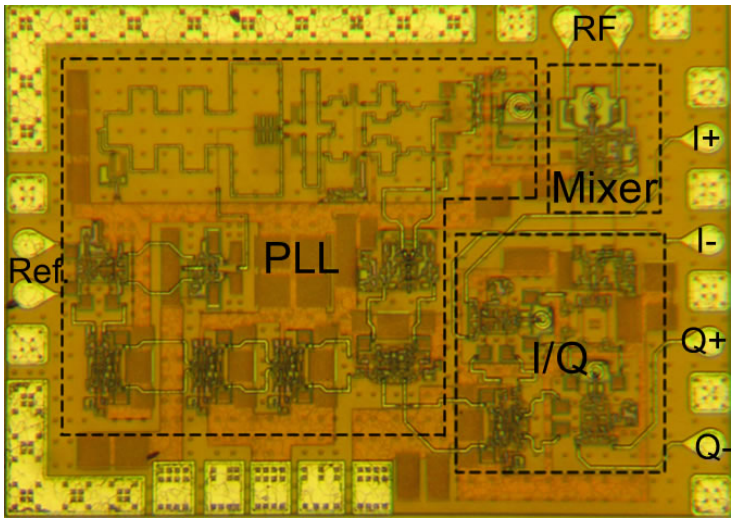
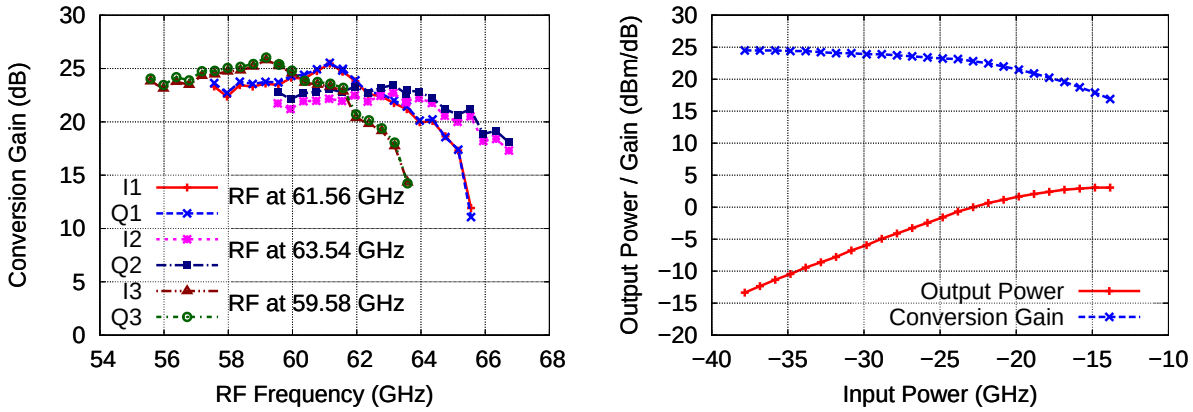


Figure 7.4: Photo of the realized sliding-IF receiver. The chip size is 1.4 ×1 mm^2.



(a) (b)

Figure 7.5: (a) Measured conversion gain for different RF frequencies. (b) Measured conversion gain and output power versus input power. RF at 61 GHz, LO at 66.664 GHz.

[2]A modified version, with direct DC coupling between the mixer and the IF amplifier has been submitted, with expected bandwidth of more than 4 GHz.

[3]These frequencies are the center frequencies of the 60 GHz channels, recommended by the ITU-R, see Chapter 2.

Chapter 8

Packaging and Modules

For the 60 GHz wireless transmission, the receiver IC is packaged in a module with connectors at the input and output. The IC is connected to the substrate board by wire-bonding. To compensate the influence of the bondwires, an "L-C-L" compensating structure was used. The design and characterization details of "L-C-L" IC-to-board bondwire interconnect is described in this chapter. Different PLL and receiver modules have been realized using the "L-C-L" interconnect, the design and performance of the modules are also described in this chapter.

8.1 IC-to-Board Interconnect

Wire-bonding is an easy, low-cost and widely used method for interconnects between ICs and boards. However, for RF and millimeter-wave applications, the inductance of the bondwire influences the performance significantly. The length of the bondwire for IC-to-board interconnect during IC packaging is strongly influenced by the height (thickness) of the IC. To reduce the bondwire length, a multi-layer stacked board is frequently used with a cavity accepting the IC, such that the IC surface is flush with the board. But the cavity requires extra processing steps, increasing fabrication time and cost. Another way of reducing the effect of bondwires is to integrate the inductance of bondwires in a low-pass filter, which has its cut-off frequency above the highest operating frequency [61]. A five-stage low-pass filter bondwire interconnect that enables the use of long bondwires has been reported in [62, 63]. However, it requires five elements for one interconnect and is not quite suited for IC-to-board interconnect, since filter-like compensation on the RF bonding pads is required [63]. Another difficulty of using this interconnect for IC-to-board connection is the ground transition from coplanar (IC pad) to microstrip (board), which is not discussed in [62,63]. An "L-C-L" compensating structure is shown in [64] to connect the IC to a differential bunny-ear antenna, where the two "L" are realized with bondwires. This is similar to the low-pass filter approach and the bondwire lengths can be longer. However, as shown later, this structure only works for differential interconnect, and no simulation or characterization of the interconnect is given in [64]. Therefore, this thesis

extends the work of [64], showing (with simulation and characterization) that with a simple "L-C-L" structure and radial stubs, the influence of the long bondwire, dominated by the height of the IC, can be compensated and low insertion loss can be achieved for both differential and single-ended interconnects.

8.1.1 Interconnect Design and Simulation

The "L-C-L" interconnect structures for differential and single-ended interconnects are shown in Fig. 8.1. Extended metal planes with via holes on either side of the IC bring the rear side ground plane of the microstrip configuration to the component side.

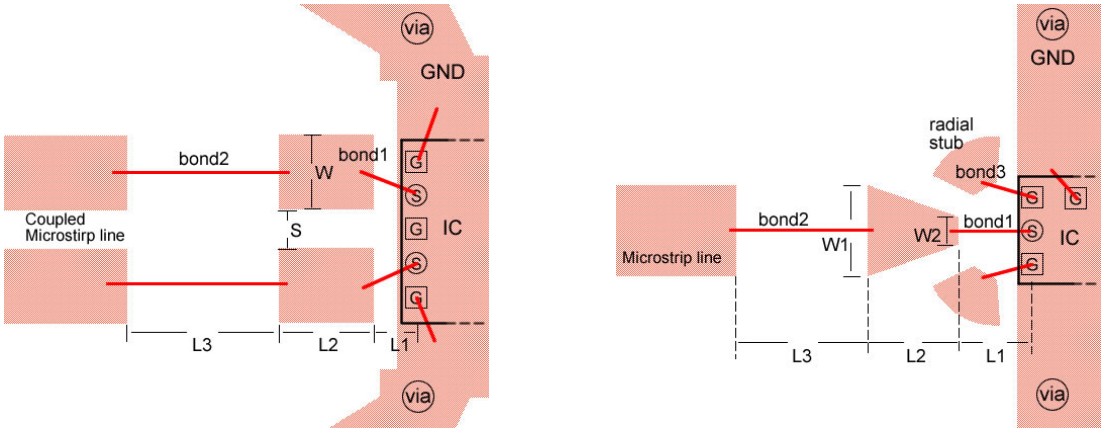


Figure 8.1: (a) Differential interconnect from IC to board. (b) Single-ended interconnect from IC to board.

For a differential interconnect (Fig. 8.1 (a)), the ICs usually have a ground-signal-ground-signal-ground ("GSGSG") or ground-signal-signal-ground ("GSSG") pad configuration, and the lines on the board form coupled microstrip lines with an odd mode characteristic impedance of 100 Ω. Instead of bonding directly from the IC to the board, a small shunt capacitor (realized by a very short microstrip line), is inserted between the IC and the on-board microstrip line. Connection from the IC to the board is done with two bondwires ("bond1" and "bond2"), which, together with the capacitance in between, form an "L-C-L" interconnect structure. By adjusting the two inductances (mainly "bond2") and the capacitance, a good transition from the IC to the board can be achieved. Provided that the signals are truly differential, a virtual ground appears both on the board and the IC, eliminating the need for a bonded RF ground connection. However, two ground pads are still bonded to the on-board ground to provide DC ground connection, which is necessary in the real application scenarios.

For a single-ended interconnect (Fig. 8.1 (b)), an "L-C-L" structure is insufficient for parasitic compensation. The ground of the IC and the board must also be well connected. Although two ground pads of the IC are bonded to the on-board ground, the ground connection at high frequencies is not good due to the inductances of the bondwires. Therefore, two small radial stubs are used for the ground connection. The radial stubs

are bonded to the ground pads of the IC ("bond3") and form a series resonant circuit with "bond3" at the design frequency, providing a good ground connection[1]. "bond3" also forms a coplanar configuration with "bond1", reducing the total inductance of "bond1" [65]. The stubs and the capacitor (microsrip line in between) are designed in a way that they can fit into a small area close to the IC.

The ICs are placed close to the interconnect, with "L_1" of 200 μm for the differential case and 300 μm for the single-ended case[2]. Two bondwires are bonded from the same IC pad to the board to reduce the resistance and inductance of "bond1". The length of the short microstrip line ("L_2") is 400 μm for both cases. "L_3" is made intentionally large (700 μm for the differential case and 600 μm for the single-ended case) and the connection is done with multiple bondwires in parallel. Compared with a single short bondwire, this increases the tolerance to varying bondwire lengths. Also, the inductance of "L_3" can be tuned by adjusting the number of bondwires and the distance between them, which can be used to compensate for design and board production errors (estimation of bondwire inductance, etc.).

To test the IC-to-board interconnects, ICs with 50 Ω through lines ("GSG" pads, 100 μm pitch) and ICs with 60 GHz baluns ("GSG" and "GSGSG" pads, 100 μm pitch) are used for the single-ended and differential cases, respectively. The height of the IC is 350 μm. An IC-board-IC through connection, which consists of two interconnect structures on both sides and a 50 Ω microstrip line (2000 μm long) in between, is realized. Fig. 8.2 shows a photo of the realized differential and single-ended through connections with bonded ICs. The insertion and return loss of the through connection can be easily measured with on-wafer probing (on the two ICs) and the performance of the IC-to-board interconnect can be evaluated.

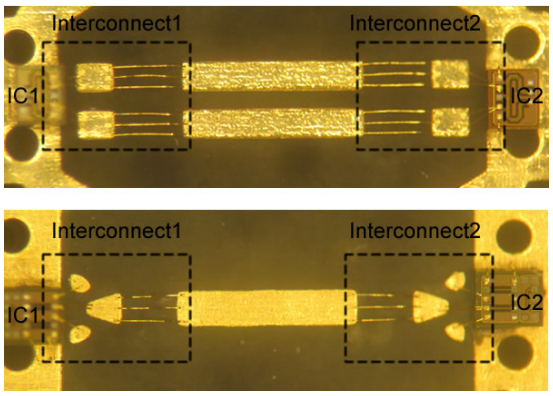


Figure 8.2: Photo of the differential and single-ended IC-board-IC through connections with bonded ICs.

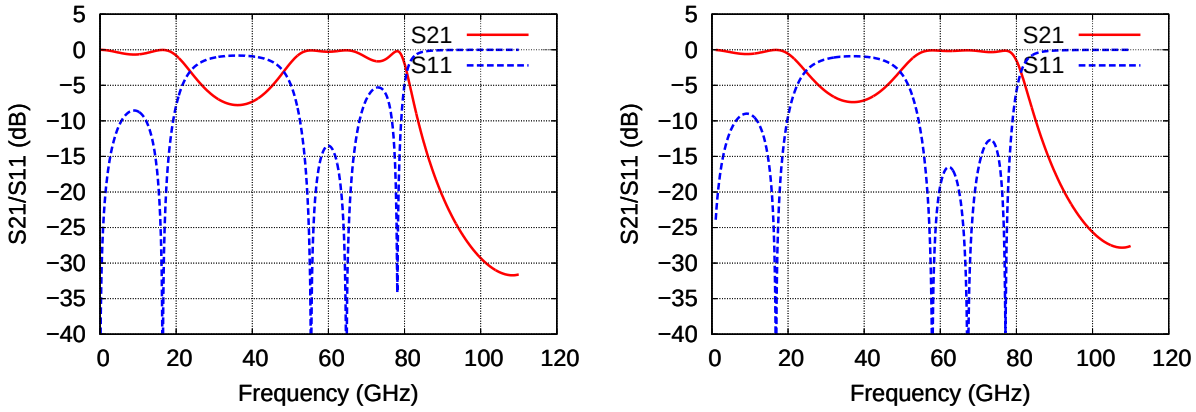
One intention of this work is to find an easy and simple way to compensate for bondwire

[1]This however does not solve the instability issues due to the inductance of bondwire on the ground pad. Therefore, reducing the ground bondwire inductance (using multiple bondwire in parallel for instance) is still necessary.

[2]"L_1" should be as small as possible to reduce the inductance. However, considering the wire bonding and board production, 200 μm is chosen for the differential interconnect. For the single-ended interconnect, "L_1" is increased to 300 μm because of the stubs.

interconnects for packaging millimeter-wave modules. Therefore, simple models, instead of full 3D EM simulations, are used to guide the design. The interconnect and through connections are simulated in ADS. The microstip line and radial stubs are modeled using corresponding ADS "Tline-Microstrip" components and the bondwires are modeled using ideal inductors, applying the "1 nH per millimeter" rule of thumb. The models are too ideal and simple to be accurate, but serve well (as shown later) as a starting point.

To simulate the through connection with differential interconnect, the balun ICs are replaced with two 100 Ω ports, which are connected differentially to the interconnect (ground connection is not needed). For the single-ended through connection, the through line ICs are replaced with 50 Ω ports and ideal ground is used in the simulation. "bond3" and the radial stubs are simulated separately to provide a good series resonance at the targeted frequency. The estimated inductance of "bond1", "bond2" and "bond3" are 0.2 nH, 0.3 nH and 0.35 nH. The radial stub has an input line width of 100 μm at the narrow end, a length of 180 μm and an angle of 60 degree. Fig. 8.3 shows the simulated insertion and return loss of the through connections under the rather simple and ideal simulation conditions. A very low insertion loss and high return loss can be achieved at 60 GHz with almost 20 GHz bandwidth.



(a) (b)

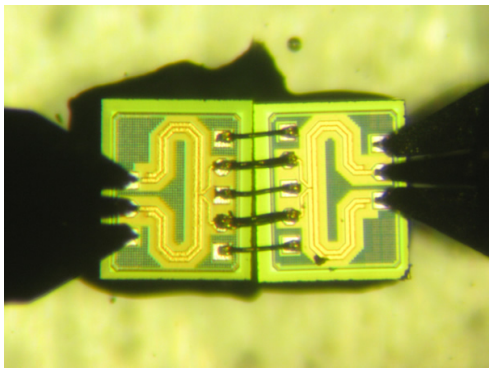
Figure 8.3: Simulation results of the through connections. (a) Differential interconnect. (b) Single-ended interconnect.

8.1.2 Experimental Results

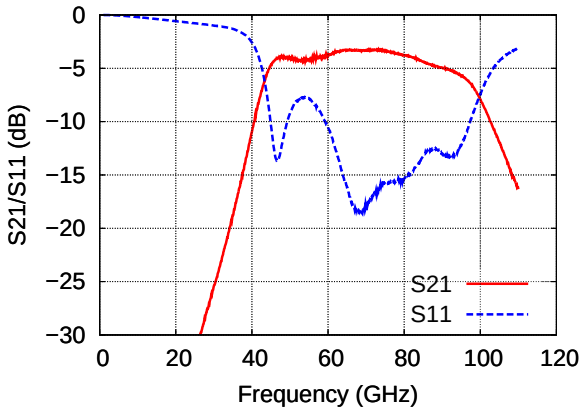
The test structures are produced on Rogers RT/Duroid 5880 substrate (ϵ_r:2.2, 127 μm thickness, 17 μm copper cladding) with a standard process (with via hole plating). A Ni/Au layer is deposited on the top and bottom metal to improve bonding. The minimum feature size of the board production is about 80 μm. During the board design, 15 μm was added on each side of the metal to compensate for underetching during production. The ICs were glued to the board with non-conducting adhesive. A manual ultrasonic wedge wire bonder (West Bond 7400A) was used to bond the ICs to the board. Gold bondwires with 17 μm diameter were used for all the bonds. The measurements were performed using 110 GHz GSG probes and vector network analyzer (Agilent E8361A and N5260).

Differential Interconnect

The differential through connection is shown in Fig. 8.2 (top). The balun IC used in the differential interconnect is a Marchand type realized with thin-film microstrip lines. To evaluate the loss of the balun, two balun ICs are bonded back-to-back and characterized, as shown in Fig. 8.4 (a). The measured insertion and return loss are provided in Fig. 8.4 (b). The insertion loss of the two baluns is roughly 3.6 dB around 60 GHz, neglecting the loss of the very short bondwires in between.



(a)



(b)

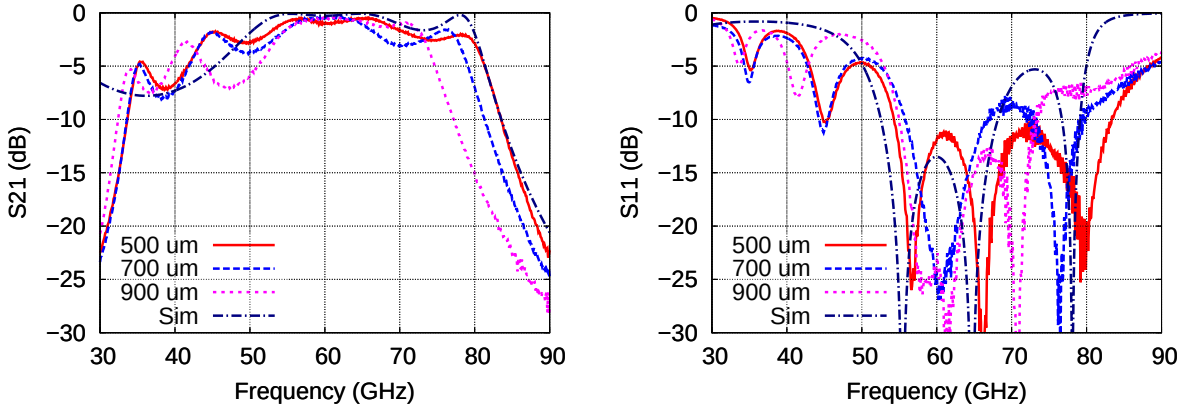
Figure 8.4: (a) Evaluation of the balun loss with two baluns bonded back-to-back. (b) Measured S-parameter of the two baluns.

Three differential through structures with different "L_3" (500 μm, 700 μm and 900 μm) were produced and tested. The measurement results, together with simulation results are shown in Fig. 8.5. To compensate the loss of the two baluns, 3.6 dB (loss of the two back-to-back baluns) is subtracted from the measured insertion loss. For the optimum structure ("L_3" of 700 μm), the insertion loss is only 0.2 dB (0.1 dB per interconnect) at 60 GHz. The insertion loss increases to 1.1 dB at 55 and 65 GHz, leading to a 1-dB bandwidth of 10 GHz (16% at 60 GHz). The return loss is above 10 dB from 56 to 66 GHz. Shorter and longer "L_3" changes the frequency response and loss slightly, although the change of "L_3" is much larger than the possible board production or bonding tolerance, which shows that the structure is not very sensitive to "bond2". The simulation predicts the measurement quite well, although the simulation models are very ideal and simple.

Single-ended Interconnect

The single-ended through structure is shown in Fig. 8.2 (bottom). The radial stubs are very small, with a length of 180 μm and a line width of 100 μm at the narrow end. Three different structures with different stub sizes (150 μm, 180 μm and 210 μm) were produced and measured[3]. Fig. 8.6 shows the measured insertion and return loss of the three structures. The through line IC has a length of 200 μm and loss of 0.45 dB at 60 GHz, so 0.9 dB is subtracted from the measured insertion loss. The simulation results is also shown in Fig. 8.6 for comparison.

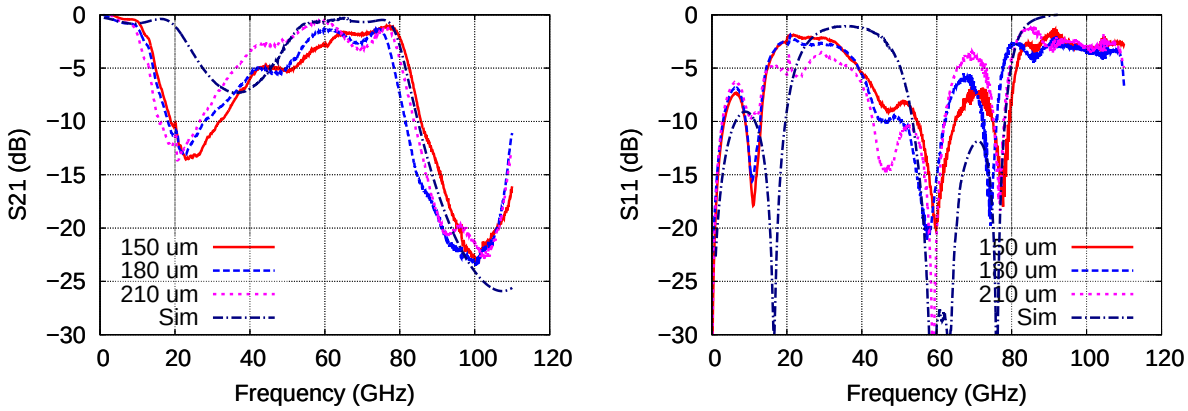
[3]At the beginning of the test, the underetching of the stubs was unknown, so three different sizes are prepared.



(a) (b)

Figure 8.5: Measured insertion and return loss of the differential through connections with different "L_3". To compensate the balun loss, 3.6 dB is added to the measured S21.

Due to more underetching, the 210 μm stub is closer to the optimum size (180 μm) after production, so the structure with 210 μm stubs shows the lowest insertion loss of 0.6 dB (0.3 dB per interconnect), with a 1-dB bandwidth of 11 GHz (53 to 64 GHz). The return loss is also above 10 dB from 43 to 63 GHz. The two structures with smaller stub size show slightly higher insertion loss and the optimum frequencies are shifted to higher frequencies. The one with 150 μm stubs has a minimum insertion loss of 1.2 dB and a 1-dB bandwidth from 62 to 79 GHz. The measured results have narrower bandwidth and higher insertion loss than the simulation. However, as a starting point without considering the bondwire loss and the ground connection using stubs, the simulation predicts the behavior quite well.

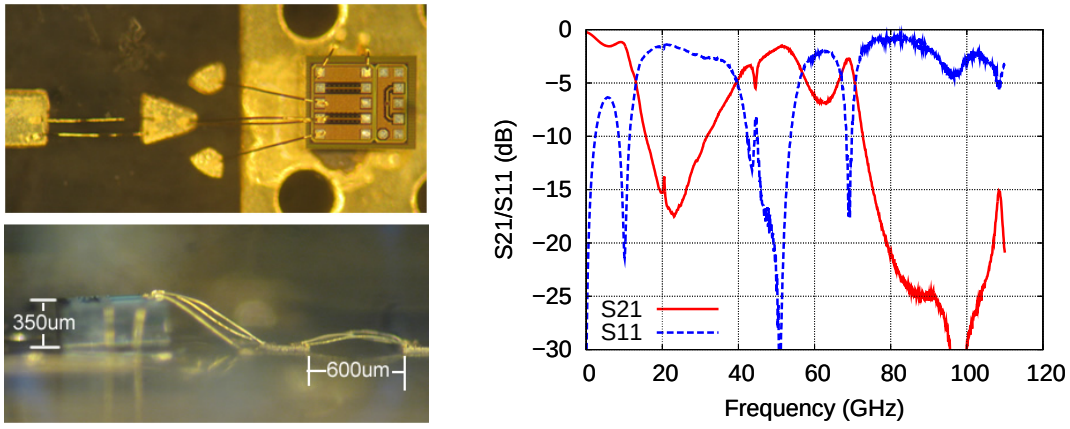


(a) (b)

Figure 8.6: Measured insertion and return loss of the single-ended through connections with different "L_3". To compensate the balun loss, 3.6 dB is added to the measured S21.

One advantage of the "L-C-L" interconnect is that it can compensate the parasitic inductance of long bondwires. To test this, the through line ICs were intentionally moved away from the interconnect structure to increase the bondwire length. Fig. 8.7 (a) shows the top and side view of the bonded structure. The length of the bondwires to the center

and to the stubs are roughly 800 μm and 700 μm. The measurement results are shown in Fig. 8.7. The frequency of optimum impedance match and minimum transmission loss is shifted to 52 GHz with 1 dB insertion loss (0.5 dB per interconnect) and the bandwidth is slightly decreased, due to the larger inductances of the long bondwires. The long bondwire in this test is an extreme case that is unlikely to happen in real designs. However, this shows that even with such excessive bondwires, a good IC-to-board transition can be achieved with the "L-C-L" interconnect structure.



(a) (b)

Figure 8.7: (a) Top and side view of the test structure with long bondwires. The wire lengths to the stubs and compensating capacitance are approximately 700 μm and 800 μm, respectively. (b) Measured insertion and return loss of the single-ended through connection with long bondwires. 0.7 dB is added to the measured S21 to compensate for through line loss.

The results shown in Fig. 8.6 are optimized for 60 GHz. By reducing the size of the radial stubs, the interconnect can be optimized for higher frequencies. Interconnect optimized for 94 GHz have also been realized, as shown in Fig. 8.8. The stub input line width (100 μm) and angle (60 degree) are kept the same as before. The stub length is reduced to 120 μm. "L_1", "L_2" and "L_3" (Fig. 8.1) are reduced to 200, 250 and 350 μm.

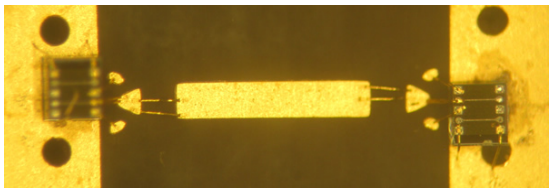
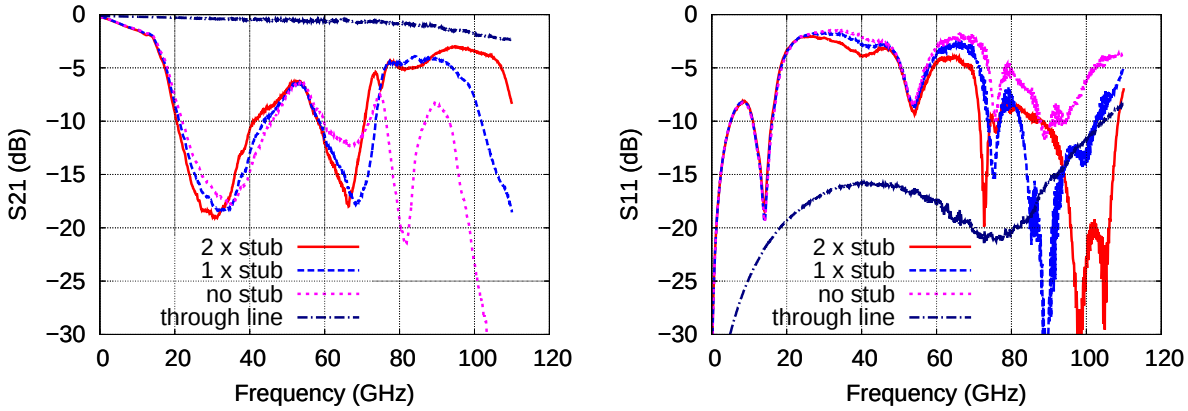


Figure 8.8: Top view of the single-ended through connection optimized for 94 GHz. The radial stubs have lengths of 120 μm, input line width of 100 μm and angle of 60 degree.

Fig. 8.9 shows the measurement results of the 94 GHz through connections and the result of a single through line IC. Low insertion loss (3 dB) and high return loss are achieved at 94 GHz, with a 1 dB bandwidth from 89 to 105 GHz. The insertion loss of the complete structure is even less than two times the loss of a single through line IC, because of the improved matching of the through line IC at this frequency range. Taking 1 dB loss for

the through line IC (with good matching), the loss of one interconnect is only 0.5 dB at 94 GHz. The return loss is better than 10 dB from 88 to 108 GHz.



(a) (b)

Figure 8.9: Measured insertion and return loss of a single-ended through connection for 94 GHz under two, one and no bonded radial stub situations. The measured insertion and return loss of a single through line IC are also shown.

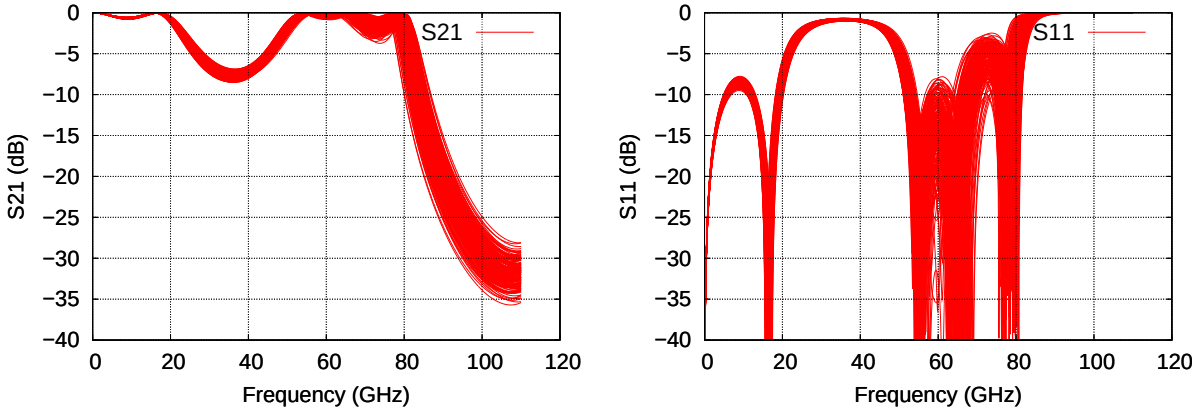
The radial stubs play an important role for the single-ended interconnection. To verify this, the bondwires to the radial stubs were removed step by step, while the two extra ground pads were still bonded to the on-board ground. Fig. 8.9 shows the measured results. After removing one stub, the insertion loss increases by roughly 1 dB and the frequency is shifted to 85 GHz. The shift of the frequency is due to the increase of the inductance of "bond1" (Fig. 8.1 (b)), when one of the ground bondwires is removed (less coupling between "bond1" and ground). After the two stubs are removed completely, the performance gets significantly worse at the design frequency, which clearly shows the importance of the radial stubs. The performance at low frequencies (below 15 GHz) is not affected by the stubs, as the low frequency ground is provided by the bond connection between the IC ground pads and the on-board ground.

8.1.3 Discussion

Repeatability

The board production is one factor that can influence the repeatability of the performance. The board production facility[4] has a tolerance of 20 μm ($\pm$ 10 μm per edge). The dimension of the differential interconnect is in the range of a few hundred micrometers (for 60 GHz), which is not very sensitive to the production variation. As an evaluation, a Monte Carlo simulation was performed, where the parameters of the microstrip lines are varied according to the board production tolerance and a $\pm$ 10% tolerance is applied to the bondwire inductance. Fig. 8.10 shows the simulation results with 200 trials. The insertion loss is less than 0.8 dB for the worst case and the return loss remains better than 8 dB at the design frequency.

[4]PCB fabrication group of Ulm University



(a) (b)

Figure 8.10: Monte Carlo simulation results of the differential through connection (Fig. 8.3 (a)) with 200 trials. The line width and length are uniformly distributed within a ± 20 μm range and the inductor values have uniform distributions within a ± 10% range.

The single-ended interconnect is more sensitive to the production variation, mainly because of the radial stubs, which have dimensions of around 100 μm. Monte Carlo simulation shows less than 0.5 dB insertion loss and better than 12 dB return loss under the same condition as the differential case. However, the effect of the stubs are not included in the simulation, because ideal ground is used for the single-ended simulation and the stubs are simulated separately[5]. To evaluate the repeatability of the single-ended interconnect, the same structures were repeated three times on the same board and the ICs were carefully glued and bonded in the same way. The measured results of the three structures are shown in Fig. 8.11. The structures are optimized for 80 GHz, with insertion loss of around 1 dB. From the measured return loss, the difference of the three structures are visible. However, the shift of frequency is only 1 or 2 GHz, which is less than 3% at 80 GHz, while the errors due to manual positioning and bonding are also included[6].

Frequency Limit

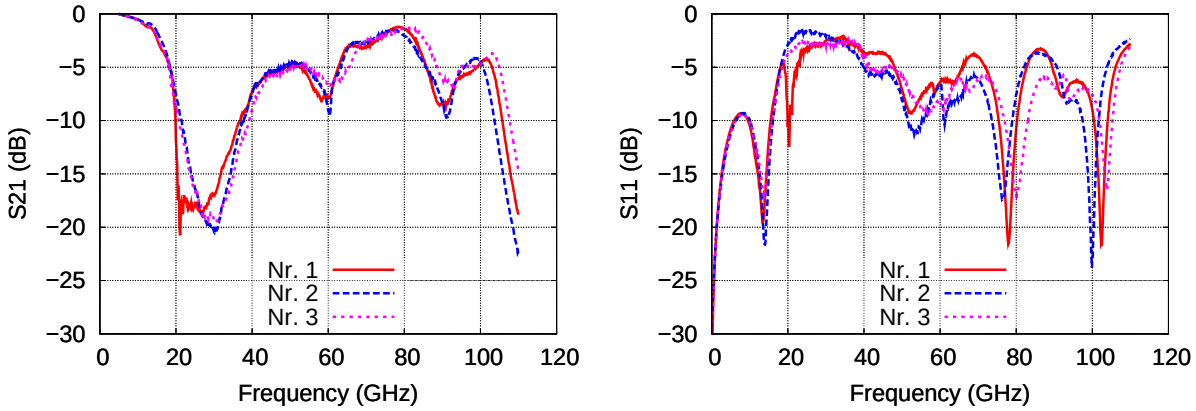
The differential interconnect is only tested at 60 GHz, due to the limitation of the balun ICs. However, it can be pushed to much higher frequencies, by reducing the compensating capacitor ("L_2" in Fig. 8.1 (a)) and slightly reduce "L_3" while keeping "L_1" the same. Fig. 8.12 shows the simulation results for 120 to 140 GHz interconnect, with "L_2" being reduced to 140 μm, which is still larger than the board production resolution.

For the single-ended interconnect, the sizes of the radial stubs (for 94 GHz) are already at the limit of what can be produced in the facility. Choosing a substrate with thinner Cu cladding (8 instead of 17 μm) can improve the production resolution (minimum structure width that can be produced) down to 50 μm. However, as the stub gets smaller and

[5]When the ground of a port is not perfected ground, simulation errors can occur.

[6]The mannual positioning of the ICs has tolerance of a few tens of micronmeters (much larger than the board production tolerance) and contributes significantly to the difference between the three samples. For industrial applications with automated pick-and-place and wire bonding, less difference is expected.

thinner, bonding on the stub becomes very difficult, and the stub can be punched into the substrate by the force of bonding. So to further increase the frequency, the bondwire ("bond1" in Fig. 8.1 (b)) needs to be shorter, which requires a board recess to bring the IC closer to the board.



(a) (b)

Figure 8.11: Measurement results of the three structures for repeatability test.

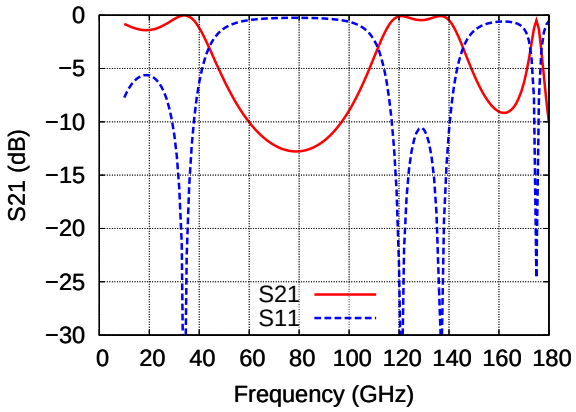


Figure 8.12: Simulated differential interconnect for 120 to 140 GHz, with "L_2" reduced to 140 μm. "L_1" is kept the same and "L_3" reduced to 400 μm (inductance of 0.2 nH).

8.2 Module Design and Characterization

As presented in Section 8.1, the "L-C-L" IC-to-board interconnect is well suited for millimeter-wave applications. A few modules have been realized in this thesis work based on the IC-to-board interconnect and very good performance is achieved. Characterization of the modules are shown in the next subsections.

8.2.1 PLL Modules

Two different PLL circuits described in Chapter 6 have been packaged in modules. One is at 33 GHz, with differential outputs and the other is at 67 GHz (after frequency doubling), with single-ended output. Fig. 8.13 shows photos of the two packaged modules and close-up photos of the bondwire interconnects.

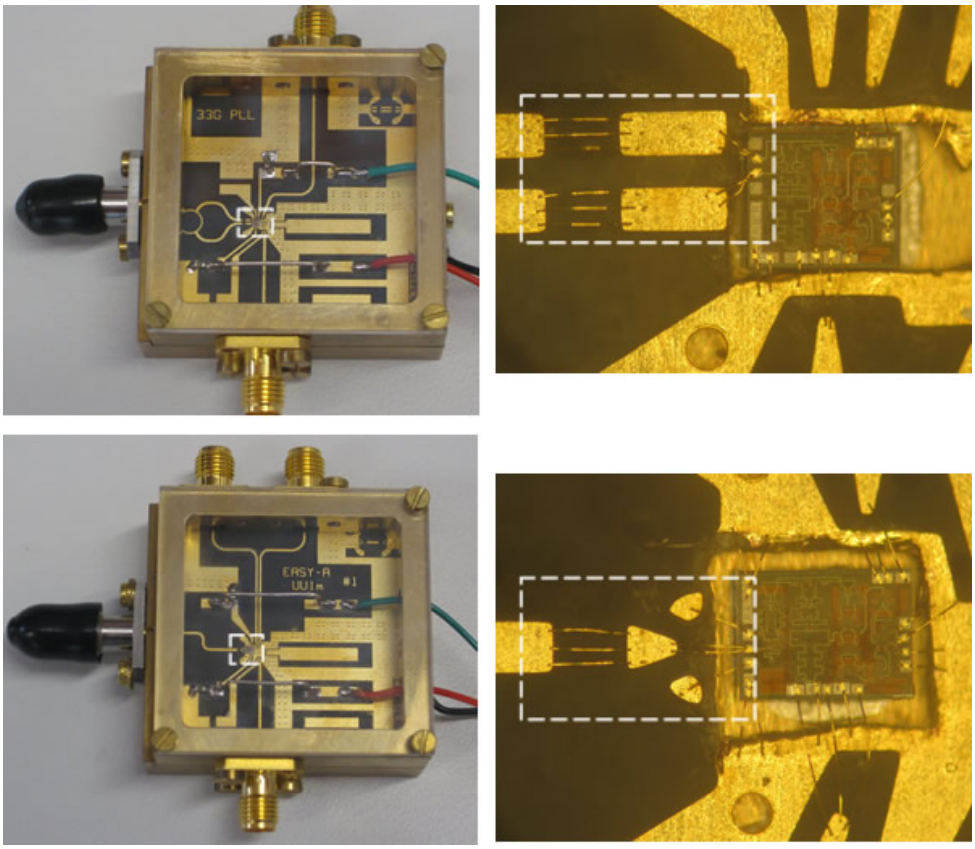
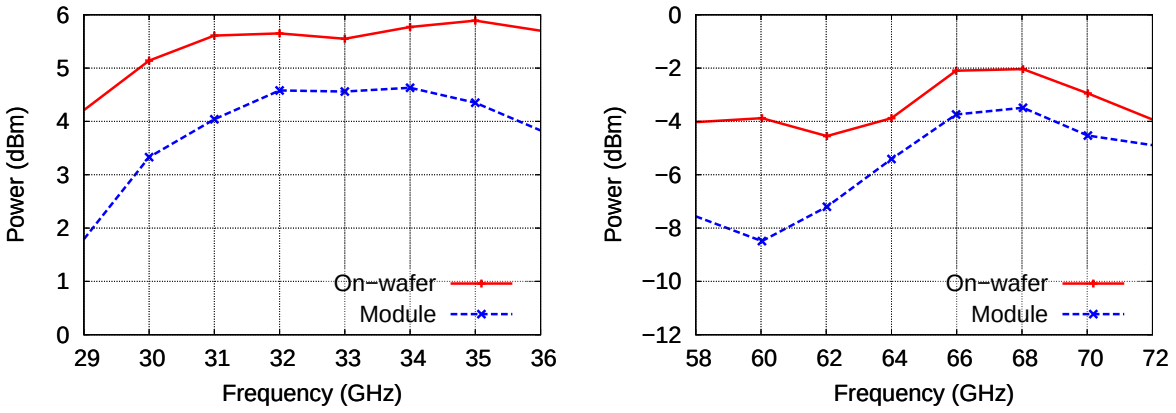


Figure 8.13: Photos of the packaged 33 GHz differential PLL and 67 GHz single-ended PLL and close-up photos of the bondwire interconnects.

The ICs are wire bonded to the substrate (Rogers RT-Duroid 5880, ϵ_r of 2.2, 127 μm substrate thickness) and enclosed in a brass housing. V-band connectors (Anritsu V-103F) are used for the output and SMA connectors for the reference input. After cutting a recess into the board, the IC is glued directly on the metal housing for better heat dissipation. The differential outputs of the 33 GHz PLL are combined on-board using a ratrace balun, while the 67 GHz PLL output feeds directly into the connector through a microstrip line. The differential (designed for 33 GHz) and single-ended (designed for 67 GHz) "L-C-L" interconnects are implemented, as shown in the dashed box. The output power of the packaged PLLs were measured and compared with the on-wafer measurements. Fig. 8.14 shows the measurement results.

For the 33 GHz PLL, the output power from the module is only 1 dB lower than the on-wafer measurement at 33 GHz and the difference slowly increases to 2 dB at 30 and 36 GHz. Considering the loss of the V-connector (0.4 dB at 33 GHz) and the balun



(a) (b)

Figure 8.14: Measured output power of the packaged 33 GHz differential PLL and 67 GHz single-ended PLL.

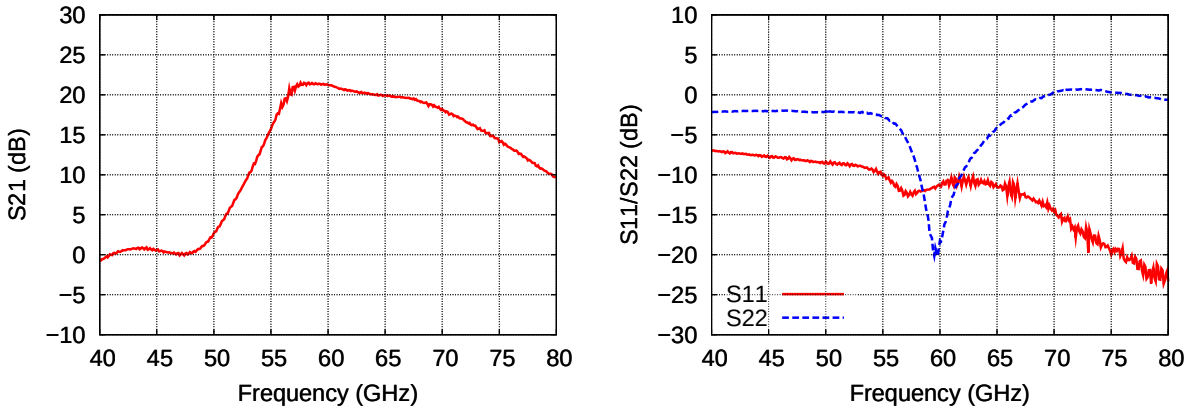
(0.6 dB), the additional loss from the bondwire interconnect is negligible. For the 67 GHz PLL, the output power is only 1.5 dB less than on-wafer measurement results at 68 GHz and the difference is less than 2 dB from 64 GHz to 72 GHz. The loss of the V-connector is roughly 1 dB and the loss of the microstrip line is 0.4 dB. So the loss of the bondwire interconnect is also negligibly small. These results agree quite well with the experimental results of the "L-C-L" bond wire interconnects. The spectrum and phase noise of the two modules were also measured and no degradation (compared to on-wafer measurement) was observed. The 33 GHz PLL module can be tuned from 29 GHz to 36 GHz with an output power of about 3 dBm, while the 67 GHz PLL module can be tuned from 58 GHz to 72 GHz with -6 dBm output power. The wide bandwidth and high output power make them very suited as signal sources for Ka and V band applications.

8.2.2 Down-converter Modules

For use in a 60 GHz wireless system, the down-converter IC that is described in Chapter 7 has also been packaged in a module with coaxial connectors at the input and output. A separate LNA was packaged together with the down-converter to improve the gain and noise figure. Different versions of down-converter modules were realized for comparison. The details of the modules are described below.

The LNA is provided by a project partner (TES Electronic Solutions GmbH). It is a two-stage cascode amplifier, realized in a 0.25 μm SiGe BiCMOS technology (IHP SiGe25H1, f_T/f_{max} of 180/220 GHz). The circuit is quasi-differential, consisting of two single-ended LNAs. The measured single-ended gain and reflection coefficients are shown in Fig. 8.15. It has a peak gain of 21.5 dB at 59 GHz and a 3 dB-bandwidth of 14 GHz (56 GHz to 70 GHz). The noise figure is about 7 dB. The details of the LNA can be found in [14].

Fig. 8.16 shows the realized down-converter module. The carrier substrate is the same as in the PLL modules (Rogers RT Duroid 5880). A V-connector is used for the 60 GHz



(a) (b)

Figure 8.15: Measured gain and reflection coefficients of the LNA.

RF input[7] and SMA connectors are used for the IF output and reference input. A rat-race balun is realized on-board to convert the single-ended input into differential signals. The microstrip lines and DC lines are routed to the vicinity of the ICs to shorten the bondwires. The RF input of the IC is bonded to the microstrip line using the "L-C-L" compensating structure. The IF outputs are bonded to the board directly, since the IF signal is at low frequency. 10 nF SMA capacitors are soldered between the DC supplies and the ground to filter out the low-frequency noise.

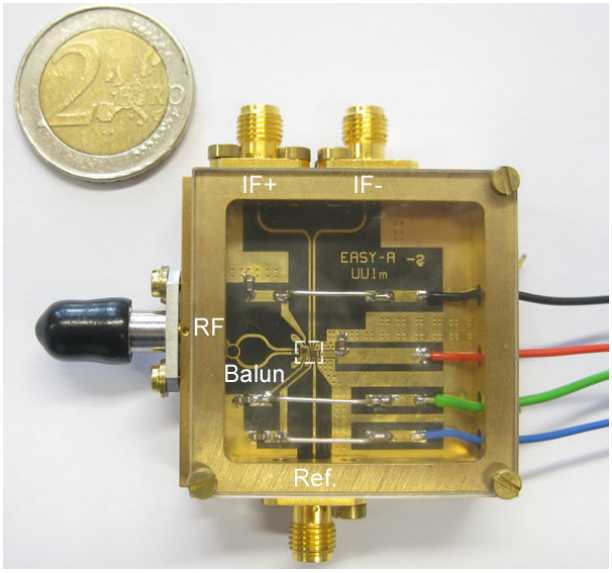
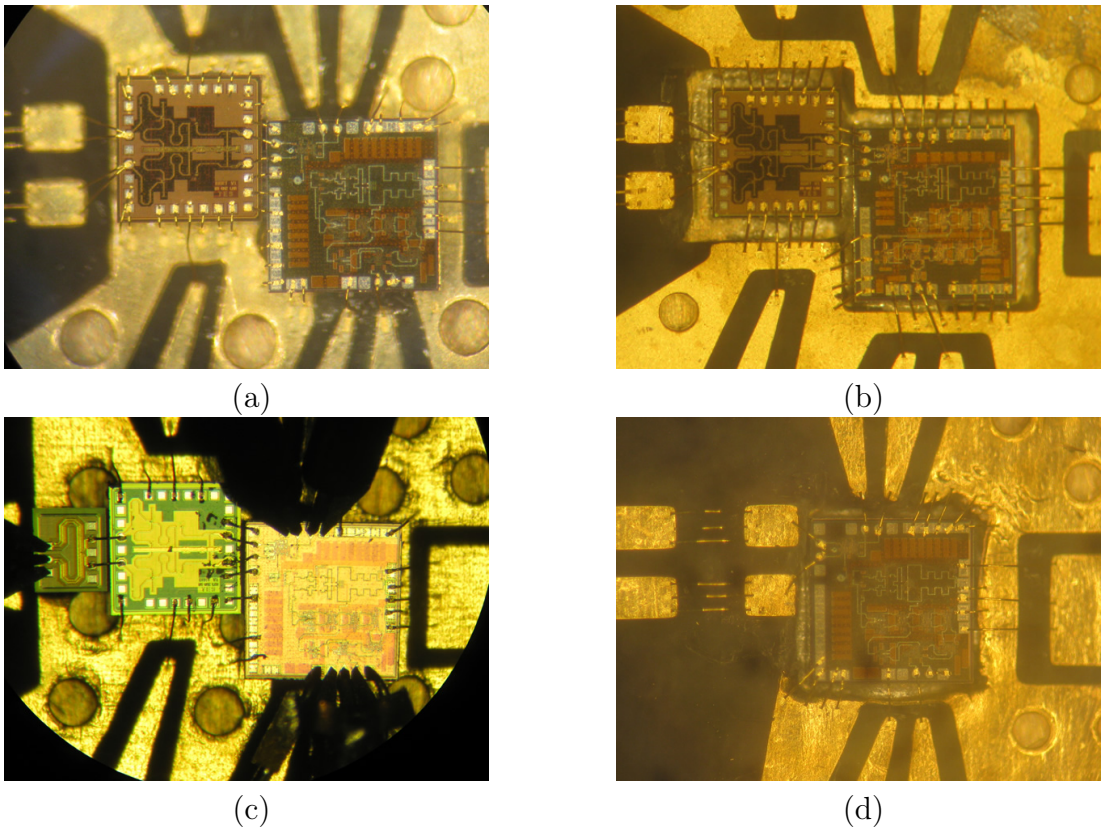


Figure 8.16: Measured gain and reflection coefficients of the LNA.

Fig. 8.17 (a) shows the close-up photo of the down-converter module. The LNA and down-converter IC are glued directly on the top metal of the board (using silver glue) and connected by wire bonds. The ICs are placed as close to each other as possible to shorten the bondwires. Vias are placed on the extended metal planes around the IC to bring the

[7]The antenna can be directly realized on the same board, which has not been done for ease of characterization. Antennas with V-connectors are used for the wireless transmission.

ground from the rear side to the component side. The input of the LNA is bonded to the board using the differential "L-C-L" interconnect (Fig. 8.5, page 82, 700 μm "L_3"). The ground of both ICs is bonded to the on-board ground using many bondwires in parallel to reduce the inductance of the bondwires. Fig. 8.17 (b) shows a second version of the down-converter module. The LNA and down-converter are glued on the metal housing, after cutting a recess in the board. This improves the heat dissipation and therefore improves the performance, as shown later. The two versions were measured coaxially using the same setup. The LO was fixed at 66.56 GHz and RF was swept from 50 to 66 GHz. The measured conversion gain is shown in Fig. 8.18 (a). As a comparison, the conversion gain was also measured on-wafer, by using a balun IC (Fig. 8.4, page 81) at the input for probing. Fig. 8.17 (c) shows a photo of the on-wafer measurement setup. The down-converter IC draws 120 mA current from a 3.5 V supply, while the LNA consume 23 mA current from a 2.5 V supply.

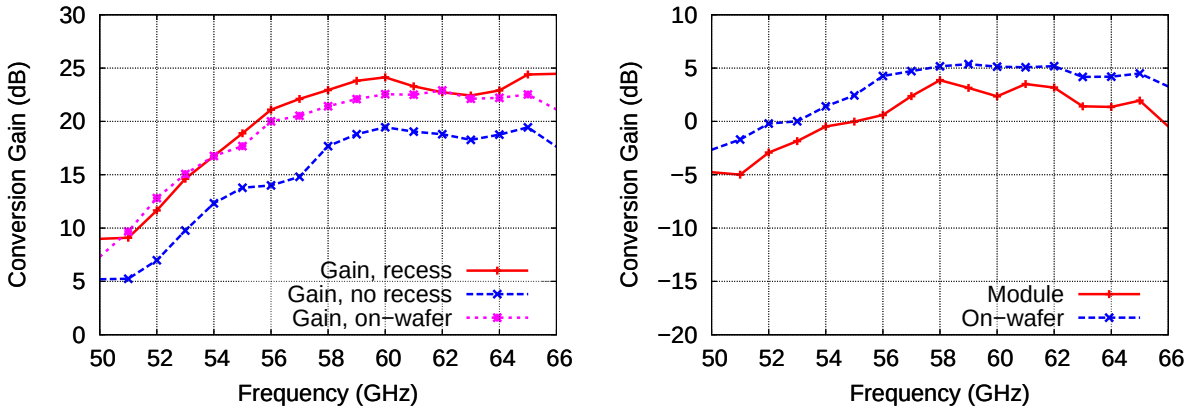


(a) (b) (c) (d)

Figure 8.17: Close-up photo of the down-converter module without board recess (a) and with board recess (b). (c) Close-up photo of the on-wafer probing. (d) Close-up photo of the down-converter module without LNA.

Conversion Gain

The on-wafer measurement shows a conversion gain of 23 dB with a 3 dB-bandwidth of 10 GHz. The balun has about 1.5 dB loss, so the gain of the LNA and down-converter IC is about 24.5 dB. The module with board recess shows slightly higher conversion gain, compared with the on-wafer measurement. The total off-IC loss is about 3 dB (1 dB for the V-connector, 1 dB for the on-board ratrace balun and bondwire interconnect and



(a) (b)

Figure 8.18: (a) Measured conversion gain of the down-converter modules with LNA in comparison to on-wafer measurement results. (b) Measured conversion gain of the down-converter module without LNA in comparison to on-wafer measurement results.

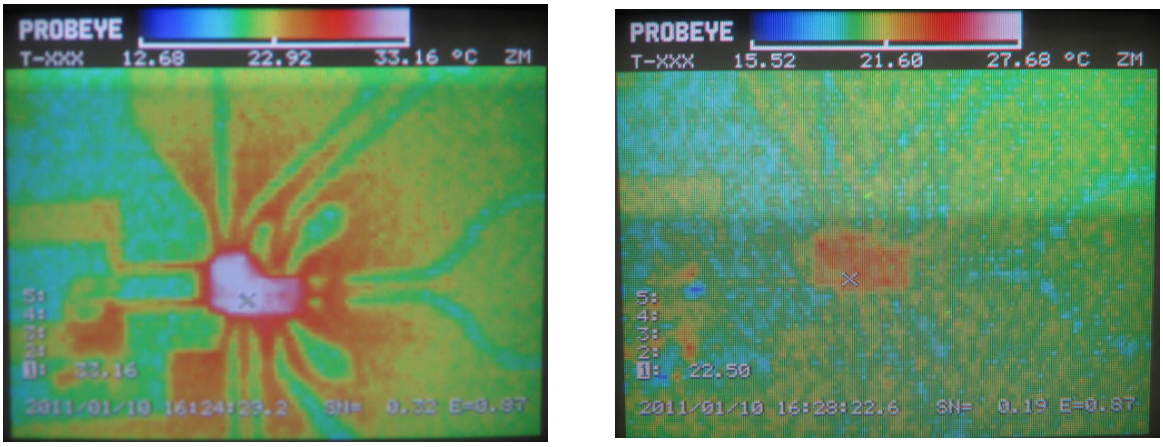
1 dB for the IF microstrip and connector loss), so the gain of the LNA and down-converter IC is about 27 dB. The bandwidth is similar to the on-wafer measurement. The module without board recess shows the lowest conversion gain of about 18.5 dB.

The conversion gain difference between the two modules (with and without recess) is about 5.5 dB. This is mainly due to the different heat dissipation in the two modules. For the on-wafer measurement, the heat dissipation is also not good[8], so the gain of the LNA and down-converter is less than in the module with recess.

To check the heat dissipation, both modules are monitored under an infrared camera. Fig. 8.19 shows the infrared picture of both modules under normal operation. It is clearly visible that the heat cannot be well dissipated in the module without the recess, due to the low thermal conductivity of the substrate material. The temperature is much higher[9] than the module with recess, where the heat is directly conducted to the metal housing. The high temperature leads to a decrease of the gain of the LNA and down-converter. Therefore, the board recess is necessary to achieve better performance, especially when the DC power consumption is high. On the other hand, the module without recess is easy to fabricate and the board does not need to be glued on the housing, easing the assembly of the module. Although the temperature is higher, the module can operate stably for hours under room temperature, which is still a viable solution, if the performance is not very critical.

As explained in Chapter 2, for very short distance transmission, a receiver front-end without LNA is possible. Therefore, a third module was realized, which has only the down-converter IC. The close-up photo of this module is shown in Fig. 8.17 (d). For better heat dissipation, the IC is also glued on the housing after cutting a recess on the board. It was measured using the same setup as the previous modules. The measured conversion gain in comparison to the on-wafer measurement is shown in Fig. 8.18 (b). The

[8]The heat is mainly conducted by the RF probe, which has limited contact to the IC.
[9]The measured temperature is not accurate due to the unknown emissivity of the IC.



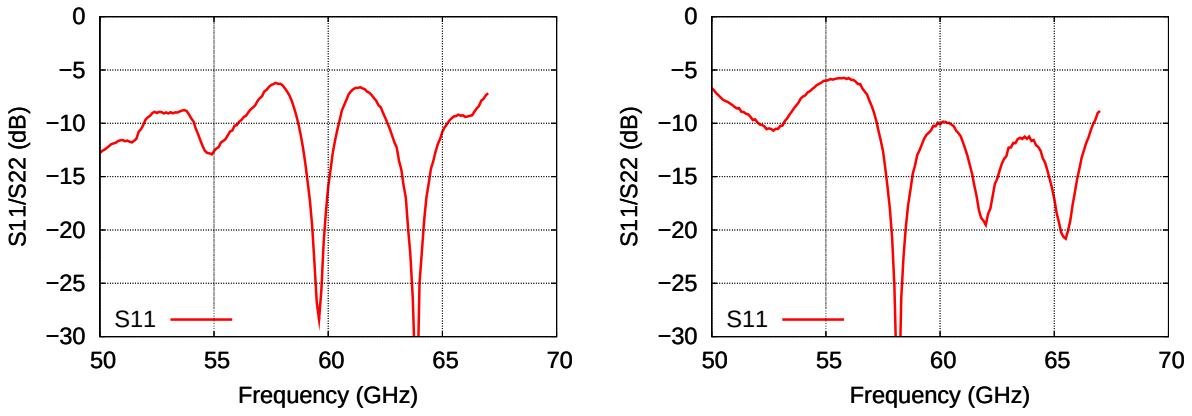
(a) (b)

Figure 8.19: Infrared picture of the module without board recess (a) and with board recess (b). The total DC power consumption is 477 mW (57 mW from LNA). The measured temperature is not accurate due to unknown emissivity of the IC. The emissivity was set to 0.86 for both measurements.

module shows about 2 dB gain and 10 GHz 3 dB-bandwidth, which agrees well with the expectation from the on-wafer measurement results, taking into account the extra off-IC losses. The total DC power consumption is 420 mW.

Input Matching

The input reflection coefficients of the two modules were measured coaxially using the VNA (up to 67 GHz). The measurement results are shown in Fig. 8.20. For the module without LNA, a relatively good matching is achieved, with S11 below -10 dB from 57 GHz to 66.5 GHz. For the module with LNA, the matching is slightly worse, with S11 below -7 dB from 58 GHz to 67 GHz. The relatively poor matching at 61 GHz is because of the bondwire interconnect and the non-perfect input matching of the LNA.

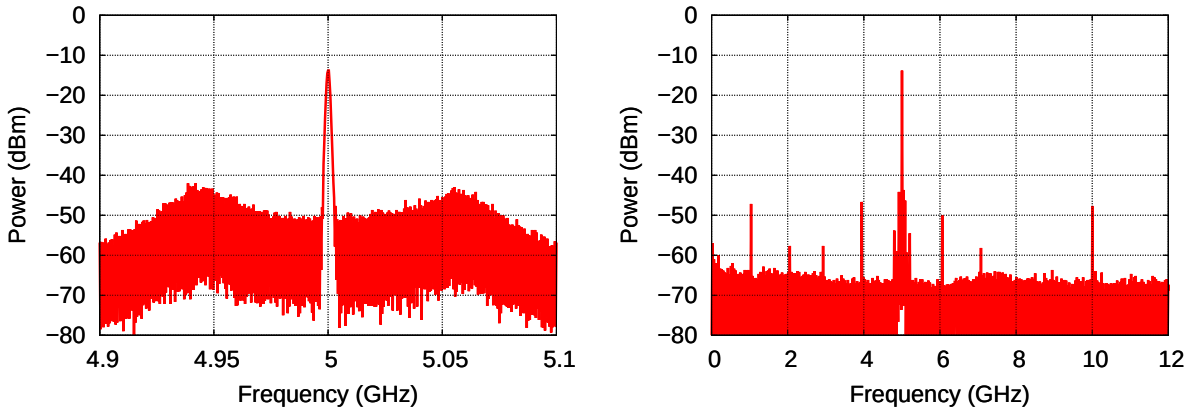


(a) (b)

Figure 8.20: Measured input reflection coefficient of the down-converter module with LNA (a) and without LNA (b).

Spectrum

Fig. 8.21 shows the down-converted IF spectrum with different frequency spans. The LO was at 66.56 GHz (1.04 GHz reference signal) and the RF signal was at 61.56 GHz. The down-converted IF signal has the same reference spur as the LO signal. Furthermore, the second harmonic of the IF signal (at 10 GHz) and the reference signal also appears in the output, due to higher order mixing, non-linearity and unwanted coupling from the reference input to the output. However, these unwanted spectral components are well separated from the IF signal and the power is very low, so the influence is negligible.



(a) (b)

Figure 8.21: Measured IF spectrum at 5 GHz with different span.

Noise Figure

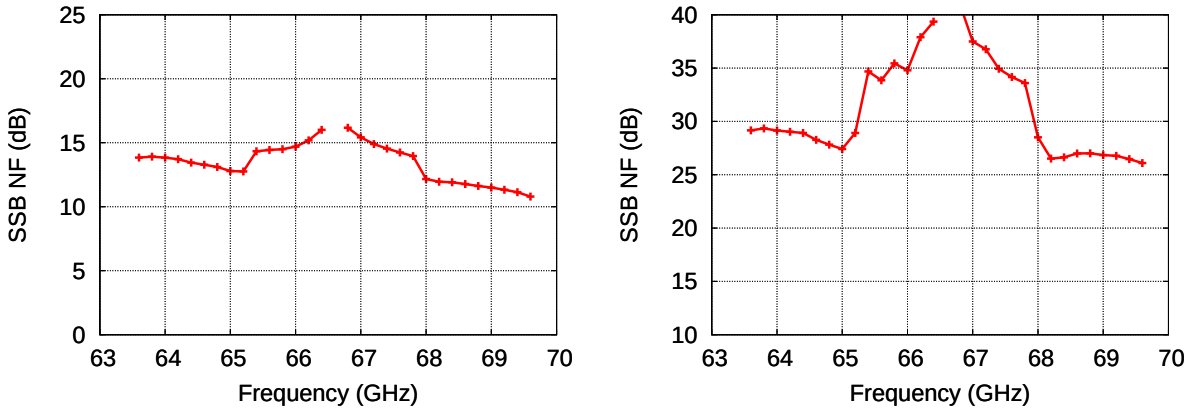
The noise figure of the down-converter modules were measured using a noise figure meter (Agilent N8973A)[10]. The LO was fixed at 66.56 GHz and the RF frequency was swept from 63.6 GHz to 69.6 GHz[11]. During the measurement, the noise source was directly connected to the down-converter without any filter, so noise from both the signal and image band will appear in the output, which led to a 3 dB higher noise figure[12]. Fig. 8.22 shows the measured noise figure of the two modules (with and without LNA). 3 dB should be subtracted to get the real single-side-band noise figure. At very low IF frequencies, the down-converter IC has very high noise figure, due to the current mirrors in the biasing circuit. At the intended operation frequency range, the noise figure of the down-converter module is about 26 dB. The noise figure of the module with LNA is about 11 dB, which agrees well with theoretical calculation[13].

[10]Measurements were performed at Fraunhofer IAF, Freiburg.

[11]Due to the limitation of the instrument, the IF frequency can go only up to 3 GHz.

[12]If the noise from the signal and image band are equal, the output noise power will double, which does not happen in the calibration [66]

[13]LNA has 21 dB gain and 7 dB noise figure. The down-converter has 5 dB gain and 24 dB noise figure. The cascaded noise figure is then 8.5 dB. The off-IC loss is about 2 dB, which makes a total noise figure of 10.5 dB.



(a) (b)

Figure 8.22: Measured single-side-band noise figure of the down-converter module with LNA (a) and without LNA (b).

8.3 Summary and Comparison

Low-cost packaging techniques have been described in this chapter. "L-C-L" compensating structures for differential and single-ended IC-to-board bondwire interconnects were design and tested at different frequencies and very good performance has been achieved. Tab. 8.1 shows a comparison of this thesis work with other state-of-art IC-to-board interconnects.

Table 8.1: Comparison of IC-to-board interconnects

Ref.	**Technique**	**Frequency**	**Insertion Loss**	**3 dB-Bandwidth**
[67] *IMS* 2011	bondwire	120 GHz	1.2 dB	110 GHz - 130 GHz
[68] *IMS* 2010	flip-chip	77 GHz	1 dB	65 GHz - 85 GHz
[69] *IMS* 2010	flip-chip	94 GHz	1.4 dB	-
[70] *IMS* 2007	flip-chip	50 GHz	1.7 dB	DC - 50 GHz
[71] *IMS* 2007	flip-chip	67 GHz	0.5 dB	DC - 67 GHz
This Work	**bondwire**	**60 GHz** **95 GHz**	**0.3 dB** **0.5 dB**	33 GHz - 81 GHz 70 GHz -110 GHz

The "L-C-L" bondwire interconnects achieves comparable low loss to flip-chip solutions. Although the bondwire interconnects have limited bandwidth compared with flip-chip techniques, the relative bandwidth (>16%) is still quite sufficient for most of the applications. The cost and effort required for the bondwire interconnect is also much lower

than that of the flip-chip solution, which is another big advantage, especially for low-cost applications.

Two PLL circuits (33 GHz differential output and 67 GHz single-ended output) have been packaged using the bondwire interconnects, with less than 2 dB power loss compared to the on-wafer measurement. Both PLL modules have very wide frequency tuning ranges, making them very suited as Ka-and V-band signal sources.

Different 60 GHz down-converter modules (with and without LNA) have also been realized and characterized. The modules have 24 dB (with LNA) and 2 dB (without LNA) conversion gain and more than 10 GHz 3 dB IF bandwidth. With a 66 GHz LO signal, the complete 60 GHz ISM band can be down-converted. The modules are successfully implemented in a 60 GHz wireless system and very good performance have been achieved, which will be described in the next chapter.

Chapter 9

60 GHz Wireless Transmission

The realized down-converter modules have been tested in a 60 GHz wireless system. The transmitter consists of a BPSK modulator and a up-converter with 56 GHz LO signal. The BPSK modulator generates a BPSK signal centered at 4.5 GHz, which is then up-converted to 60.5 GHz. The baseband data is a random data stream (PN-31) generated by a FPGA board. The up-converter has a V-connector as RF output, with an output power of 10 dBm. The 60 GHz BPSK signal is transmitted via a V-band horn antenna (20 dB gain). Fig. 9.1 shows the block diagram of the transmitter.

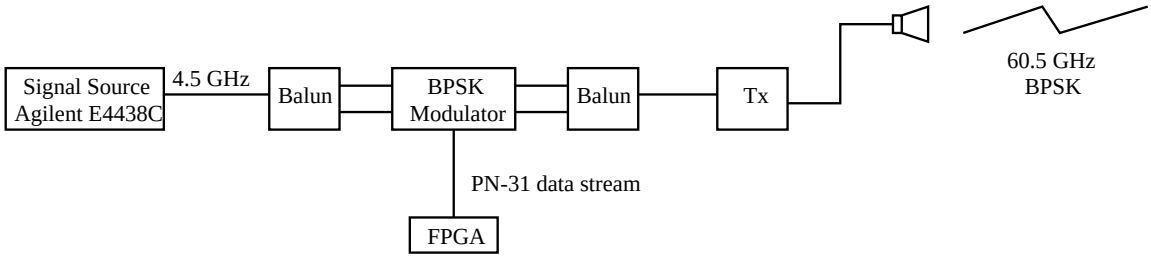


Figure 9.1: Transmitter setup.

The receiver consists of the down-converter (described in Chapter 8) and a BPSK demodulator. The received BPSK signal is first down-converted to an IF of 5.1 GHz. The analog BPSK demodulator takes the IF signal as input and performs analog BPSK demodulation [13]. The down-converted spectrum and the demodulated data stream are monitored using a spectrum analyzer and oscilloscope simultaneously. Fig. 9.2 shows the block diagram of the receiver. A 4×4 patch antenna is connected to the RF input of the down-converter modules to receive the 60 GHz signal. The antenna is realized using the same substrate as the down-converter (Rogers RT Duroid 5880). It has 15 dB gain at 61 GHz, and the gain variation from 58 GHz to 63 GHz is less than 2 dB. The main beam 3 dB bandwidth is about 12 degrees. Fig. 9.2 (b) shows a photo of the down-converter module connected with the antenna.

For the wireless transmission, the transmitter and receiver modules were fixed on an optical rail. As a first step, the horn antenna was fixed on the transmitter. Fig. 9.3 shows a photo of the measurement setup. By proper alignment of the transmitter and

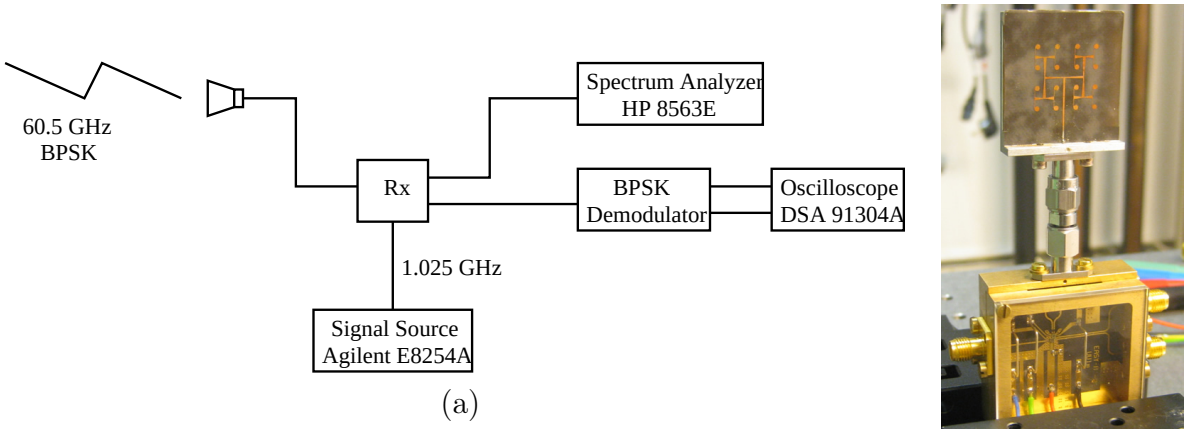


Figure 9.2: (a) Receiver setup. (b) Down-converter module with 4×4 patch antenna.

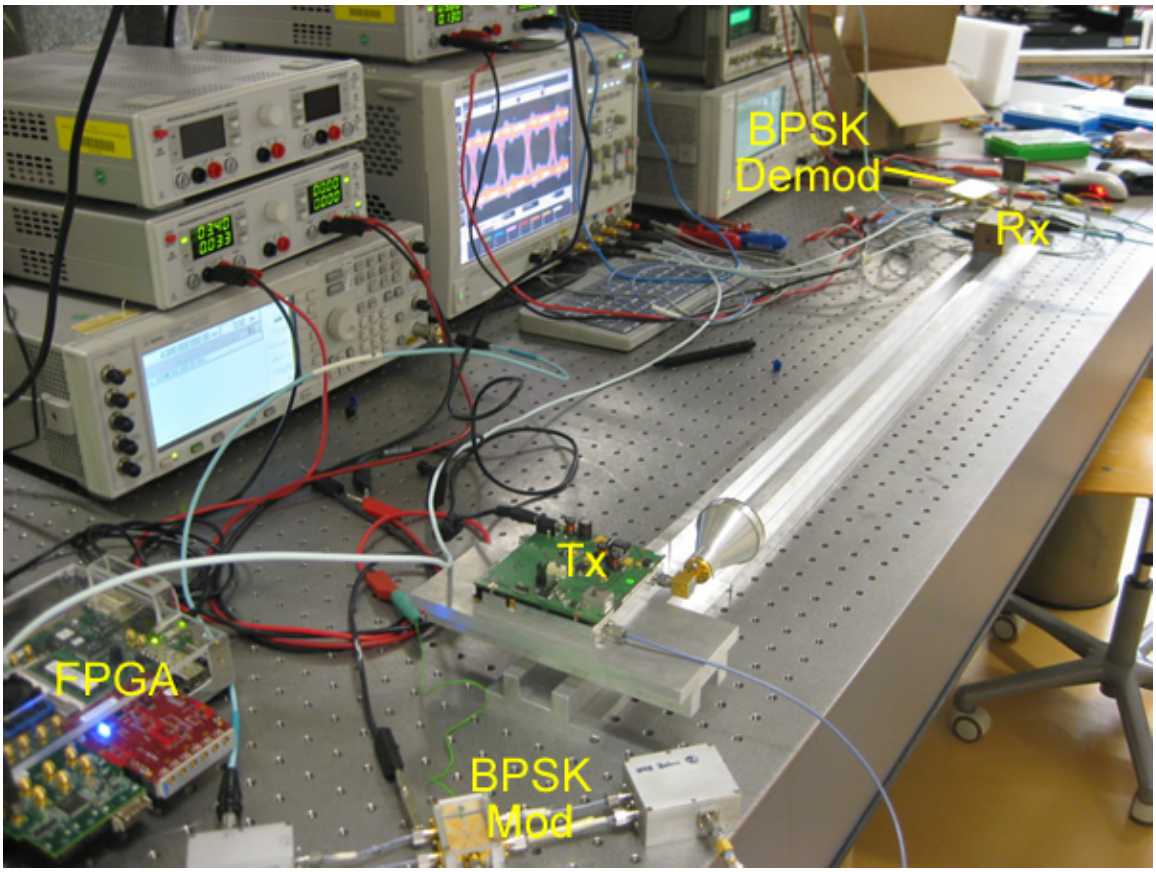


Figure 9.3: Photo of the 60 GHz wireless transmission setup with fixed transmitter antenna.

receiver, a very good transmission could be achieved. After this test, the horn antenna was held by hand and connected to the transmitter through a 1 meter long cable (about 10 dB loss), which is more close to the hand-held scenario in real applications. When the horn antenna was pointed towards the receiver (with angular precision of about ± 10 degrees), robust transmission could be achieved, even when the person held the antenna and moved the antenna back and forth continuously. Fig. 9.4 shows a photo of the hand-held measurement scenario.

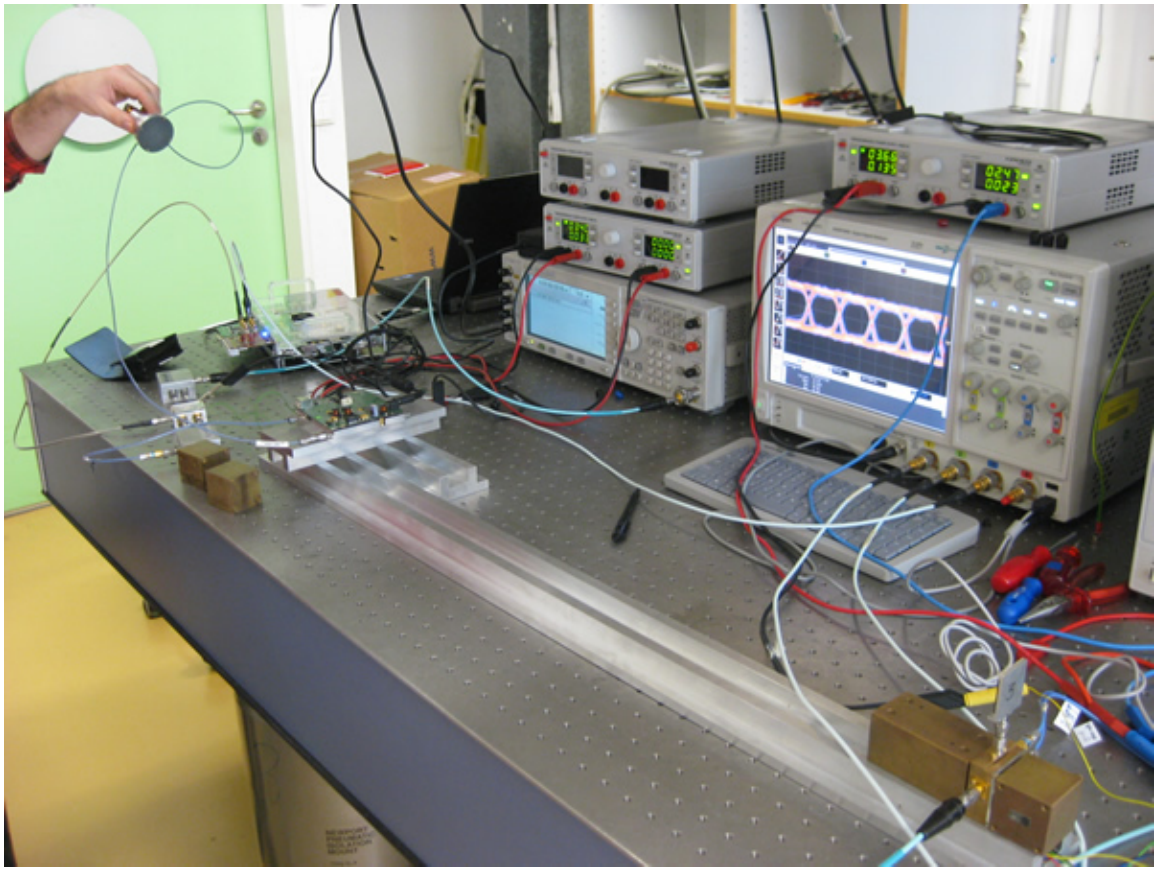


Figure 9.4: Photo of the 60 GHz wireless transmission setup with hand-held transmitter antenna.

As described in Chapter 2, for short range transmission, the LNA in the down-converter module is not necessary. Therefore, the down-converter module without LNA was first used in the system. For both the fixed antenna and hand-held antenna scenarios, error-free transmission could be achieved. Fig. 9.5 (a) and (b) shows the down-converted spectrum for 1 Gbit/s and 2 Gbit/s BPSK transmission over 1 meter distance, which shows that the frequency response of the transmitter and receiver is quite flat. Because of the limited bandwidth of the transmitter (4 GHz RF bandwidth, at around 60 GHz), higher data rate can not be tested. The power of the down-converted signal is about -20 dBm. Fig. 9.5 (c) and (d) shows the measured eye diagram of the demodulated data, which shows clear error-free transmission. The 1 meter distance is mainly limited by the measurement setup (optical rail). With hand-held antenna, the distance can be further increased, but pointing of the antenna becomes more difficult. At 1 meter distance, the SNR of the down-converted signal is about 22 dB. Taking 16 dB as the accepted SNR,

the maximum transmission distance is about 2 meters.

The down-converter module with LNA was also tested in the same setup. At 1 meter distance (with fixed antenna), the power at the receiver is too high and saturates the LNA. Therefore, the antenna was not pointed directly to the receiver to reduce the signal power. Fig. 9.6 (a) and (b) shows the down-converted spectrum with 1 Gbit/s and 2 Gbit/s data rate. Fig. 9.6 (c) and (d) shows the measured eye diagrams. For the module with LNA, the transmission distance can be much further. The distance was increased to 2.2 meters, with hand-held antenna, and error-free transmission could be achieved. Further distance could not be tested, due to the limitation of the setup. The module with LNA has 20 dB more gain and 15 dB less NF than the module without LNA, so the maximum transmission distance is about 64 times further (about 128 m), to achieve the same SNR at the receiver.

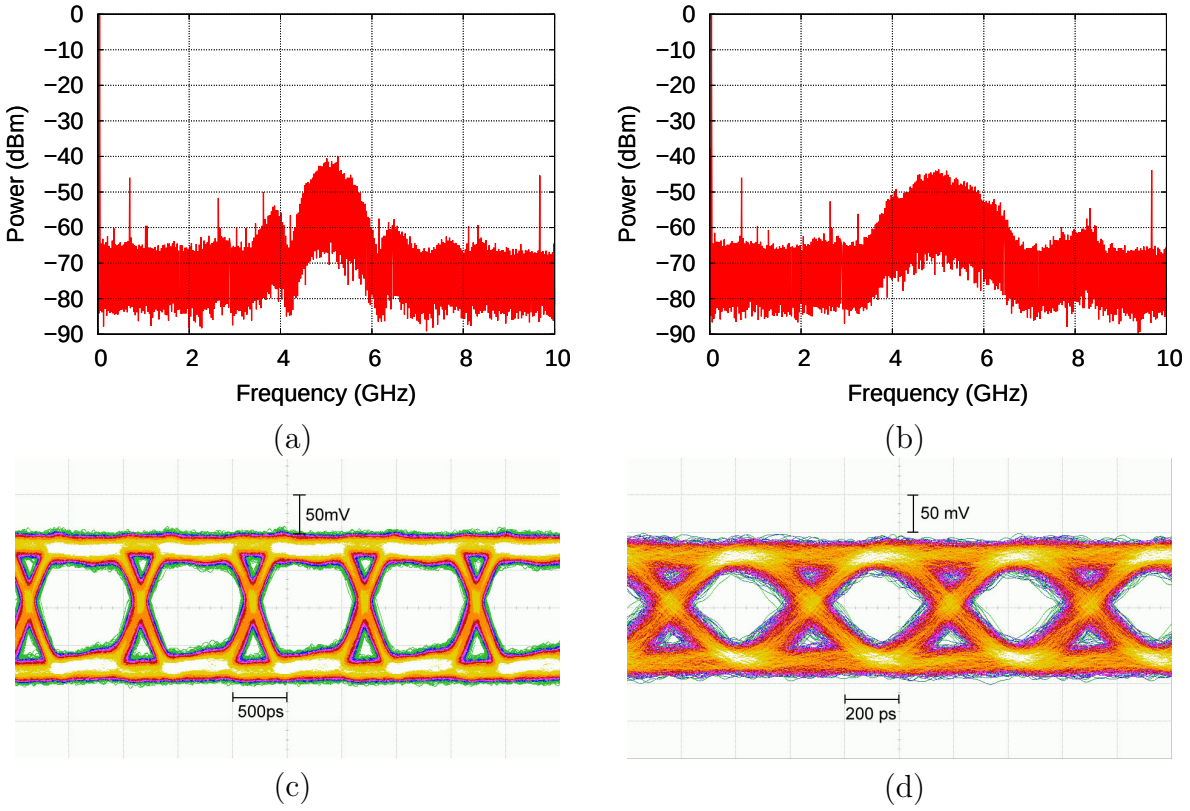


Figure 9.5: Down-converted BPSK spectrum (a) (b) and eye diagram of the demodulated data (c) (d) at a transmission distance of 1 meter, using the down-converter module without LNA. (a) (c) are with 1 Gbit/s data and (b) (d) are with 2 Gbit/s data rate.

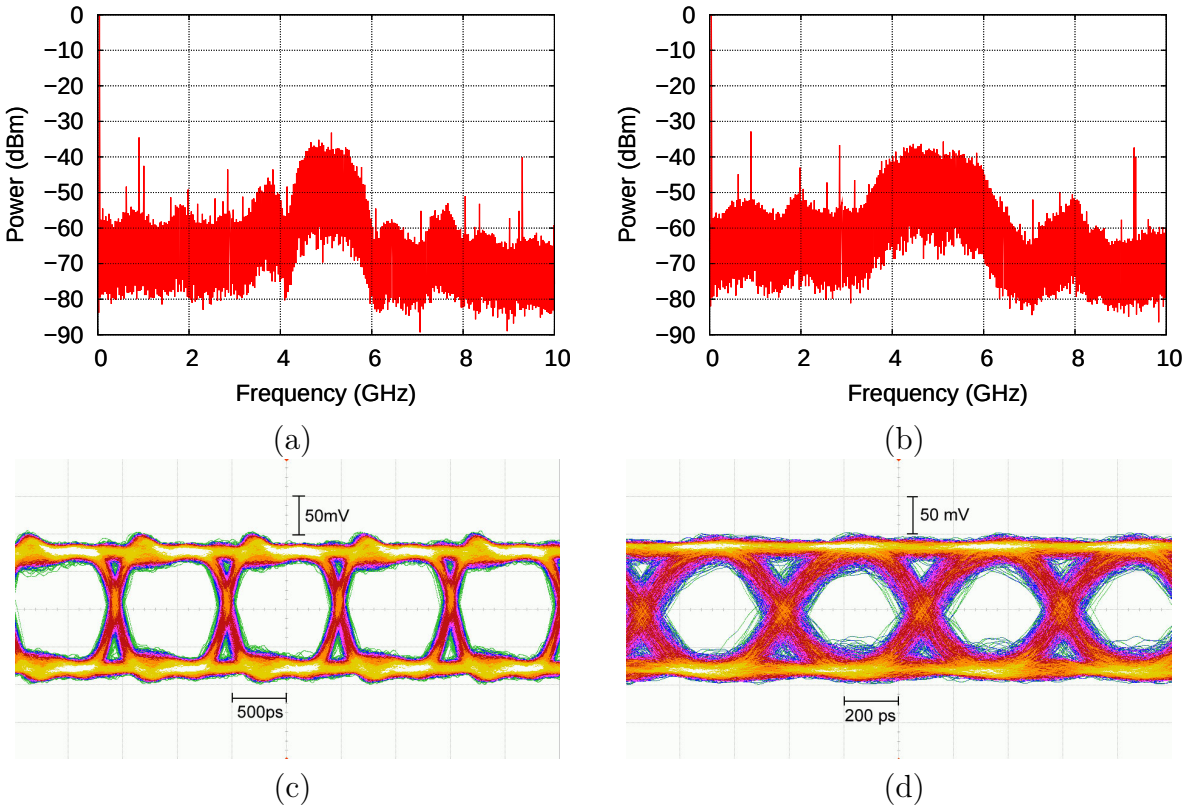


Figure 9.6: Down-converted BPSK spectrum (a) (b) and eye diagram of the demodulated data (c) (d) at a transmission distance of 1 meter, using the down-converter module with LNA. The transmitter antenna is not pointed directly towards the receiver to reduce the received power at the receiver. (a) (c) are with 1 Gbit/s data and (b) (d) are with 2 Gbit/s data rate.

Summary

This chapter shows the high data-rate 60 GHz wireless transmission using available transmitter and the down-converter modules realized in this thesis work. It is experimentally shown that at a distance of 1 meter, error-free transmission with up to 2 Gbit/s data rate (limited by the transmitter) can be achieved with a down-converter IC that is fully integrated in an 80 GHz SiGe HBT technology, enabling low-cost solutions for short-range, high data-rate wireless transmission at 60 GHz. This is also the first 60 GHz receiver front-end, realized using such a low-cost semiconductor technology.

Chapter 10

Conclusion

A 60 GHz receiver front-end for multi-gigabit wireless transmission has been realized in this thesis work, using low cost semiconductor technology and packaging techniques. The design and characterization of the key building blocks (mixer, VCO, frequency doubler, frequency divider, PLL) and the fully integrated circuits, as well as the packaged modules were presented in this thesis.

The key feature of the down-converting mixer is the wide IF bandwidth, which is achieved through a transimpedance load. The 10 GHz IF bandwidth covers the complete 60 GHz ISM band, and is the widest bandwidth among reported 60 GHz receivers, making it very suited for broadband applications.

A VCO plus frequency doubler approach was adopted for the LO signal generation. The VCO achieves state-of-art wide tuning range with high output power and low phase noise. After frequency doubling, signal generation up to 86 GHz (close to f_{max}) with relatively high output power (-2 dBm at 81 GHz) has been realized, which is also much higher than other reported signal generation circuits at frequencies close to f_{max}.

Static and dynamic frequency dividers were characterized for use in the PLL. The maximum operating frequency of these dividers were analyzed and design guidelines were discussed. Based on the guidelines, both types of dividers achieve state-of-art speed (relative to f_T/f_{max}), which is also better than previously published dividers realized in the same technology.

The realized analog PLL achieves the widest frequency locking range and lowest phase noise among the reported millimeter-wave PLLs reported to date.

The complete down-converter IC is realized in an 80 GHz SiGe HBT technology, with a relatively low DC power consumption of 434mW. It is also the first 60 GHz down-converter realized using such a low-cost semiconductor technology.

The fully-integrated down-converter IC was packaged in modules using low-cost carrier substrate and wire bonding techniques. "L-C-L" compensating structures, which reduce the influence of the bondwires, were designed and characterized at different frequencies.

The bondwire interconnects achieve comparably low insertion loss as the state-of-art flip-chip interconnects and require much less effort, making it very suited for millimeter-wave packaging and module design.

The realized front-end modules have been tested in a 60 GHz wireless system with analog BPSK demodulation. Error-free transmissions over a distance of 1 meter with fixed antenna (limited by measurement setup), and 2.2 meters with hand-held antenna (limited by measurement setup) have been shown. Furthermore, the feasibility of a 60 GHz receiver front-end without LNA has been demonstrated, enabling a really low-cost solution for short-range, ultra-high data-rate wireless transmissions.

The input and output matching of the down-converter is not very good in the current design and can be improved for future work. The antenna and the IC can also be integrated on the same board, eliminating the V-connector and decreasing the system NF. LNAs can be integrated at the IF output to increase the total conversion gain.

Appendix A

TFML

The thin-film microstrip lines (TFML) are used in the VCO design as inductors and matching networks. The line is formed by the top and bottom metal layers, as shown in Fig. A.1. The minimum line width of 3 μm is used for the signal line to have the highest possible characteristic impedance and therefore highest unit inductance. The characteristic impedance is about 65 Ω.

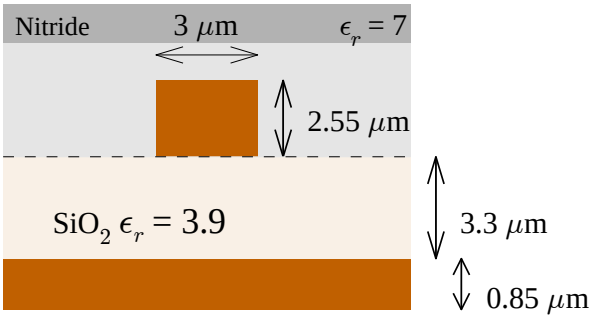


Figure A.1: Cross section of the thin-film microstrip line.

To ease the design, a length-scalable model of the TFML has been built. The model is a lumped-element Π model [2], as shown in Fig. A.2. To represent the distributed nature of the line, the lumped elements are split into 10 stages. This also solves the problem caused by the self resonance of the Π model.

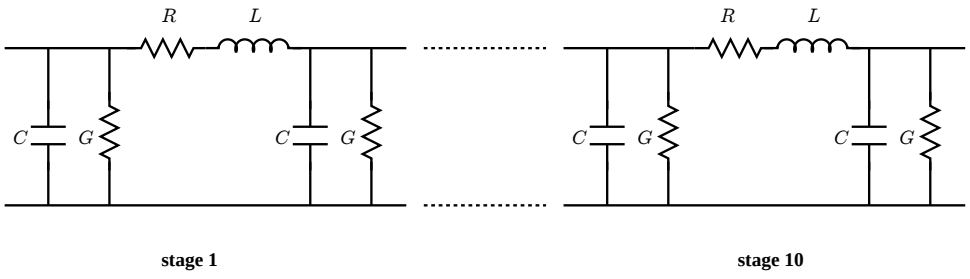


Figure A.2: Distributed lumped-element Π model of the TFML.

The lumped elements can be extracted from the Y-parameter of the TFML. According to the definition of Y-parameter and the equivalent model shown in Fig. A.3,

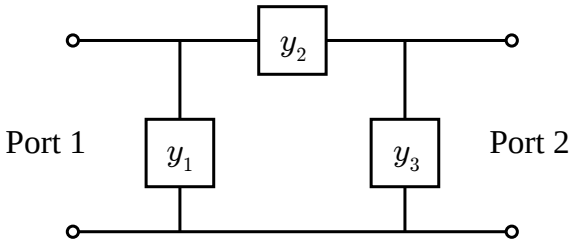


Figure A.3: Equivalent lumped-element Π model of the TFML.

$$Y_{11} = \left.\frac{I_1}{U_1}\right|_{U_2=0} = y_1 + y_2 \tag{A.1}$$

$$Y_{12} = \left.\frac{I_1}{U_2}\right|_{U_1=0} = -y_2 \tag{A.2}$$

$$Y_{21} = \left.\frac{I_2}{U_1}\right|_{U_2=0} = -y_2 \tag{A.3}$$

$$Y_{22} = \left.\frac{I_1}{U_2}\right|_{U_1=0} = y_3 + y_2 \tag{A.4}$$

Solving for y_1,y_2 and y_3 gives

$$y_1 = Y_{11} + Y_{12} \tag{A.5}$$

$$y_2 = -Y_{12} \tag{A.6}$$

$$y_3 = Y_{22} + Y_{21} \tag{A.7}$$

Since

$$y_2 = \frac{1}{R + j\omega l} \tag{A.8}$$

$$R = -\Re\left(\frac{1}{y_2}\right) \tag{A.9}$$

$$L = \Im\left(\frac{1}{\omega y_2}\right) \tag{A.10}$$

G and C can be extracted from both y_1 and y_3. Due to the symmetry, y_1 should be equal to the y_3. So

$$G = \Re\left(Y_{11} + Y_{12}\right) \tag{A.11}$$

$$C = \Im\left(\frac{Y_{11} + Y_{12}}{\omega}\right) \tag{A.12}$$

In this thesis work, the TFML is simulated using a EM simulation tool (Momentum). The simulated S-parameter is converted to Y-parameter and the lumped elements are

extracted based on the above equations. Fig. A.4 (extracted) shows the extracted lumped elements per unit length.

The R, L, G, C are defined as following in the model of a TFMSL with length l:

$$R = lR_0\sqrt{1+\frac{f}{F_0}} \tag{A.13}$$

$$L = (L_0 - S_L f)\, l \tag{A.14}$$

$$C = (C_0 + S_C)\,\frac{l}{2} \tag{A.15}$$

$$G = (G_0 + S_G)\,\frac{l}{2} \tag{A.16}$$

$R_0, F_0, L_0, S_L, C_0, S_C, G_0, S_G$ are constants. These values are chosen to fit R, L,C and G to the parameters extracted from the EM simulation. The fitted curve are also shown in Fig. A.4. Very good agreement between the model and the EM simulation results has been achieved.

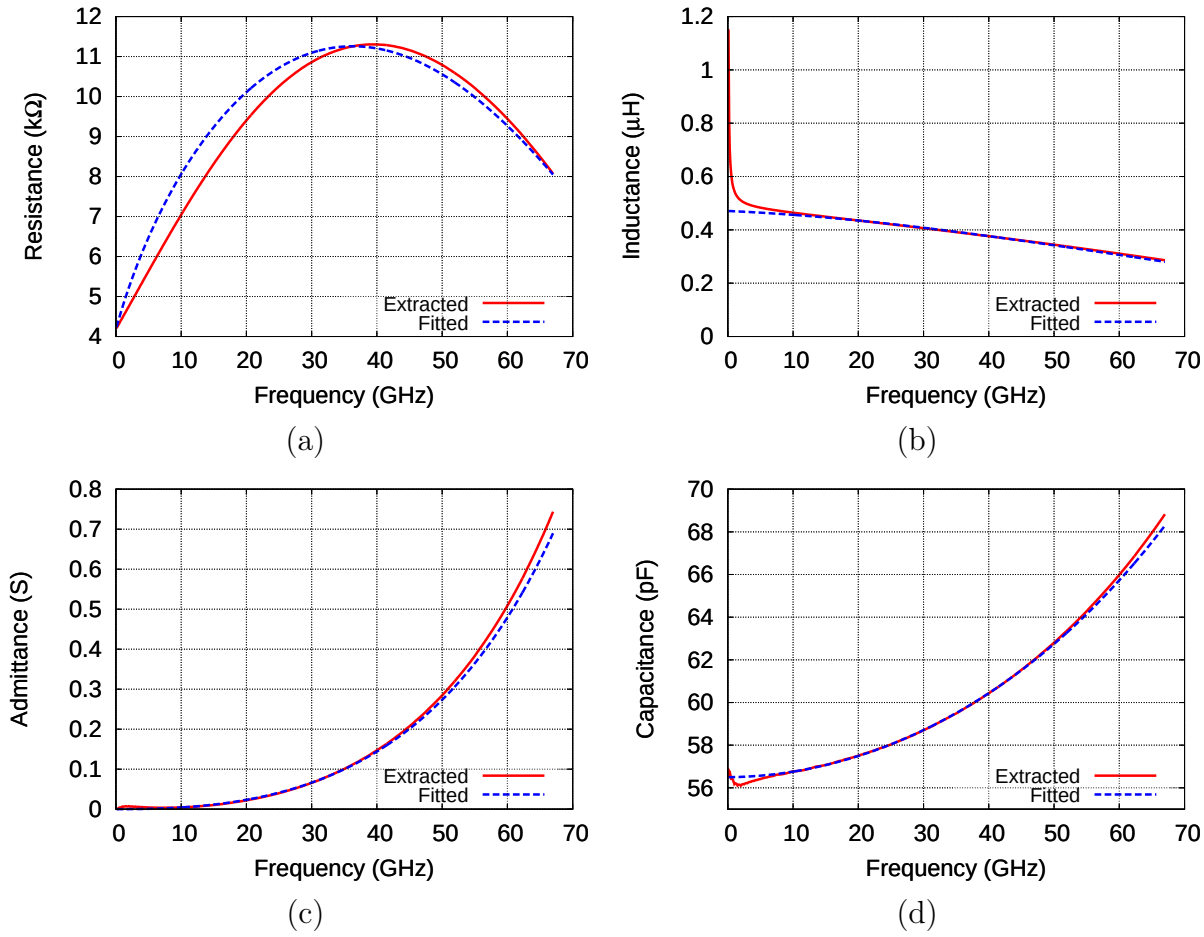


Figure A.4: Extracted and fitted lumped elements of the TFML.

Fig. A.5 shows the comparison between the model and the EM simulation.

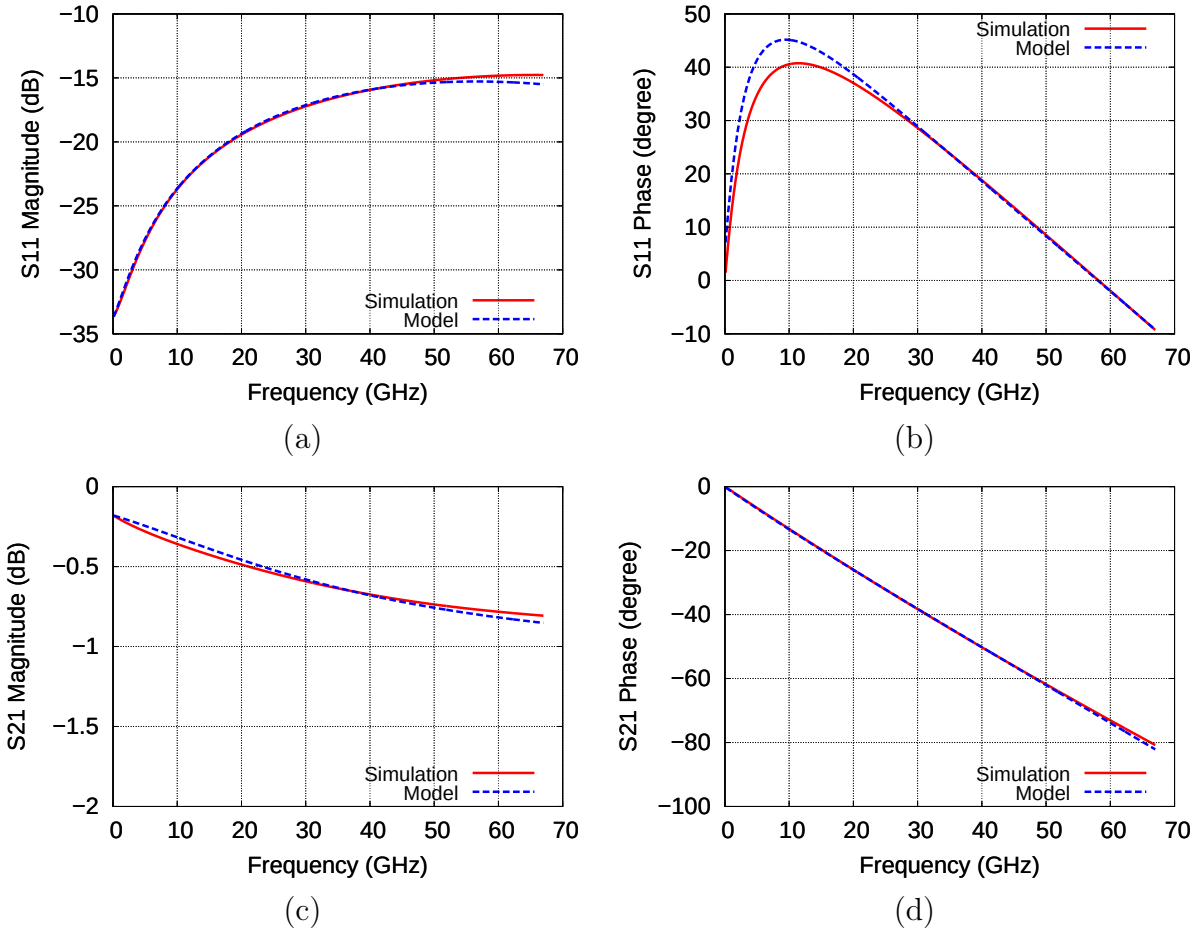


Figure A.5: Comparison of the model and EM simulation.

Appendix B

Colpitts VCO Simulation

The input impedance looking into the base of Q_1 (Fig. 4.2, page 25) is calculated in Chapter 4 (Equation 4.1, page 24), based on the simplest small signal equivalent circuit model of the transistor. This can explain the generation of negative impedance, but can not explain the change of the negative resistance versus frequency, because the base-collector capacitance, which strongly influences the negative resistance, especially at higher frequencies, is not included in the transistor model. In this appendix, the influence of the base-collector capacitor on the input impedance of the colpitts VCO is simulated.

The simulation has been done using the s-parameter simulation, base on a simplified small signal equivalent circuit model of the HBT, as shown in Fig. B.1. The transistor parameters are estimated from the transistor model. R_b is about 12 Ω. r_π is 400 Ω. The voltage controlled current source (VCCS) has an infinite input impedance ($R_1 = 1$ MΩ) and zero output impedance ($R_2 = 0$). The admittance of the VCCS is 0.1 S, to represent the transconductance (g_m) of the transistor (at 30 GHz). C_π is 300 fF and C_3 is 35 fF. For simplicity, the collector is terminated with a transmission line ($L_2 = 120$ μm). Capacitor C_2 represent the varactor diode. L_1 is 800 μm, as in the VCO circuit.

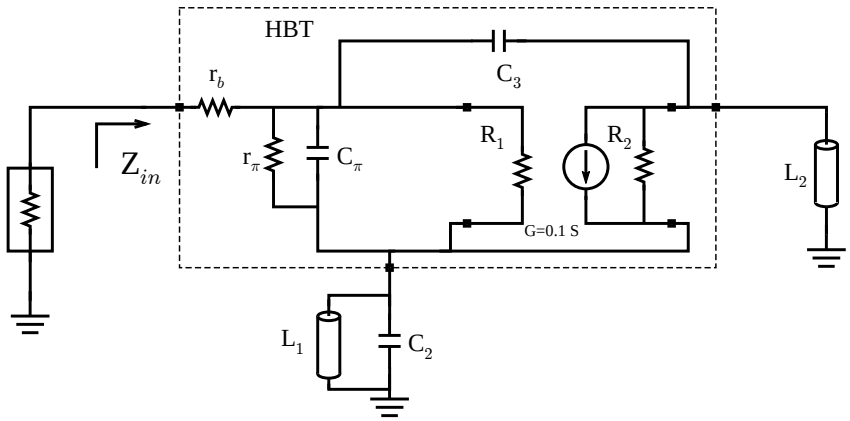
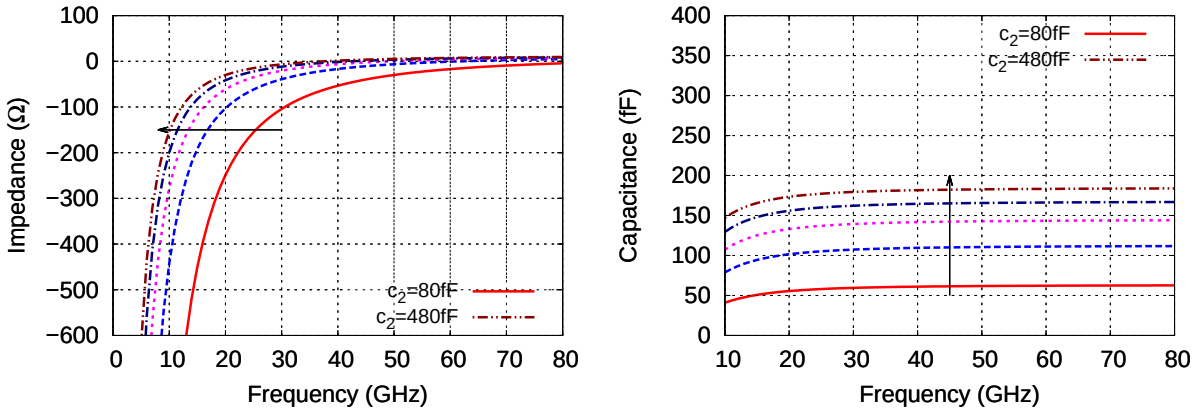


Figure B.1: Small signal equivalent circuits of the Colpitts VCO for negative impedance simulation.

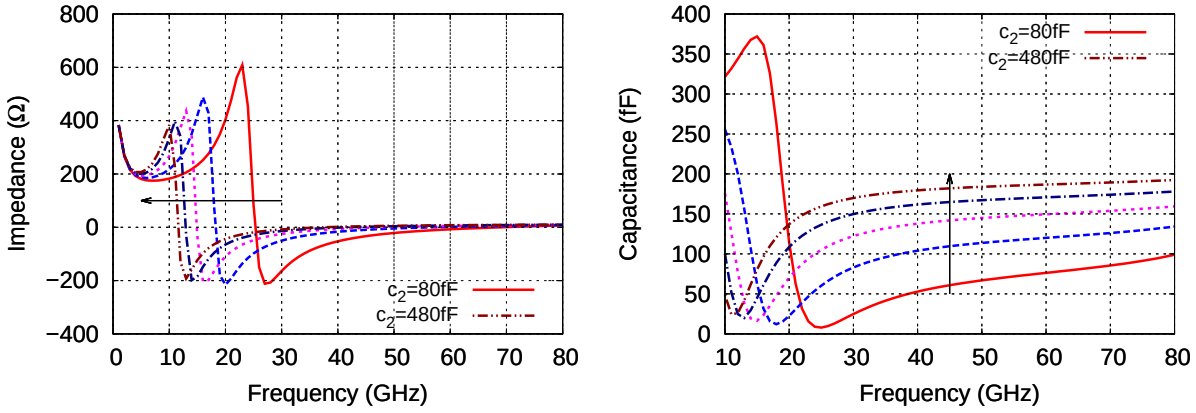
The input impedance is first simulated without L_1 and C_3. Fig. B.2 shows the simulated resistance and equivalent capacitance looking into the base of the transistor, when C_2 is swept from 80 fF to 480 fF in 100fF steps. The resistance is negative and increases with increasing frequency, as calculated using Equation 4.1. The equivalent capacitance also equals the series of C_π and C_2.



(a) (b)

Figure B.2: Simulated resistance and equivalent capacitance looking into the base without L_1 and C_3. The capacitor C_2 is swept from 80 fF to 480 fF in 100fF steps.

As a second step, the inductor L_1 is added in the simulation. Fig. B.3 shows the simulated resistance and equivalent capacitance. A resonance in the resistance is observed. The resistance becomes positive below the resonance frequency of L_1 and C_2, where the combination of both becomes inductive. Also, the equivalent capacitance is slightly dependent on frequency, as shown in Fig. B.3 (b).

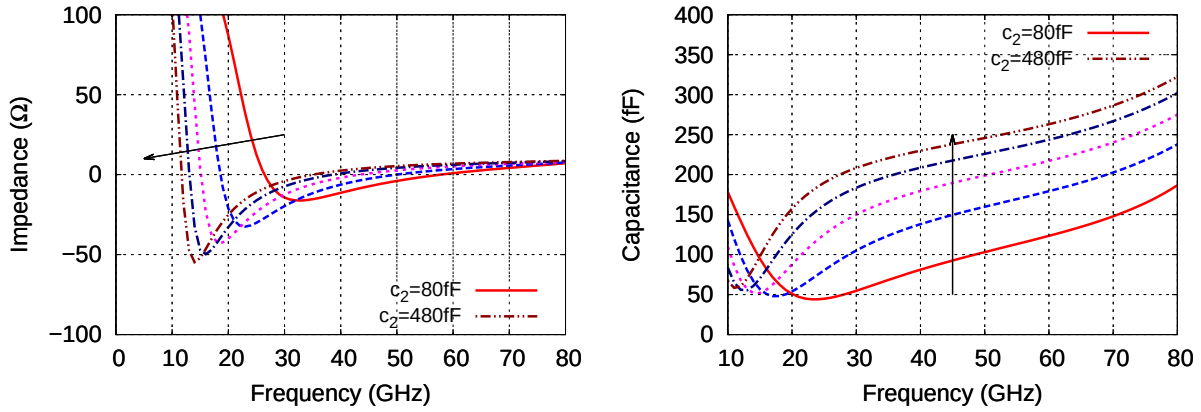


(a) (b)

Figure B.3: Simulated resistance and equivalent capacitance looking into the base with L_1. The capacitor C_2 is swept from 80 fF to 480 fF in 100fF steps.

As the last step, the base-collector capacitor (C_3) is also included in the simulation. Fig. B.3 shows the simulated resistance and equivalent capacitance. Different from Fig. B.3 (a), the negative resistance becomes smaller as C_2 decreases. This is because

of the transistor gain decrease, caused by the feedback capacitor. Also, the equivalent capacitance is increased and becomes more dependent on frequency.



(a) (b)

Figure B.4: Simulated resistance and equivalent capacitance looking into the base with L_1 and C_3. The capacitor C_2 is swept from 80 fF to 480 fF in 100fF steps.

Appendix C

Circuit Details

C.1 Mixer

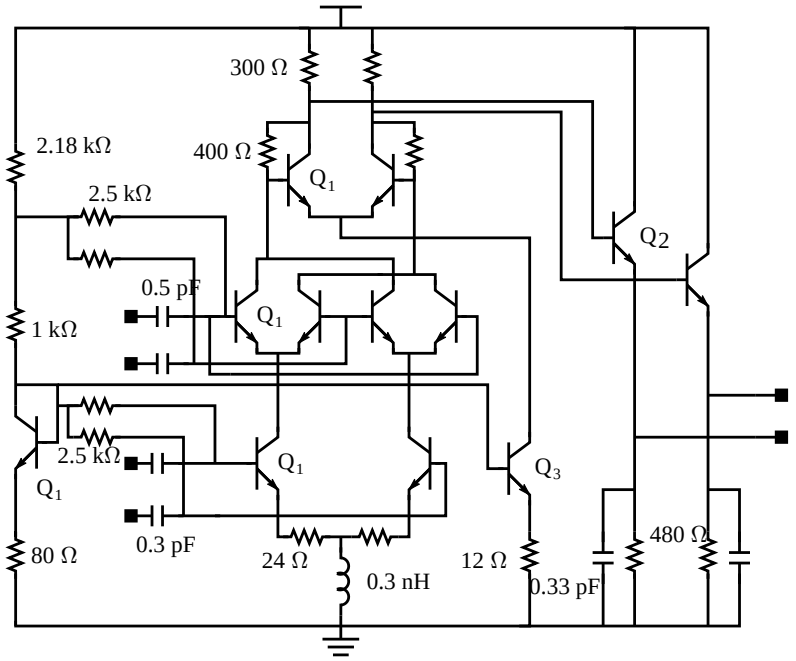


Figure C.1: Full schematic of the down-converting mixer. Q_1: 0.5 $\times$5 μm^2. Q_2: 0.5 $\times$30 μm^2. Q_3: 0.5 $\times$10 μm^2.

C.2 VCO & Doubler

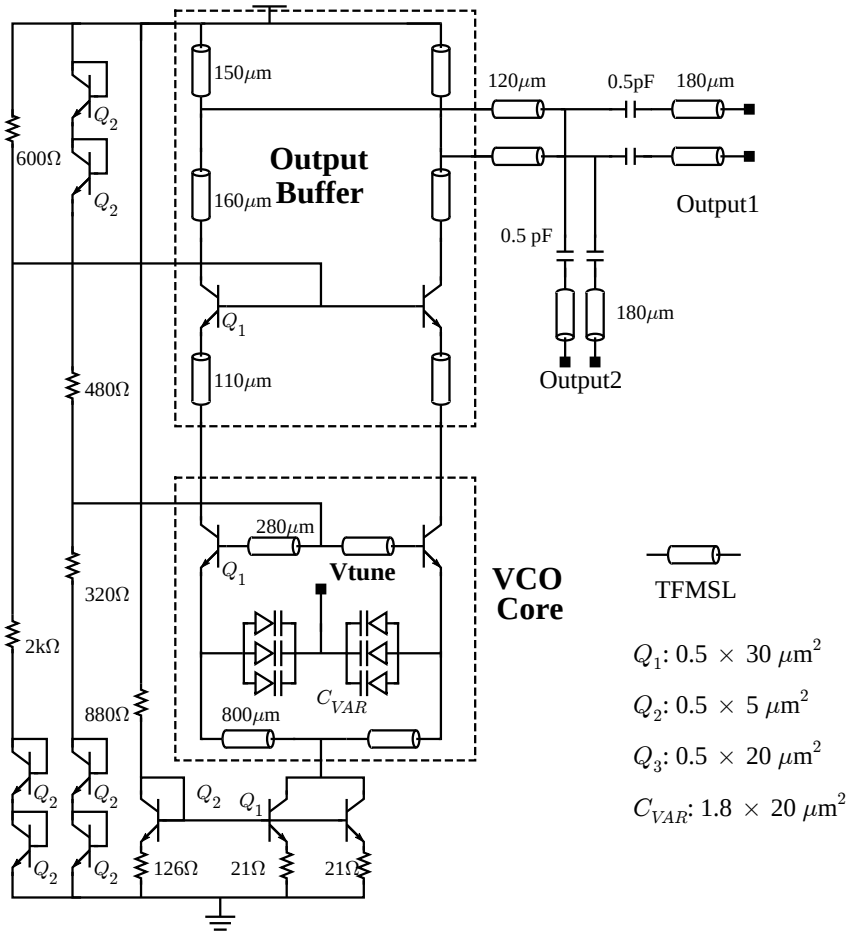


Figure C.2: Full schematic of the VCO with common base output buffer.

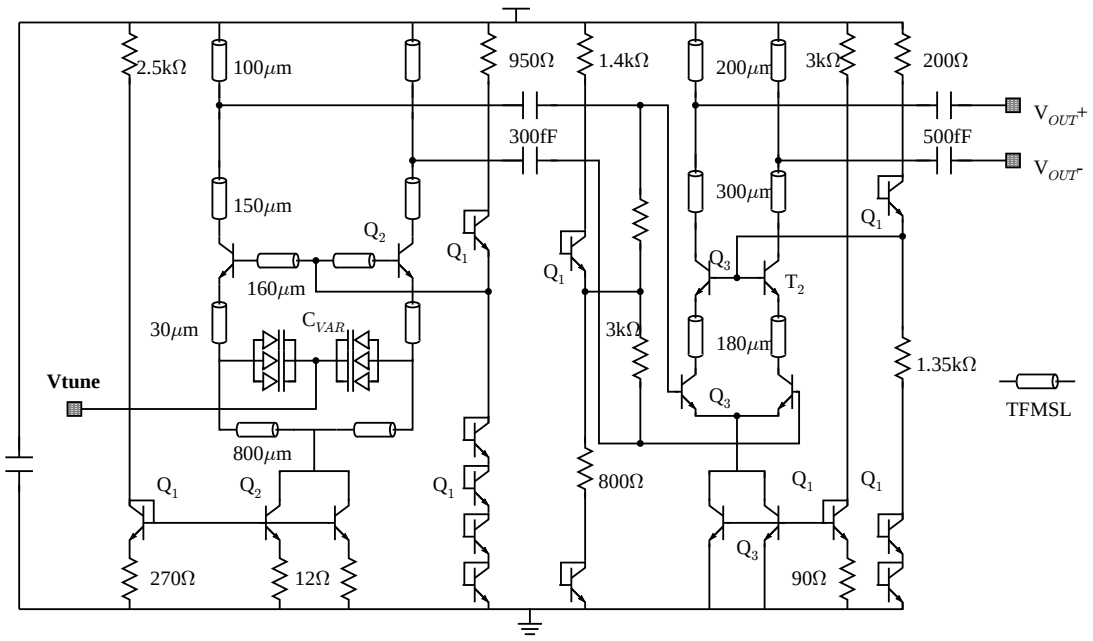


Figure C.3: Full schematic of the VCO with cascode amplifier buffer. Q_1: 0.5 $\times$5 μm^2. Q_2: 0.5 $\times$30 μm^2. Q_3: 0.5 $\times$20 μm^2. C_{VAR}: 1.8 $\times$20 μm^2.

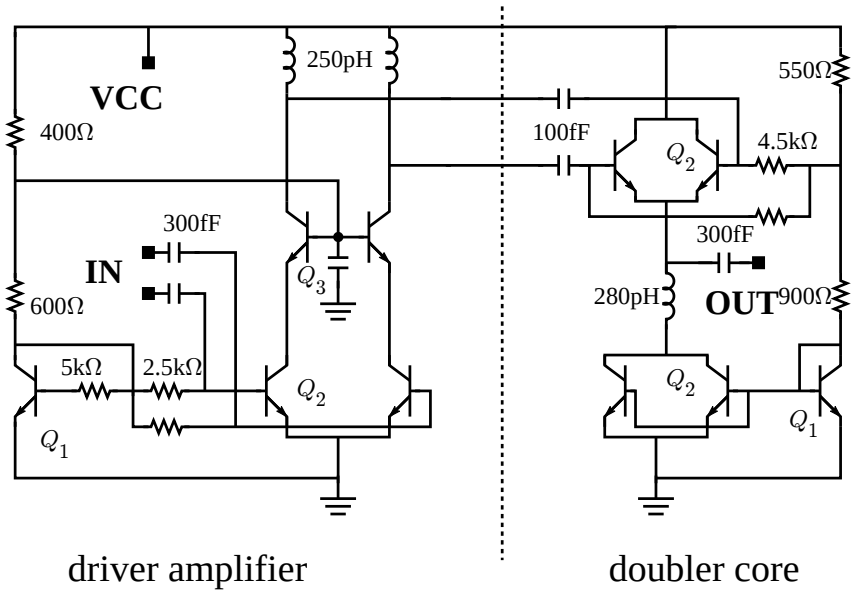


Figure C.4: Full schematic of the push-push doubler with driver amplifier. Q_1: 0.5 $\times$5 μm^2. Q_2: 0.5 $\times$20 μm^2. Q_3: 0.5 $\times$10 μm^2.

C.3 Frequency divider

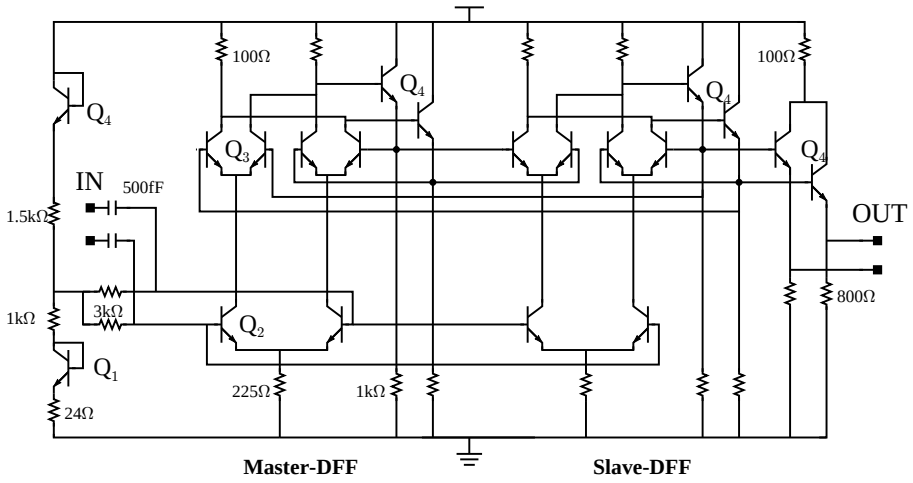


Figure C.5: Full schematic of the static divider. Q_1: 0.5 $\times$1.1 μm^2. Q_2: 0.5 $\times$1.7 μm^2. Q_3: 0.5 $\times$2 μm^2. Q_4: 0.5 $\times$5 μm^2.

C.4 PD and LF

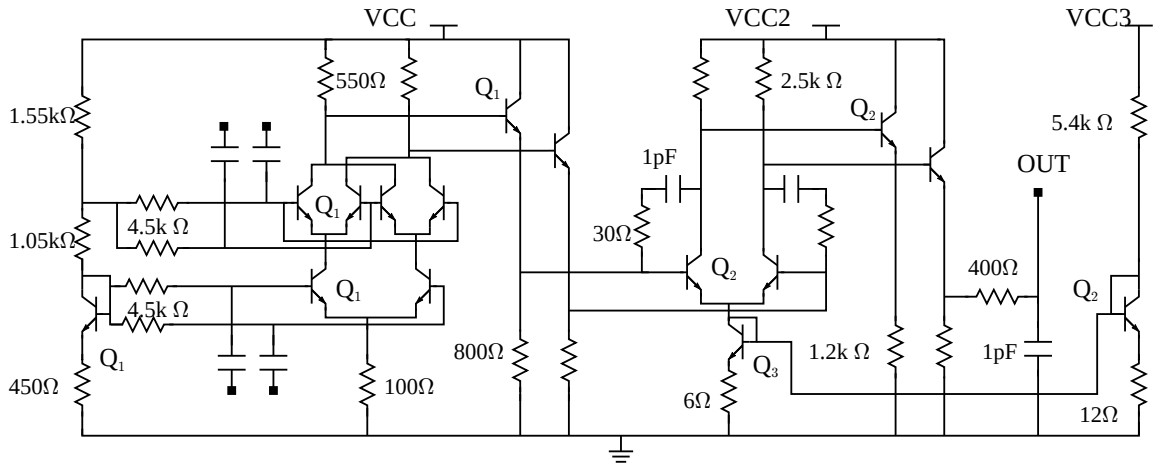


Figure C.6: Full schematic of the phase detector and active loop filter. Q_1: SIC, 0.5 $\times$5 μm^2. Q_2: non-SIC, 0.5 $\times$5 μm^2, Q_3: non-SIC, 0.5 $\times$10 μm^2.

Appendix D

Acronyms and Symbols

D.1 List of Acronyms

ISM	Industrial, scientific and medical
EIRP	Equivalent isotropically radiated power
OOK	On-off keying
BPSK	Binary phase-shift keying
QPSK	Quadrature phase-shift keying
HDTV	High-definition television
WLAN	Wireless local area network
EASY-A	Enablers for ambient services & systems, part A
IC	Integrated circuit
mHEMT	Metamorphic high electron mobility transistor
SiGe	Silicon gemenium
CMOS	Complementary metal-oxide-semiconductor
HBT	Heterojunction bipolar transistor
MIM	Metal-insulator-metal
TFML	Thin-film-microstripline
MIMO	Multiple input multiple output
ADC	Analog to digital converter
LOS	Line of sight
BER	Bit error rate
AWGN	Additive white Gaussian noise
SNR	Signal to noise ratio
NF	Noise figure
LO	Local Oscillator
VCO	Voltage controlled oscillator
PLL	Phase locked loop
FD	Frequency Divider
PD	Phase Detector

LF	Loop Filter
CEP	Common Emitter Pair
SSB	Single Side Band
CEP	Common-Emitter-Pair
MS-DFF	Master-Slave D Flip-Flop
ECL	Emitter-Coupled-Logic
PFD	Phase-Frequency Detector
CP	Charge Pump

D.2 List of Symbols

f_T	Transit frequency
f_{max}	Maximum oscillation frequency
P_{tx}	Tx power
G_{tx}	Tx antenna gain
L_{path}	Path loss @ 1 meter
G_{rx}	Rx antenna gain
L_{mis}	Polarization mismatch & misalignment loss
L_{AFE}	Analog front end implementation loss
BW	Signal bandwidth
P_{noise}	Noise power at Rx
$NF_{receiver}$	Receiver noise figure
BV_{CEO}	Collector-emitter breakdown voltage
VCE	Collector-emitter biasing voltage
V_{out}	Output voltage
I_{EE}	Emitter current
V_T	Thermal voltage
A_0	Open-loop DC voltage gain
R_G	Source impedance
R_F	Feedback resistance
ω_0	Cutoff frequency
Z_{in}	Input impedance
f_{LO}	LO frequency
v_{in}	Input voltage
i_{in}	Input current
g_m	Transconductance
C_π	Base-emitter junction capacitance
L_B	Base inductor
L_E	Emitter inductor
L_C	Collector inductor
L_M	Matching inductor
I_{max}	Biasing current for maximum f_T/f_{max}
C_{VAR}	Varactor Diode

C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
$\Delta\omega$	Frequency offset
f_c	Cutoff frequency for low-frequency noise
K_0	VCO gain
τ_D	Propagation delay
τ_F	Transistor forward transit time
R_B	Base resistance
C_{JC}	Base-collector junction capacitance
C_{JE}	Base-emitter junction capacitance
C_{JS}	Collector-substrate junction capacitance
C_D	Base-emitter diffusion capacitance
f_{osc}	Oscillation frequency
f_{in}	Input frequency
$\Delta\phi$	Phase difference
ΔV	Voltage difference
K_D	Phase detector gain
K_V	VCO gain
Φ_{in}	Input phase
Φ_{out}	Output phase
ϵ_r	Relative permittivity

Bibliography

[1] E. Grass, K.T.-Helmrich, C.-S. Choi, F. Winkler, T. Ohlemüller and R. Kraemer, "Communication systems operating in the 60 GHz ISM band: Overview," *International Journal of Microwave and Wireless Technologies*, vol. 3, Special Issue 02, 2011.

[2] D.M. Pozar, "Microwave Engineering (Second Edition)," John Wiley & Sons., 1998.

[3] H.M. Cheema, R. Mahmoudi and Arthur H.M. van Roermund, "60-GHz CMOS Phase-Locked Loops," Springer Science+business Media B.V, 2010.

[4] http://www.easy-a.de/

[5] S.E. Gunnarsson, C. Kärnfelt, H. Zirath, R. Kozhuharov, D. Kuylenstierna, A. Alping and C. Fager, "Highly integrated 60 GHz transmitter and receiver MMICs in a GaAs pHEMT technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2174-2186, Nov. 2005.

[6] S.E. Gunnarsson, C. Kärnfelt, H. Zirath, R. Kozhuharov, D. Kuylenstierna, C. Fager, M. Ferndahl, B. Hansson, A. Alping and P. Hallbjörner, "60 GHz Single-Chip Front-End MMICs and Systems for Multi-Gb/s Wireless," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1143-1157, May. 2007.

[7] Y. Sun, S. Glisic and F. Herzel, "A Fully Differential 60 GHz Receiver Front-End with Integrated PLL in SiGe:C BiCMOS," *European Microwave Integrated Circuits Conference*, pp. 198-201, Manchester, 10-15 Sep. 2006.

[8] S.K. Reynolds, B.A. Floyd, U.R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher and M. Soyuer, "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2820-2831, Dec. 2006.

[9] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi and I. Seto, "A 60-GHz CMOS Receiver Front-End With Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 1030-1037, Apr. 2008.

[10] Y. Katayama, C. Haymes, D. Nakano, T. Beukema, B. Floyd, S. Reynolds, U. Pfeiffer, B. Gaucher, and K. Schleupen, "2-Gbps Uncompressed HDTV Transmission over 60-GHz SiGe Radio Link," *IEEE Consumer Communications and Networking Conference*, pp. 12-16, Las Vegas, 11-13 Jan. 2007.

[11] A. Schüppen, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus, M. Averweg, "An 80 GHz SiGe production technology," *III-V Review*, vol. 14, pp. 42-46, Aug. 2001.

[12] A.C. Ulusoy, G. Liu, A. Trasser, S. Chartier, and H. Schumacher, "Analog synchronous receiver for multi-gigabit wireless communications," *IEEE Radio and Wireless Symposium*, pp. 247-250, Phoenix, 16-19 Jan. 2011.

[13] A.C. Ulusoy, and H. Schumacher, "A System-on-Package Analog Synchronous QPSK Demodulator for Ultra-High Rate 60 GHz Wireless Communications," *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, 5-10 Jun. 2011.

[14] D. Grujić, M. Savić, C. Bingöl, and L. Saranovac, "Wide-bandwidth 60 GHz differential LNA in SiGe:C technology," *European Conference on Circuits and Systems for Communications*, pp. 71-74, Belgrade, 23-25 Nov. 2010.

[15] M. Schröter and A. Chakravorty, "Compact Hierarchical Bipolar Transistor Modeling With Hicum," World Scientific Publishing Company, 2010.

[16] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365-373, Dec. 1968.

[17] P.R.Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits (4th Edition)," John Wiley & Sons., 2001.

[18] S.A. Mass, "Microwave Mixers (second edition)," Artech House, Norwood, MA, 1992.

[19] H. Schumacher, "Monolithic Microwave ICs in High Speed Communication Systems," Lecture script, Ulm, 2011.

[20] E. M. Cherry and D. E. Hooper, "The Design of Wide-Band Transistor Feedback Amplifiers," *Proc. IEEE*, vol. 110, pp. 375-389, Feb. 1963.

[21] T. K. Johansen, J. Vidkjaer and V. Krozer, "Analysis and Design of Wide-Band SiGe HBT Active Mixers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 7, pp. 2389-2397, Jul. 2005.

[22] S. Prasad, H. Schumacher and A. Gopinath, "High-Speed Electronics and Optoelectronics: Devices and Circuits," Cambridge University Press, 2009.

[23] H. Li and H.-M. Rein, "Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe bipolar production technology," *IEEE ournal of Solid-State Circuits*, vol. 38, no. 2, pp. 184-191, Feb. 2003.

[24] G. Niu, J. Tang, Z. Feng, A.J. Joseph and D.L. Harame, "Scaling and technological limitations of 1/f noise and oscillator phase noise in SiGe HBTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 506-514, Feb. 2005.

[25] U.L. Rohde, A. K. Poddar, and G. Böck, "The Design of Modern Microwave Oscillators for Wireless Applications : Theory and Optimization," John Wiley & Sons., 2005.

[26] D. Leeson, "A simple model for feedback oscillator noise spectrum," *Proc. IEEE*, pp. 329-330, vol. 54, no. 2, Feb. 1966.

[27] G. Liu, A. Trasser and H. Schumacher, "33-43 and 66-86 GHz VCO With High Output Power in an 80 GHz f_T SiGe HBT Technology," *IEEE Microwave and Wireless Components Letters*, pp. 557-559, vol. 20, no. 10, Oct. 2010.

[28] R. Han and E. Afshari, "A broadband 480-GHz passive frequency doubler in 65-nm bulk CMOS with 0.23mW output power," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 203-206, Montreal, 17-19 Jun. 2012.

[29] J.-H. Chen and H. Wang, "A High Gain, High Power K-Band Frequency Doubler in 0.18 μm CMOS Process," *IEEE Microwave and Wireless Components Letters, IEEE*, pp. 522-524, vol. 20, no. 9, Sep. 2010.

[30] X. Zhang and Y.-H. Yun, "A DC to X-band frequency doubler using GaAs HBT MMIC," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1213-1216, Denver, 8-13 Jun. 1997.

[31] F. Gruson, G. Bergmann, H. Schumacher, "A frequency doubler with high conversion gain and good fundamental suppression," *IEEE MTT-S International Microwave Symposium Digest*, pp. 175-178, Fort Worth, 7-12 Jun. 2004.

[32] J.-J. Hung, T.M. Hancock and G.M. Rebeiz, "High-Power High-Efficiency SiGe Ku- and Ka-Band Balanced Frequency Doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 754-761, Feb. 2005.

[33] N. Pohl, H.-M. Rein, T. Musch, K. Aufinger and J. Hausner, "An 80 GHz SiGe Bipolar VCO with Wide Tuning Range Using Two Simultaneously Tuned Varactor Pairs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2655-2662, Oct. 2009.

[34] O. Lee, J-G. Kim, K. Lim, J. Laskar and Songcheol Hong, "A 60 GHz Push-Push InGaP HBT VCO With Dynamic Frequency Divider," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 10, Oct. 2005.

[35] R. Wanner, R. Lachner and G.R. Olbrich, "A SiGe monolithically integrated 278 GHz push-push oscillator," *IEEE MTT-S International Microwave Symposium Digest*, pp. 333-336, Honolulu, 3-9 Jun. 2007.

[36] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate and Y. K. Chen, "Highly Efficient Harmonically Tuned InP D-HBT Push-Push Oscillators Operating up to 287 GHz," *IEEE MTT-S International Microwave Symposium Digest*, pp. 341-344, Honolulu, 3-9 Jun. 2007.

[37] R. Wanner, R. Lachner and G.R. Olbrich, "A Monolithically Integrated 190-GHz SiGe Push-push Oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 12, Dec. 2005.

[38] C. Cao, E. Seok and K.K. O, "192 GHz push-push VCO in 0.13 μm CMOS," *Electronics Letters*, vol. 42, no. 4, Feb. 2006.

[39] D. Huang, T.R. Larocca, L. Samoska, A. Fung and M.-C.F. Chang, "324GHz CMOS Frequency Generator Using Linear Superposition Technique," *IEEE ISSCC Digest of Technical Papers*, pp. 476-477, Feb. 2008.

[40] H.-M. Rein and R. Reimann, "3.8 Gbit/s Bipolar Master/Slave D-Flip-Flop IC as a Basic Element for High-Speed Optical Communication Systems," *Electronics Letters*, vol. 22, no. 10, pp. 543-544, May. 1986.

[41] H. Knapp, T.F. Meister, W. Liebl, D. Claeys, T. Popp, K. Aufinger, H. Schäfer, J. Böck, S. Boguth, R. Lachner, "Static Frequency Dividers Up to 133GHz in SiGe:C Bipolar Technology," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 29-32, Austin, 4-6 Oct. 2010.

[42] W. Fang, A. Brunnschweiler and P. Ashburn, "An Analytical Maximum Toggle Frequency Expression and Its Application to Optimizing High-Speed ECL Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 920-931, Aug. 1990.

[43] K. Ishii, H. Ichino and C. Yamaguchi, "Maximum Operating Frequency in Si Bipolar Master-Slave Toggle Flip-Flop Circuit," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 7, pp. 754-760, Jul. 1994.

[44] W. Fang, "Accurate analytical delay expressions for ECL and CML circuits and their applications to optimizing high-speed bipolar circuits," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 572-583, Apr. 1990.

[45] S. Chartier, E. Sonmez, J. Dederer, B. Schleicher and H. Schumacher, "Millimeter-Wave Si/SiGe HBT Frequency Divider Using Dynamic and Static Division Stages," *Asia-Pacific Microwave Conference*, Bangkok, 11-14 Dec. 2007.

[46] K. Ishii, H. Ichino, M. Togashi, Y. Kobayashi and C. Yamaguchi, "Very-High-Speed Si Bipolar Static Frequency Dividers With New T-type Flip-Flops," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, pp. 19-24, Jan. 1995.

[47] R.L. Miller, "Fractional-Frequency Generators Utilizing Regenerative Modulation," *Proceedings of the IRE*, vol. 27, no. 7, pp. 446-457, Jul. 1939.

[48] R.H. Derksen, H.-M. Rein and K. Wörner, "Monolithic integration of a 5.3 GHz regenerative frequency divider using a standard bipolar technology," *Electronics Letters*, vol. 21, no. 22, pp. 1037-1039, Oct. 1985.

[49] E. Laskin and A. Rylyakov, "A 136-GHz Dynamic Divider in SiGe Technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 168-171, San Diego, 19-21 Jan. 2009.

[50] H. Knapp, T. F. Meister, W. Liebl, K. Aufinger, H. Schäfer, J. Böck, S. Boguth and R. Lachner, "168 GHz Dynamic Frequency Divider in SiGe:C Bipolar Technology," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 190-193, Capri, 12-14 Oct. 2009.

[51] S. Ahamed, J. Irvin, H. Seidel, "Study and Fabrication of a Frequency Divider-Multiplier Scheme for High-Efficiency Microwave Power," *IEEE Transactions on Communications*, vol. 24, no. 2, pp. 243-279, Feb. 1976.

[52] R.E. Best, "Phase-Locked Loops - Design, Simulation, and Applications (Fourth Edition)," McGraw-Hill, 1999.

[53] C.-C. Wang, Z. Chen, and P. Heydari, "W-Band Silicon-Based Frequency Synthesizers Using Injection-Locked and Harmonic Triplers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1307-1320, May. 2012.

[54] Z. Xu, Q.J. Gu, Y.-C. Wu, H.-Y. Jian and M.-C.F. Chang, "A 70-78-GHz Integrated CMOS Frequency Synthesizer for W-Band," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 12, pp. 3206-3218, Dec. 2011.

[55] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada and A. Matsuzawa, "A Low Phase Noise Quadrature Injection Locked Frequency Synthesizer for MM-Wave Applications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2635-2649, Nov. 2011.

[56] S. Kang, J.-C. Chien and A.M. Niknejad, "A 100 GHz Phase-Locked Loop in 0.13μm SiGe BiCMOS Process," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 79-82, Baltimore, 6-7 Jun. 2011.

[57] H.-K. Chen, T. Wang and S.-S. Lu, "A Millimeter-Wave CMOS Triple-Band Phase-Locked Loop With A Multimode LC-Based ILFD," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1327-1338, May. 2011.

[58] S. Shahramian, A. Hart, A. Tomkins, A.C. Carusone1, P. Garcia, P. Chevalier and S.P. Voinigescu, "Design of a Dual W- and D-Band PLL," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1011-1022, May. 2011.

[59] V. Jain, B. Javid, and P. Heydari, "A BiCMOS Dual-Band Millimeter-Wave Frequency Synthesizer for Automotive Radars," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2100-2113, Aug. 2009.

[60] K. Scheir, G. Vandersteen, Y. Rolain and P. Wambacq, "A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS," *IEEE International Solid-State Circuits Conference*, pp. 494-495, San Francisco, 8-12 Feb. 2009.

[61] M. Boheim and U. Goebel, "Low Cost Packages for Micro- and Millimeterwave Circuits," *European Microwave Conference 1994*, pp. 122-132, Cannes, 5-8 Sep. 1994.

[62] U. Goebel, "DC to 100 GHz chip-to-chip interconnects with reduced tolerance sensitivity by adaptive wirebonding," *IEEE 3rd Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 182-185, Monterey, 2-4 Nov.1994.

[63] T.P. Budka, "Wide-bandwidth millimeter-wave bond-wire interconnects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 4, pp. 715-718, Apr. 2001.

[64] R. Wang, Y. Sun and J.-C. Scheytt, "An on-board differential Bunny - Ear Antenna design for 60 GHz applications," *German Microwave Conference*, pp. 9-12, Berlin, 15-17 Mar. 2010.

[65] A.C.W. Lu, F. W and L.L. Wai, L.A. Low, F.X. Ke, K.C. Yip and Y.P. Lim, "Modeling and characterization of wire bonding for RF applications," *Electronic Components and Technology Conference*, pp. 905-909, San Diego, 28-31 May. 2002.

[66] "Noise Figure Analyzers NFA Series - User Guide," pp. 176, Agilent.

[67] S. Beer, B. Ripka, S. Diebold, H. Gulan, C. Rusch, P. Pahl, T. Zwick, "Design and Measurement of Matched Wire Bond and Flip Chip Interconnects for D-band System-in-Package Applications," *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, 5-10 Jun. 2011.

[68] F.J. Schmückle, U. Pursche, W. Heinrich and J. Purden, "A 77 GHz Broadband Flip-Chip Transition on LTCC Submount," *IEEE MTT-S International Microwave Symposium Digest*, pp. 453-456, Anaheim, 20-28 May. 2010.

[69] C.-C. Kuo, P.-A. Lin, H.-C. Lu, Y.-S. Jiang, C.-M. Liu, Y.-M. Hsin and H. Wang, "W-band flip-chip assembled CMOS amplifier with transition compensation network for SiP integration," *IEEE MTT-S International Microwave Symposium Digest*, pp. 465-468, Anaheim, 20-28 May. 2010.

[70] C.-H. Li, C.T. Fu, T.-Y. Chao, C.-N. Kuo, Y.T. Cheng and D.-C. Chang, "Broadband Flip-Chip Interconnects for Millimeter-Wave Si-Carrier System-on-Package," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1645 - 1648, Honolulu, 3-9 Jun. 2007.

[71] W.-C. Wu, L.-H. Hsu, E.Y. Chang, C. Karnfelt, H. Zirath, J.P. Starski, Y.-C. Wu, "60 GHz Broadband MS-to-CPW Hot-Via Flip Chip Interconnects," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 11, pp. 784-786, Nov. 2007.

Publications

- **Gang Liu**, Andreas Trasser and Hermann Schumacher, "A 64 to 84 GHz PLL with Low Phase Noise in an 80 GHz SiGe HBT Technology," *IEEE Transactions on Microwave Theory and Techniques*, accepted, early access available.

- **Gang Liu**, Andreas Trasser, A. Çağrı Ulusoy and Hermann Schumacher, "A Low-Cost, Wide-Band 60 GHz Down-Converter Module for Multi-Gigabit per Second Wireless Communication," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Austin, 21-23 Jan. 2013.

- **Gang Liu** and Hermann Schumacher, "47-77 GHz and 70-155 GHz LNAs in SiGe BiCMOS Technologies," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), pp. 84-87, Portland, 30 Sep.-3 Oct 2012.*

- **Gang Liu**, Andreas Trasser and Hermann Scehumacher, "A 64 to 81 GHz PLL with Low Phase Noise in an 80 GHz SiGe HBT Technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 171-174, Santa Clara, 16-18 Jan. 2012.

- **Gang Liu**, Mehmet Kaynak, Tatyana Purtova, A. Çağrı Ulusoy, Bernd Tillack and Hermann Schumacher, "Dual-Band Millimeter-Wave VCO with Embedded RF-MEMS Switch Module in BiCMOS Technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 175-178, Santa Clara, 16-18 Jan. 2012.

- **Gang Liu**, Andreas Trasser, A. Çağrı Ulusoy and Hermann Schumacher, "Low-loss, Low-cost, IC-to-Board Bondwire Interconnects for Millimeter-Wave applications," *IEEE MTT-S International Microwave Symposium Digest*, Baltimore, 5-10 Jun. 2011.

- **Gang Liu**, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "A 60 GHz Down-Conversion Mixer with 6.6 dB Gain and 11 GHz IF Bandwidth in an 80 GHz SiGe HBT Technology," *German Microwave Conference (GeMIC)*, Darmstadt, 14-16 Mar. 2011.

- **Gang Liu**, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "60-80 GHz Frequency Doubler Operating Close to f_{max}," *Asia-Pacific Microwave Conference Proceedings (APMC)*, pp. 770-773, Yokohama, 7-10 Dec. 2010.

- **Gang Liu**, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "A 60 GHz Frequency Down-Converter with Divided LO Output in an 80 GHz SiGe HBT Technology," *Asia-Pacific Microwave Conference Proceedings (APMC)*, pp. 936-939, Yokohama, 7-10 Dec. 2010.

- **Gang Liu**, Andreas Trasser and Hermann Schumacher, "33-43 GHz and 66-86 GHz VCO With High Output Power in an 80 GHz SiGe HBT Technology," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 10, pp. 557-559, Oct. 2010.

- **Gang Liu**, Yinmei Su and Hermann Schumacher, "A SiGe 7 Gbit/s Analog BPSK/QPSK Demodulator," *Conference on Ph.D. Research in Microelectronics & Electronics (PRIME)*, Berlin, 18-21 Jul. 2010.

- **Gang Liu**, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher, "64 to 86 GHz VCO Utilizing Push-Push Frequency Doubling in a 80 GHz f_T SiGe HBT Technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 239-242, New Orleans, 11-13 Jan. 2010.

- **Gang Liu**, Bernd Schleicher, Tatyana Purtova and Hermann Schumacher, "Fully integrated millimeter-wave VCO using slow-wave Thin-Film Microstrip Lines for chip size reduction," *European Microwave Integrated Circuits Conference (EuMIC)*, pp. 116-119, Rome, 28-29 Sep. 2009.

- **Gang Liu**, Sébastien Chartier, Andreas Trasser and Hermann Schumacher, "Fully Integrated Millimeter-Wave VCO with 32% Tuning Range," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, San Diego, 19-21 Jan. 2009.

- Yinmei Su, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "U- and V-band Signal Sources in Si/SiGe Technology," *Semiconductor Conference Dresden (SCD)*, Dresden, 27-28 Sep. 2011.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "A hardware efficient receiver for ultra high rate wireless communications," *International Journal of Microwave and Wireless Technologies (IJMWT)*, vol. 3, no. 2, pp. 121-129, Apr. 2011.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "An Analog Synchronous QPSK Demodulator for Ultra-High Rate Wireless Communications," *German Microwave Conference (GeMIC), 2011*, Darmstadt, 14-16 Mar. 2011.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "Analog Synchronous Receiver for Multi-Gigabit Wireless Communications," *IEEE Radio and Wireless Symposium (RWS)*, Phoenix, 17-19 an. 2011.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "A BPSK/QPSK Receiver Architecture Suitable for Low-Cost Ultra-High Rate 60 GHz Wireless Communications," *European Microwave Conference (EUMC)*, pp. 381-384, Pairs, 28-30 Sep. 2010.

- Xiaolei Gai, **Gang Liu**, Sébastien Chartier, Andreas Trasser and Hermann Schumacher, "A PLL with Ultra Low Phase Noise for Millimeter Wave Applications," *European Microwave Conference (EUMC)*, pp. 69-72, Paris, 28-30 Sep. 2010.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "A Narrow Bandwidth Microstrip Bandpass Filter Suitable for System-on-Package Integration," *Mediterranean Microwave Symposium (MMS)*, pp. 216-219, Cyprus, 25-27 Aug. 2010.

- Yinmei Su, **Gang Liu** and Hermann Schumacher, "Limiting Amplifiers for Bits Recovery of Gbps Analog BPSK/QPSK Demodulator," *Conference on Ph.D. Research in Microelectronics & Electronics (PRIME)*, Berlin, 18-21 Jul. 2010.

- A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "A SiGe Frequency Quadrupler for M-QAM Carrier Recovery," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 17-20, New Orleans, 11-13 Jan. 2010.

- Yinmei Su, A. Çağrı Ulusoy, **Gang Liu**, Andreas Trasser and Hermann Schumacher, "W-band Microstrip Bandpass Filters for Image Rejection," *Conference on Ph.D. Research in Microelectronics & Electronics (PRIME)*, Aachen, 12-15 Jun. 2012.

- Andreas Trasser, Hermann Schumacher, A. Çağrı Ulusoy and **Gang Liu**, "Low cost solutions for 60 GHz ultra-high-rate networks," *Sixth Joint Symposium on Opto- and Microelectronic Devices and Circuits (SODC)*, Berlin, Oct. 2010.

- Mehmet Kaynak, M. Wietstruck, W. Zhang, J. Drews, R. Barth, D. Knoll, F. Korndoerfer, R. Scholz, K. Schulz, C. Wipf, B. Tillack, K. Kaletta, K. Zoschke, M. Wilke, O. Ehrmann, Tatyana Purtova, A. Çağrı Ulusoy, **Gang Liu** and Hermann Schumacher, "Packaged BiCMOS Embedded RF-MEMS Switches with Integrated Inductive Load," *IEEE MTT-S International Microwave Symposium (IMS)*, Montreal, 17-22 Jun. 2012.

Curriculum Vitae

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