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A High Speed/High Linearity Continuous-Time Delta-Sigma Modulator

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To my family

"I have loved analog design because it deals with compromises, as does life itself."

Prof. Willy Sansen

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Abstract

Modern wireless communication systems demand wideband ADCs with high resolution and high linearity. Among different ADC topologies, CT $\Delta\Sigma$ modulators are very popular due to inherent anti-aliasing filtering and relative insensitivity to circuit non-idealities. By combining the advantages of oversampling and noise shaping, CT $\Delta\Sigma$ modulators enhance the SQNR performance covering a signal bandwidth from several tens of kHz up to tens of MHz.

This work presents a 15MHz bandwidth, CT $\Delta\Sigma$ modulator with a 70dB dynamic range designed for a high input frequency RF receiver. The high speed and high linearity requirements of such a receiver for signal above 5GHz require to employ a SiGe technology with sufficiently high f_T. Thus, the employed high-speed ADC must also be implemented in the same SiGe technology. To meet the target specifications of 12-bit resolution, 14-bit linearity and better than 10MHz bandwidth, a third-order single-loop CT $\Delta\Sigma$ modulator with a single-bit quantizer was chosen to operate at 1.92GHz, as a reasonable compromise between sampling frequency and circuit complexity. Since the single-bit internal quantizer is inherently linear, no digital DAC linearization technique is required. All the op-amps in the modulator have been designed to feature a finite GBW of $1.5\times f_S$, and the differentiator based ELD compensation method has been extended to counteract the effect of these finite GBW. Fabricated in a 0.25µm SiGe BiCMOS technology, the experimental prototype chip achieves 66.5dB SNDR and 78.1dB SFDR for a signal bandwidth of 15MHz. It dissipates 215.9mW and occupies an active area of 0.4mm^2.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BW	Bandwidth
CIFB	Cascade of Integrators with Distributed Feedback
CIFF	Cascade of Integrators with Distributed Feed-forward
CMFB	Common Mode Feedback
CT	Continuous-Time
DAC	Digital-to-Analog Converter
dB	Decibel
dBFS	Decibels relative to the Full Scale
Demux	Demultiplexer
DEM	Dynamic Element Matching
DLL	Delay Locked Loop
DR	Dynamic Range
DSP	Digital Signal Processor
DT	Discrete-Time
DUT	Device-Under-Test
EC	Emitter-Coupled
ECL	Emitter-Coupled Logic
ELD	Excess Loop Delay
EM	Electromagnetic
ENOB	Effective Number of Bits
FB	Feedback
FF	Feedforward
FFT	Fast Fourier Transformation

FIR	Finite-Impulse-Response
FOM	Figure of Merit
FPGA	Field-Programmable Gate Array
FS	Full Scale
GBW	Gain-Bandwidth product
HBT	Heterojunction Bipolar Transistor
HD	Harmonic Distortion
IBN	In-Band Noise
IM3	Third-Order Inter-Modulation Rejection
I/O	Input/Output
I/Q	In-phase/Quadrature-phase
ISI	Intersymbol Interference
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MASH	Multi-stage noise shaping
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSA	Maximum Stable Amplitude
MUX	Multiplexer
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
Op-amp	Operational-amplifier
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PSD	Power Spectral Density
RF	Radio Frequency
RZ	Return-to-Zero
SFDR	Spurious Free Dynamic Range
SiGe	Silicon-Germanium
Sin2rec	Sinusoidal to rectangular

SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoA	State-of-the-Art
SoC	System-on-Chip
S-Parameter	Scattering Parameter
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function
TF	Transfer Function
THD	Total Harmonic Distortion
Verilog-A	Analog Extensions to Verilog HDL
VGA	Variable Gain Amplifier

Chapter 1

Introduction

1.1 Motivation

The rapidly expanding communication market has fostered an increasing demand for high speed analog-to-digital converters (ADCs) with high resolution and high linearity. For example, WCDMA needs a signal-to-noise ratio (SNR) of 70dB or more, but at least 80dB third-order inter-modulation rejection (IM3) is required to reduce cross modulation. In such a communication application, ADCs with high spurious free dynamic range (SFDR) are required; otherwise a strong interferer in an adjacent channel could interrupt the weak signal of interest by generating harmonics or inter-modulation products. Similar requirements are set in radar receivers, where harmonic distortion is not degrading the signal or communication quality but tones are simply recognized as targets.

The requirement of wide bandwidth, high resolution and high linearity imposes significant challenges in the ADC design. Among various types of ADCs, continuous-time (CT) $\Delta\Sigma$ modulators have gained popularity as they offer high resolution without requiring stringent component matching [1]. By utilizing a combination of oversampling and noise shaping, $\Delta\Sigma$ modulators efficiently achieve sufficient noise suppression for a signal bandwidth from several tens of kHz up to tens of MHz [2] [3] [4]. In addition, CT $\Delta\Sigma$ modulators feature inherent anti-aliasing filtering which suppresses the out-of-band interference by the signal transfer function (STF), and offer a simple resistive input which is much easier to drive compared to the Nyquist-rate ADCs with switched-capacitor inputs.

This work targets a 12-bit effective number of bits (ENOB), 15MHz bandwidth CT $\Delta\Sigma$ modulator with better than 85dB SFDR for a RF receiver system-on-chip (SoC). This receiver consists of one RF frontend and two ADCs. The high speed and performance specifications of such a receiver front-end for signal above 5GHz require the employment of a Silicon-Germanium (SiGe) technology with sufficiently high transit frequency. Consequently, a 0.25µm SiGe BiCMOS technology was chosen by the industrial cooperation partner, since it provides heterojunction bipolar transistors (HBTs) with a high transit frequency of 110GHz with the associated low manufacturing cost, compared to the comparably fast deep-submicron technology.

In order to realize the SoC, the employed high-speed ADC must also be implemented in the same SiGe technology. Therefore, the main objective of this thesis work is to investigate high linearity solutions for the receiver SoC at both the system and circuit levels. In the chosen 0.25µm SiGe BiCMOS technology, the feasibility and viability of realizing a 15MHz bandwidth 12-bit $\Delta\Sigma$ modulator has been explored and investigated. Since both CMOS transistors and HBTs are provided in the employed technology, it is worthwhile to carry out a comparative study to figure out which devices are more suitable to realize the modulator, since the transistor type significantly affects the choice of modulator architecture.

Finally, the model of CMOS transistors in the BiCMOS technology was found to be insufficiently accurate; therefore, a HBT based third-order single-loop $\Delta\Sigma$ modulator with a single-bit internal quantizer was chosen to operate at 1.92GHz sampling frequency to meet the target specifications. There is no denying that the HBT based $\Delta\Sigma$ modulator consumes more power than its fine-line MOS based counterpart, but in this application the power dissipation is not a limiting factor. In the used 0.25µm SiGe BiCMOS technology, the choice of HBT based third-order single-bit $\Delta\Sigma$ modulator was found to be a reasonable compromise between circuit complexity and sampling frequency.

1.2 Thesis Organization

This thesis is organized as follows:

Following this introduction, Chapter 2 provides fundamentals about CT $\Delta\Sigma$ modulators, as well as the specifications and performance metrics used throughout this thesis. Then, a system-level design procedure of CT $\Delta\Sigma$ modulators is described.

Chapter 3 proposes a detailed architectural selection of the modulator, followed by performance verification through behavioral simulations. After that, electrical parameters of the building-block are derived from the modulator-level specifications.

Chapter 4 presents a detailed transistor-level and layout-level implementation of the proposed modulator, and covers the issues of high speed evaluation board design as well as the experimental results of the prototype chip. The measurement results demonstrate the effectiveness of the proposed CT modulator for the receiver SoC.

Chapter 5 presents the implementation of the receiver SoC, which consists of one Radio Frequency (RF) front-end, two CT $\Delta\Sigma$ modulators and other auxiliary circuits.

Chapter 6 discusses the enhancement techniques used to improve the performance of the single-bit $\Delta\Sigma$ modulator presented in Chapter 4. The differentiator based ELD and GBW compensation technique has been improved, and the op-amps and quantizer have been redesigned to achieve better performance.

Chapter 7 investigates the nonlinear effect of the first op-amp in CT $\Delta\Sigma$ modulators with finite gain-bandwidth product (GBW) compensation. Simulations indicate that the linearity requirement on the first op-amp becomes more stringent if the modulator is compensated for lower GBW. In the end, two methods to relax the op-amp's linearity requirement have been proposed.

Chapter 8 concludes the overall thesis and gives considerations for further research.

1.3 Research Contributions

The primary contributions of this research are summarized as follows:

- Comparative study of a variety of CT low-pass $\Delta\Sigma$ modulator architectures. System level considerations for the target high-frequency (>5GHz) RF receiver application are addressed, and the modulator's specifications are derived.

- Design of a high linearity third-order CT low-pass $\Delta\Sigma$ modulator for a high input frequency RF receiver. The theoretical resolution is derived and verified by simulations, while the modulator performance is analyzed, taking into account critical circuit non-idealities. A systematic design methodology is used for the proposed CT $\Delta\Sigma$ modulator [5].

- Transistor-level implementation and experimental verification of the CT third-order $\Delta\Sigma$ modulator. Measurement results show that the prototype modulator achieves a 70dB dynamic range with a 78.1dB SFDR over a 15MHz signal bandwidth. Fabricated in a low-cost 0.25µm SiGe BiCMOS process, the modulator dissipates 215.9mW and occupies an active area of $0.4mm^2$ [6].

- Implementation of a receiver SoC, which consists of one RF front-end (designed by the industrial cooperation partner), two CT $\Delta\Sigma$ modulators and other auxiliary circuits. This SoC has been well accepted by the industrial cooperation partner.

- Analysis on the mixed-signal differentiator based ELD compensation technique, and this technique is then improved to completely compensate for the finite GBW of the op-amps [7].

- Analysis on the nonlinear effect of the first op-amp in a single-bit CT $\Delta\Sigma$ modulator with finite GBW compensation. A behavioral op-amp model has been created and verified to approximate the op-amp nonlinear characteristics. Transient simulations indicate that more stringent linearity requirement on the first op-amp must be satisfied in the modulator compensated for lower GBW [8].

Chapter 2

Fundamentals of $\Delta\Sigma$ Modulators

In this chapter, the operating principle of $\Delta\Sigma$ modulators will be discussed. After that, the performance metrics used to evaluate the modulator will be illustrated. Finally an overview of the top-down hierarchical design methodology [9] [10] will be presented, which is commonly adopted in the design of CT $\Delta\Sigma$ modulators.

2.1 Operation of $\Delta\Sigma$ Modulators

The basic idea of $\Delta\Sigma$ modulation was first introduced in 1962 by Inose et. al. as a modification of Delta modulation [11]. Over the last few decades, $\Delta\Sigma$ converters are becoming increasingly attractive as they show important advantages in terms of high resolution and common insensitivity to analog circuit imperfection, compared to Nyquist rate converters. The $\Delta\Sigma$ modulator is an oversampling converter with sampling frequency multiple times higher than the signal bandwidth. The ratio of the oversampling frequency, to the Nyquist-frequency, $2f_{BW}$, is defined as the oversampling ratio (OSR):

$$OSR = \frac{f_S}{2f_{BW}} \tag{2.1}$$

Since oversampling spreads the quantization noise over the entire sampled bandwidth (f_S), the signal-to-quantization noise ratio (SQNR) in the band of interest (f_{BW}) can be improved. Additionally, the $\Delta\Sigma$ modulator implements a function called noise shaping, which pushes the majority of the quantization noise out of the desired signal bandwidth. Consequently, the noise outside the signal band can be

removed by a digital decimation filter which locates at the output of the modulator. By combining the advantages of oversampling and noise shaping, ΔΣ modulators are capable of converting a signal bandwidth of tens of MHz with high dynamic range [1] [12].

Fig. 2.1a illustrates the basic block diagram of a ΔΣ modulator, which is a closed-loop system consisting of a loop filter H, a typically low resolution quantizer (ADC) and a feedback digital-to-analog converter (DAC). The loop filter can be realized in direct time domain as $H(z)$, leading to a DT ΔΣ modulator. In contrast, a CT ΔΣ modulator is obtained if the implementation of the loop filter is performed using CT, $\mathcal{S}$-domain filters. In addition, based on the loop filter architecture, ΔΣ modulators can be divided into two different categories: single-loop and cascade or multi-stage noise shaping (MASH). Furthermore, the loop filter in ΔΣ modulators can feature either low-pass or band-pass characteristic to the input signal.

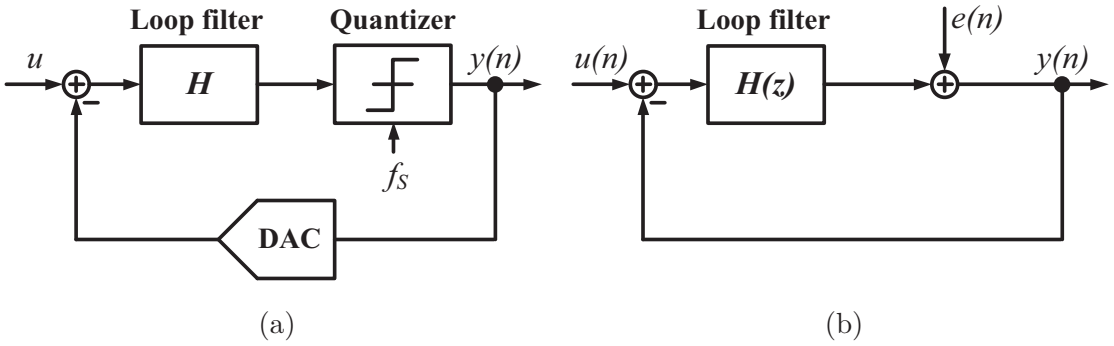


Figure 2.1: Basic ΔΣ modulator architecture (a) basic block diagram, and (b) linearized model of a DT modulator

To simplify the analysis, the loop filer in the modulator is assumed to be a DT, $\mathcal{Z}$-domain filter $H(z)$ at first. When replacing the internal quantizer with an additive white noise model, the ΔΣ modulator in Fig. 2.1a can be represented by its linearized model depicted in Fig. 2.1b. The quantizer is modeled as an adder with additional quantization noise input $e(n)$, which is assumed to be independent of the modulator input signal [13] [14]. Besides, the quantizer gain is assumed to be unity for simplicity. In this generic model, the feedback DAC is implemented with the same low resolution as the quantizer and offers an ideal transfer function. Consequently, no additional quantization error is introduced by the internal feedback DAC.

Obviously, the ΔΣ modulator can be considered as a two-input (u, e), one-output (y) system which can be represented by

$$Y(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{2.2}$$

where $U(z)$, $Y(z)$ and $E(z)$ are $\mathcal{Z}$-domain representations of the input, output and quantization error. Simultaneously, the STF and the noise transfer function (NTF) can be derived:

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{2.3}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.4}$$

Since the input signal and the quantization noise are influenced by different transfer functions, the loop filter can be designed such as to suppress the in-band quantization noise significantly while leaving the input signal unaffected. To satisfy both of these objectives, the loop filter should show a large gain within the band of interest, while its gain may decrease outside of the desired bandwidth.

In order to suppress the in-band quantization noise more significantly, a higher order NTF can be used, which results in a higher order ΔΣ modulator. According to Eq.(2.4), the order of NTF is determined by the number of poles in the loop filter. By adding more integrators and feedback paths, a Lth-order NTF equals [1]:

$$NTF(z) \mid_{L_{th}} = (1 - z^{-1})^L \tag{2.5}$$

Thus the accumulated IBN can be calculated as

$$IBN \mid_{L_{th}} = \frac{\Delta^2}{12} \frac{\pi^{2L}}{2L + 1} \frac{1}{OSR^{2L+1}} \tag{2.6}$$

where Δ is the least significant bit (LSB) of a N_B bit ADC quantized over a full scale range (FS), and can be defined as:

$$\Delta = \frac{FS}{2^{N_B} - 1} \tag{2.7}$$

Note the STF of the modulator is desired to be as flat as possible in the band of interest. Consequently, for a sinusoidal input signal with an amplitude equal to half of the quantizer full scale range, the ideal SQNR of an Lth-order $\Delta\Sigma$ modulator incorporating a N_B bit quantizer can be estimated as:

$$\begin{aligned} SQNR\,|_{L_{th}}\,[dB] &= 10\log_{10}\left(\frac{P_{FS/2}}{IBN\,|_{L_{th}}}\right) \\ &\approx 10\log_{10}\left(\frac{\Delta^2\cdot 2^{2N_B-3}}{IBN\,|_{L_{th}}}\right) \\ &= 10\log_{10}\left(\frac{3}{2}\frac{2L+1}{\pi^{2L}}OSR^{2L+1}(2^{N_B-1})^2\right) \\ &= 6.02N_B + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}OSR^{2L+1}\right) \end{aligned} \tag{2.8}$$

It can be seen from Eq.(2.8) that the SQNR performance of a $\Delta\Sigma$ modulator is determined by three parameters: the loop order L, the quantizer's number of bits N_B and the OSR. By increasing these parameters independently and collectively, the quantization error can be shaped out of band further, leaving less noise in-band. However, the predicted performance from Eq.(2.8) should be cautiously considered in practice, since this prediction does not consider coefficients selection and scaling within the loop filter design. Furthermore, the stability of modulators should be guaranteed during the design process, especially for single-bit high-order modulators which tend to be unstable [1].

2.2 CT $\Delta\Sigma$ Modulators

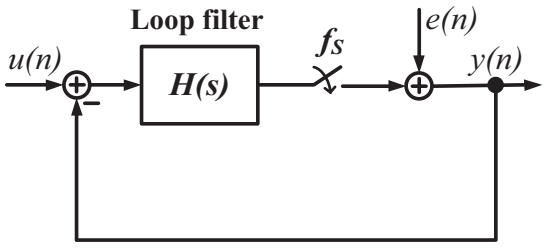


Figure 2.2: Linearized model of a CT $\Delta\Sigma$ modulator

Beyond the DT modulator design, the loop filter can also be implemented with CT circuits, resulting in a CT $\Delta\Sigma$ modulator. Nowadays the design and simulation of an ideal CT modulator is commonly performed in DT domain to speed up the whole design process. A DT-to-CT conversion can be subsequently adopted using impulse invariant transformation [15] [16], modified $\mathcal{Z}$-transformation [17] [18], as well as the state-space method [19].

Fig. 2.2 shows the corresponding linearized model. Compared to the DT implementation, the sampling operation is shifted inside the CT $\Delta\Sigma$ modulator, in front of the quantizer. Consequently, the sampling process is now subject to noise-shaping, making the quantizer the most uncritical building block in the loop. Another advantage of placing the sampling operation before the quantizer is that an intrinsic anti-aliasing property is introduced, which significantly relaxes the anti-aliasing requirements in front of the modulator. Besides, all signals in CT modulators are represented by analog, CT waveforms; thus the settling and bandwidth restrictions on the active building blocks of the loop filter can be significantly relaxed. Consequently, CT modulators usually have better power efficiency, and can be clocked at a much higher frequency to cover a larger bandwidth, compared to the DT counterpart. However, CT modulators are sensitive to delays introduced by the circuitry in the loop. All the non-idealities encountered during the presented CT $\Delta\Sigma$ modulator design process will be discussed in Chapter 3 and Chapter 4.

2.3 Performance Metrics

Before discussing the system design of CT $\Delta\Sigma$ modulators, several performance metrics that have been used throughout this work are presented.

In-band noise (IBN) is defined as the total noise power at the output of the ADC integrated over the desired bandwidth.

Signal-to-quantization noise ratio (SQNR) is the ratio of the signal power to the power of the in-band quantization noise at the modulator output, expressed in decibel (dB).

Signal-to-noise ratio (SNR) is the ratio of the signal power to the in-band noise power at the modulator output, expressed in dB.

$$\text{SNR [dB]} = 10\log_{10}\left(\frac{P_{Signal}}{P_{Noise}}\right) \tag{2.9}$$

Signal-to-noise plus distortion ratio (SNDR) is the power ratio between the input signal and the sum of in-band noise and all distortion components, expressed in dB.

$$\text{SNDR [dB]} = 10\log_{10}\left(\frac{P_{Signal}}{P_{Noise} + P_{Distortions}}\right) \tag{2.10}$$

Effective number of bits (ENOB) is generally a metric to specify the resolution of an ADC, and it can be calculated as:

$$\text{ENOB [bits]} = \frac{\text{SNDR[dB]} - 1.76}{6.02} \tag{2.11}$$

Spurious free dynamic range (SFDR) is the ratio between the power of the fundamental signal to the power of the strongest spurious component in-band, often expressed in dB or dBc.

Dynamic range (DR) usually refers to the input signal range in which the modulator achieves an SNDR above 0dB. It is obtained by measuring the SNDR variation while sweeping the input signal power from full scale to the smallest detectable signal.

2.4 Design Strategy

One of the most popular approaches adopted in the design of CT ΔΣ modulators is the top-down hierarchical design methodology [9] [10], which has been proven to be extremely successful in practice. As illustrated in Fig. 2.3, this approach starts from the system-level design, with the intention of figuring out the most suitable modulator topology which fulfills a given set of system requirements. The performance of the chosen modulator is evaluated to ensure that it meets both the bandwidth

and resolution specifications with guaranteed stability and reasonable power consumption. Next, the CT $\Delta\Sigma$ modulator is implemented with Analog Extensions to Verilog HDL (Verilog-A) based behavioral building blocks in Cadence. In this behavioral model, the design parameters of passive elements, that is, capacitors and resistors, are mapped from system-level coefficients of the modulator. In contrast, the minimum requirements on the operational-amplifier (op-amp) or transconductors - such as DC gain, finite GBW, slew-rate and so on - are determined by iteratively decreasing their values until the performance of the modulator starts to decrease.

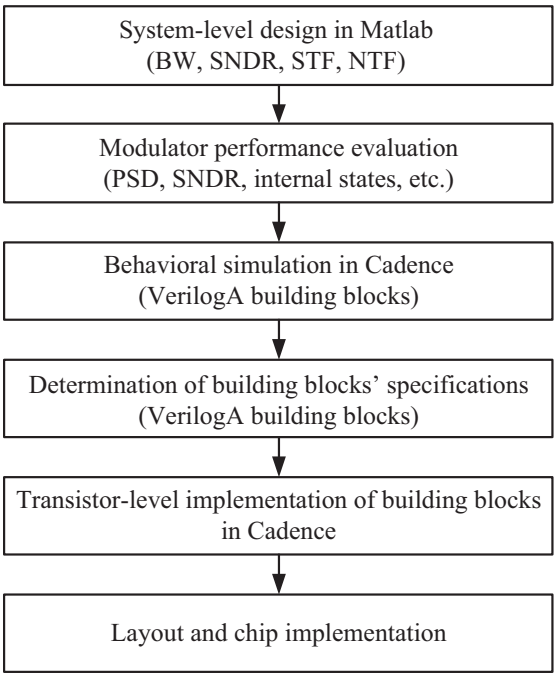


Figure 2.3: Top-down hierarchical design methodology

Once these building blocks are specified, the transistor-level implementation can start. After that, the available transistor-level design could substitute the behavioral element in the Verilog-A based $\Delta\Sigma$ modulator, first individually, then in pairs or groups and finally all at once, so that time-domain simulations can verify whether the block fits into the system environment. Then the layout can be developed, and multiple iterations on the design may be required, until the results of the post-layout simulation satisfy the imposed design requirements. Finally, a chip implementation can be obtained for experimental verification.

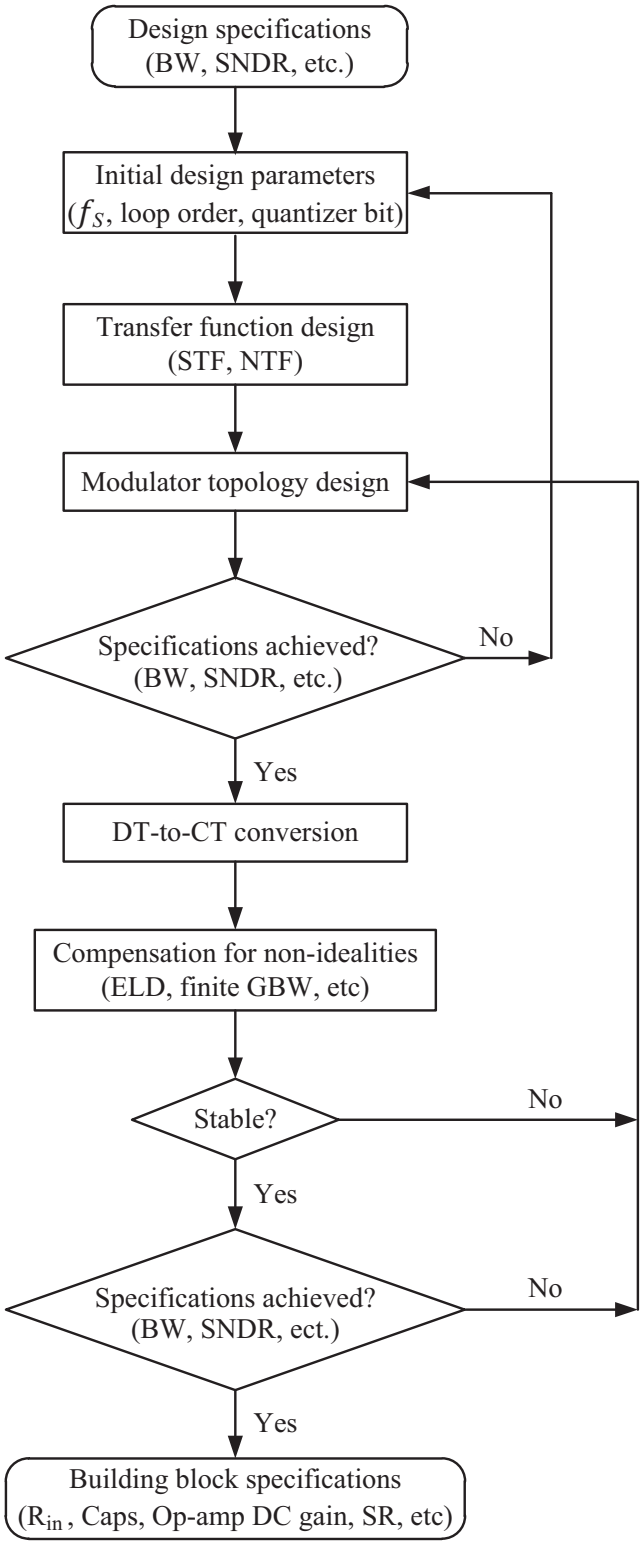


Figure 2.4: System-level design flow of a CT ΔΣ modulator [10]

The first step in the design process of a CT $\Delta\Sigma$ modulator is the system-level design, which provides efficient simulation algorithms to verify the system concept with a high degree of accuracy and computational efficiency. As illustrated in Fig. 2.4, it starts with the system-level specifications, such as signal bandwidth, SNDR, etc. According to these given specifications, initial design parameters of the modulator can be derived, including the sampling frequency f_S, the order of the loop filter and the internal quantizer resolution. Following this, the noise transfer function of the modulator can be calculated, which allows the determination of the most appropriate modulator architectures. To this objective, Schreier's Delta-Sigma Matlab toolbox is widely utilized in generating the required coefficients for a given DT topology [12] [20].

Once the DT modulator is verified to be capable of realizing the required performance, a DT-to-CT conversion should be proceeded to obtain the equivalent CT modulator. The most common approaches for this conversion include the impulse-invariant transformation [15] [16], the modified $\mathcal{Z}$-transformation [17] [18] as well as the state-space method [19]. After that, the non-idealities in the CT modulator - such as excess loop delay (ELD) and op-amp finite GBW - have to be taken into consideration, since they adversely affect the modulator performance. Compensation techniques can be applied to counteract the influence of these non-ideal behaviors by tuning the modulator coefficients. Finally, the performance of the modulator is evaluated again to check whether this implementation meets the requirements of the system with guaranteed stability. If the system constraints are not satisfied, redesign iterations have to be carried out until all these specifications are fulfilled [21].

Chapter 3

System-Level Design and Simulation Strategy

In this chapter, the system-level design of a CT $\Delta\Sigma$ modulator for a receiver SoC is discussed and presented. This chapter starts with the system-level requirement of the $\Delta\Sigma$ modulator, then the architectural selection of the modulator is described, followed by performance verification through behavioral simulations. After that, a step-by-step procedure is discussed to transform the modulator-level specifications into the building-block electrical (circuit-level) parameters.

3.1 Target Specifications

The CT $\Delta\Sigma$ modulator presented in this work is designed for a RF receiver project. In this application, the designed $\Delta\Sigma$ modulator follows an RF front-end and performs the digitization. The main requirements for the $\Delta\Sigma$ modulator are summarized as follows:

- Input bandwidth: 15MHz
- Resolution $\geq$ 12-bit
- Linearity: SFDR $\geq$ 85dB
- STF: no peaking to avoid overload by the out-of-band interferers
- Technology: IHP SiGe 0.25µm BiCMOS technology

The designed $\Delta\Sigma$ modulator is required to achieve at least 12-bit resolution with better than 85dB SFDR over a 15MHz bandwidth. In addition, the modulator must feature a flat STF frequency response so as to prevent potential jamming of the receiver. In order to integrate the RF front-end with $\Delta\Sigma$ modulators to realize a receiver SoC, the modulator has to be implemented using the same technology as the RF font-end, which is a SiGe 0.25µm BiCMOS process. Since both CMOS transistors and HBTs are available in the employed technology, a comparative study has been carried to figure out which devices are more suitable to realize the modulator.

3.2 Architecture Selection

There are two major types of architecture for CT $\Delta\Sigma$ modulators, that is, single-loop and multi-loop architecture. The latter one is commonly denoted as cascade or MASH (multi-stage noise shaping). Since the multi-loop topology suffers from stringent requirements on non-idealities of circuit implementations and quantization noise leakage, the single-loop architecture is chosen in this work.

For single-loop $\Delta\Sigma$ modulators, two kinds of loop filter architectures are commonly used: cascade of integrators with distributed feed-forward (CIFF) and cascade of integrators with distributed feedback (CIFB). Although CIFF relaxes the linearity and slew rate requirements on the op-amps due to smaller internal signal swings [1], it leads to out-of-band peaking in the STF and therefore cannot satisfy the design requirement. In this work the CIFB architecture is utilized, which generates a flat STF in the band of interest and a Butterworth roll-off at higher frequencies.

3.2.1 Architecture of the CMOS Based Modulator

In the beginning, a CMOS implementation was preferred to realize the modulator due to its reduced power consumption when using excessive digital calibration, compared to HBTs. According to Eq.(2.8), the ideal SQNR performance of the $\Delta\Sigma$ modulator depends on three parameters, namely the resolution of the internal quantizer N_B, the order of the loop filter L and the OSR [12]. From previous design experience,

250nm CMOS limits the speed of digital and sampling circuitry below 500MHz, and thus the maximum OSR is approximately 15 for a 15MHz bandwidth. For such a low OSR, multi-bit internal quantization must be employed both to stabilize the modulator and further to reduce the quantization noise. Therefore, a 4-bit quantizer was intended for this modulator, as a compromise between circuit complexity and power consumption.

In considering the loop filter order, calculations based on Eq.(2.8) were performed to ensure the designed 4-bit modulator meet the target resolution requirement. As shown in Fig. 3.1, a third-order 4-bit modulator is able to achieve almost 90dB SQNR with an OSR of 15. Therefore, the basic parameters are all determined, and a third-order 4-bit modulator with an OSR of 15 could be chosen for the receiver application.

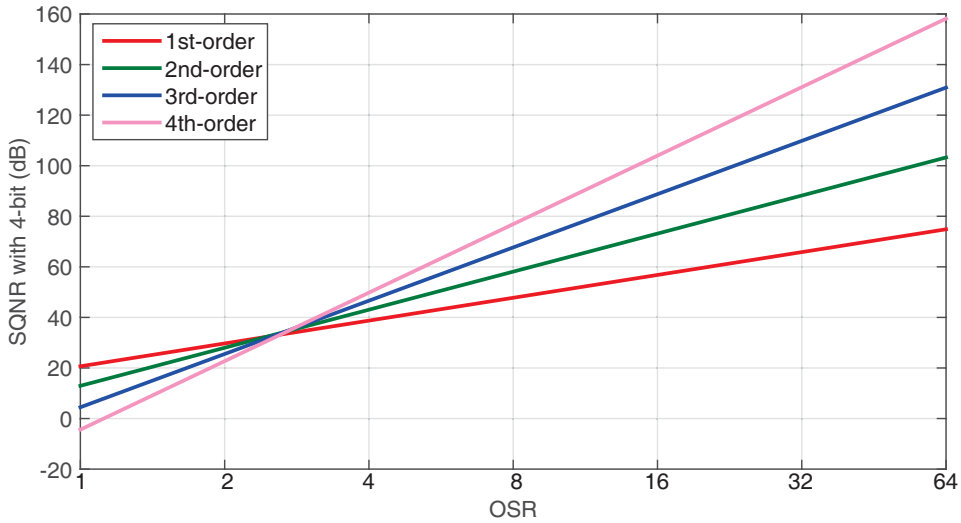


Figure 3.1: Calculated SQNR versus OSR for a 4-bit modulator, according to Eq.(2.8)

The Schreier Toolbox was utilized for the NTF and STF design by using the *Clans* function having $NTF = clans(order = 3, OSR = 15, Quantization_level = 16, rmax = 0.005, opt = 1)$ [22]. By setting $rmax = 0.005$ a flat SFT can be obtained, and the $opt = 1$ specifies that the NTF zeros are optimally spread over the band of interest. Fig. 3.2 shows the simulated performance of the 4-bit modulator. Obviously, the STF is flat and a notch appears in the NTF due to the zero optimization. The modulator achieves a peak SQNR of 91.9dB so that the resolution requirement of 12-bit can be satisfied.

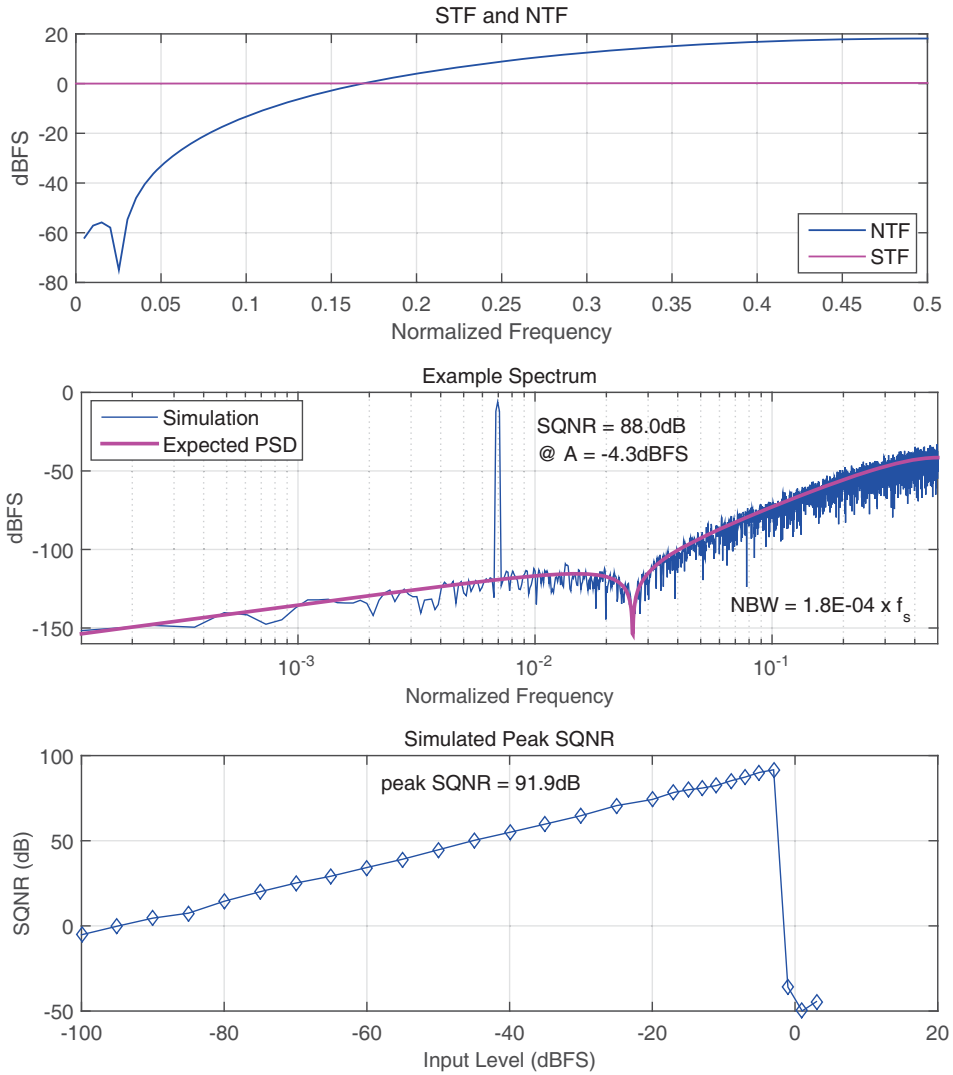


Figure 3.2: DT design example using Schreier Toolbox

3.2.1.1 Test-tapeout

During the architecture design of the modulator, a test-tapeout was carried out to examine the CMOS transistor performance in the chosen SiGe 0.25µm BiCMOS process. A latched comparator, which is a part of the internal quantizer, was chosen to be a test-prototype design based on the following reasons:

- The internal quantizer is based on CMOS transistors, and it is timing critical in the 250nm technology, which limits the maximum sampling frequency of the modulator.

- The decision time of the latched comparator is critical, since its delay directly adds to the loop-delay of the ΔΣ modulator.
- The matching of measurement and post-layout simulation with extracted parasitic would reveal how accurate the simulation results could be.
- The comparator will be needed as part of the multi-bit quantizer and thus is useful for the ΔΣ modulator design - rather than just being a test-tapeout.

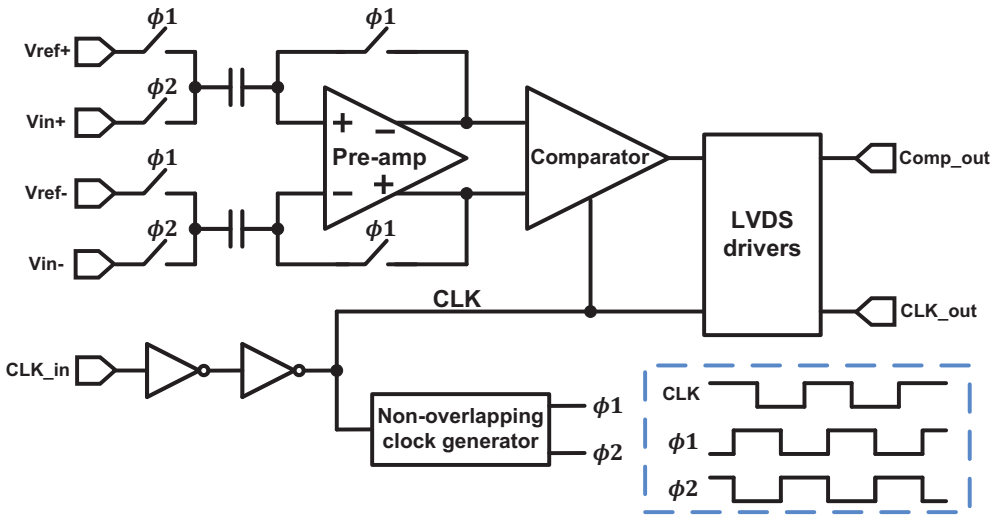


Figure 3.3: Block diagram of the test tapeout

Fig. 3.3 shows the block diagram of the test-tapeout, which consists of a pre-amplifier, a CMOS latched comparator, a non-overlapping clock generator, as well as custom designed low voltage differential signaling (LVDS) drivers. The pre-amplifier consists of a NMOS differential pair with a resistive load. In order to reduce the input offset of the pre-amplifier, the auto-zero technique has been applied, which incorporates two series capacitors at the input [23]. Transmission gate is used to realize the switches, while the amplifier is configured in a unity-gain feedback loop to store its offset on the input capacitors during the offset cancellation phase. This pre-amplifier features a 3-dB bandwidth of 600MHz with a power consumption of 150µW.

The schematic of the latched comparator is shown in Fig. 3.4, and this topology was favored due to its high power efficiency [24]. Simulations show that the sensitivity of this comparator is 5mV, while the average dynamic power consumption is 116µW from a 2.5V DC voltage.

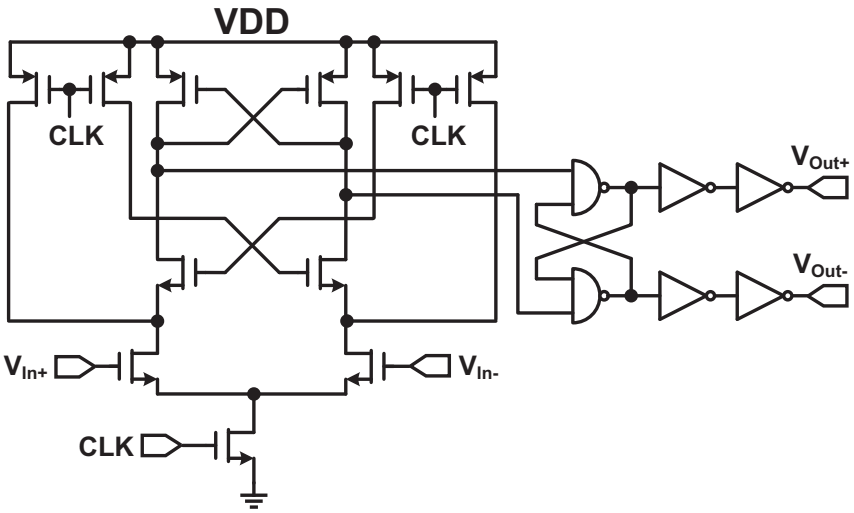


Figure 3.4: Schematic of the comparator

In order to trigger the comparator, a sinusoidal signal is inserted externally and converted to a square wave *CLK* by employing several inverters. This clock signal *CLK* is also applied to a non-overlapping clock generator to generate non-overlapping clocks used in the auto-zero technique, as shown in Fig. 3.3. Note in this test tapeout, both the clock signal *CLK* and the comparator output are visible over LVDS drivers; therefore the propagation delay can be measured.

For an input overdrive voltage of 20mV with a 10MHz clock, the measured propagation delay of the comparator was 1.4ns. However, this delay is much higher than the post-layout simulated value, which was only 450ps. The post-layout simulation test bench was identical to the measurement setup, and the parasitic effects of bounding wire and pads had been taken into consideration. Since there is a large mismatch between simulation and measurement results of the test-tapeout of the comparator, the model of analog CMOS transistors in the BiCMOS technology was found to be inaccurate. Since the comparator delay would become almost a full clock cycle, and the digital DAC linearizer would need unexpectedly large time in the multi-bit CMOS modulator, the CMOS implementation was unacceptable due to the inaccurate model. Therefore, a decision was made to change the topology of the $\Delta\Sigma$ modulator to an architecture in which only HBTs could be used for high-speed (sampling speed) operation. There is no denying that the power consumption of the

HBT based $\Delta\Sigma$ modulator is much higher than its fine-line MOS based counterpart, but the power dissipation is not a limiting factor in this application.

3.2.2 Architecture of the Bipolar Based Modulator

Since HBTs in the employed technology have been chosen to realize the $\Delta\Sigma$ modulator, the architecture described in Section 3.2.1 must be reconsidered.

Although the incorporation of multi-bit quantizer increase the SQNR by approximately 6dB per bit, it could cause unsuppressed distortion since the nonlinear errors introduced by the multi-bit feedback DACs are directly injected at the modulator input. In order to minimize the DAC linearity degradation from mismatch, many different techniques have been proposed. Special layout techniques can be applied in the DAC design to achieve inherently good matching, but this inevitably results in considerable area requirement and imposes significant parasitics. Dynamic element matching (DEM) [2, 25, 26] is popular to improve the DAC linearity, but it requires a significant amount of digital hardware and usually increases the loop delay. These linearization techniques are feasible for fine-line CMOS, but turn out to be power hungry and hard to realize in the target 0.25µm SiGe BiCMOS technology. Thus, for the Bipolar based modulator, the inherently linear single-bit quantization is preferred, since it greatly simplifies the circuit-level implementation, and avoids complicated DAC linearization techniques. Furthermore, in a single-bit modulator, the design of the last amplifier can be simplified since its loading capacitor, the input capacitor of the quantizer, is much smaller compared to the one used in a multi-bit topology.

Fig. 3.5 shows the calculated SQNR over OSR for different modulator orders when single-bit quantization is incorporated, according to Eq.(2.8). Note Eq.(2.8) only calculate SQNR for the *ideal* model, and in practice the integrator gain must be properly scaled to ensure stability with sufficient internal signal swings [12]. Therefore, Schreier Toolbox was used to calculate the real achievable SQNR considering the coefficient scaling, and the calculated results are also given in Fig. 3.5. During the calculation, the *synthesizeNTF* function was used with the out-of-band gain of 1.5.

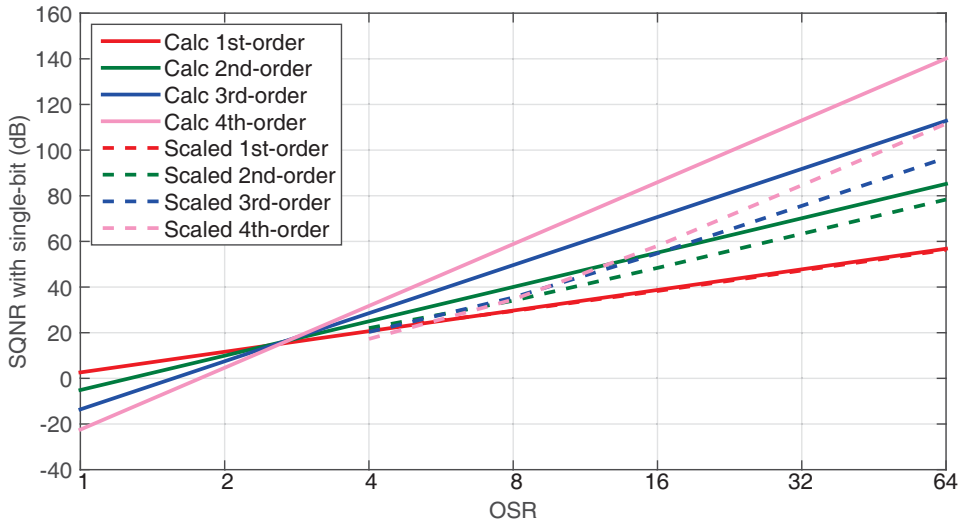


Figure 3.5: SQNR versus OSR for a single-bit modulator, calculated according to Eq.(2.8) as well as simulated using Schreier Toolbox with coefficients scaling

Based on Fig. 3.5, the modulator order and sampling frequency can be determined to meet the target requirement.

Since the incorporation of single-bit internal quantization tends to make higher order $\Delta\Sigma$ modulators unstable, a medium modulator order is required and a loop filter order of three is reasonable. To suppress quantization noise sufficiently for at least 12-bit resolution, a high sampling frequency is necessary. According to Fig. 3.5, an SQNR of approximately 90dB can be achieved for a single-bit modulator operating at 1.92GHz with an OSR of 64. Note this high sampling frequency requirement is feasible in the target SiGe BiCMOS technology, since HBTs have a much higher transit frequency (f_T) compared to MOS transistors in similar submicron technologies. Therefore, up to now the basic parameters are all determined, and a third-order single-bit modulator with an OSR of 64 is chosen for the receiver application.

In addition, the feedback DAC scheme is of special importance to consider in the CT $\Delta\Sigma$ modulator design, since the DAC induced errors directly add to the modulator input through the outermost feedback paths. Considering the high sampling frequency of this modulator, rectangular feedback pulses in a non-return-to-zero (NRZ) implementation are incorporated by the proposed single-bit $\Delta\Sigma$ modulator to simplify high speed circuitry. The two-level single-bit feedback DAC features inherent linearity, and thus no complicated linearization technique is required. Fur-

thermore, when compared to the return-to-zero (RZ) feedback, the NRZ feedback not only features slightly less sensitivity to clock jitter, but also relaxes the slew rate requirements on the corresponding op-amps.

As introduced in Section 2.4, the design of the loop filter for a CT $\Delta\Sigma$ modulator starts in discrete-time domain to speed up the whole development process. In this work, the used third-order DT topology is an optimal implementation published in [27] [1], as shown in Fig. 3.6. The loop filter $LF(z)$ of this modulator is given by:

$$LF(z) = -a_3 I_3(z) - a_2 a_3 I_2(z) I_3(z) - a_1 a_2 a_3 I_1(z) I_2(z) I_3(z) \tag{3.1}$$

where a_i denotes the DT scaling factors with {a1, a2, a3} = {0.2, 0.5, 0.5}. Note this modulator is implemented with two DT resonators $\{I_{1,2}(z) = 1/(1 - z^{-1})\}$ and one DT integrator $\{I_3(z) = z^{-1}/(1 - z^{-1})\}$.

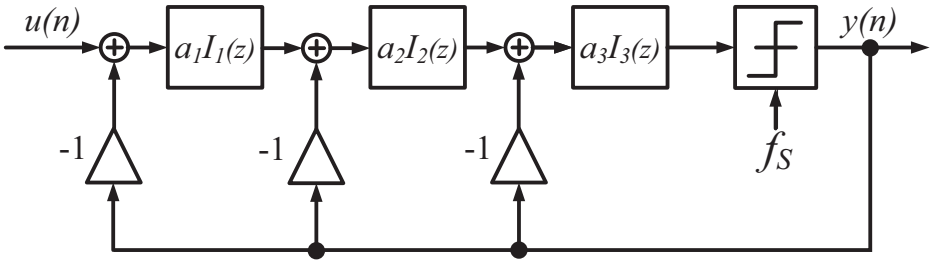


Figure 3.6: Architecture of the third-order DT $\Delta\Sigma$ modulator

This third-order DT loop filter can be transferred into an equivalent CT counterpart with a CIFB topology, which can be written as:

$$LF(s) = -k_3 I_3(s) - k_2 I_2(s) I_3(s) - k_1 I_1(s) I_2(s) I_3(s) \tag{3.2}$$

where k_i denotes the CT scaling coefficients for the i_{th} feedback path, while $I_{1,2,3}(s)$ equals f_S/s. In this design the NRZ DAC pulse shape is incorporated with a transfer function:

$$R_{DAC,NRZ}(s) = \frac{1 - e^{-sT_S}}{s} \tag{3.3}$$

Therefore, the CT loop filter can be found by the impulse invariant transformation [15] [16]:

$$\mathcal{Z}^{-1}\{LF(z)\} = \mathcal{L}^{-1}\{R_{DAC,NRZ}(s) LF(s)\}|_{t=nT_S} \tag{3.4}$$

After a coefficient comparison, the CT scaling coefficients k_i can be derived, and summarized in Table 3.1 [1]. Fig. 3.7 presents the architecture of this CT $\Delta\Sigma$ modulator, which incorporates a single-loop third-order CIFB loop filter. A local resonator, k_{res}, is added to optimally place the NTF zeros. Therefore, the quantization noise can be further reduced.

Table 3.1: Scaling coefficients for the CT third-order modulator; no ELD

k_{sig}	k_1	k_2	k_3	k_{res}
0.05	0.05	0.3	0.641	0.0016

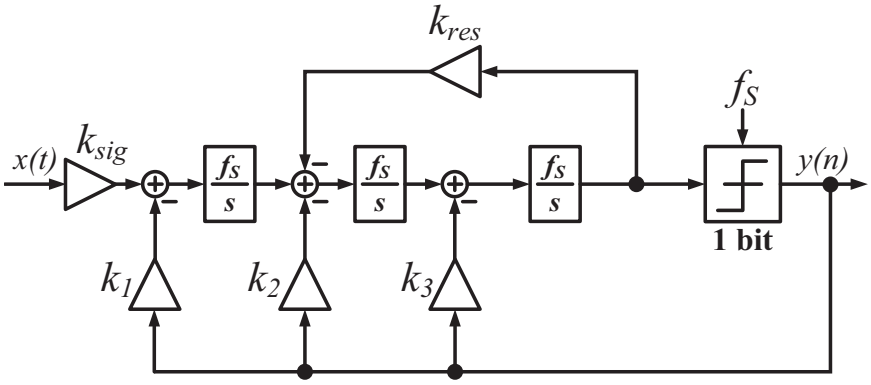


Figure 3.7: Architecture of the CT third-order CIFB $\Delta\Sigma$ modulator

Both STF and NTF of the CT third-order CIFB modulator are depicted in Fig. 3.8. The STF shows a flat frequency response within the band of interest, while the NTF contains a notch located at 11.5MHz due to the local resonator. Simulations show an ideal resolution of 88dB SNDR for the chosen architecture.

3.2.3 ELD Compensation

Excess loop delay (ELD) is an inevitable problem in all CT $\Delta\Sigma$ modulator designs, especially when the conversion bandwidth and the clock rates become ever higher [1] [28]. Associated from the limited speed of the available transistors in the quantizer and the feedback DAC, ELD degrades the stability and lowers the resolution. Various techniques have been proposed in the literature to cancel out the influence of ELD for single-loop modulators, while the usual strategy is to realize an additional fast

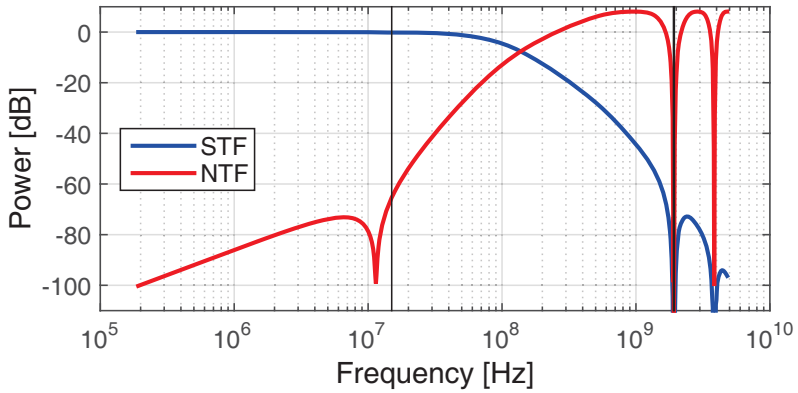
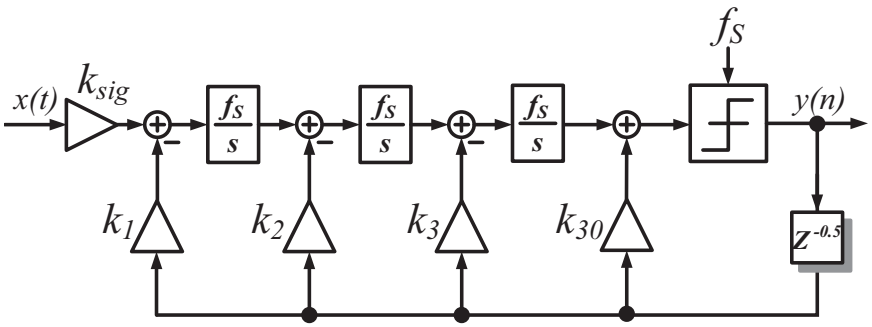
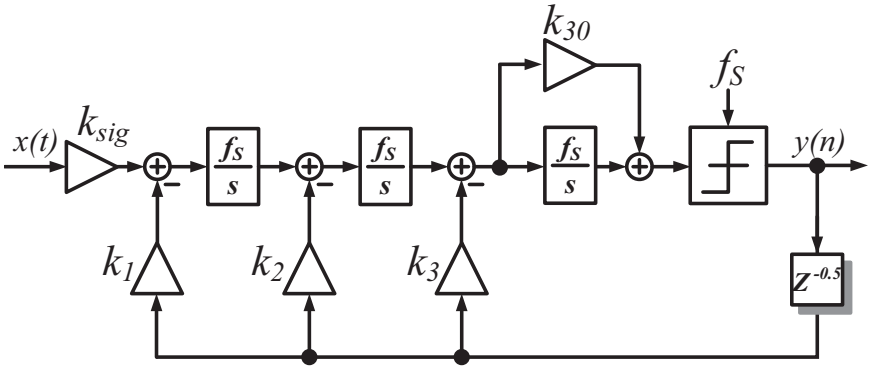


Figure 3.8: STF and NTF of the CT third-order CIFB ΔΣ modulator



(a) ELD compensation by adder



(b) ELD compensation by PI integrator

Figure 3.9: Different ELD compensations for a CT third-order ΔΣ modulator

feedback loop around the quantizer while tuning the filter coefficients to restore the NTF to its original [29]. A direct feedback path [30] can be inserted after the last integrator to compensate for the loop delay, as shown in Fig. 3.9a. However, this requires an extra power-hungry summing amplifier which must achieve a wide bandwidth. The ELD compensation technique can also be implemented by adding

an additional proportional path through the last integrator as illustrated in Fig. 3.9b [31], but this gives rise to an unwanted out-of-band peaking in the STF. Therefore, this approach is not suitable for this application since a flat STF is required.

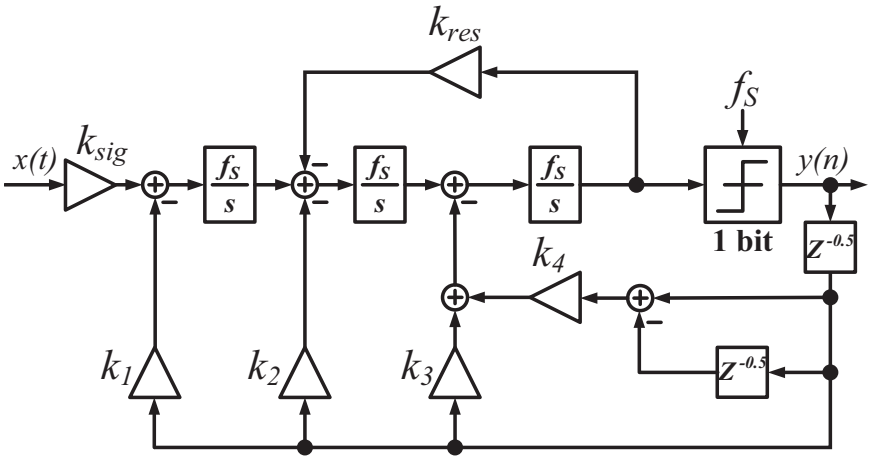


Figure 3.10: Architecture of the CT third-order single-bit $\Delta\Sigma$ modulator with ELD compensation

In this work, ELD is set to half a sampling period, giving the quantizer sufficient time to make a decision. This delay is compensated by adding a mixed-signal differentiating path from the quantizer output to the input of the last integrator [32], as shown in Fig. 3.10. By proper coefficient tuning, the original NTF can be restored. In order to verify this ELD compensation method, a Matlab based modulator model has been developed, which will be discussed in next section.

3.3 Matlab Based CT $\Delta\Sigma$ Modulator

Fig. 3.11 illustrates the block diagram of the Matlab Simulink model for the chosen CIFB topology. Each CT integrator is represented by a transfer function of f_S/s, and k_i account for the feedback scaling. Besides, the parameters c_i are used for proper scaling of the internal state variables. At the quantizer output, a D-latch is used to intentionally generate a half sampling period ELD to provide the transistor-level quantizer with sufficient time for quantization, and this delay is compensated by the mixed-signal differentiating path (realized by k_3 and k_4) as mentioned in the

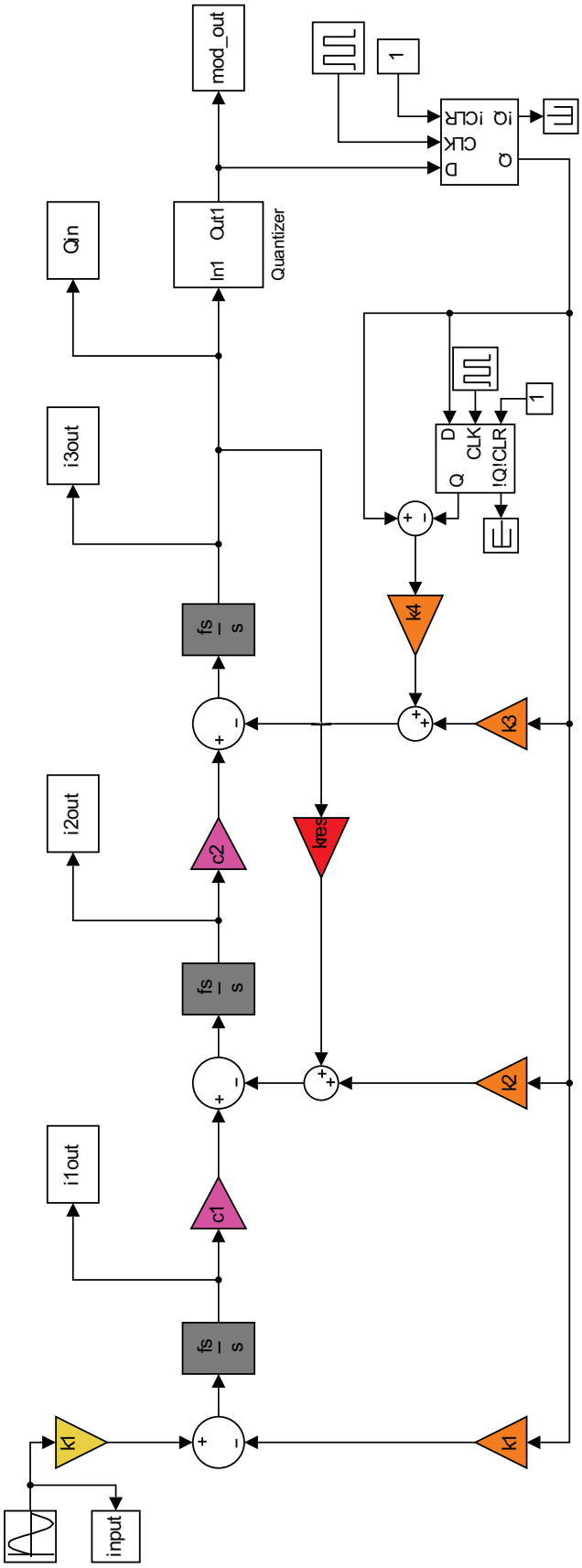


Figure 3.11: Matlab based model for the selected ΔΣ modulator

previous section. Lastly, the scaling coefficients for the CT modulator with ELD are given in Table3.2.

Table 3.2: Scaling coefficients for the single-bit modulator with ELD=$0.5/f_S$ and infinite op-amp GBW

k_{sig}	k_1	k_2	k_3	k_4	k_{res}	c_1	c_2
0.05	0.05	0.325	0.398	0.3585	0.003	1	0.5

Since the integrator output of the CIFB modulator contains a significant amount of input signal amplitude [33], proper coefficient scaling must be carried out to achieve suitable swings at the integrator output [27] [34].

The simulated spectrum of the Matlab based $\Delta\Sigma$ modulator model is illustrated in Fig. 3.14. For a -6dBFS sine wave input at 2.75MHz, this modulator achieves 88.1dB SQNR, which matches very well with the ideal DT modulator performance. Therefore, the DT-to-CT conversion and ELD compensation have been realized successfully.

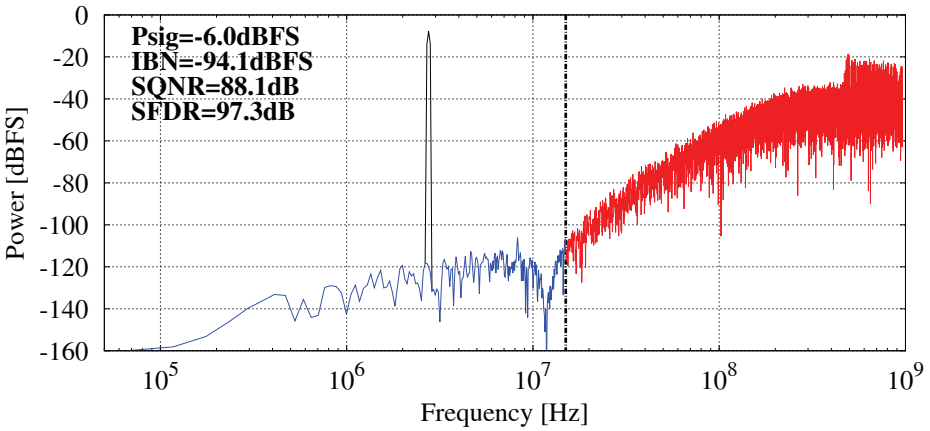


Figure 3.12: Simulated spectrum of the Maltab based modulator model

3.4 Finite GBW Compensation

Besides the ELD due to the non-zero switching time of the transistors in the quantizer and DACs, the finite GBW of the amplifiers is another issue which should be addressed when designing high speed low-power CT $\Delta\Sigma$ modulators. Over the years,

the on-going trend for wide-band CT $\Delta\Sigma$ modulators continues to push the sampling frequency f_S to the technology limit, and modulators at gigahertz-sampling frequencies have been realized [35] [36] [37]. This results in an increase in the GBW of op-amps used in the modulator, since normally a finite GBW of 2-3 times f_S is required to avoid significant performance degradation. As a consequence, an increase in power consumption is inevitable in order to satisfy this high GBW constraint for very high sampling frequencies. One possible approach for addressing this issue is to incorporate the finite GBW compensation technique [1] [31], which shows that the limited op-amp GBW in CT $\Delta\Sigma$ modulators can be chosen even below f_S while maintaining the original noise shaping behavior, resulting in a stable and power-efficient design.

In order to incorporate the influence of the finite GBW in a CT $\Delta\Sigma$ modulator, the amplifier can be modeled as a single pole system. Consequently, the transfer function of the ith integrator can be expressed as [38]:

$$ITF_{GBW_i} \approx \frac{k_i f_s}{s} \frac{GE_i}{\frac{s}{\omega_i} + 1} \tag{3.5}$$

As shown in Eq.(3.5), the influence of the finite GBW of the amplifier can be lumped into an integrator gain error GE_i and a non-dominant pole ω_i, which can be represented by [1]:

$$GE_i = \frac{GBW_i}{GBW_i + \sum_j k_{ij} \cdot f_s},\ \omega_i = GBW_i + \sum_j k_{ij} \cdot f_s \tag{3.6}$$

where GBW_i is the GBW of the amplifier in the ith integrator, and k_{ij} are the scaling coefficients at the input of the ith integrator. In addition, the non-dominant pole ω_i can be modeled as a feedback delay which can be expressed as:

$$\tau_{Ai} = \frac{1 - e^{-\omega_i / f_s}}{\omega_i} \tag{3.7}$$

The finite GBW induced integrator gain error can be easily compensated. For the last integrator, this error is eliminated by the single-bit quantization, which makes

decision depending on the input polarity. For the preceding integrators, the gain error can be counteracted by adjusting the input gain of the next stage.

For the finite GBW induced delay, the compensation method is the same as treating ELD, which is tuning the scaling coefficients to restore the original loop filter. Therefore, the mixed-signal differentiating path can be used to compensate for both ELD and finite GBW induced delay. Note that iterative calculation has to be performed since the finite GBW induced delays depend on the scaling coefficients and vice versa [1].

In order to facilitate the transistor-level implementation of the op-amps, the GBW of all the three op-amps incorporated in the loop filter is set to $1.5\times f_S$. The finite GBW induced errors have been counteracted by the mixed-signal differentiating path, resulting in the scaling coefficients in Table 3.3.

Table 3.3: Scaling coefficients for the third-order modulator with ELD=$0.5/f_S$ and GBW=$1.5\times f_S$

k_{sig}	k_1	k_2	k_3	k_4	k_{res}	c_1	c_2
0.0982	0.0982	0.1662	0.3092	0.1410	0.0021	0.25	0.72

3.5 Verilog-A Based Behavioral Model of the CT $\Delta\Sigma$ Modulator

To validate the proposed architecture, behavioral simulations have been performed in the circuit simulator Spectre to examine the influence of a number of circuit-level non-idealities on the modulator performance, such as op-amp DC gain, gain bandwidth product (GBW), slew rate as well as the RC variation. Additionally, the minimum requirements on the amplifiers can be derived by simulating this behavioral model.

The architecture of the behavioral model is depicted in Fig. 3.13, and all building blocks are modeled in Verilog-A with independently controllable parameters. Fully differential operation not only suppresses the common mode noise, but also realizes

the sign changes in transfer functions through simple wire-crossing. Active *RC*-integrators are chosen to implement the loop filter to satisfy the requirement of high linearity. The ELD is set to half a sampling period, and has been compensated by adding DAC4 and a D-latch to realize the mixed-signal differentiating path around the quantizer. Note the feedback through k_3 and the non-delayed part of k_4 in Fig. 3.10 are merged into a combined DAC3 in Fig. 3.13, while the delayed part of k_4 is realized by DAC4 in Fig. 3.13. The feedback DACs are simply implemented by voltage controlled current sources, which provides feedback currents to the virtual ground nodes of the op-amps. In addition, all the op-amps in the loop filter have been implemented with a GBW of 3GHz ($1.5\times f_S$), and the finite GBW effect has been compensated within the loop filter design.

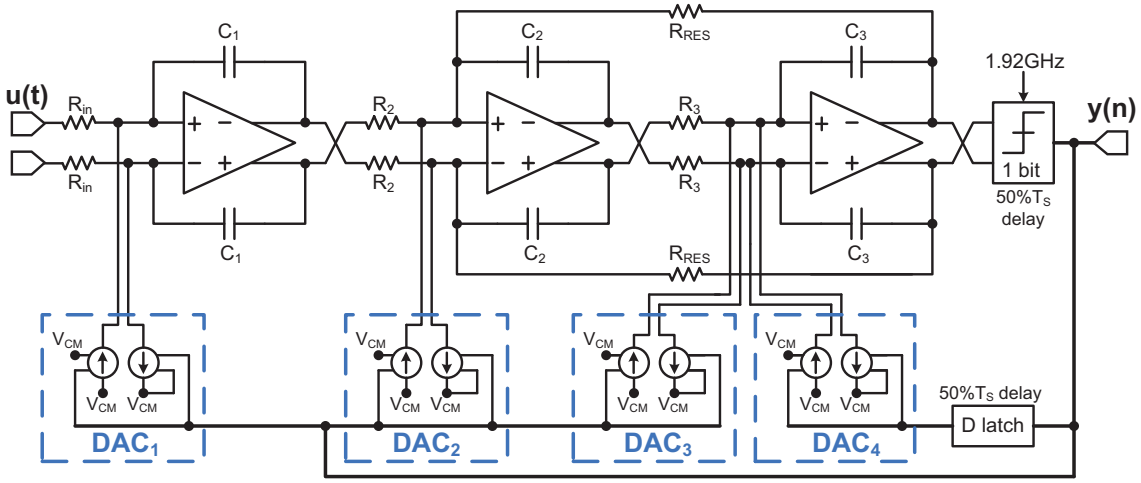


Figure 3.13: Architecture of the behavioral model

Lastly, Table 3.4 provides the implemented integrator resistor and capacitor values, which are mapped from the scaling coefficients in Table 3.3 with the sampling frequency of 1.92GHz.

3.5.1 Verification of the Finite GBW Compensation

In order to verify the finite GBW compensation, the Verilog-A based op-amps were set with a finite GBW of 3GHz ($1.5\times f_S$). The other properties of the op-amps were the same as an ideal amplifier, including extremely high DC gain, slew rate, and 90° phase margin (PM) induced by the single pole system model. The modulator was fed

Table 3.4: Passive component values for the third-order modulator; ELD=0.5/f_S and GBW=1.5×f_S for all op-amps

R	Value (Ω)
R_{in}	500
R_2	2.08K
R_3	723
R_{res}	247.88K

g_m	Value (µS)
g_{m1}	1998.6
g_{m2}	319.1
g_{m3}	593.7
g_{m4}	270.7

C	Value (pF)
C_1	10.6
C_2	1
C_3	1

with a -6dBFS sine wave at 2.75MHz while thermal noise was not activated in this simulation. The simulated spectrum is illustrated in Fig. 3.14, indicating that the modulator achieves 85.5dB SQNR. Compared to the spectrum of the ideal modulator shown in Fig. 3.14, a 3dB degradation in SQNR can be found. This is because the NRZ feedback scheme used in the DAC4 cannot completely compensate for the delay introduced by the finite GBW of the third op-amp, and a detailed analysis will be given in Section 6.1.1.

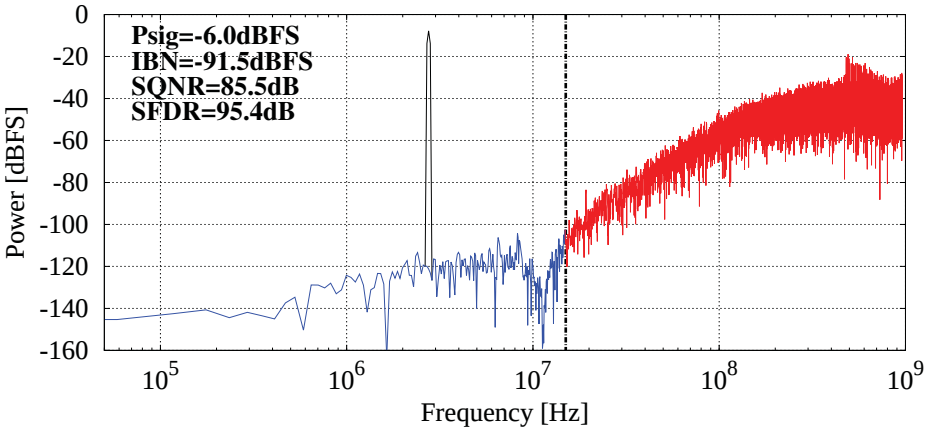


Figure 3.14: Simulated spectrum of the Verilog-A based modulator with ELD=0.5/f_S, GBW=1.5×f_S, ideal DC gain and ideal slew rate

3.5.2 RC Variation within the Modulator

In CT ΔΣ modulators implemented with active *RC*-integrators, the gains of integrators are mapped into resistor-capacitor products (*RC*-products) [16] [39], which vary greatly due to the combined effect of temperature and process variations. In

present sub-micron technologies, the absolute values of resistors and capacitors are subject to process variations in the order of 10-20%, introducing a possible variation of the RC-product of more than 30% [40]. Taking the additional effect of temperature variation into consideration, uncertainty in the RC-product becomes even larger. For such an active RC-integrator suffering from the RC variation, the integrator transfer function can be modeled as follows [1]:

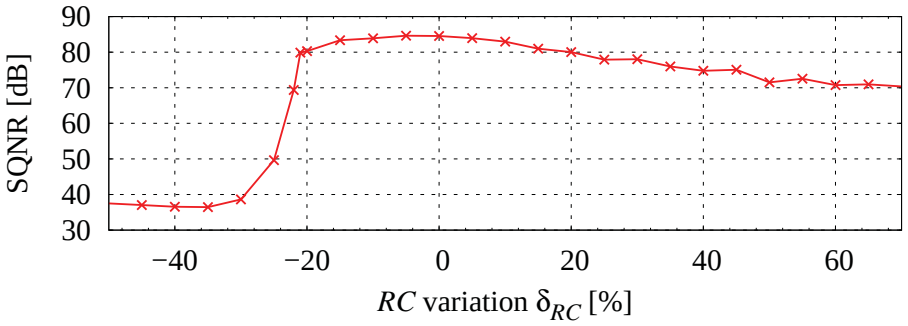
$$INT_i(s) = \frac{1}{s \cdot R_i C_i (1 + \delta_{RC})} = \frac{f_S}{s} \frac{k_i}{1 + \delta_{RC}} = GE_{RC} \cdot k_i \cdot \frac{f_S}{s} \tag{3.8}$$

where δ_{RC} is the RC variation and k_i is the integrator scaling coefficient. Apparently, an integrator gain error GE_{RC} has been introduced by the RC variation.

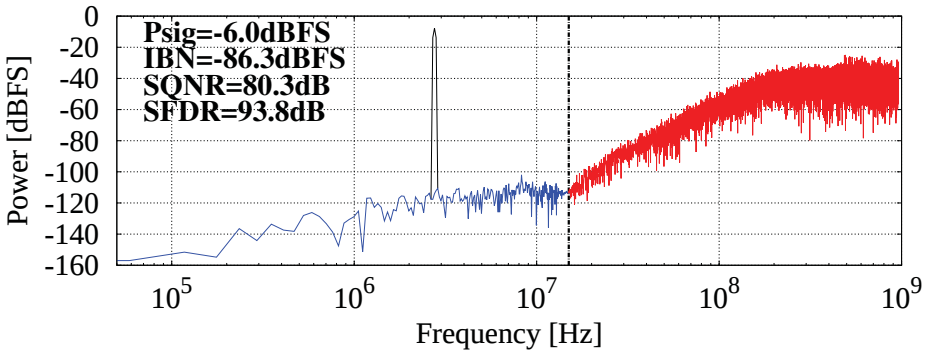
In the chosen architecture, the variation of integrator gains not only causes the deviation of the target location of the NTF poles, but also the zeros of the NTF. This is because in the proposed modulator the NTF zeros are optimally spread by the local resonator, k_{res}, which depends on the absolute value of the passive components.

In order to investigate the modulator robustness against integrator gain variations, the proposed architecture was simulated with an input signal of -6dBFS at 2.75MHz. It can be seen that the location of the spectral notch - the NTF zero - changes as the RC-product varies, as illustrated in Fig. 3.15 (b) and (c). Additionally, a degrading in SNDR can be observed for $\delta_{RC} > 0$ in Fig. 3.15 (a), since a positive shift of the RC-product reduces the integrator gain, leading to a less aggressive noise-shaping behavior. In contrast, as the RC-product decreases from the nominal value, the SNDR experiences a slight increase, followed by a drastic degradation since the simulated third-order modulator becomes unstable for $\delta_{RC} < -20\%$. The negative shift of the RC-product yields more aggressive noise shaping, but eventually lead to instability caused by an insufficient scaling [1].

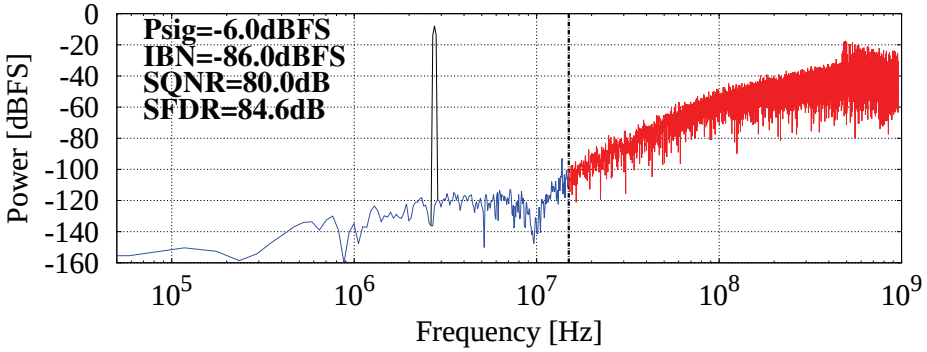
Fig. 3.15 (a) also reveals that the RC-product variation of this modulator can deviate as much as ±20% from its nominal value with guaranteed SQNR above 80dB. Note in this simulation, all the RC-products are assumed to vary with the same spread, which is not true in practice since the absolute value of the resistor and capacitor varies independently in real implementations. In order to achieve optimal



(a) Simulated SQNR as a function of RC variation δ_{RC}



(b) RC variation $\delta_{RC} = -20\%$



(c) RC variation $\delta_{RC} = +20\%$

Figure 3.15: Simulated Verilog-A based modulator in Fig. 3.13 over RC variation

performance, an adoption of integrator gain tuning is required. In this work, the integrator gains are trimmed by a tunable capacitor array, which will be discussed in Section 4.1.6.

3.5.3 Op-amp DC Gain Requirement

For an active RC-integrator implemented with an ideal op-amp, its transfer function is given by:

$$ITF(s) = \frac{k_i f_S}{s} \tag{3.9}$$

where k_i is the integrator scaling coefficient. However, the op-amp features a finite DC gain in practical realizations, leading to a nonideality known as leaky integration. Consequently, the virtual ground node of the integrator moves and current flows through every input resistor connected to it. Taking the finite op-amp DC gain A_{DC} into account, the transfer function of the ith input path of an RC-integrator can be derived as [33]

$$ITF_{A_{DC}}(s) \mid_i = \frac{k_i f_S}{s(1+\frac{1}{A_{DC}}) + A_{DC}\sum_{l=1}^{N} k_l f_S} \tag{3.10}$$

Apparently, not only the DC gain of the integrator but also the pole location is affected by the finite op-amp gain. The pole of the integrator is displaced away from its ideal DC position. As a consequence, the NTF zeros are shifted from DC to higher frequency, degrading the noise shaping behavior of the modulator.

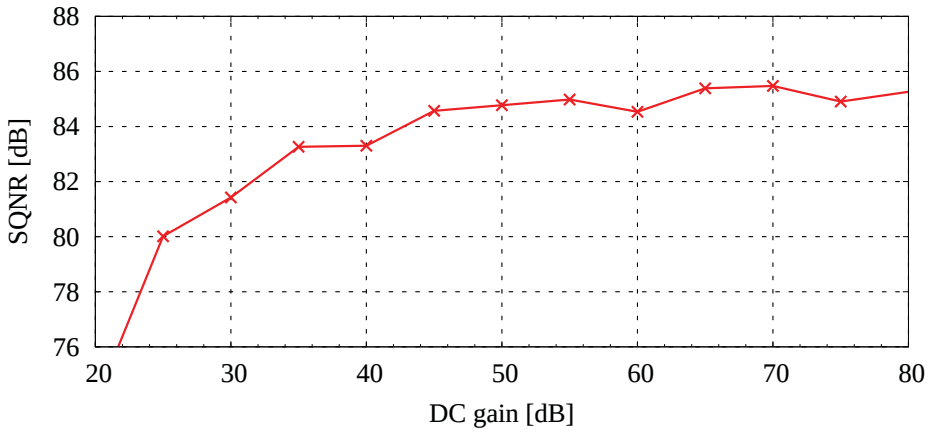


Figure 3.16: Schematic of the first op-amp

As a rule of thumb, the DC gain of the op-amps in a single-loop modulator should be in the range of the OSR to guarantee sufficient noise shaping [41] [42]. In order to investigate the effect of finite op-amp DC gain on the chosen single-loop modulator, transient simulations were carried out. In this simulation, all the DC gain of op-

amps are swept with the same spread. As illustrated in Fig. 3.16, when the op-amp DC gain is equal to OSR, the modulator achieves an SQNR of 83dB, which is only 5dB lower than the ideal case. However, the small value of op-amp DC gain imposes a stringent requirement on the op-amp's linearity, thus the minimum DC gain of the op-amp is set to 55dB in this work. The trade-off of op-amp gain, GBW and linearity will be further looked at in Chapter 7.

3.5.4 Op-amp Slew Rate Requirement

Another dynamic limitation of the op-amp is the finite slew rate. This issue stems from the limited biasing current, which is available to charge or discharge the integrating capacitor or the internal frequency compensation capacitor. Since the slew rate limitation is a nonlinear effect, it introduces harmonic distortions and increases the in-band noise floor [43] [44]. In order to achieve an optimum performance, the slew rate effect should be dealt with carefully, especially in a single-bit modulator. This is because the slew rate influence is highly signal dependent. In a single-bit modulator, the slew-rate requirement is more stringent, compared to the multi-bit implementation where the input signals to the integrators are reduced [45]. For the chosen single-bit modulator with NRZ feedback pulses, the required slew rate of an integrator can be approximated by [1]:

$$SR = f_S \cdot V_{in} \mid_{max} = f_S \cdot (\sum_{i=1}^{m} k_i \mid_{fb} \cdot V_{ref} + \sum_{i=1}^{n} k_i \mid_{fw} \cdot V_{fw} \mid_{max}) \tag{3.11}$$

where V_{ref} is the reference voltage, V_{fw} are forward signals from the proceeding stage, while $k_i \mid_{fb}$ and $k_i \mid_{fw}$ are the feedback and feed-forward scaling coefficients respectively. Table 3.5 lists the calculated slew rate requirement according to Eq.3.11. It should be noted that Eq.3.11 only gives an approximated calculation of the required slew rate, since the error suppression is not taken into account when calculating for op-amp2 and op-amp3. The finite slew rate induced errors in the integrators after the first one are suppressed by the respective preceding loop filters. Therefore, behavioral simulations should be performed to figure out the minimum slew rate requirements on the op-amps.

Table 3.5: Calculated slew rate requirement according to Eq.3.11

	Op-amp1	Op-amp2	Op-amp3
Slew rate (V/µs)	754	826	2285

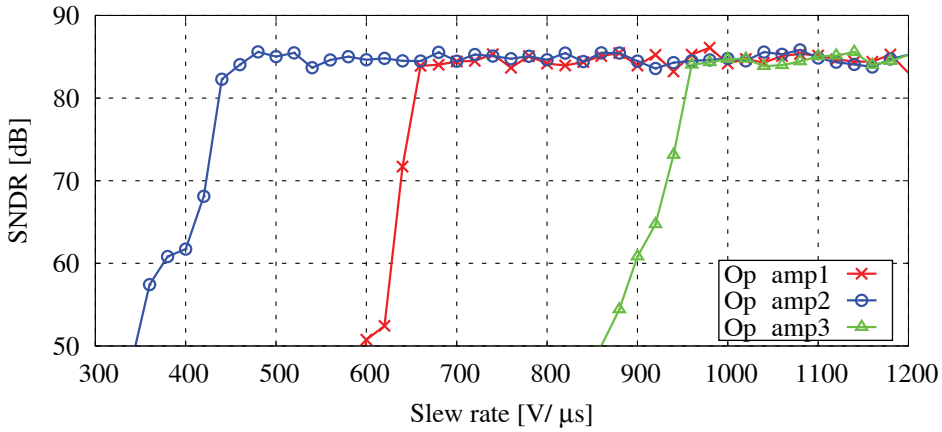


Figure 3.17: Slew rate requirement of each op-amp within the modulator; GBW=1.5×f_S

Fig. 3.15 shows the simulated SNDR of the proposed modulator versus the op-amp's slew rate. A -6dBFS input tone at 2.75MHz was applied to the modulator input, and all the op-amps feature a finite GBW of 1.5×f_S. Op-amp1 requires a slew rate larger than 700V/µs, which matches well with the calculated value of 754V/µs from Eq.3.11. For op-amp2 a slew rate as low as 500V/µs is sufficient to avoid degrading the SNDR performance. The slew rate requirement on the second amplifier is relaxed compared to the first one, since the errors induced by finite slew rate are suppressed by the preceding filter. Additionally, the op-amp3 in the last integrator has to fulfill the most stringent slew rate requirement of approximately 1000V/µs, which corresponds to $0.5V_{ref}f_S$. This is because more input signals are summed at the last integrator input with larger scaling coefficients, compared to the preceding two stages. Furthermore, the fast settling demand of the employed ELD compensation path also imposes tough slew rate requirement on the last op-amp for stability reasons.

3.5.5 Summary of Op-amps Requirements

By simulating the Verilog-A based modulator, the minimum requirements on the op-amps - such as DC gain and slew rate - can be determined by iteratively decreasing their values until the performance of the modulator starts to decrease. A summary of the required amplifier specifications is shown in Table 3.6. All amplifiers should be designed to feature a GBW of 3GHz ($1.5\times f_S$) while the phase drop and gain error due to the finite GBW have been compensated within the architecture [31]. In addition, all the op-amps should provide at least 55dB DC gain to achieve a reasonable linearity. Lastly, different slew rate requirements should be satisfied for these three op-amps. The second op-amp should meet the most relaxed slew rate constraints, while the last op-amp has to fulfill the most stringent requirement on the slew rate due to a higher scaling coefficient as well as the employed ELD compensation path within it.

Table 3.6: Requirements on Op-amps

Performance	Op-amp1	Op-amp2	Op-amp3
GBW (GHz)	3	3	3
DC gain (dB)	55	55	55
Slew rate (V/µs)	700	500	1000

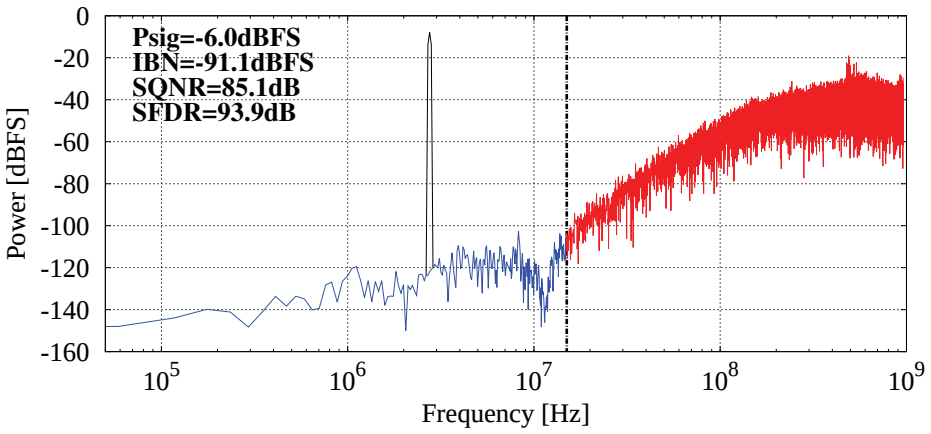


Figure 3.18: Simulated spectrum of the Verilog-A based modulator with ELD=$0.5/f_S$ and Op-amp specifications listed in Table 3.6

Transient simulation has been performed for the Verilog-A based behavioral modulator when the op-amps are set with the specifications in Table 3.6. Fig. 3.18 depicts the simulated spectrum, indicating that the modulator achieves a 85.1dB SQNR. Compared to the case when the op-amps feature extremely high DC gain and slew rate, only 0.4dB SQNR degradation can be found. If the specifications listed in Table 3.6 are reduced further, the performance of the chosen ΔΣ modulator would decrease significantly. Since the minimum requirements on the op-amps have been derived, the transistor-level implementation can start, which will be described in the next chapter.

Chapter 4

A 15MHz BW CT $\Delta\Sigma$ Modulator

This chapter presents the transistor-level implementation and experimental results of a CT 15MHz third-order low-pass $\Delta\Sigma$ modulator, following the system-level design described in Chapter 3. The proposed $\Delta\Sigma$ modulator operates at 1.92GHz, taking advantage of the high transit frequency of a low-cost 0.25µm SiGe BiCMOS process. In order to achieve high linearity, single-bit quantization is incorporated, which is inherently linear and therefore no digital DAC linearity enhancement technique is required.

This chapter covers the design of op-amps, DAC elements, a single-bit quantizer and other supporting blocks. As the transistor-level design progresses, the Verilog-A based building blocks in the behavioral modulator model presented in Section 3.5 are gradually replaced by transistor-level implementations. In order to guarantee that the implemented $\Delta\Sigma$ modulator meets the design requirements, the performance of the circuit-level realization is analyzed and verified in the behavioral modulator model while retaining other blocks at abstraction-levels using Verilog-A. Once the transistor-level building blocks are verified, layouts are created and post-layout simulations are performed. Finally the prototype chip was fabricated in IHP 0.25µm SiGe BiCMOS process, and an evaluation board was designed to perform the measurement. The experimental chip achieves a dynamic range of 70dB with an SFDR of 78.1dB for a signal bandwidth of 15MHz. It dissipates 215.9mW and occupies an active area of 0.4mm^2.

4.1 Transistor-Level Implementation

In this section, the transistor-level implementation of the continuous-time ΔΣ modulator will be described. Fig. 4.1 illustrates the circuit diagram of the implemented modulator. Active *RC*-integrators are chosen to implement the loop filter for high linearity, and all the three op-amps feature a finite GBW of $1.5\times f_S$. Single-bit quantization is incorporated not only to simplify the circuit-level implementation, but also to avoid DAC linearization techniques, which would be costly in the target 0.25µm SiGe technology.

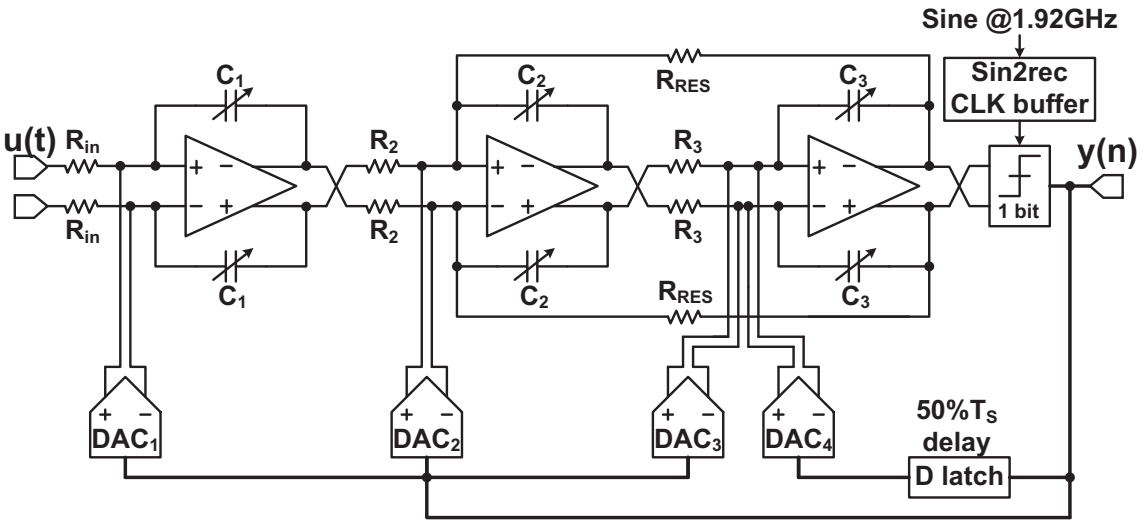


Figure 4.1: Architecture of the CT single-bit ΔΣ modulator

In this work, a sinusoidal to rectangular (sin2rec) clock buffer is required to provide a low jitter rectangular clock at 1.92GHz for the single-bit quantizer from an off-chip generator to the on-chip modulator. In order to provide the quantizer with sufficient time to make a decision, one D-latch is placed at the quantizer output to set the ELD to half a sampling period ($50\%T_S$). Note the output of the feedback DAC4 was delayed by another $50\%T_S$. As a consequence, a mixed-signal differentiating path through DAC4 and DAC3 is realized from the quantizer output to the input of the last integrator. Thanks to this mixed-signal differentiating path, not only the $50\%T_S$ ELD but also the influence of finite GBW can be compensated to restore the original noise shaping behavior. Additionally, all the integration capacitors in

this modulator can be calibrated with a tuning range of ±30% to cover RC-product variations.

4.1.1 Op-amps

The loop filter of the ΔΣ modulator incorporates three active RC-integrators. The op-amp in each integrator has the same topology for the sake of reusability, which is a fully differential two-stage Miller-compensated architecture, as shown in Fig. 4.2. NPN HBT transistors are applied in the high-frequency signal path, since the MOSFET in the target 0.25µm SiGe BiCMOS technology only provides a transit frequency of around 35GHz, which is too slow to fulfill the op-amp GBW requirement of 3GHz. All the HBTs are biased at 6.5mA/µm^2, corresponding to the peak f_T current density of 110GHz.

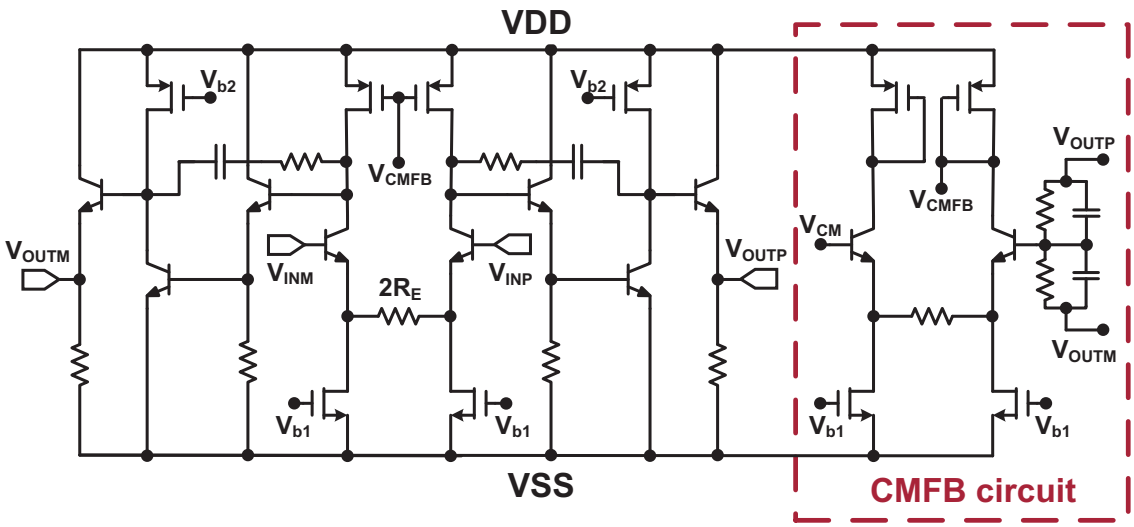


Figure 4.2: Schematic of the op-amps

In analyzing the input stage, emitter degeneration is applied to fulfill the slew rate requirement while achieving a GBW of 3GHz. Here, the input tail current is increased by a factor of $1+g_mR_E$, giving an increased slew rate. The input differential pair is biased by two tail current sources due to the limited voltage headroom. Furthermore, PMOS current mirrors serve as active load due to the absence of PNP transistors in the chosen technology. Between the two stages, emitter followers are inserted as level shifters. Additionally, emitter followers are also employed at the output as buffers

to reduce the output impedance while providing an appropriate DC voltage level for the next stage.

The common mode feedback (CMFB) circuit is composed of two polysilicon sensing resistors and a single stage op-amp, which is similar to the input stage but with diode connected loads. Thanks to the emitter follower at the output, a small common-mode sensing resistor can be used without degrading the DC gain. Furthermore, a small capacitor is placed in parallel to the common-mode sensing resistor to ensure that the CMFB loop is stable. By adopting the CMFB circuit, the op-amp outputs are referred to a common mode voltage of 1.25V, thus the op-amp output swing can be maximized at a supply voltage of 2.5V.

All three op-amps feature a GBW of 3GHz ($1.5\times f_S$), and this finite GBW has been compensated within the loop filter design. [1] [31]. In this work, the second integrator employs the same op-amp design used in the first integrator due to the limited design time, and this op-amp is called op-amp1. For the third op-amp (op-amp3), the topology is the same but the biasing current has been adjusted, since it has to fulfill a more stringent slew rate requirement compared to the preceding stages, as mentioned in Section 3.5.4.

The commonly used test configuration for the AC response is to connect the designed op-amp as a unity gain buffer, but only the DC output can be fed back so that the op-amp can be biased correctly. Then the loop can be broken to determine the op-amp's DC gain, GBW as well as PM [46]. This approach, named Breaking-the-Loop method, is suitable in dealing with low frequency designs, but it can lead to lower than simulated GBW and PM when designing high speed op-amps used in a feedback system. This is because when the loop is broken, the AC impedances seen by both input and output of the op-amp are different from that in the closed-loop case, i.e. due to the broken loop, the parasitic capacitor at the input cannot be seen by the output, while the input is not loaded by any impedance from the output [47].

In order to accurately determine the op-amp's frequency response, the op-amp must be simulated in the actual feedback configuration in which it is used [48] [49] [50]. In this work, the Tian's Method [51] [48] is utilized, considering not only the capacitive load from the next stage, but also the self-loading of op-amp input, as well as the

feedback DAC capacitor. It is important to note that the input self-loading and the DAC capacitor are not taken into account in the Breaking-the-Loop method.

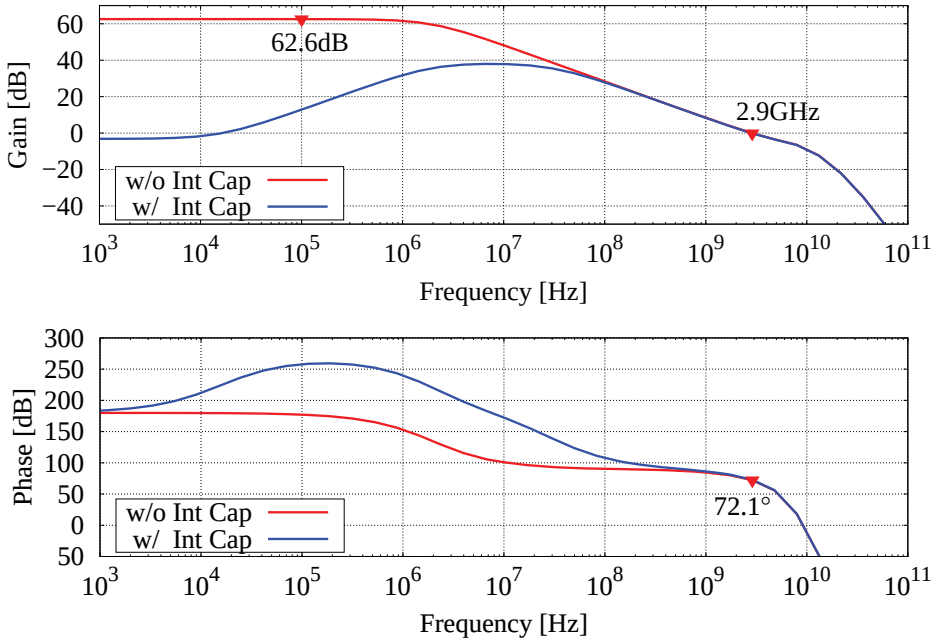


Figure 4.3: Simulated frequency response of the op-amp1

Fig. 4.3 demonstrates simulated loop gain when the first integrator is implemented by op-amp1. The GBW and phase margin can be determined when including the integration capacitor in the feedback, while the DC gain of the op-amp can be derived by shorting out the integration capacitor. Note in the op-amp design, it is required that the two curves e.g. with and without integration capacitor, overlap at high frequencies, otherwise the op-amp have to be re-compensated [51]. In addition, the loop gain including the integration capacitor bends down to zero at low frequencies. This is because a RC high-pass characteristic is offered by the integration capacitor as well as the input resistor of the integrator.

As shown in Fig. 4.3, op-amp1 typically achieves a GBW of 2.9GHz with 72.1° PM. The DC gain is 62.6dB and the slew rate obtained is 800V/µs for some safety margin. Apparently, this design satisfies the op-amp requirement derived in Section 3.5.4. After layout and parasitic extraction, a Monte Carlo analysis consisting of 500 simulations was carried out to check the effects of mismatch and process variations. As illustrated in Fig. 4.4, the DC gain of this op-amp1 features a mean of 62dB with a standard deviation of 9.5dB. Referring to the GBW, this op-amp has a mean

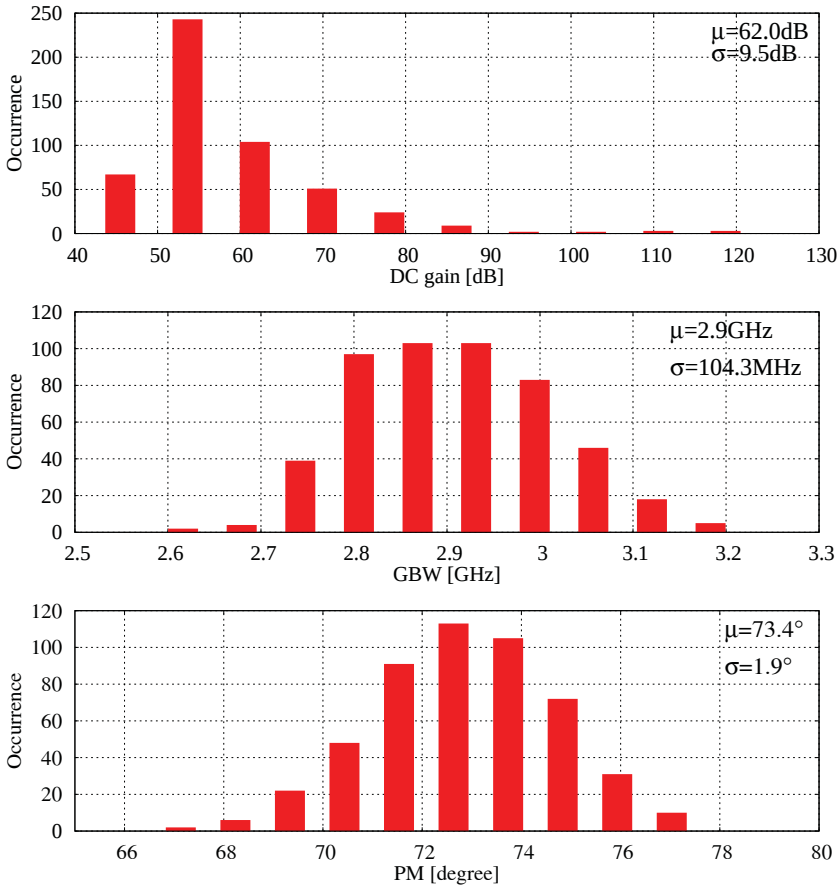


Figure 4.4: Histogram of the op-amp1's frequency response (500 Monte Carlo runs)

GBW of 2.9GHz with σ = 104.3MHz. Furthermore, the standard deviation of the PM is only 1.9° at a mean of 73.4°, indicating a good robustness against process variation and mismatch.

Similarly, the frequency response of op-amp3 has also been investigated. As illustrated in Fig. 4.5, this op-amp typically features a DC gain of 58.8dB, a GBW of 3GHz as well as a PM of 72.1°. The simulated slew rate is 1200V/μs, which is higher than the preceding stages in order to drive the following quantizer as well as the fast ELD compensation path. Additionally, Fig. 4.6 shows the histograms of a Monte Carlo simulation with 500 runs performed on the parasitic-extracted op-amp3. It can be seen that this op-amp achieves a mean value of 56.4dB for DC gain, 3GHz for GBW, and 67.3° for PM, whereas the corresponding standard deviations are 9.7dB, 104.1MHz and 1.6°, respectively.

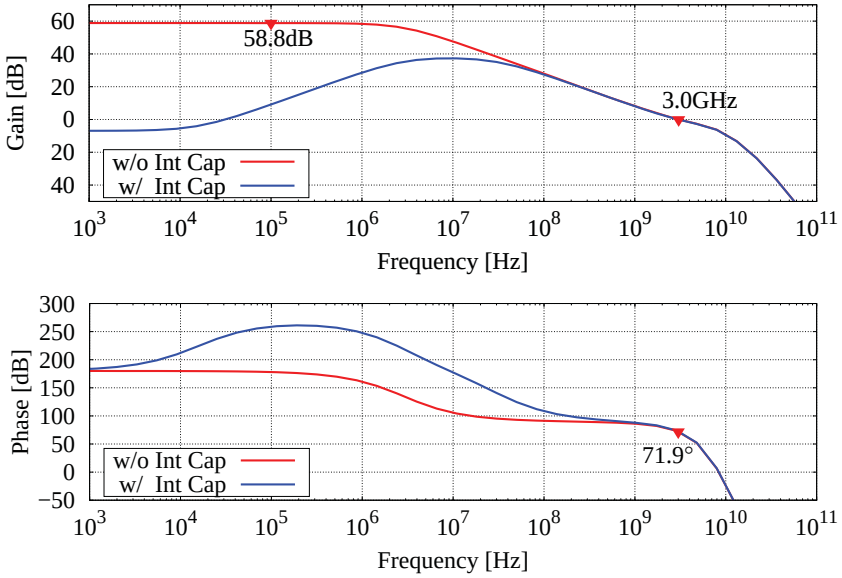


Figure 4.5: Simulated frequency response of the op-amp3

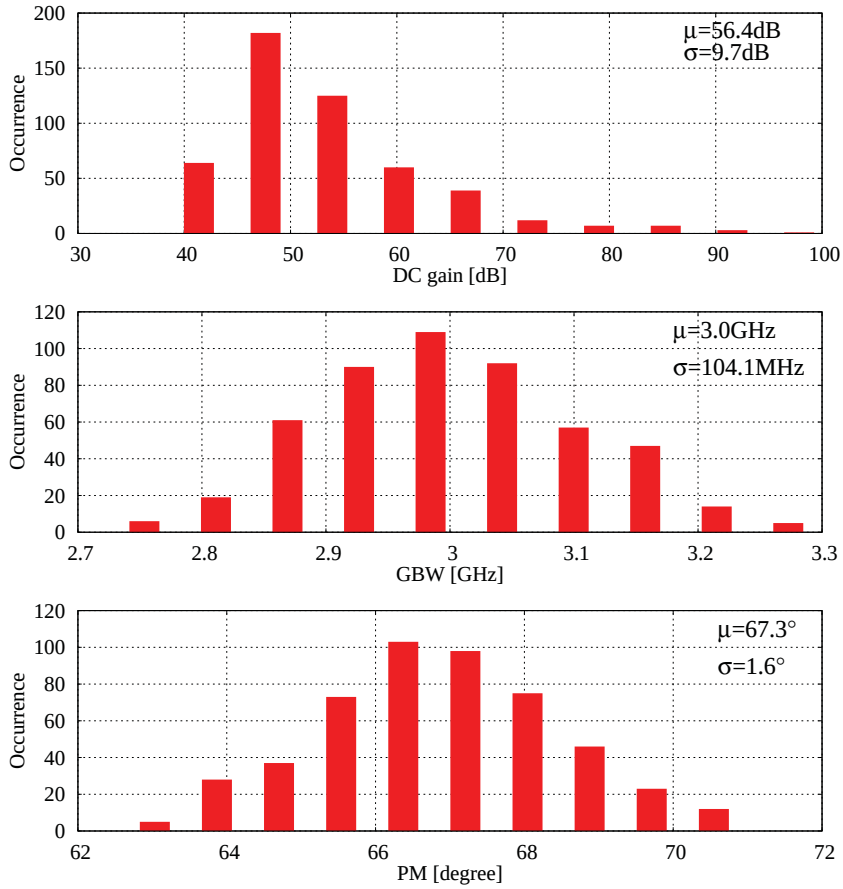


Figure 4.6: Histogram of the op-amp3's frequency response (500 Monte Carlo runs)

In the op-amp design, the HBTs are biased at the maximum f_T current density of 6.5mA/μm^2 in order to achieve a high GBW. The designed op-amp1 consumes 30.3mW from a 2.5V supply, while the power consumption for op-amp3 is 30.7mW. Most of the power is dissipated by the emitter followers. As it will be discussed in Section 6.2, the HBTs in emitter follower do not have to be biased at the peak f_T current density, consequently the power consumption in the op-amps could be reduced significantly while satisfying the system requirement.

4.1.2 Single-Bit Quantizer

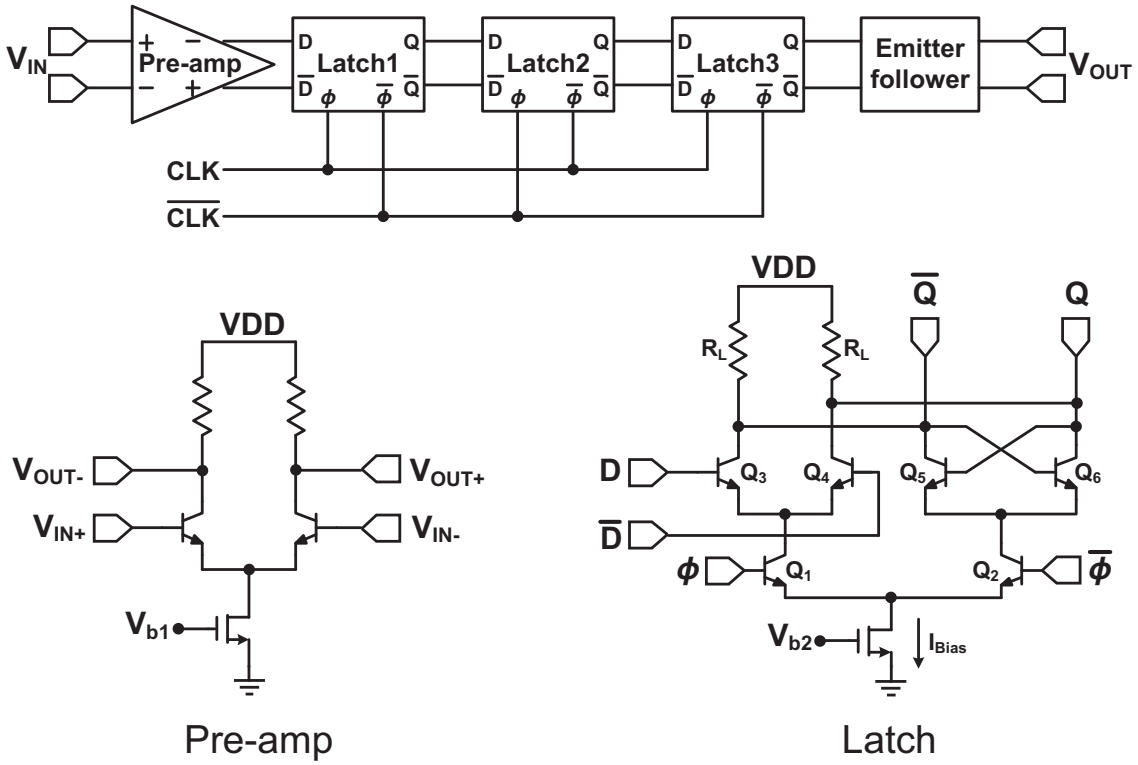


Figure 4.7: Schematic of the single-bit quantizer

The single-bit quantizer is realized based on the conventional emitter-coupled logic (ECL) master-slave latched comparator. In order to reduce the errors imposed by quantizer metastability, a third latch (latch3) is placed at the output of the conventional master-slave comparator to realize a single-bit quantizer in this design [52] [53]. As illustrated in Fig. 4.7, this single-bit quantizer consists of one pre-amplifier, three cascaded latches as well as emitter followers. The biasing circuit

of the pre-amplifier is separated from the latch biasing in order to reduce the clock feed-through via the tail current sources.

The pre-amplifier, which is a simple HBT differential pair with resistive load, improves the sensitivity to small input signals and suppresses the kick-back noise from the sampling clock. In addition, although the voltage swing at the pre-amplifier input is larger than 1 $V_{pp\text{-}diff}$, the pre-amplifier provides a limited output voltage swing, which guarantees a high speed operation by preventing transistors in the first latch from entering saturation region. The HBTs in the pre-amplifier are biased at the maximum f_T current density of 6.5mA/µm^2, and consequently the pre-amplifier provides a DC gain of 22.3dB over a -3dB bandwidth of 3.3GHz for a capacitive load of 50fF (an estimation of input capacitor for the latch stage). Additionally, this pre-amplifier achieves a GBW of 35.8GHz with a PM of 60.9°, as indicated in Fig. 4.8.

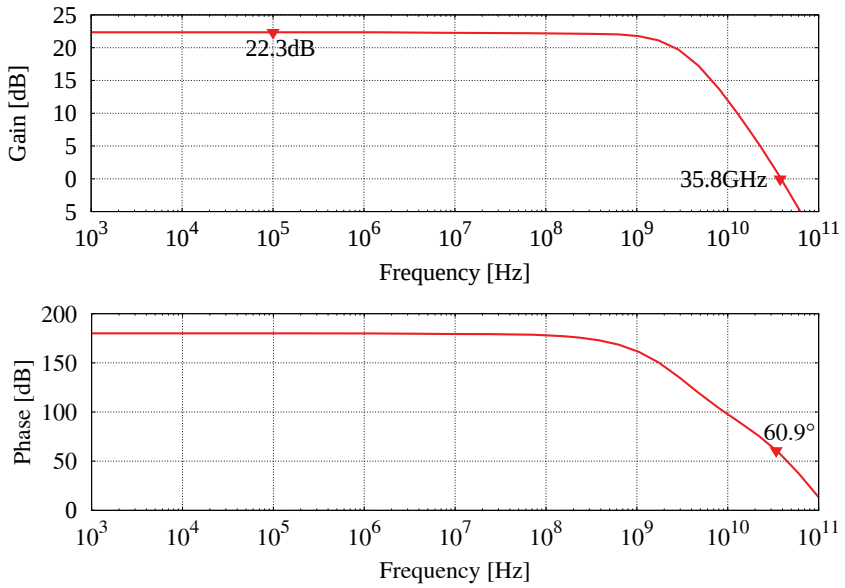


Figure 4.8: Simulated frequency response of the pre-amplifier

All latches in the single-bit quantizer have the same architecture, which is shown in Fig. 4.7. The latch has two modes of operation: tracking mode and latching mode. When ϕ is high, the latch is in the tracking mode and the tracking pair (Q_3 and Q_4)

amplifies the input signal. In this process the latch recovers from a full digital swing to the input determined value δv. The recovery time can be expressed as [54]

$$t_{rec} = R_L C_{total}(1 + \frac{1}{tanh(V_{in}/2V_T)}) \tag{4.1}$$

where R_L is the loading resistor, C_{total} is the total capacitance at the collector of the tracking pair, and V_T is the thermal voltage. Apparently, the recovery time t_{rec} is proportional to the loading resistor R_L.

At the falling edge of ϕ, the latch enters the latching mode. The latch pair (Q_5 and Q_6) starts to regenerate and further amplifies the initial voltage difference δv until it is fully switched to the full scale output logic level ΔV, where ΔV equals to $I_{Bias} \cdot R_L$. The regeneration time constant of the latch is given by [54]

$$\tau_{reg} = \frac{R_L C_{total}}{g_m R_L - 1} \tag{4.2}$$

where g_m is the transconductance of the latching pair. This regeneration time constant is much shorter than the latch recovery time, so that a small loading resistor R_L is desired in order to optimize t_{rec} [54]. However, a small R_L will reduce the voltage swing at the latch output and consequently degrade the current switching operation in the following differential pair. As a result, a compromise has to be found. In order to obtain an optimal speed, the HBTs in the latch are biased at peak f_T current density of 6.5mA/μm^2 when all the tail current I_{Bias} is switched to one side [55]. Based on simulations, the value of R_L is set to 50Ω, which results in a 300mV output voltage swing with a recovery time of 57ps for a 1mV input.

A cascade of three latches increases the quantizer gain and reduces the effect of metastability [53]. These three latches are driven by different clock phases, and are configured in a master-slave-master configuration [56]. Consequently, a delay of half a sampling clock period has been introduced. This ELD is compensated by using the mixed-signal differentiating path from the quantizer output to the input of the last integrator with proper coefficient tuning, as described in Section 4.1.6.

Fig. 4.9 shows the timing diagram of the quantizer as well as latch4, which is located at the quantizer output to assume a 50%T_S delay for DAC4. The cascaded latches

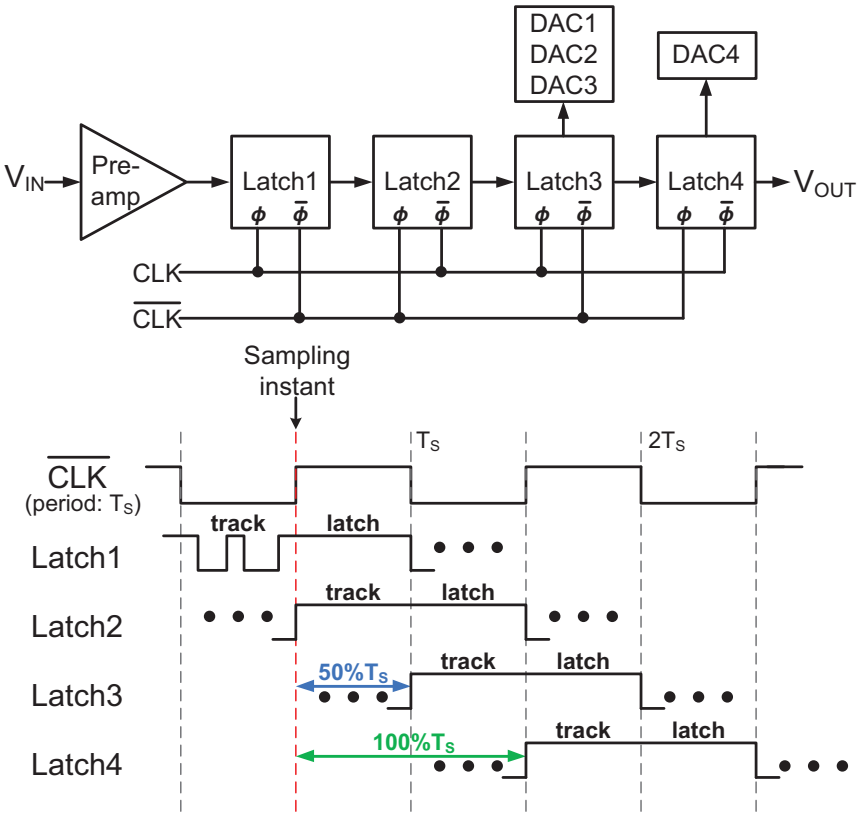


Figure 4.9: Timing diagram of the single-bit quantizer followed by latch4

in the quantizer operate as follows. When clock is high, latch1 tracks the input, and regeneratively amplifies the input until the falling edge of the clock. When clock is low, latch1 goes into the latch mode, while latch2 tracks the output of latch1, which is a locked digital value. In the next clock phase, latch2 is isolated from its input, and enters the latch mode. Therefore, the output of latch2 remains constant for one clock period, generating one digital signal. Similarly, latch3 is clocked in such a way that it tracks the latched signal of latch2 during its tracking mode. The output of latch3 is a replica of latch2, but delayed by half a sampling period. Finally, the same digital signal appears at the output of latch4 with a delay of one sampling period. The output of latch3 is fed into DAC1, DAC2 and DAC3 through emitter followers, while latch4 drives DAC4 to perform the ELD compensation.

The single-bit quantizer exhibits an input sensitivity of 1mV at 500MHz input frequency with a sampling frequency of 1.92GHz. Fig. 4.10 shows the waveforms of the quantizer when the input is a 1mV square wave, and transient noise is activated in the simulation. The quantizer is driven by a clock generated by a sin2rec clock

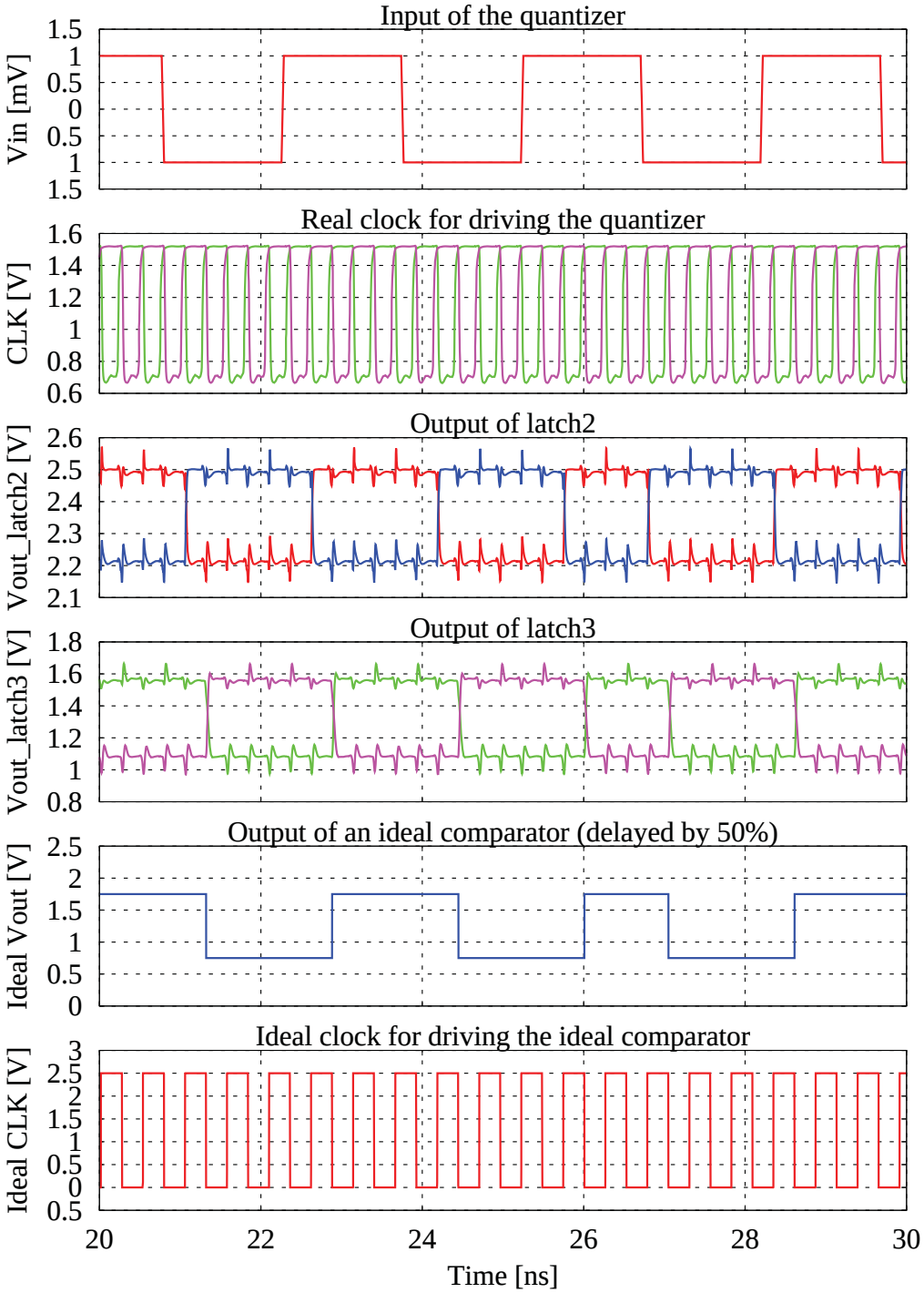


Figure 4.10: Transient response of the single-bit quantizer

buffer, which will be described in Section 4.1.5. Both outputs of latch2 and latch3 are shown and apparently the latch3 output is delayed by half a sampling period. The common mode voltage difference between the output of latch2 and latch3 is due to the emitter followers at latch3 output which are introduced to drive the feedback DACs. In addition, the same input signal has been applied into an ideal comparator with a delay of $50\%T_S$. The ideal comparator is driven by an ideal clock and it generates the same digital output, proving the sensitivity of the designed single-bit quantizer.

4.1.3 Feedback DAC

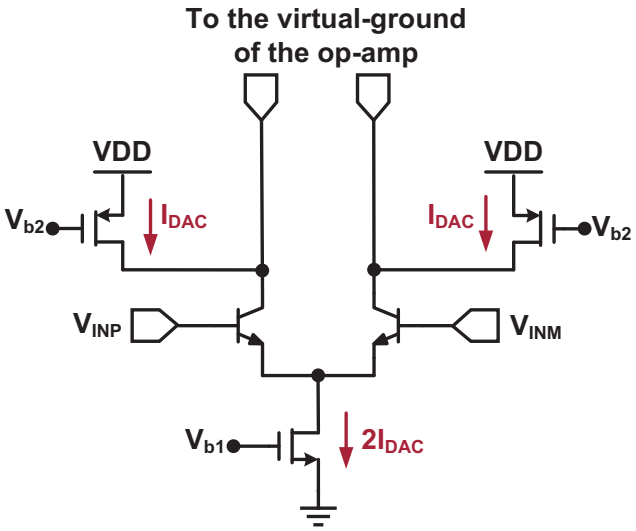


Figure 4.11: Schematic of the feedback DAC

In this modulator, rectangular feedback pulses in a NRZ implementation are incorporated to simplify the high speed circuitry. The two-level single-bit feedback DAC features inherent linearity, and thus no complicated linearization technique is required.

Fig. 4.11 shows the schematic of the NRZ DAC, which consists of two current sources conducting a current of I_{DAC}, and a differential pair with a tail current of $2I_{DAC}$ [5]. Depending on the output state of the single-bit quantizer, the tail current of the differential pair can be switched between the two output branches of the DAC to provide a virtually bi-directional current to the virtual ground of the op-amps.

Additionally, large on-chip bypass capacitors are placed at the gate of the current mirrors to suppress noise.

After the transistor-level implementation of the DACs, they are used to replace the corresponding building blocks in the Verilog-A based modulator to verify if they fit into the modulator. Fig. 4.12 shows the post-layout simulated spectrum of the modulator when only the first DAC and a ECL D-latch as the DAC driver are transistor-level implemented including parasitics, while the other building-blocks are ideal Verilog-A models. In this simulation the transient noise is activated, and an -6dBFS input signal at 2.75MHz has been applied at the modulator input. It can be seen that no harmonic distortion is visible in the spectrum; therefore, there are no mismatched rise and fall times for the DAC pulses. Additionally, the SNDR is limited to 79.4dB due to the noise from the input resistor as well as the first feedback DAC. The first DAC is the most dominant noise source of the modulator. In order to limit the noise contributed by the first DAC, the value of the input resistor has to be chosen small, which will be discussed in the next section.

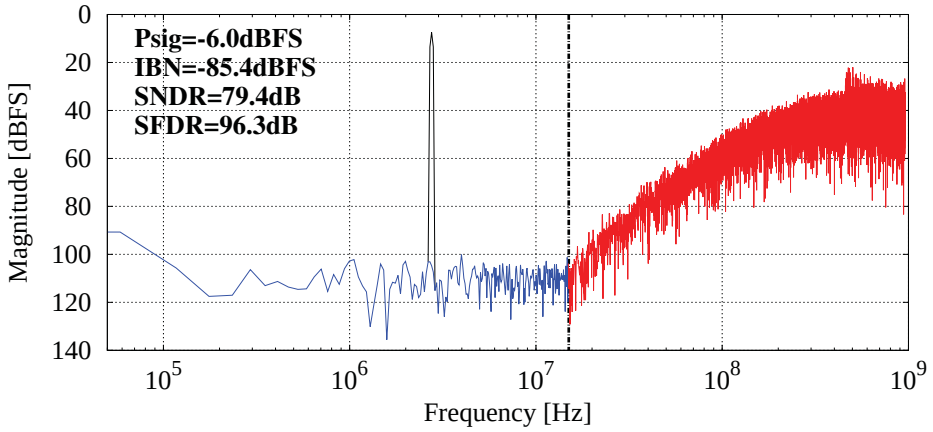


Figure 4.12: Simulated spectrum of the modulator when only the first DAC and a ECL D-latch as the DAC driver are transistor-level implemented

4.1.4 Noise of the Input Resistor

The optimal value of the input resistor R_{in} is a trade-off between feedback capacitor size, DAC current and noise [57]. In this architecture, the first DAC is the dominant

noise contributor. To reduce the noise form the first DAC, the input resistor can be chosen as a smaller value. The reason is given by the following.

If the input resistor value halves, the feedback current I_{DAC} is doubled. Since $g_m = \frac{2I}{V_{GS}-V_T}$, the transconductance of the current source is doubled for a constant overdrive voltage. Thus the current noise of the DAC is doubled due to $\bar{i}^2_{n,DAC} = 4KT \cdot \frac{2}{3} g_m \cdot \Delta f$. Consequently, at the input of the $\Delta\Sigma$ modulator, the accumulated IBN is reduced by a factor of 2 since $IBN = \bar{i}^2_{n,DAC} \cdot R^2_{in} \cdot BW$, which means the IBN drops by 3dB and the SNDR is improved by the same amount.

Therefore, the input resistor R_{in} was set to 500Ω to reduce the noise generated by the first DAC. Transient simulations show that the SNDR of the modulator is limited to 82.4dB by the thermal noise from the resistors. However, even for such a small input resistor, the first DAC is still the dominant noise source, as shown in Fig. 4.12.

4.1.5 Sin2rec Clock Buffer

In order to provide a 1.92GHz low jitter clock for the single-bit quantizer, a sin2rec clock buffer has been designed to convert a 1.92GHz low jitter differential sine wave to a rectangular signal. The schematic of the clock buffer is shown in Fig. 4.13. It consists of a differential pair with resistive load and emitter followers as output buffer. Since the switches in the quantizer are realized by emitter coupled (EC) pairs, customized rectangular clock levels at 1.92GHz are required to turn on and off the EC pairs periodically.

As shown in Fig. 4.14, the common mode voltage of the differential input signal is 1.5V. The waveform of the input signal is not purely sinusoidal since a bonding wire model has been inserted at the clock buffer input to include parasitic effects of the bonding wire. For the output signal of the clock buffer, the high voltage level is around 1.5V while the low level is around 0.7V in order to achieve sharp rising and falling edges. The difference between the high level and the low level of the clock output should not be too large, otherwise one HBT in the EC pairs of

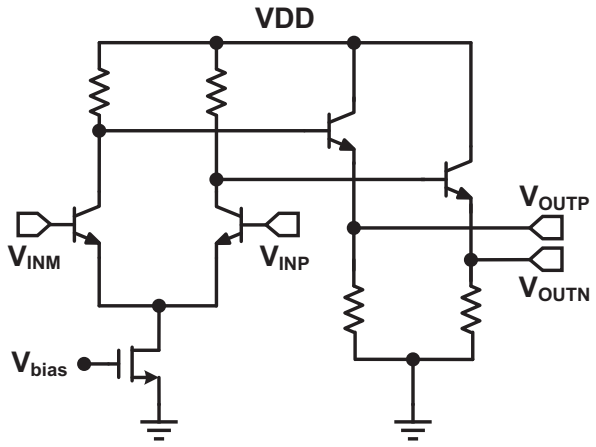


Figure 4.13: Schematic of the sin2rec clock buffer

the quantizer would enter saturation region and consequently the switching speed would be reduced.

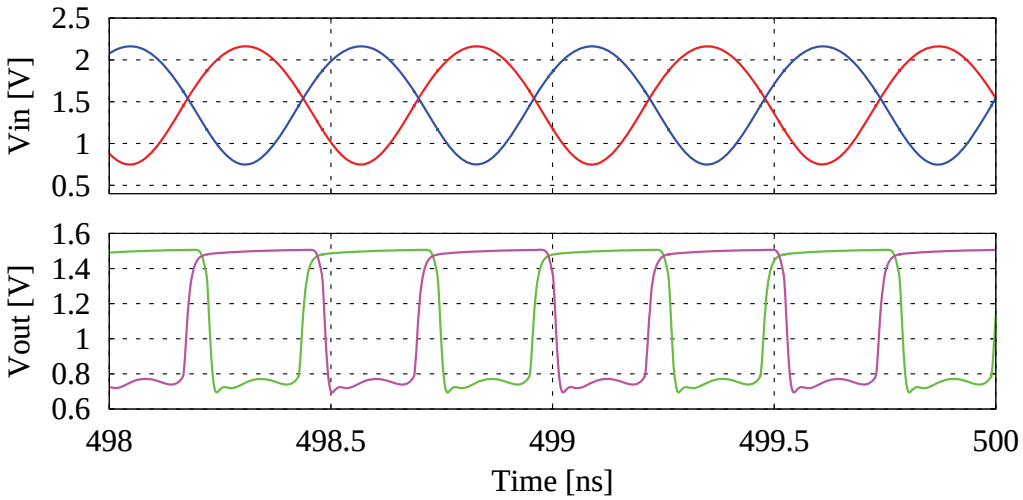


Figure 4.14: Transient response of the sin2rec clock buffer

Since CT ΔΣ modulators with single-bit feedback suffer from high sensitivity to clock jitter, tough requirements are imposed on the clock generation. Therefore, the jitter performance of this clock buffer has been simulated when an ideal sinusoidal signal at 1.92GHz was fed in. A histogram has been constructed based on 1000 periods of the clock buffer output when the circuit is operating in its designed operating points. As shown in Fig. 4.15, the introduced jitter is 31.07fs on top of an ideal jitter free sinusoidal input, which is too low to degrade the performance of the proposed single-bit modulator.

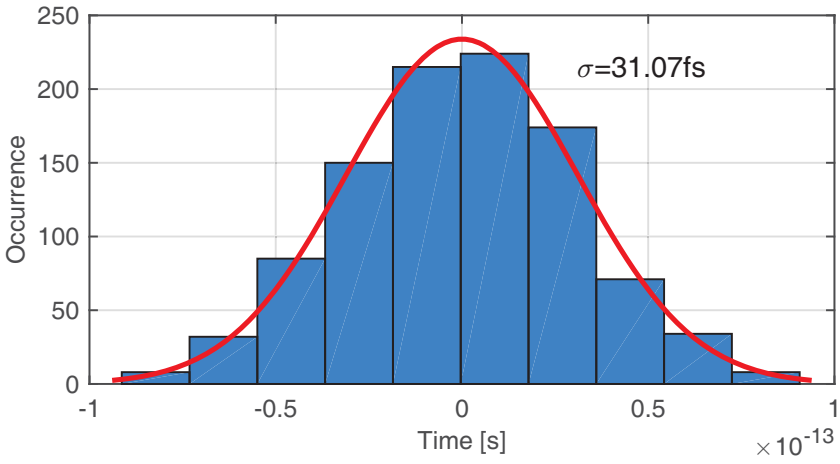
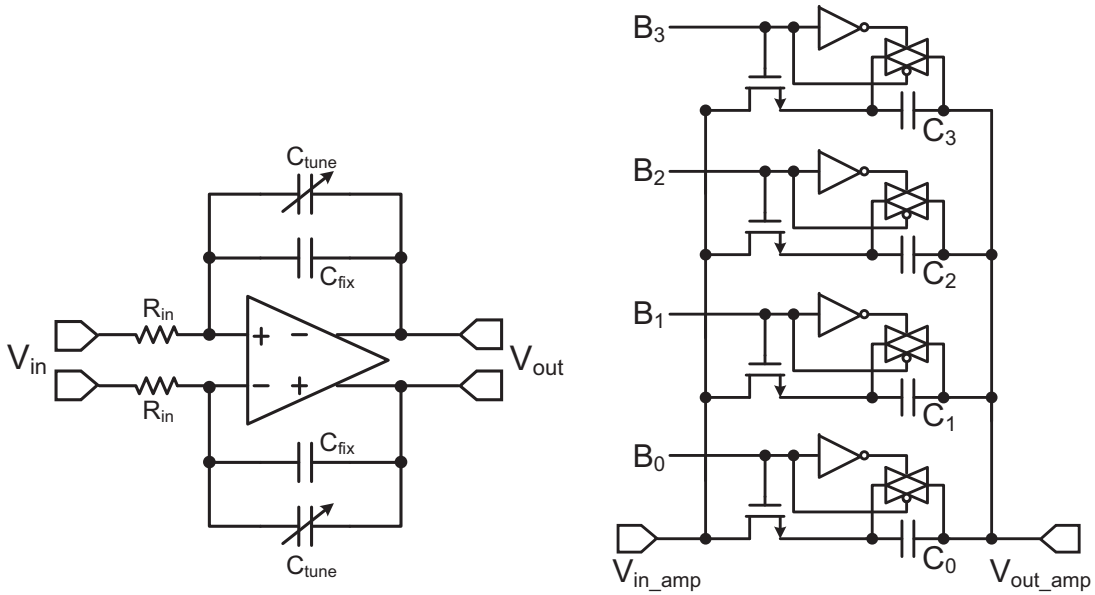


Figure 4.15: Histogram of the clock jitter introduced by the sin2rec clock buffer (1000 samples)

4.1.6 Tunable Capacitor Array



(a) (b)

Figure 4.16: Tunable integration capacitors. (a) active *RC*-integrator, and (b) tunable capacitive array

Since *RC* time constants of the CT integrators suffer from process variations, a tunable resistor or capacitor array is commonly required. Compared to the series resistor array, the parallel capacitive array features better performance, considering the switch on-resistance and parasitic capacitance [58] [59]. Therefore, a 4-bit

parallel capacitive array plus a fixed capacitor, C_{fix}, are employed to implement the integration capacitor in order to calibrate the modulator coefficients. Fig. 4.16 depicts the schematic of the tunable integration capacitors. The fixed capacitor C_{fix}, which is set to 80% of the desired integration capacitance, is always included in the integrator feedback path, while the capacitor array can be tuned by a externally supplied 4-bit control word to calibrate the feedback capacitors with a tuning range of ±30%.

Since the input node to the op-amp is virtual ground which is always kept around V_{CM}, no transmission gate is required and a simple NMOS transistor is used to implement the switch with sufficient low on-resistance. However, the switches in parallel with the capacitors have to be realized with transmission gate due to the high swing at the output of the op-amp. These switches are used to short the corresponding capacitors when they are not included in the feedback, otherwise one terminator of the capacitors is floating and may cause unwanted effects.

4.1.7 Layout and Fabricated Circuit

The CT ΔΣ modulator is essentially a nonlinear mixed-signal system. It consists of the continuous-time analog block (e.g., the loop filter) as well as the digital circuits (e.g., the feedback DACs and the quantizer). In order to achieve high resolution and linearity in such a mixed-signal system, a great deal of caution has been taken in the layout to reduce the effects of parasitics and mismatch. The noisy digital circuits are separated and isolated from analog building blocks, while the power supplies and grounds are separated between analog and digital circuitry in order to prevent digital noise from corrupting analog performance. Additionally, on-chip by-pass metal-insulator-metal (MIM) capacitors were used on DC supply lines and at the gate of current mirrors for high frequency decoupling.

The prototype modulator was fabricated in a 0.25µm SiGe BiCMOS process with 110GHz f_T HBT, occupying an active area of 1.35mm × 0.9mm. Fig. 4.17 shows the microphotograph of the chip with layout views and labels [6]. This chip includes a ΔΣ modulator, a sin2rec clock buffer, a 1:2 demultiplexer and customized LVDS output drivers [60]. The core area of the modulator without demultiplexer and LVDS drivers

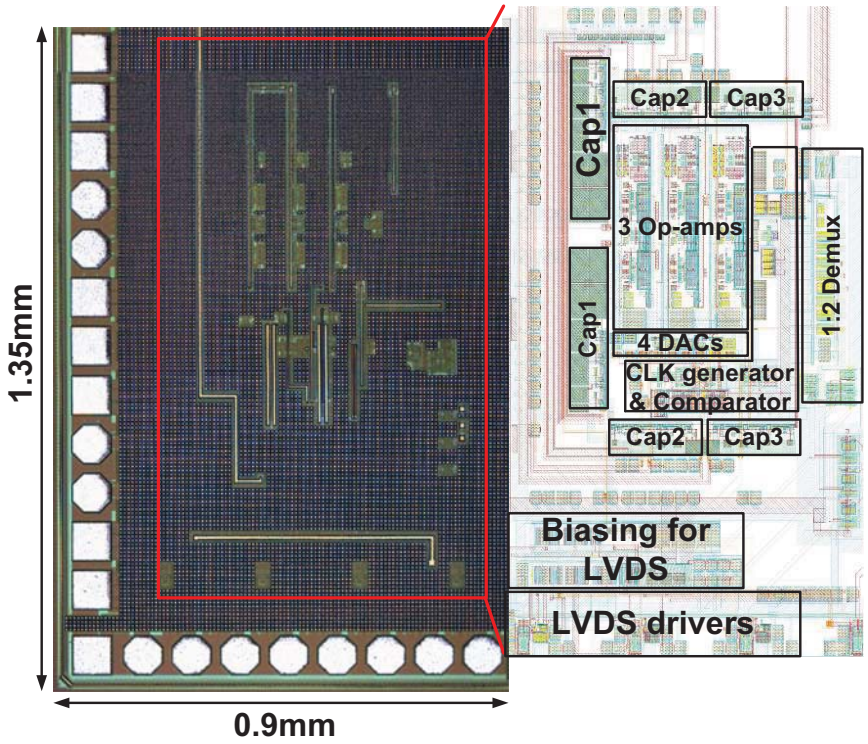


Figure 4.17: Chip micrograph with layout views of the modulator

is 0.4mm^2. In order to ease the interface with the field-programmable gate array (FPGA) based test equipment, the one-bit output data stream of the modulator is broken into two 960MS/s data streams by the 1:2 demultiplexer, and brought out through on-chip custom designed LVDS drivers.

4.2 Top Level Simulations

In this section the top-level simulation results are discussed, which include the modulator output spectrum, the clock jitter influence, Monte Carlo simulation results as well as the temperature effect.

4.2.1 Simulated Spectrum

Fig. 4.18 displays the simulated spectrum of the CT single-bit $\Delta\Sigma$ modulator implemented with the circuits presented in Section 4.1. Transient noise is enabled in

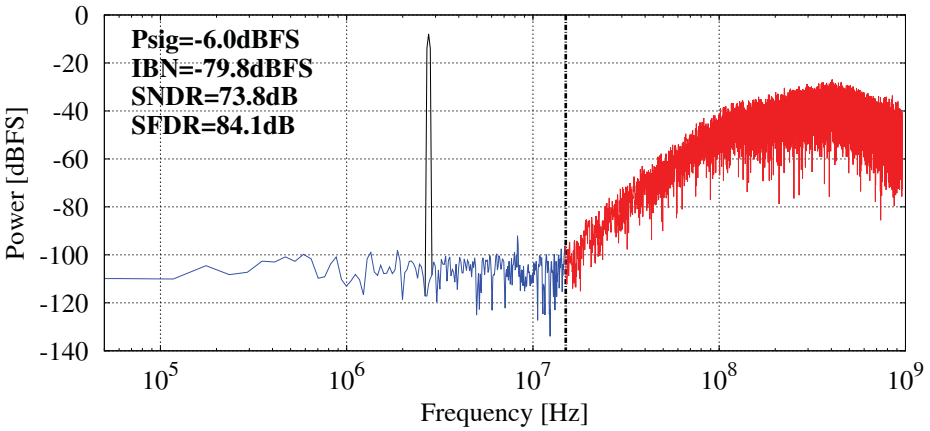


Figure 4.18: Spectrum of the transistor-level ΔΣ modulator

this transistor-level simulation. At each Input/Output (I/O) port, a 600fF capacitor is used to model the pad parasitic, in addition to a bond wire model which consists of a 120mΩ resistor and a 2nH inductor. With a -6dBFS input at 2.75MHz, the modulator achieves an SNDR of 73.8dB with an SFDR of 84.1dB.

Compared to the output spectrum of the Verilog-A based behavioral modulator shown in Fig. 3.18, a noise floor at around -105dBFS appears in Fig. 4.18 due to the noise from resistors and feedback DACs. The third-order harmonic component is increased by approximately 10dB and therefore the SFDR is reduced by the same amount for the same input signal. Additionally, in Fig. 4.18 the out-of-band NTF shows a drop rather than a slight peaking. The increase of third-order harmonic as well as the drop in the high frequency NTF are due to the fact that the output swing of the last integrator is slightly smaller than the required value in the transistor level implemented modulator.

After layout and parasitic extraction, an SNDR of 70.5dB is obtained from a post-layout simulation with an SFDR of 79.6dB, as shown in Fig. 4.19. In comparison to the transistor-level modulator, Fig. 4.18, a loss of 5dB in SFDR is seen due to the increase in the third-order harmonic. In addition, the second-order harmonic appears above the noise floor. This is because the routing of the connections between the single-bit quantizer and the feedback DACs is not fully symmetric.

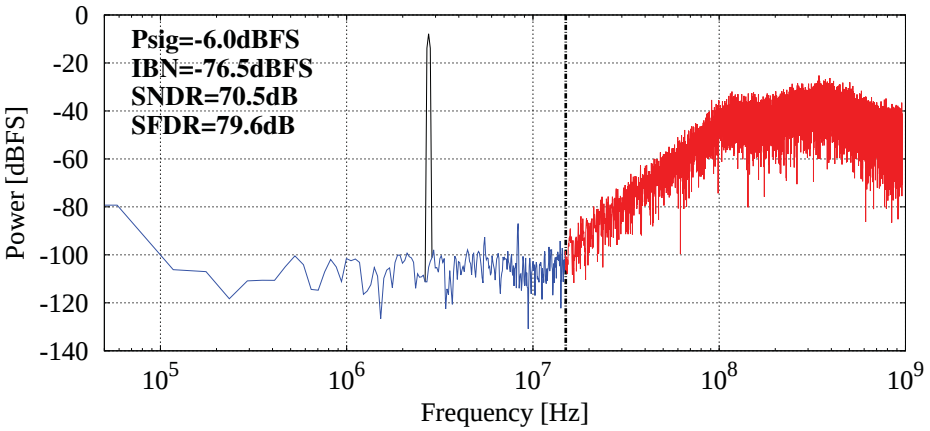


Figure 4.19: Spectrum of the parasitic extracted ΔΣ modulator

4.2.2 Clock Jitter Requirement

One of the major concerns of CT single-bit ΔΣ modulators is the clock jitter, which causes a statistical variation of the feedback waveforms and results in an increase of the noise floor. For modulators sampled at GHz frequency rates, clock jitter becomes one of the bottlenecks in the SNR performance. Therefore, it is important to ensure that the jitter requirement is reasonable and feasible in real applications. The effect of clock jitter in CT ΔΣ modulators has been extensively analyzed in the literature [1] [52], and the jitter induced in-band noise for a CT single-bit ΔΣ modulator with rectangular NRZ DACs can be expressed as [1]:

$$\mathrm{IBN}_{\sigma_t}|_{\mathrm{NRZ}} \approx \Delta^2 \left(\frac{\sigma_t}{T_S}\right)^2 \frac{\mathrm{A_{NRZ}}}{\mathrm{OSR}} \tag{4.3}$$

where Δ stands for the step width of the DAC, σ_t for the clock jitter and T_S for the clock period. $\mathrm{A_{NRZ}}$ is the NRZ activity factor, which approximately equals 0.7 for large input signals. Thus, the SNDR of the modulator becomes:

$$\mathrm{SNDR_{dB}} \approx \mathrm{P_{signal,dB}} - 10\log_{10}\left[\Delta^2 \left(\frac{\sigma_t}{T_S}\right)^2 \frac{\mathrm{A_{NRZ}}}{\mathrm{OSR}}\right] \tag{4.4}$$

Furthermore, transient simulations in Spectre were performed to investigate the jitter tolerance of the proposed transistor-level modulator. Fig. 4.20 shows the sim-

ulation results, which is in direct agreement with the theoretical prediction according to Eq.(4.4). As shown in Fig. 4.20, an rms jitter less than 1ps is required to avoid degrading the modulator performance significantly. For the designed modulator, this low jitter requirement can be fulfilled by reusing the precise local oscillator anyhow required in the receiver.

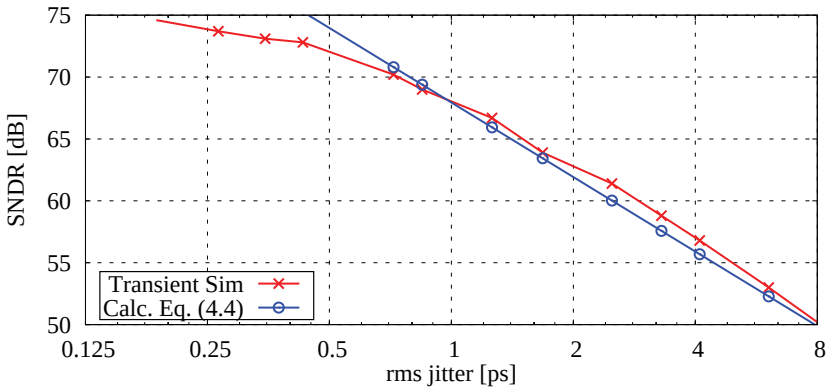


Figure 4.20: Simulated SNDR versus clock jitter with a -6dBFS sine-wave input at 2.75MHz, including a curve fit to Eq. (4.4)

4.2.3 Monte Carlo Analysis

A Monte Carlo analysis with 50 runs on post-layout simulations of the designed ΔΣ modulator was performed to investigate how the performance of the modulator is affected by mismatch and process variations. Since each run is extremely time-consuming (5 days to finish one run), only 50 runs were carried out. Although 50 runs are not enough to provide accurate statistical results, they can reveal how process variations and mismatch affect the ΔΣ modulator in general terms. Note in these simulations no coefficients tuning is performed.

Histograms of the simulation results is given in Fig. 4.21. From post-layout simulations, this modulator achieves an average SNDR of 69.4dB with a standard deviation of 1.5dB. For the SFDR, the mean value is 77.8dB with a 2dB standard deviation. Therefore, even without coefficients tuning, the modulator performance is not significantly affected by mismatch and process variations.

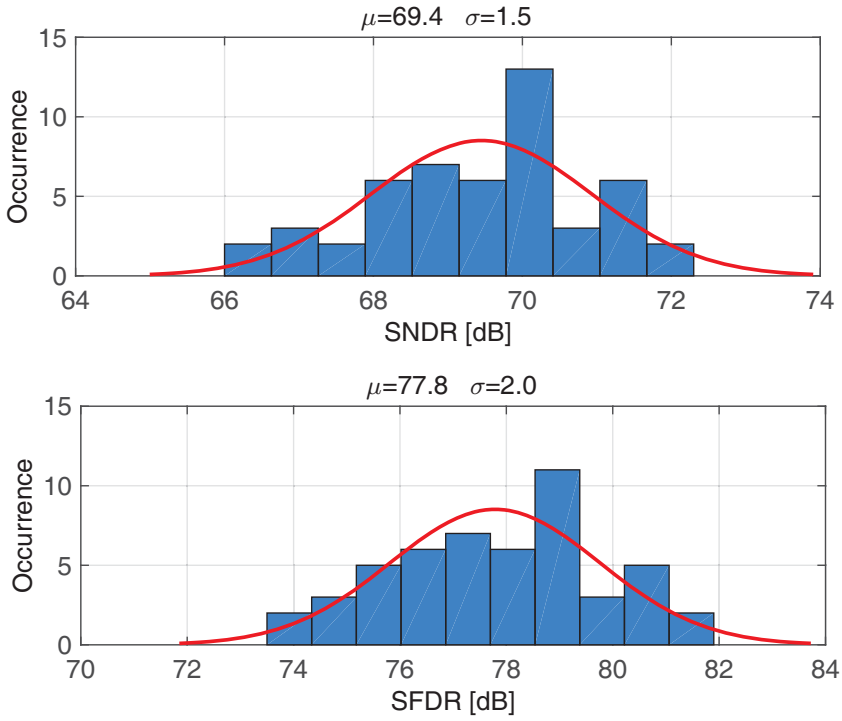


Figure 4.21: Histograms of the 50 runs Monte Carlo simulation results without tuning the on-chip Capacitor arrays

4.2.4 Temperature Effect

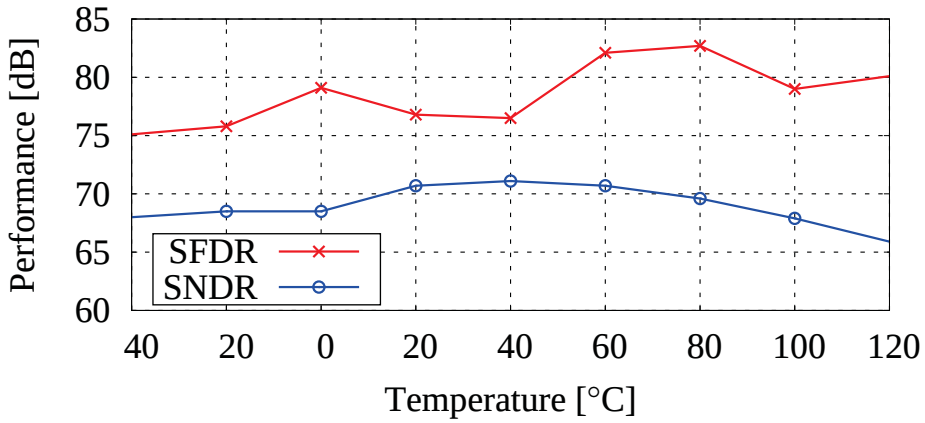


Figure 4.22: Modulator performance over temperature variation

With respect to temperature variation, the parasitic extracted modulator has been analyzed over an industrial temperature range from -40°C to 120°C. Fig. 4.22 shows the simulation results. As the temperature varies, the SNDR of this modulator is

only degraded by 5dB over temperature, while the worst SNDR of 66dB is obtained at 120°C due to the high thermal noise. In analyzing SFDR, the variation remains between 75.1dB and 82.7dB over temperature. The SFDR of this modulator is relatively constant at around 78dB, indicating a reasonable robustness to temperature variation.

4.3 Measurement Setup

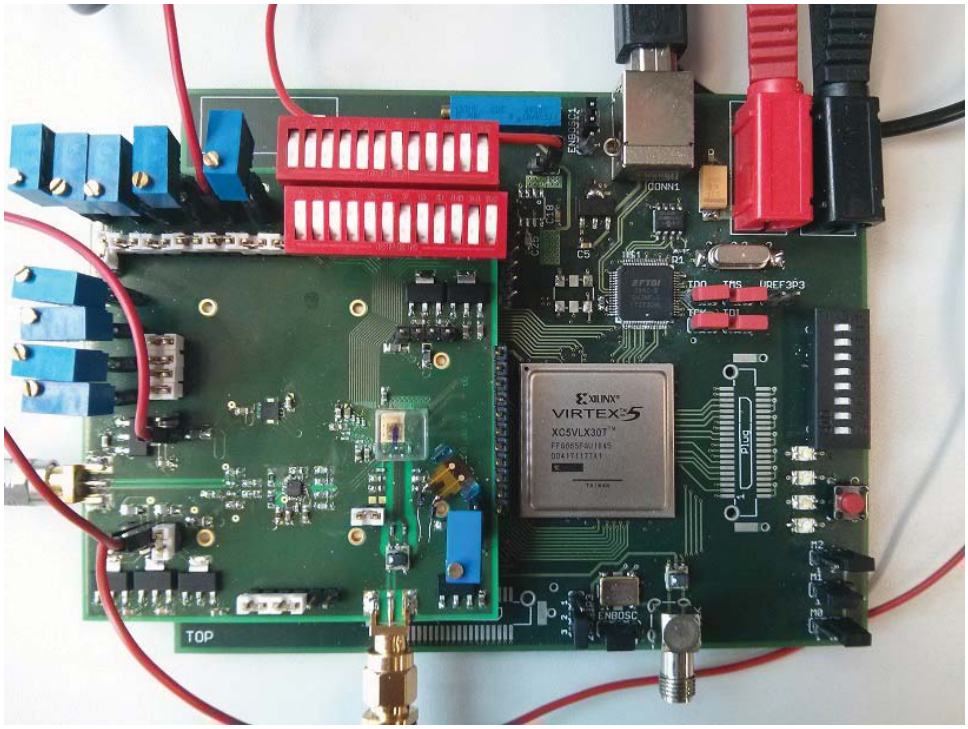


Figure 4.23: Photograph of the customized evaluation PCB set

In order to evaluate the performance of the fabricated ΔΣ modulator, a PCB setup has been designed. Fig. 4.23 depicts the designed PCB interface. The PCB set consists of two parts, one PCB header and one main board. The 4-layer PCB header, the top one on the left side of Fig. 4.23, features mainly input signal conditioning and voltage/current biasing. The main board, reused from earlier ΔΣ modulator projects [51], employs a XILINX *Virtex-5* FPGA to collect and store the output data of the modulator, and then send it to Matlab for further signal processing.

The measurement setup used to evaluate the ΔΣ modulator's performance is depicted in Fig. 4.24. Two Rohde&Schwarz signal generators are used to insert the test signal, one for the in-band (≤15MHz) signal Vin and the other one for the clock signal CLK at 1.92GHz. Both signals are brought on board through SMA connectors. The single-ended in-band signal Vin is converted to differential by an ADI *ADA4930* op-amp driver [61], and then passed through a single-pole low-pass RC filter so that the noise contribution from the driving circuit can be reduced. Note that the op-amp driver contributes noise at the modulator input, therefore, the performance of the op-amp has been investigated to make sure that the integration of its noise over the operational bandwidth will not degrade the modulator's conversion performance. Simultaneously, a balun *TC1-1-13MA+* from Mini-Circuits [62] is employed to perform the single-ended to differential conversion for the 1.92GHz clock signal. Furthermore, the clock signal is band-pass filtered at the balun input in order to remove any harmonic distortion coming from the signal generator. Note all these input signal conditionings are performed on the PCB header.

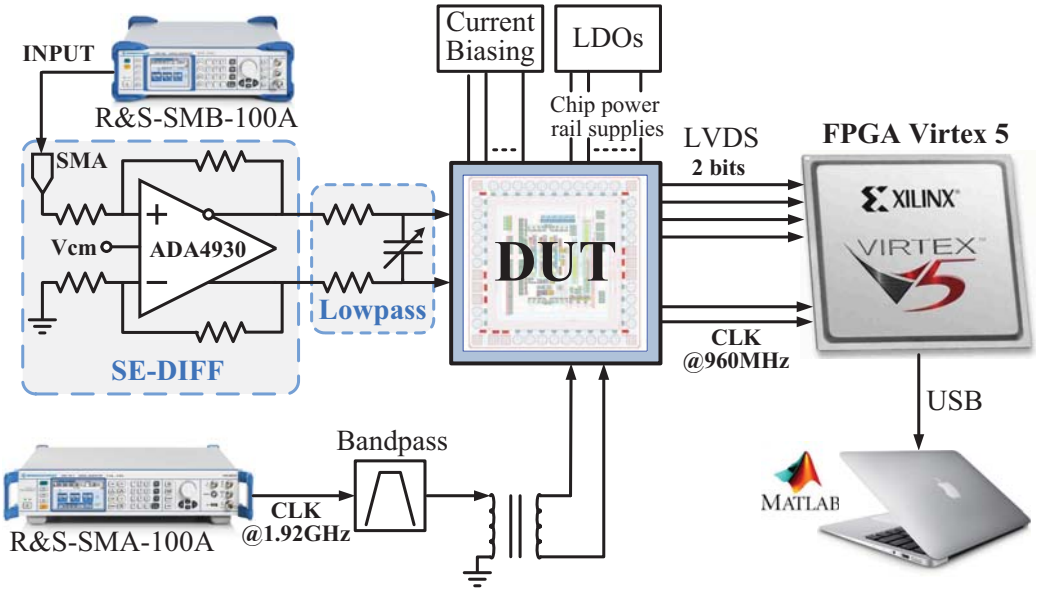


Figure 4.24: Simplified block diagram of the measurement setup

In addition, the PCB header is used to configure the modulator since the die of the ΔΣ modulator is directly mounted on it. For the power supplies and voltage references required for the modulator operation, low-dropout regulators (LDOs) are used to suppress noise and voltage ripples. From these on board power supplies, biasing

currents of the chip are generated by using potentiometers and series resistors. In order to reduce noise from the power supplies and biasing, intensive filtering and decoupling strategies are included on the PCB header. Moreover, proper impedance terminations are realized for the clock distribution path to avoid signal reflections and thus reduce the clock jitter, as discussed further in Section 4.3.1.

On the main board, the high speed Rocket I/Os of the *Virtex-5* FPGA are used to interface with the on-chip custom designed LVDS drivers. The two-bits output data of the ΔΣ modulator as well as the 960MHz clock signal, are captured by the FPGA Rocket I/Os which are able to operate up to 1.25GHz. Subsequently the modulator output data are multiplexed in Matlab for Fast Fourier Transformation (FFT) processing. The FFT length is 2^{18}, and the modulator output data is weighted by a Hann window so that the spectral leakage can be prevented.

4.3.1 Clock Input Path on the PCB Header

Since CT single-bit ΔΣ modulators suffer from high sensitivity to clock jitter, a great deal of effort has been spent on the verification board design, especially for the clock distribution path. Impedance matching has been implemented in order to minimize jitter in the clock distribution, considering the effect of the balun and PCB routing parasitics. The PCB header was designed in Allegro, and then the PCB layout of the clock input stage was transferred into Agilent ADS, where S-parameter simulations can be performed to check the electromagnetic (EM) behavior using Momentum.

The test bench of the S-parameter simulations is given in Fig. 4.25. The clock input stage consists of an SMA connector, a microstrip line, a balun, an edge-coupled microstrip line and a narrow wire connecting the off-chip 50Ω resistor and the modulator pads. Every part of the clock input stage should be designed properly and the effect of each part should be verified. When performing the S-parameter simulations, the port *Term1* with 50Ω impedance is fixed at the center conductor of the SMA connector, while the port *Term2* with 50Ω impedance is placed at two different points along the clock input stages:

- Balun input (point A)

- Between pads of the off-chip 50Ω resistor (point B)

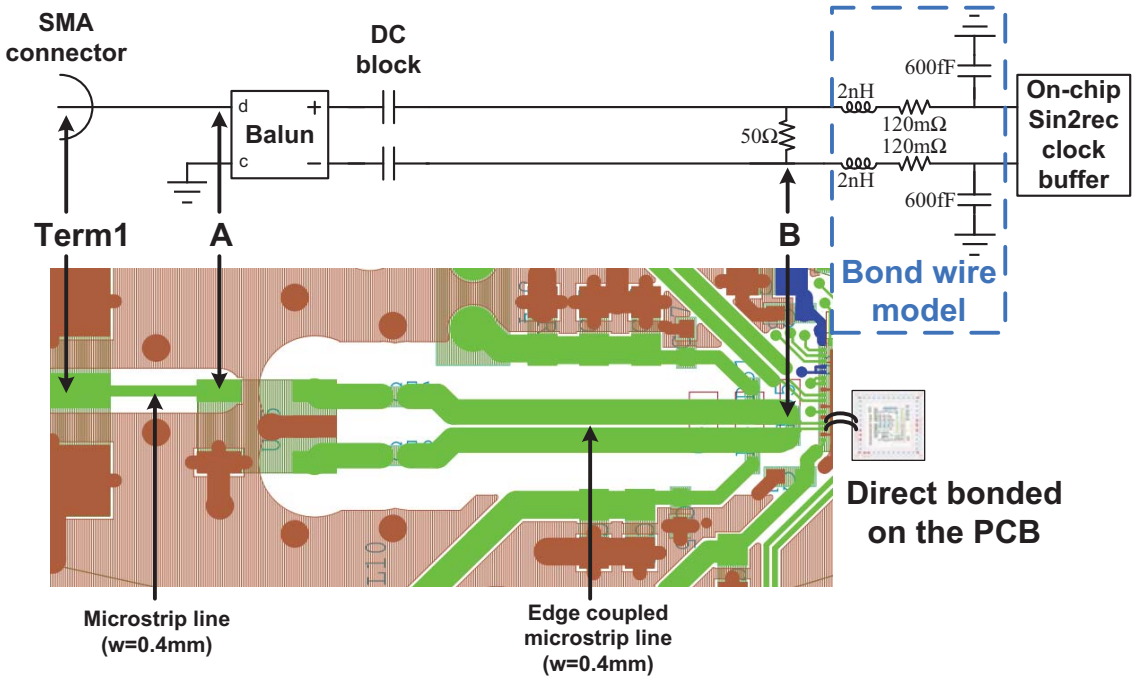
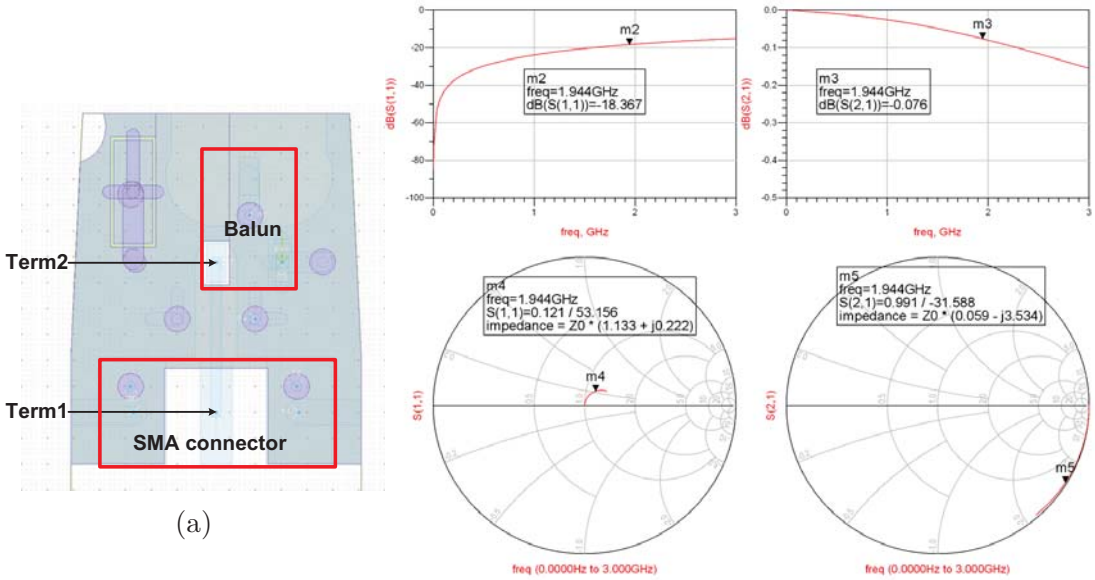


Figure 4.25: PCB layout of the clock distribution path

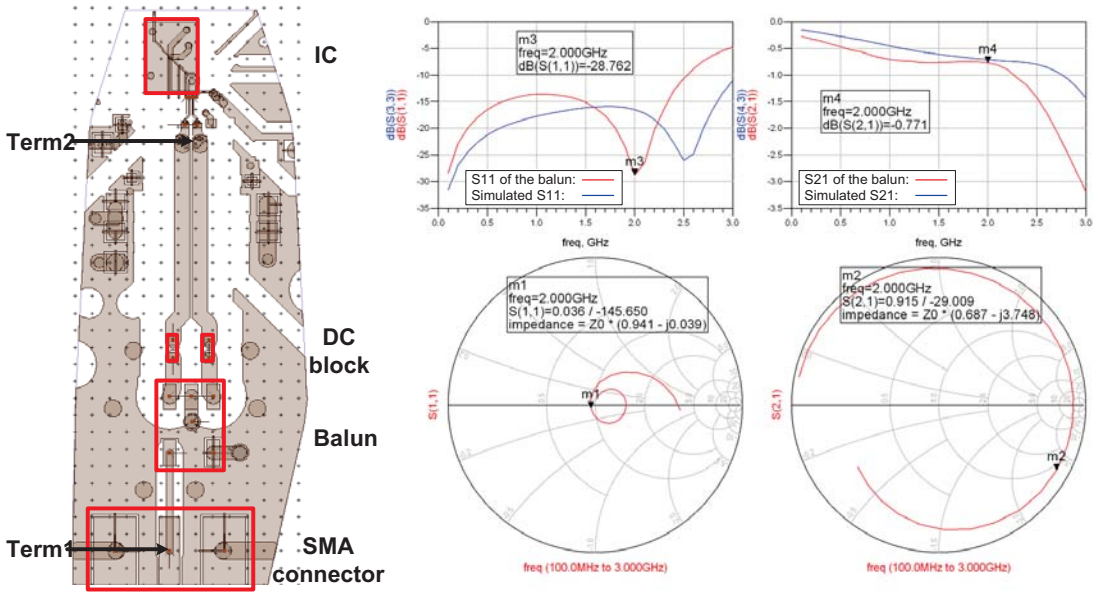
The PCB layout around the SMA connector and the balun was cut out, and exported to ADS, as shown on the left part of Fig. 4.26. The microstrip line, connecting the SMA connector with the balun, has a width of 0.4mm in order to achieve a characteristic impedance of 50Ω. In addition, the underlying ground under the SMA connector center pad and the balun input pad are cleared, so that the stray capacitance at these pins can be minimized and the impedance matching can be improved. The simulated S-parameter for the PCB layout of the clock input stage is given on the right part of Fig. 4.26. Apparently, the simulated S11 is -18.4dB at 1.944GHz, indicating a successful impedance matching.

In order to simulate the effect of the edge-coupled microstrip line at the balun output, Term2 (50Ω) was moved to the position of the off-chip 50Ω resistor, as shown on the left part of Fig. 4.27. The edge-coupled microstrip line was designed to feature a differential characteristic impedance of 50Ω. At the end of the edge-coupled microstrip line, a simple bonding wire model was used to connect the PCB board and the transistor-level clock buffer to reflect the real situation. In this bonding wire model, the 120mΩ resistor represents the parasitic resistance, and the parasitic



(a) (b)

Figure 4.26: S-parameter simulation with Term2 at balun input. (a) PCB layout in ADS, and (b) Simulated S-parameter



(a) (b)

Figure 4.27: S-parameter simulation with Term2 at off-chip 50Ω resistor. (a) PCB layout in ADS, and (b) Simulated S-parameter

capacitor of 600fF originates from the pad [63]. As a rule of thumb, the bonding wire inductance is estimated with 1nH/mm. Since the estimated bonding wire has a length of 2mm in this setup, an inductance of 2nH was used in this model.

The right part of Fig. 4.27 shows the simulated S-parameters when Term2 (50Ω) is placed at the off-chip 50Ω resistor. The S-parameter for the balun loaded with 50Ω - downloaded from its on-line data sheet - is also given as a reference. Thanks to the impedance matching, a notch locates at the desired clock frequency of 1.92GHz in the S11 plot.

4.4 Measurement Results

This section presents the measurement results of the fabricated chip, which includes the S11 at the modulator clock input, the spectra at the modulator output, as well as the jitter present on the input clock signal.

4.4.1 S11 at the Clock Input

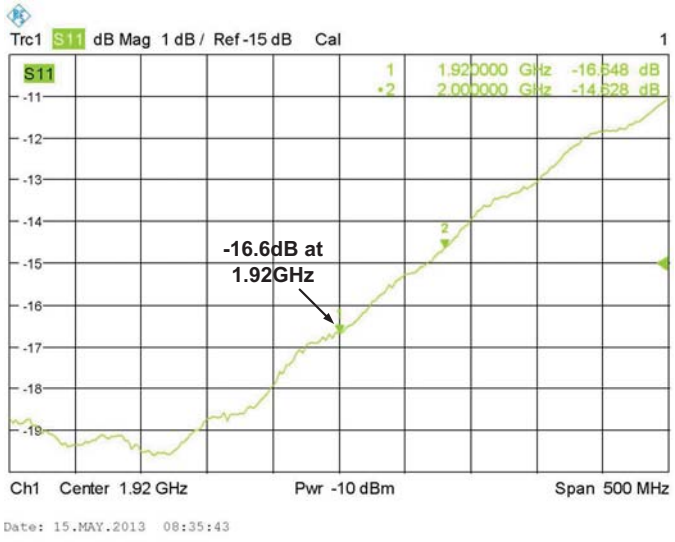


Figure 4.28: Measured S11 at the clock input

First the S11 at the SMA connector for the clock input was measured. As shown in Fig. 4.28, at the clock frequency of 1.92GHz the measured S11 is -16.6dB, which is

only 2dB worse than the simulation result shown in Fig. 4.26. Therefore, impedance matching for the clock trace was successfully conducted in the PCB header design.

4.4.2 SNDR/SFDR with Measured Spectrum

It is important to mention that the optimum performance of the fabricated ΔΣ modulator can only be achieved for a voltage supply of 2.8V, although the modulator was designed to operate with a 2.5V supply. This is due to IR drop, which will be discussed in Section 4.4.4.

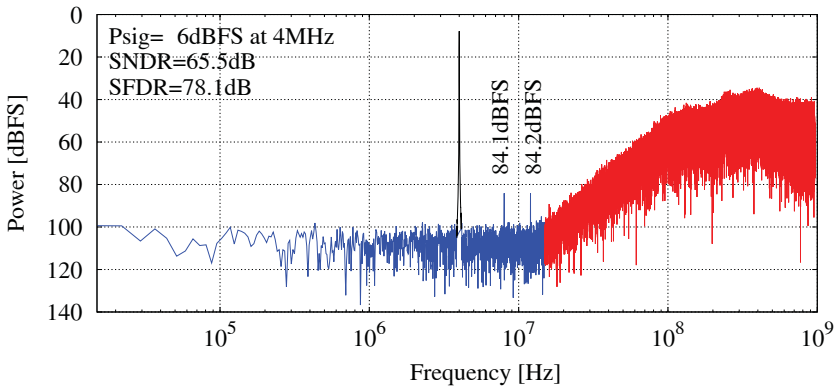


Figure 4.29: Measured output spectrum for a -6dBFS sine wave input at 4MHz

Fig. 4.29 illustrates the measured spectrum when the modulator is excited by a -6dBFS input at 4MHz. The full-scale input signal (0dBFS) refers to a sine wave with $2V_{pp\text{-}diff}$. The modulator achieves an SNDR of 65.5dB with 78.1dB SFDR. From the spectrum, it can be seen that the second and third harmonics appear with a power of -84.1 and -84.2dBFS, respectively. The second harmonic observed in the spectrum originates from the non-symmetric connections between the single-bit quantizer and the feedback DACs in the layout, which has been revealed by post-layout simulations. This even-order distortion problem could be solved in future designs.

In addition, the input signal power was measured by an oscilloscope in time-domain with a feasible active probe head to avoid any attenuation of the input signal. This measurement is necessary in order to verify the value of P_{sig} indicated in Fig. 4.29, which is calculated based on the ΔΣ modulator output data stream. A screenshot of the oscilloscope is given in Fig. 4.30, wherein markers are used to measure the

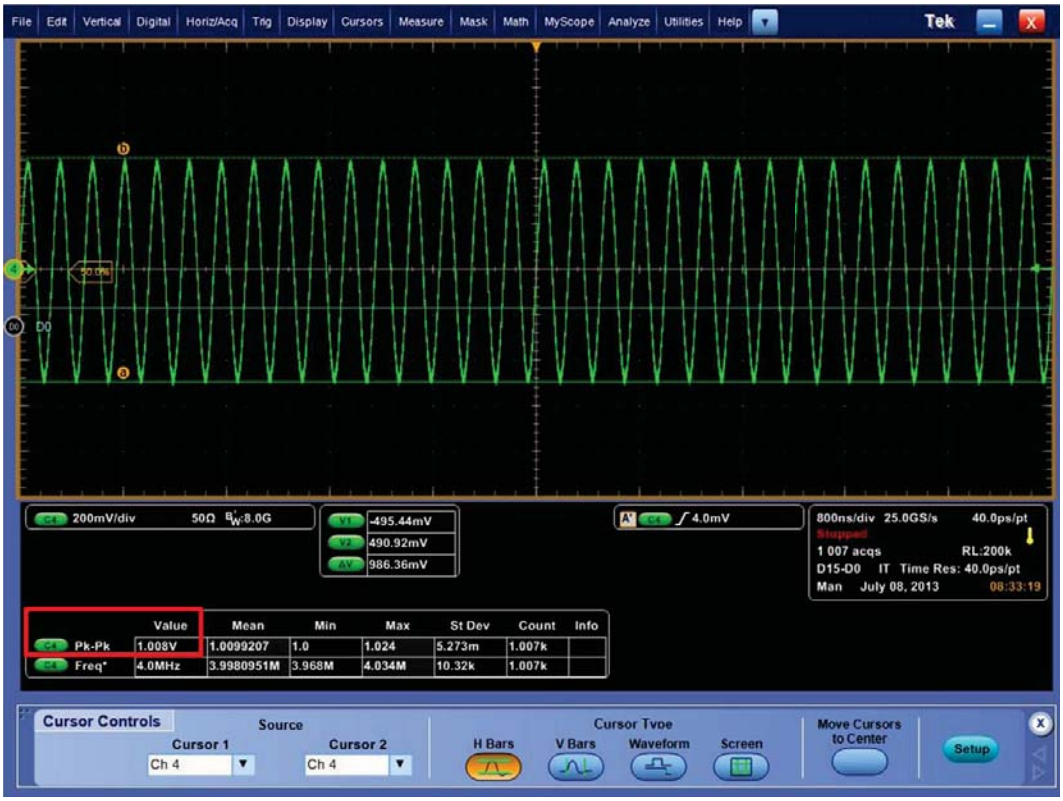


Figure 4.30: Measured input signal for -6dBFS P_{sig} shown in Fig. 4.29

differential peak-to-peak input amplitude. Clearly, the measured amplitude of the sinusoidal input is equal to 1.008$V_{pp\text{-}diff}$, which corresponds to -6dBFS since the full scale 0dBFS is 2$V_{pp\text{-}diff}$ in this design. Therefore, the calculation of input power through FFT is correct in this measurement.

In Fig. 4.31, the measured SNR and SNDR are plotted as a function of the input level of a 4MHz sinusoidal input signal. Over a 15MHz signal bandwidth, the modulator achieves 66.9dB peak SNR and 65.5dB peak SNDR. Compared to the post-layout simulation results, a 5dB degradation in SNDR is observed, which is caused by clock jitter and will be discussed in Section 4.4.3. The measured dynamic range of the modulator equals 70dB, which corresponds to an 11.3-bit resolution.

Furthermore, the fabricated experimental chip was also measured by the industrial cooperation partner, and similar performance had been achieved. Fig. 4.32 illustrate the peak performance for two further modulators. For a -6.3dBFS sinusoidal input at 3MHz, one modulator achieved 69.9dB SNDR with 75.3dB SFDR, while the other one achieved 67.7dB SNDR with 81.1dB SFDR.

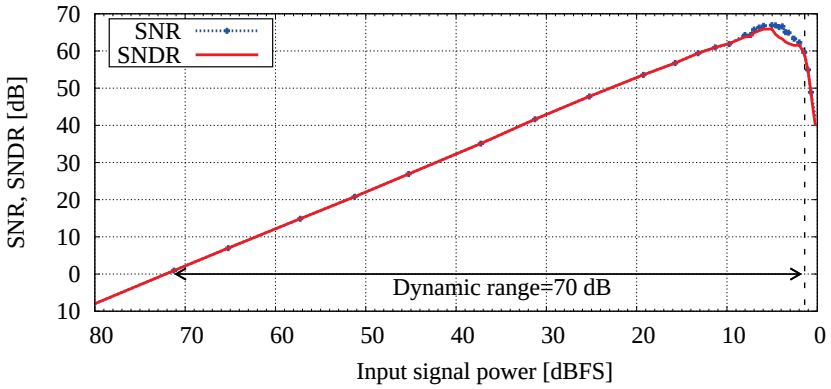


Figure 4.31: Measured SNR and SNDR versus input signal power

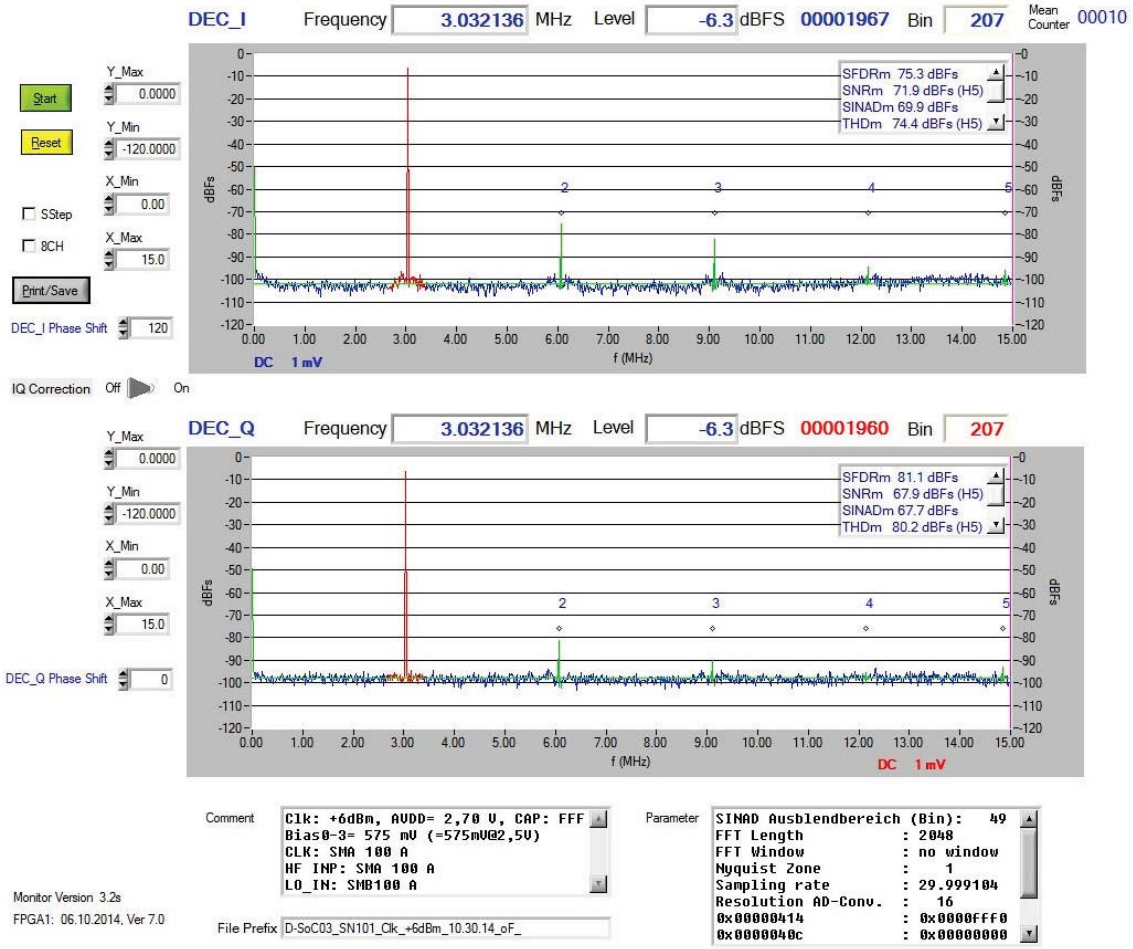


Figure 4.32: Measured output spectra for a -6.3dBFS sine-wave input at 3.03MHz by co-operation parter

4.4.3 Measured Clock Jitter

Since the CT single-bit ΔΣ modulator with a NRZ feedback scheme suffers severely from high sensitivity to the clock jitter, it is necessary to measure the jitter present on

the input sampling clock signal of the modulator. As shown in Fig. 4.23, one solder-in probe accessory was soldered at the balun output on the PCB header, wherein the jitter was estimated by a real-time 40GS/s oscilloscope (Tektronix 70804) through an active differential probe (P7380A) as well as the solder-in probe accessory. Fig. 4.23 gives the jitter histogram measured from 15,999 samples. Clearly, this jitter is random and it follows a Gaussian distribution with a standard deviation of 0.96ps.

According to Eq.(4.4), a clock jitter of 0.96ps limits the SNDR of a CT single-bit $\Delta\Sigma$ modulator with a NRZ feedback scheme to 67.9dB, which is only 2dB higher than the measured peak SNDR. Therefore, the clock jitter is one of the main bottlenecks of the designed modulator.

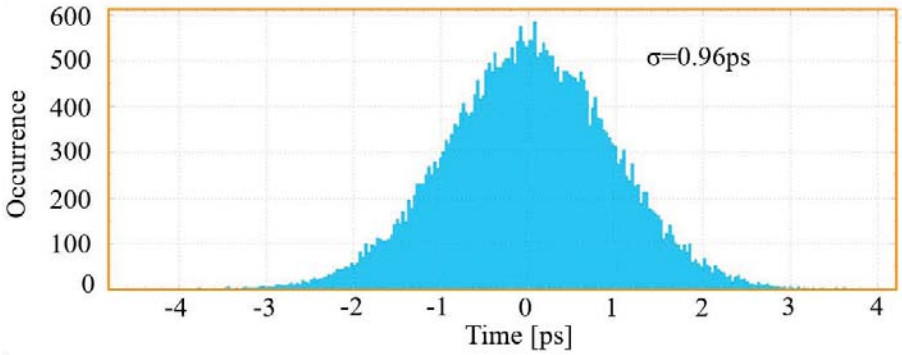


Figure 4.33: Measured histogram of the input clock jitter (15,999 samples)

4.4.4 Power Consumption and Supply Drop

In the measurement, the experimental chip was measured with a power supply voltage of 2.5V at first. However, it was found that the current fed into the chip was smaller than the simulated value, while the initially measured SNDR was around 57dB, which is much worse than expected. Therefore, the power supply of the chip was increased in order to achieve a better performance.

Table 4.1 gives the measured current feeding into the chip while sweeping the supply voltages. The current flowing through both analog (AVDD) and digital (DVDD) power supplies were measured, since in the layout the power supplies and grounds were separated between analog and digital circuitry to avoid coupling digital signals into the analog circuits. Clearly, the applied current raises with the power supply.

Table 4.1: Measured current consumption for different supplies

VDD (V)	2.5	2.6	2.7	2.8	2.9
Measured I from AVDD (mA)	47	52	55	58	61
Measured I from DVDD (mA)	44	47	50	52	54

Note that transient simulation showed that a current of 56.8mA is drawn from AVDD while the current through DVDD is 50.2mA. Therefore, in order to ensure the same amount of current is drawn by the experimental chip, the power supply was increased to approximately 2.8V.

Comparing the simulated and measured current, it is easy to see that the measured current is smaller than the simulated for a voltage supply of 2.5V. Thus, IR drop is the most obvious reason why the ΔΣ modulator only achieves good performance with higher supplies. Since the IR drop phenomenon comes from power supply resistance, it can be solved by increasing the width of power distribution network in a re-layout.

In addition, the SNDR of the ΔΣ modulator has been simulated and measured while sweeping the power supply VDD (VDD=AVDD=DVDD). These simulations of the modulator did not take the parasitics into consideration for a short simulation time. Transient simulations show that the SNDR starts dropping below 2.4V. However, in the measurement the ΔΣ modulator does not achieve optimum performance until the power supply VDD is increased to 2.8V. For a 2.8V supply, the modulator achieved a peak SNDR of 65.5dB with 78.1dB SFDR, which has been discussed in Section 4.4.2. Furthermore, the power supply VDD was also increased to 2.9V in the measurement, but no performance improvement was achieved.

For a supply of 2.8V, the measured total power consumption of the chip is 407mW, where the ΔΣ modulator itself dissipates 215.9mW, and the power consumption for the sin2rec clock buffer, the demultiplexer and the output LVDS driver is 33.7mW, 68.5mW, and 88.9mW respectively. The significantly higher power consumption - when compared to fine-line CMOS implementations - is a trade-off to the high performance transistors required for the above 5GHz input of the RF receiver.

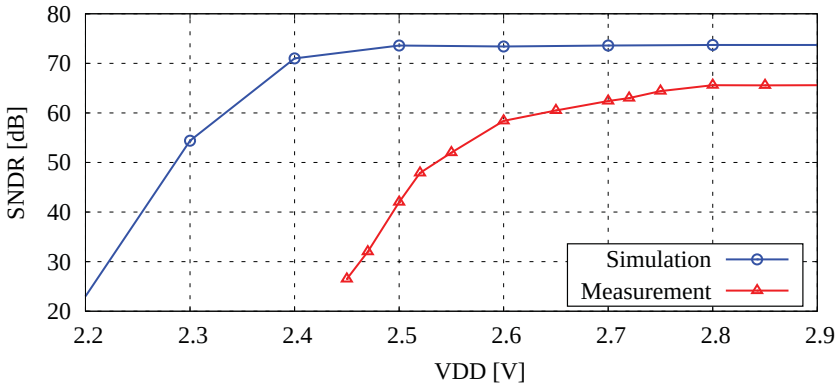


Figure 4.34: Power supply influence on the nominal simulated and measured SNDR

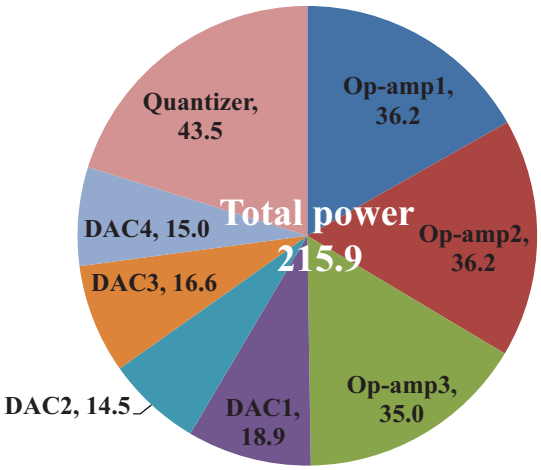


Figure 4.35: Pie chart of measured power consumption for the presented ΔΣ modulator (Unit: mW)

Additionally, the pie chart in Fig. 4.35 shows the measured power dissipation for different components of the presented ΔΣ modulator. The measured power consumption is approximately 15% higher than the simulated value, since the supply voltage has been increased from 2.5V to 2.8V in the measurement. From Fig. 4.35 it is clear that the power consumption of the ΔΣ modulator is dominated by op-amps and the single-bit quantizer. Additionally, it is worthwhile to note that approximately 30% of the power is dissipated by emitter followers used in the circuitry.

4.5 Performance Summary and Discussion

The measured characteristics of the developed ΔΣ modulator are summarized in Table 4.2. The third-order CT low-pass ΔΣ modulator has been implemented in a low-cost 0.25µm SiGe BiCMOS process, and achieves 66.9dB peak SNR and 65.5 dB peak SNDR over a 15MHz signal bandwidth. The dynamic range of the modulator equals 70dB, which corresponds to an 11.3-bit resolution. Clocked at 1.92GHz, the modulator achieves 78.1dB SFDR by employing a single-bit internal quantizer which is inherently linear, and no digital DAC linearization technique is required. The modulator dissipates 215.9mW and occupies an active area of 0.4mm^2 [6].

Table 4.2: Measured performance summary for a 4MHz sinusoidal input

Signal bandwidth	15MHz
Clock frequency	1.92GHz
Oversampling ratio	64
Full scale	$2V_{pp\text{-}diff}$
Dynamic range	70dB
Peak SNR	66.9dB (at -5dBFS input)
Peak SNDR	65.5dB (at -6dBFS input)
SFDR	78.1dB
Power consumption from 2.8V	215.9mW
Core area	0.4mm^2
Technology	0.25µm BiCMOS

After design, implementation and measurement of the presented ΔΣ modulator, it is worthwhile to analyze the performance loss of the modulator compared to the ideal spectrum. Generally speaking, there are four main causes of the SNDR degradation for the presented modulator:

- ELD and GBW compensation
- Thermal noise
- Quantizer metastability

- Clock jitter

Table 4.3: SNDR degradation in the design flow

ΔΣ modulator	**SNDR(dB)**
Ideal model	88.1
Modulator with ELD and GBW compensation	85.5
Modulator considering only the thermal noise from resistors	82.4
Modulator with transistor-level op-amps; other components: Verilog-A *	79.3
Modulator with transistor-level DACs; other components: Verilog-A *	79.1
Modulator with transistor-level comparator driven by the sin2rec buffer; other components: Verilog-A *	76.4
Transistor-level ΔΣ modulator *	73.8
Post-layout simulation of the transistor-level ΔΣ modulator *	70.5
Measured result with 0.96ps clock jitter	65.5

*Thermal noise included

Table 4.3 lists the achieved SNDR when different non-idealities of circuit implementation are taken into account in the design flow. For the ideal third-order CIFB loop filter, an SNDR of 88.1dB can be achieved. A loss of 3dB in SNDR is caused by the employed differentiator based ELD and GBW compensation method. A detailed analysis will be given in Section 6.1.1, showing that the NRZ feedback scheme used in DAC4 cannot completely compensate for the delay introduced by the finite GBW of the third op-amp.

When taking the thermal noise from resistors into account, the SNDR of the modulator is limited to 82.4dB. After the transistor-level design of the op-amps, they are included in a modulator while the other building blocks are Verilog-A based ideal model. Time-domain simulation including transient noise shows that this modulator achieved an SNDR of 79.3dB, and the additional 3dB loss in SNDR was mainly due the emitter degeneration in the first op-amp. Similarly, in a modulator wherein only the DACs are transistor-level implemented, an SNDR of 79.1dB can be obtained, indicating that the DACS are one of the major noise contributors in this modu-

lator. In addition, when only the single-bit quantizer and the sin2rec clock buffer are transistor-level designed, the modulator achieves 76.4dB SNDR under the effect of metastability. When all the building blocks of the modulator are available at transistor-level, transient simulation leads to an SNDR of 73.8dB, and the SNDR loss is caused by the slow rising/falling of the quantizer output. After layout and parasitic extraction, post-layout transient simulation shows that the modulator achieves 70.5dB SNDR. Additionally, with only 1ps clock jitter and no other non-idealities, the modulator achieves 67.5dB SNDR as shown in Fig. 4.20. Finally, measurement shows that this modulator obtained an SNDR of 65.5dB, and the 0.96ps clock jitter is one of the main bottlenecks of the designed modulator.

Chapter 5

RF Receiver SoC

In this chapter, the implementation of a RF receiver SoC will be presented, which consists of one RF front-end, two CT $\Delta\Sigma$ modulators and other auxiliary circuits. The RF front-end was previously designed, layouted and prototyped by the industrial cooperation partner, while the CT $\Delta\Sigma$ modulator was the one presented in Chapter 4. The SoC integration of the RF front-end and the CT $\Delta\Sigma$ modulators in a low-cost BiCMOS technology offers a cost efficient solution for the receiver. Note, the accuracy and functionality of a SoC does not only rely on the electrical performance of individual building block, but also on the interaction between various components involved within the whole signal link [64]. Therefore, the overall SoC performance has to be evaluated to ensure that the CT $\Delta\Sigma$ modulator would not deteriorate the performance of the RF front-end.

5.1 Introduction

Fig. 5.1 illustrates the block diagram of the receiver SoC. The RF front-end, which was designed and implemented by the industrial cooperation partner, is composed of a low noise amplifier (LNA), an RF buffer, two Mixers, a local oscillator (LO), a frequency divider, as well as two variable gain amplifiers (VGAs). The incoming RF signal at around 5GHz is amplified by an LNA, and then goes into an In-phase/Quadrature-phase (I/Q) mixer through an RF buffer. The two LO output signals to the I/Q mixer are 90° out of phase, generated by a divide-by-two circuit. After the down-conversion through the mixer, the baseband signal is obtained and

fed into an VGA. This VGA amplifies the incoming signal while serving as a driver for the following ADC. Since the gain of the VGA is adjustable, the ADC dynamic range can be used in the most efficient way. Then the I/Q outputs are digitized by the quadrature CT ΔΣ modulators, which significantly relax the requirements on analog anti-aliasing filters. The outputs of the CT ΔΣ modulator are fed into the 1:2 demultiplexer and then brought out through the on-chip custom designed LVDS drivers. Finally decoding and demodulation can be performed in the off-chip baseband digital signal processor (DSP) subsystem.

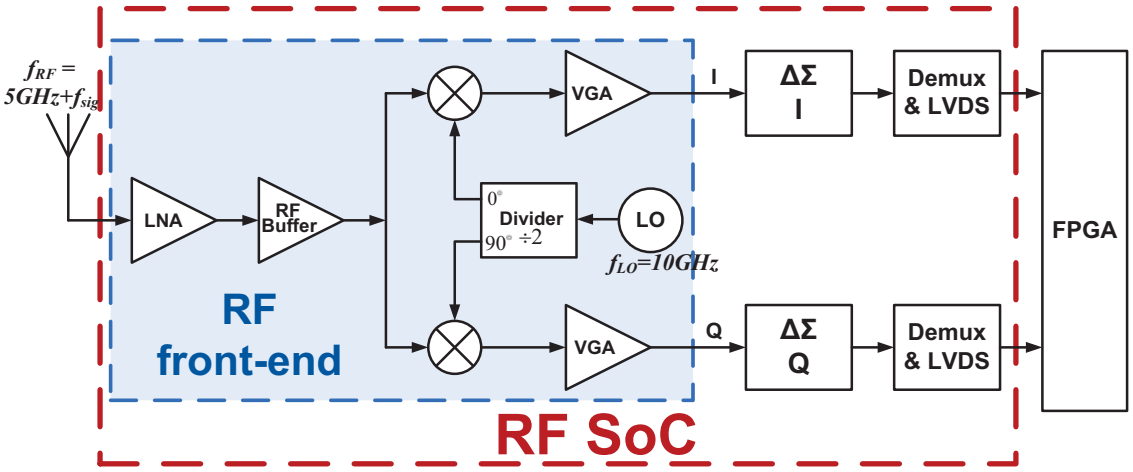


Figure 5.1: Block diagram of the receiver SoC

In this work, the clock signal for the ΔΣ modulators is not generated by the on-chip LO, but fed in externally, as illustrated in Fig. 5.2. As discussed in Chapter 4, the sin2rec clock buffer converts a differential 1.92GHz sine wave into a rectangular signal, which triggers the quantizer in the ΔΣ modulators. Furthermore, this 1.92GHz rectangular clock is also applied to a clock divider, which provides a 960MHz clock, as well as a 480MHz clock. The 960MHz clock is required by the 1:2 demultiplexer to split the ΔΣ modulator output into lower rate data stream. Finally, the 480MHz clock and the outputs of the 1:2 demultiplexer are brought out through the on-chip LVDS drivers.

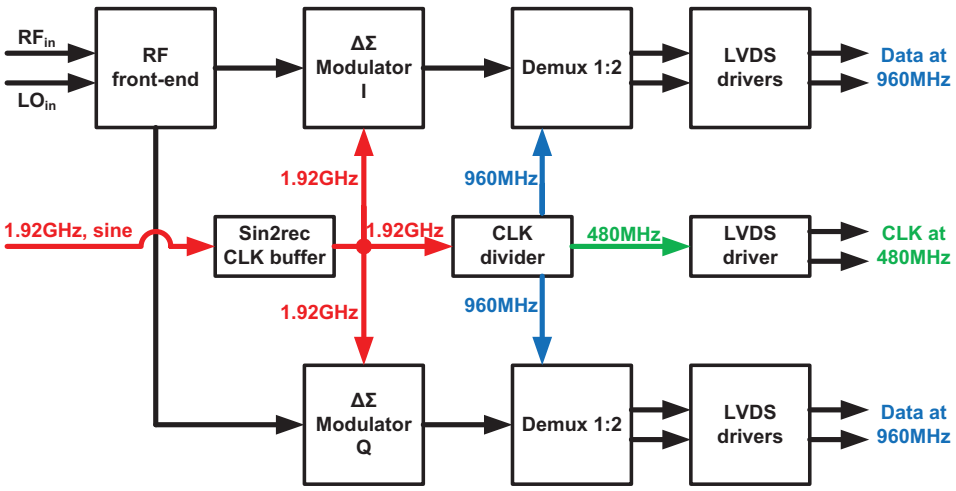


Figure 5.2: Block digram of the SoC with clock path

In the previous design, the sin2rec clock buffer only drives one $\Delta\Sigma$ modulator, however, it has to control two modulators in both I/Q channels in this tapeout. Therefore, the driving capability of the clock buffer has been examined, and stronger emitter followers were added at the clock buffer output. Similarly, the driving capability of the clock divider had been improved. Note in this design, the clock divider offers the 480MHz clock as the clock output, instead of the 960MHz clock in the previous design. Since the output data of the demultiplexer is at 960MHz, both rising and falling edges of the 480MHz clock should be utilized to sample the data.

Fig. 5.3 shows the layout of the receiver SoC, where filler layers are excluded in order to display the sub-circuit layout clearly. The total die area is 3.16mm×3.16mm =10mm^2. The layout of the RF front-end was placed at the left upper corner of the die, while the clock buffer and clock divider were positioned in such a way that the clock paths to both $\Delta\Sigma$ modulators are approximately equal. The layout of the $\Delta\Sigma$ modulator used in this chip is almost the same as the one presented in Section 4.1.7, but the power routing has been made much wider in order to alleviate the IR drop problem found in the measurement. Additionally, large decoupling capacitors are placed between power and ground lines in the unused chip area to suppress high-frequency noise in power supplies.

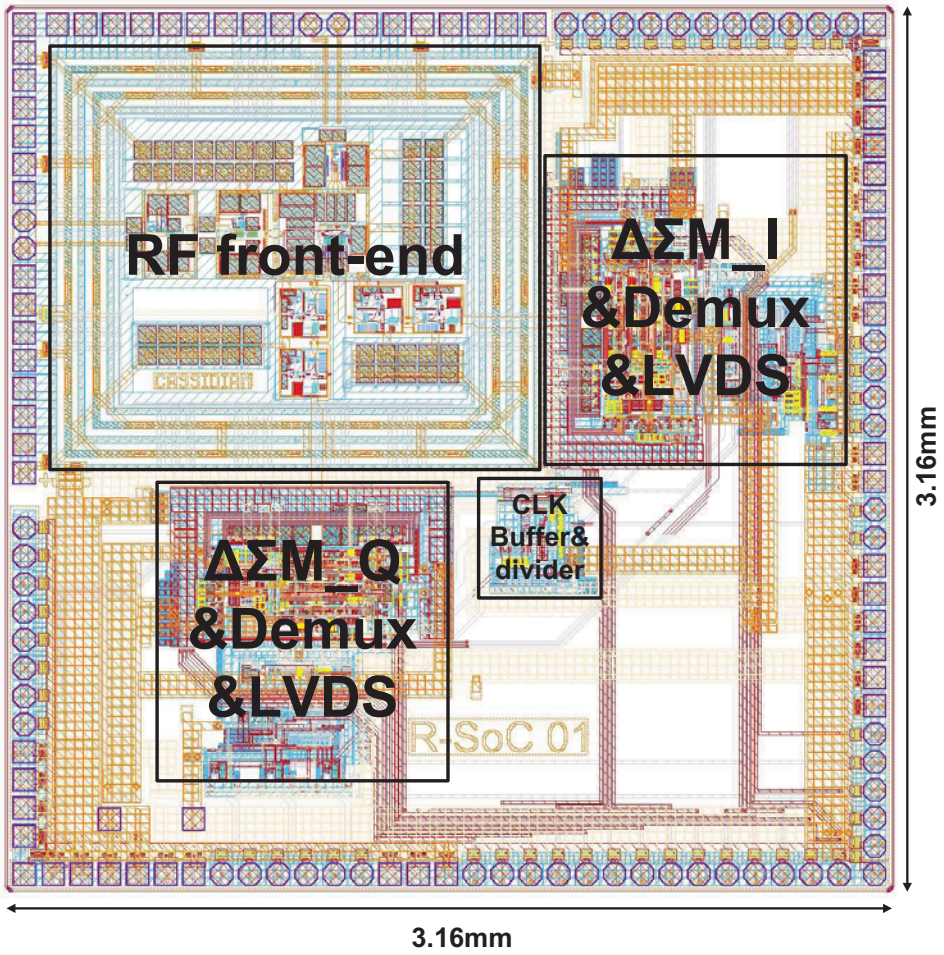


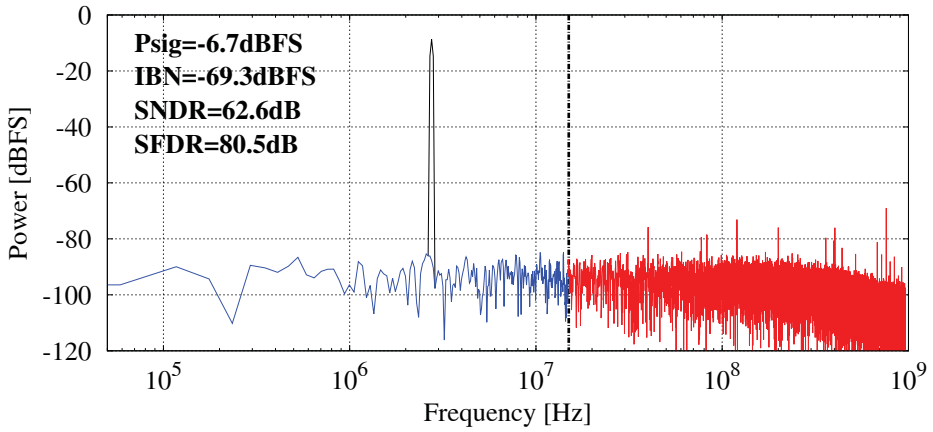
Figure 5.3: Layout of the receiver SoC

5.2 Post-layout Simulation Results

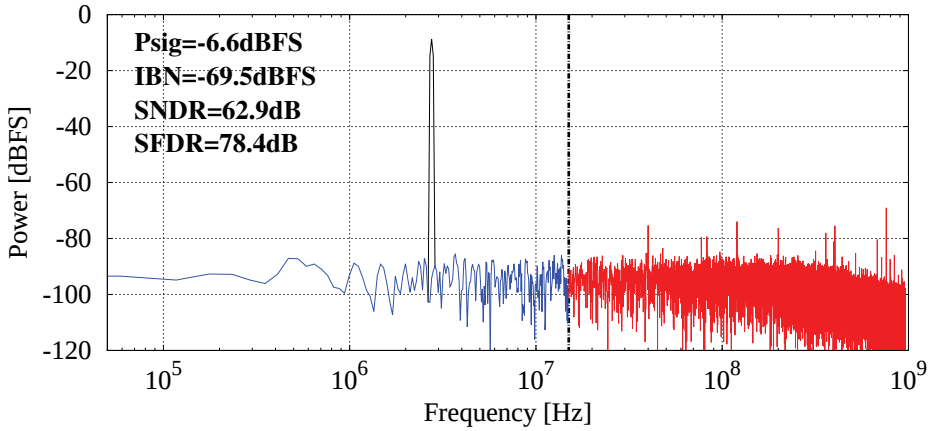
5.2.1 Spectra at the RF Front-end Output

Since the RF font-end was designed by the industrial cooperation partner, it is necessary to carry out post-layout transient simulations to investigate the spectra of the RF front-end output data, which is the input of the designed quadrature CT $\Delta\Sigma$ modulators.

In the transient simulation, each of the RF front-end outputs were loaded by a 1000Ω resistor, which is the differential input resistor of the designed $\Delta\Sigma$ modulator. The input of the RF front-end equals -47dBm at 5,002.75MHz, while the LO input is



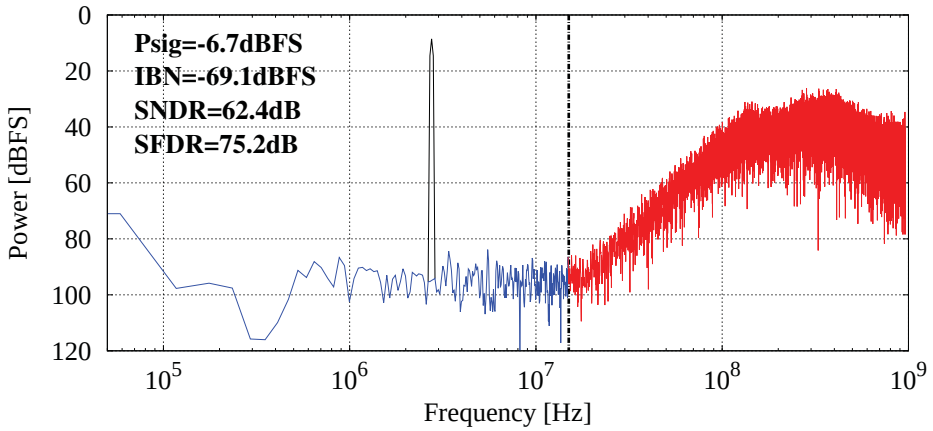
(a) Channel I



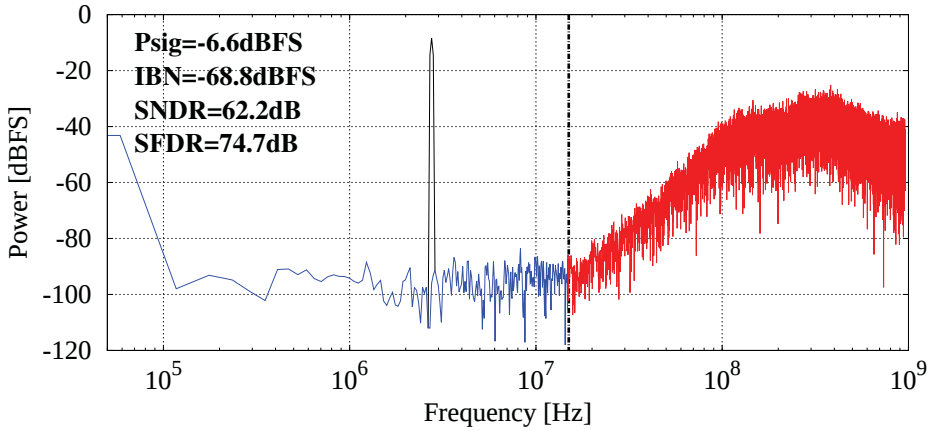
(b) Channel Q

Figure 5.4: Simulated I/Q output spectra of the RF front-end

-3dBm at 10GHz. The FFT length is 2^{15} and a Hann window is applied to the samples. Fig. 5.4 shows the simulated I/Q output spectra. Apparently the RF front-end features a noise floor of approximately -90dBFS with an accumulated IBN of -69.5dB over the 15MHz band of interest. For a -6.7dBFS input, the simulated SNDR is equal to approximately 62.6dB. In addition, at high frequencies close to 1GHz the spectrum shows a roll-off characteristic, which is introduced by the low-pass filter composed of the loading resistor and parasitic capacitors.



(a) ΔΣ modulator I



(b) ΔΣ modulator Q

Figure 5.5: Post-layout simulated spectra of the I/Q ΔΣ modulators

5.2.2 Spectra at the SoC Output

Fig. 5.5 presents the post-layout simulated power spectra at the I/Q output of the receiver SoC. The input of the RF front-end equals -47dBm at 5,002.75MHz while the LO input is -3dBm at 10GHz, which are exactly the same as the input used in the previous simulation of the RF front-end. In analyzing Fig. 5.5, it is clearly visible that the obtained spectra feature a third-order noise shaping characteristic. The outputs of both ΔΣ modulators show a noise floor of approximately -90dB as well as an accumulated IBN of around -69dBFS. Compared to the output spectra of the RF front-end given in Fig. 5.4, the noise floor remains constant, while the accumulated IBN over the interested 15MHz bandwidth is only increased by approximately

0.5dB. Both ΔΣ modulators achieve an SNDR of around 62dB, showing negligible performance degradation compared to the RF front-end output with the same input power. In addition, the simulated SFDR at the output of the SoC is about 75dB, which is only 3dB lower than the 78dB achieved at the RF front-end output. Therefore, in this SoC the RF front-end is the dominant noise contributor, while the following ΔΣ modulator has been designed successfully to perform the A/D conversion without degrading the performance of the RF front-end.

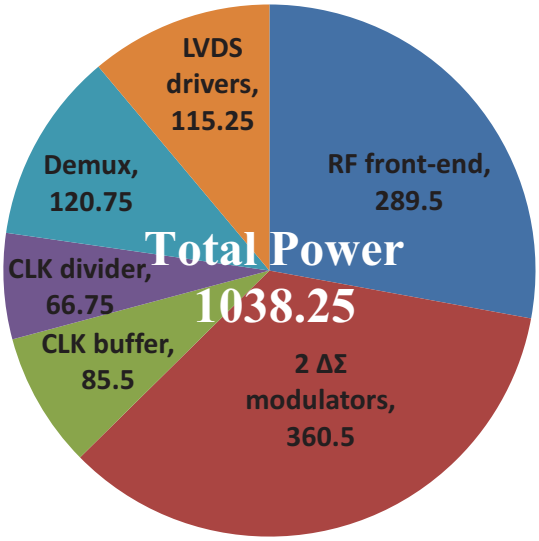


Figure 5.6: Pie chart of simulated power consumption for the receiver SoC (Unit: mW)

Additionally, the simulated power dissipation for different building-blocks of the presented receiver SoC is shown in a pie chart in Fig. 5.6. The power consumption is dominated by the RF font-end and the two ΔΣ modulators. The significantly higher power consumption of the ΔΣ modulator- when compared to fine-line CMOS implementations - is a trade-off to the high performance transistors required for the above 5GHz input of the receiver. Furthermore, it should be mentioned that according to the industrial cooperation partner, the power consumption constraints of this receiver are very relaxed.

Finally, the prototype chip of the SoC was measured by the industrial cooperation partner. In this measurement, the outputs of both modulators were measured 10 times, and averaging was performed to improve SNR. Since the SNR benefit is in proportion to the square root of the number of measurements [65], the SNR should be

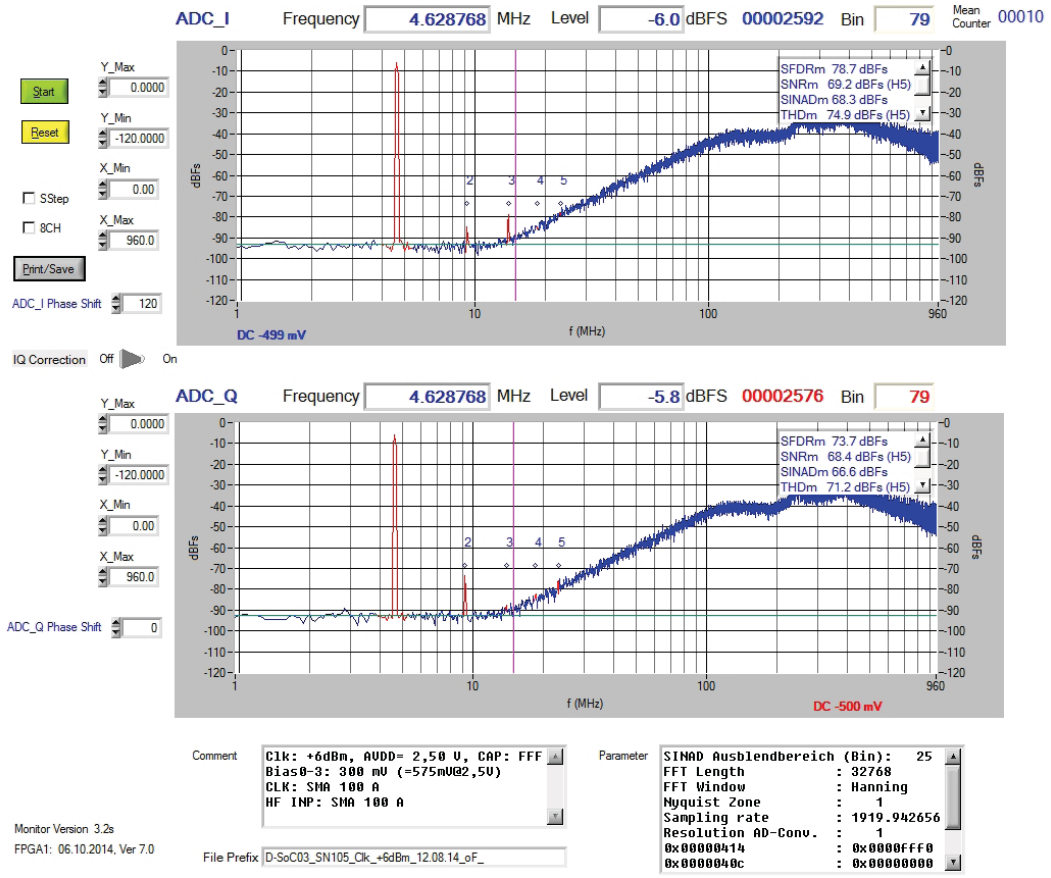


Figure 5.7: Measured spectra of the SoC with 10-times averaging

improved by 10dB ideally. As shown in Fig. 5.7, the measured SNR is around 68dB for both channels, which is 6dB higher than the simulated value shown in Fig. 5.5. The 4dB loss in SNR is due to the parasitics and imperfections of measurement setup. In addition, the measured SFDR of the SoC is approximately 76dB, which is similar to the simulated 74dB shown in Fig. 5.5. Therefore, the measurement results are in good agreement with simulation, and the designed modulator has been well accepted by the industrial cooperation partner.

5.3 SoC Version2

After the successful tapeout of the receiver SoC, another tapeout was required to include a shift register for trimming the SoC. The feedback capacitors in the integrators can be trimmed by switching on or off additional capacitors in the capacitor

array, as described in Section 4.1.6. Additionally, the bias currents of the op-amps can be adapted to tune the GBW. For the previous tapeouts, the biasing currents of the building blocks were generated externally by using potentiometers and series resistors.

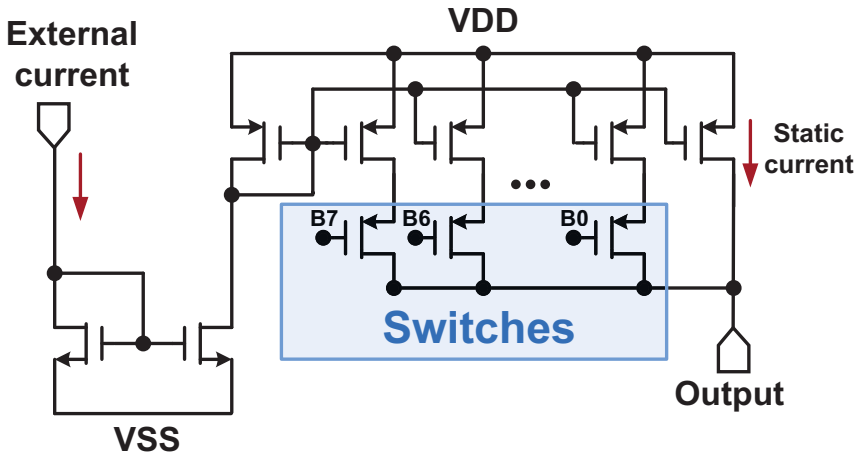


Figure 5.8: Bias trimming circuit

In the second version, a shift register was employed to load the appropriate control bit, and control the capacitor array as well as a set of bias trimming circuits. The bias trimming circuit has been designed to replace the external resistive trimming which was used in the previous tape-outs. As illustrated in Fig. 5.8, several switchable current mirrors are placed in parallel with a static current source to realize a programmable biasing circuit. By loading appropriate configuration bits to the shift register, the biasing current can be scaled properly to bias all the building blocks in the SoC. Furthermore, it is worth mentioning that large on-chip bypass capacitors are placed at the gate terminal of transistors to suppress noise.

The prototype SoC (version 2) was fabricated in a 0.25µm SiGe BiCMOS process with 110GHz f_T HBT, occupying an active area of 10mm^2. Fig. 5.9 shows the microphotograph of the chip with labels. Compared to the previous layout shown in Fig. 5.3, the shift register and the bias trimming circuit are added at the right bottom part of the layout. After the chip fabrication, this prototype SoC will be measured by the industrial cooperation partner.

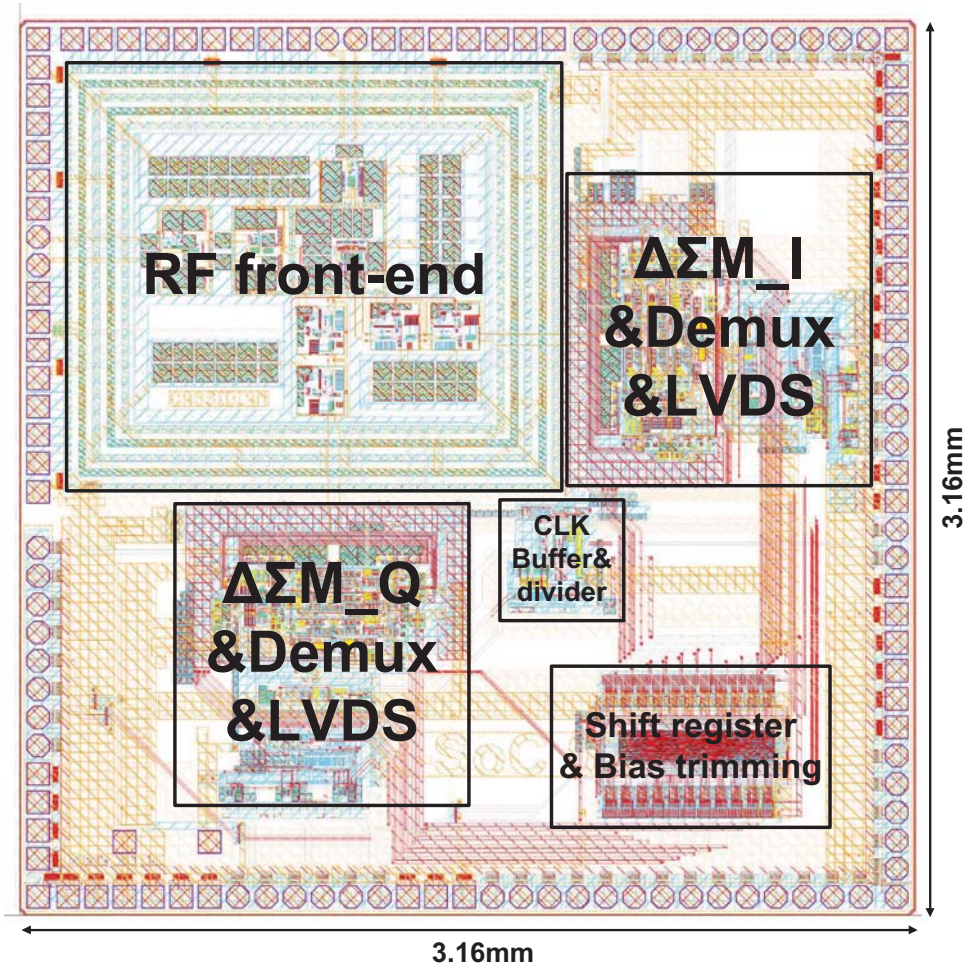


Figure 5.9: Layout of the receiver SoC (version 2)

Chapter 6

Improvements to the Designed $\Delta\Sigma$ Modulator

In Chapter 4, a 15MHz CT single-bit $\Delta\Sigma$ modulator has been proposed, implemented and evaluated. Although the experimental results meet the design requirement from the industrial cooperation partner, there still exist areas for continued development. This chapter discusses enhancement techniques of the single-bit $\Delta\Sigma$ modulator. First, in Section 6.1, the differentiator based ELD compensation technique will be analyzed and then improved to completely compensate for the finite GBW of the op-amps [7]. Additionally, the redesign of the three op-amps will be described in Section 6.2. The op-amps have been redesigned with improved power efficiency while maintaining the same frequency response. Lastly, the redesigned single-bit quantizer and the sin2rec clock buffer will be presented with improved performance.

6.1 Improved Finite GBW Compensation

As discussed in Section 3.4, the mixed-signal differentiator ELD compensation has been extended to counteract the effect of the finite GBW of the op-amps. However, simulations demonstrate that a loss of 3.5dB in SNDR is caused by the employed ELD and GBW compensation, as shown in Table 4.3. Therefore, a more detailed analysis is conducted, and then a modified compensation technique is introduced such that the original NTF of the modulator can be restored.

6.1.1 Finite GBW Problem in Differentiator Based ELD Compensation Technique

As shown in Fig. 6.1, the modulator features an ELD of half a sampling period in order to avoid any signal dependency due to the comparator settling. This constant delay has been compensated for by feeding the differentiated quantizer output to the input of the last integrator [32]. To carry out the differentiation, the quantizer output is delayed by half a clock period, and then the delayed signal (k_{42} output) is subtracted from the non-delayed quantizer output (k_{41} output). No additional summation node is required since the virtual ground input of the last integrator is utilized to sum the differentiated signal in the current domain.

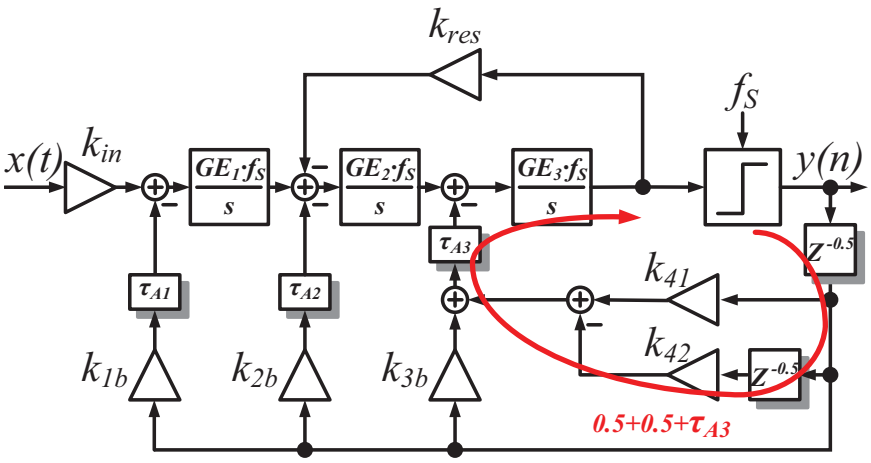


Figure 6.1: Influence of the ELD and finite GBW of the op-amps

Fig. 6.1 illustrates the influence of the ELD and finite GBW of the op-amps in the chosen architecture. It consists of the gain errors caused by the finite GBW ($GE_{1,2,3}$), as well as the delays in the feedback loops. The delays include the constant delay of half a clock cycle which exists between the quantizer clock and the DAC output pulse, another fixed delay of $50\%T_s$ through k_{42} which is employed to implement the differentiation, and the delays ($\tau_{A1,2,3}$) induced by the finite GBW of each op-amp. The last delays ($\tau_{A1,2,3}$) depend on the limited GBW and the input scaling coefficients of each corresponding integrator, as shown in Eq.(3.6) and Eq.(3.7). Therefore these delays have different values for various feedback loops.

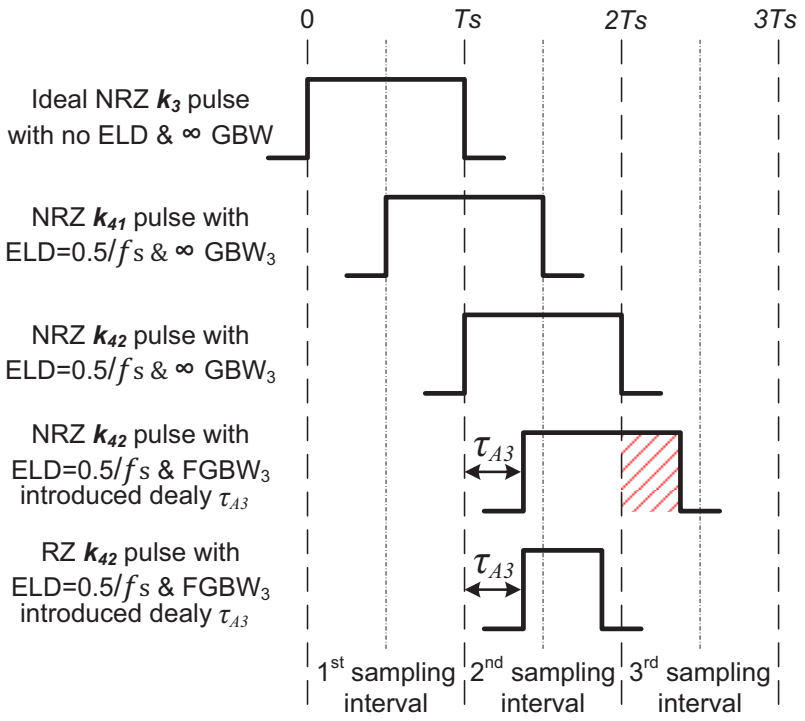


Figure 6.2: Timing diagram of DACs at the input of the last integrator Fig. 6.1

Fig. 6.2 shows the timing diagram of the feedback DACs at the input of the last integrator to graphically illustrate the effect of the delays in the modulator. The node of the input of the last integrator was chosen since it is the critical summation node of the compensation path, which determines the modulator stability. NRZ feedback scheme is incorporated to implement the DAC, as proposed in [32]. For the ideal modulator, the op-amp in the integrator offers infinite GBW, and no ELD exist. Thus the NRZ k_{41} holds the value of the digital data for the whole desired sampling interval (1st T_s). Next the influence of ELD is taken into account, and the ELD is set to half a clock period. Considering the modulator with differentiator based ELD compensation, the NRZ k_{41} is shifted into the 2nd sampling interval due to the $50\%T_s$ ELD, and the NRZ k_{42} output covers the entire period of the 2nd sampling interval since it is delayed by $2\times 50\%T_s$. The part of k_{41} pulse which extends into the 2nd sampling interval increases the order of the modulator, but it can be canceled out by k_{42} pulse which simultaneously exists in the 2nd sampling interval by proper coefficients scaling. In the ELD compensation technique using a differentiator, the k_{42} pulse introduces one additional degree of freedom to counteract the pulses shifted

into the 2nd sampling interval. Consequently, the DT equivalent loop filter of the CT modulator with ELD can be matched to the ideal DT modulator.

However, at the summation node of the compensation path, the finite GBW of the last op-amp introduces another delay (τ_{A3}). Therefore, the k_{42} pulse is shifted and split into two separate feedback pulses, one in the 2nd sampling interval, as well as the other one in the 3rd sampling interval, which has been represented by the red shaded area in Fig. 6.2. Due to the k_{42} pulse in the 3rd sampling interval, the actual modulator order is increased by two, and the DT equivalent loop filter of the non-ideal CT modulator cannot be mapped into the ideal DT modulator. Thus the maximum stable amplitude is decreased and the noise shaping performance is degraded. Consequently, in the chosen architecture employing an NRZ feedback scheme, the last op-amp has to offer a wide GBW in order to minimize the added delay. This wide GBW requirement must be fulfilled since the GBW determines the quality of the virtual ground at high frequencies, which is important to implement the summation node in the compensation technique using a digital differentiator. This stringent requirement results in a power-hungry op-amp.

6.1.2 Proposed Compensation Technique

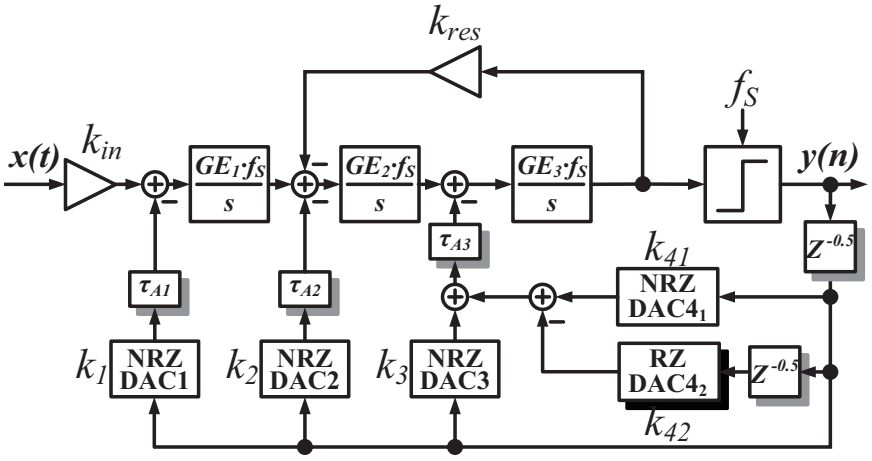


Figure 6.3: The modified third-order CT ΔΣ modulator architecture including ELD and finite GBW compensation

From the above analysis, the high GBW requirement of the last op-amp originates from the part of the NRZ k_{42} pulse shifted into the 3rd sampling interval. Therefore, a RZ pulse scheme can be utilized in k_{42} to eliminate the impact of the finite GBW of the last op-amp, as shown in the bottom of Fig. 6.2. Calculations based on Eq.(3.7) shows that the GBW_3 induced delay τ_{A3} would not shift the k_{42} pulse into the 3rd sampling interval if a RZ pulse scheme with $\{\alpha = 0, \beta = 1/2\}$ is incorporated in the modulator compensated for a finite GBW3=$1.5\times f_S$.

Fig. 6.3 illustrates the CT modulator architecture which incorporates this finite GBW compensation technique [7]. The ELD compensation path is simultaneously used to counteract the effect of the finite GBW of the op-amps. The k_{42} now employs a RZ pulse scheme with $\{\alpha = 0, \beta = 1/2\}$ to prevent its pulse from shifting into the next clock cycle due to the finite GBW_3 induced delay τ_{A3}. The other DAC can either be realized using a NRZ or RZ pulse scheme. In this design, the NRZ pulse scheme is utilized due to its higher cock jitter tolerance and reduced requirement on the op-amp slew rate. In addition, the k_3 and k_{41} can be merged into one DAC when both are NRZ.

For the proposed CT modulator architecture, its loop filter $H(s)$ is determined, and can be mapped into an equivalent DT filter $H(z)|_{CT}$. This mapping is performed taking into account not only the fixed ELD ($50\%T_s$), but also the finite GBW induced delays ($\tau_{A1,2,3}$) and the gain errors ($GE_{1,2,3}$). Subsequently, $H(z)|_{CT}$ is mapped into the original DT loop filter $H(z)$. By comparing the coefficients, the scaling coefficients of the proposed modulator with finite GBW compensation can be calculated, which are given in Table 6.1. Note that since the finite GBW induced delay depends on the scaling coefficients, iterative calculation has to be carried out to achieve a certain accuracy [1].

Table 6.1: Coefficients for the CT single-bit modulator with ELD=$0.5/f_S$, GBW=$1.5\times f_S$ and RZ k_{42}

k_{sig}	k_1	k_2	k_3	k_{41}	k_{42}	k_{res}	c_1	c_2
0.15	0.15	0.1534	0.9081	1.036	1.036	0.0017	0.1831	0.9321

Overall, by utilizing the ELD compensation path and adjusting the coefficients accordingly, the impact of limited GBW induced delays as well as gain errors can be eliminated. Consequently, the original NTF can be perfectly restored and the stability can be preserved. By using the proposed compensation method, the GBW requirement of the op-amps can be significantly relaxed, which is beneficial to reduce the power consumption of the op-amps, especially for the last one [7].

6.1.3 Simulation Results

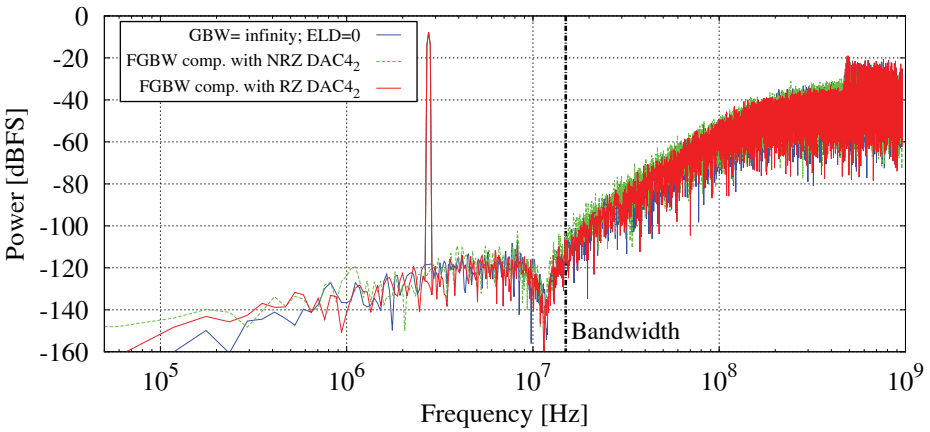


Figure 6.4: Simulated spectra of the ΔΣ modulator with 1. ideal op-amps and no ELD; 2. being compensated for GBW=1.5×f_S and ELD=50%T_s with NRZ k_{42} discussed in Section 3.4; 3. being compensated for GBW=1.5×f_S and ELD=50%T_s with RZ k_{42}

In order to validate the effectiveness of the proposed GBW compensation technique, the ΔΣ modulator in Fig. 6.3 has been simulated in Spectre with transient noise deactivated. Active *RC*-integrators were chosen to implement the loop filter, and all building blocks in the modulator were modeled in Verilog-A with independently controllable parameters. All op-amps featured a limited GBW of 1.5×f_S and the ELD was set to half a sampling period. The compensation path for ELD was simultaneously adapted to eliminate the impact of the finite GBW of the op-amps. The test input signal was at 2.75MHz with an amplitude of -6dBFS. Fig. 6.4 illustrates the simulated spectrum, in addition to the spectrum of the ideal modulator with all op-amps having infinite GBW and no ELD, as well as the spectrum of modulator compensated for GBW=1.5×f_S and ELD=50%T_s with NRZ k_{42} (discussed

in Section 3.4). Compared to the compensation technique with NRZ k_{42}, the compensation method using RZ k_{42} achieves lower in-band noise floor, offering a better approach to the original NTF. From the simulation results it can be observed that the original NTF can be perfectly restored by using RZ k_{42}. Therefore, the presented method with RZ k_{42} succeeds in compensation for both ELD and finite GBW of the op-amps.

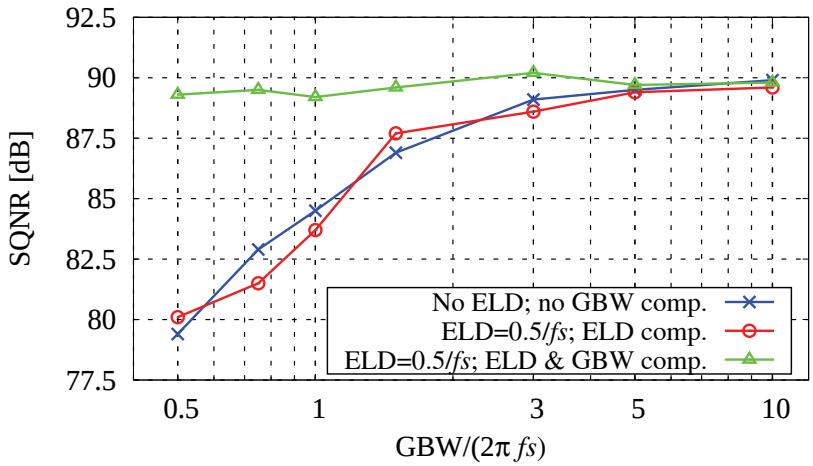


Figure 6.5: SQNR of third-order CT modulator with finite GBW op-amps

Fig. 6.5 illustrates the simulation results for the third-order CT modulator over various GBW values. All the op-amps in the modulator have the same GBW for simplicity, and properly adjusted compensation for the finite GBW has been applied as proposed above. Extremely low values of GBW were not considered since the op-amps also have to fulfill slew rate requirement which cannot be achieved in too low GBW designs. For the modulator without ELD compensation, the SQNR degrades dramatically for GBW below f_S, as shown in red in Fig. 6.5. Similar effects can be seen for the modulator which is only compensated for the $50\%T_s$ ELD. On the other hand, a constant SQNR performance can be maintained for vary small op-amp GBWs by utilizing the proposed compensation method, as shown in green in Fig. 6.5.

In order to verify the robustness of the proposed GBW compensation method, transient simulations were performed with different variations of GBW. All the op-amps in the loop filter were using the same GBW. The ELD of the modulator was set to $50\%T_s$, and the proposed modulator was compensated for GBW of $0.75\times f_S$, $1\times f_S$,

and 1.5×f_S respectively. The GBWs of all three op-amps were swept by the same percentage, while the other coefficients of the modulator were held constant. Fig. 6.6 demonstrates the simulated results on finite GBW over ±30% variation. Obviously, a positive variation upto 30% leads to little influence on the single-loop modulator for all the three coefficients. However, below 90% a gradual decline in SQNR can be seen for the negative variation of GBW, especially for the coefficient compensated for lower GBW. This is because for the coefficient compensated for lower GBW, the same amount of negative variation of GBW induces relatively larger delay, which causes more SQNR degradation compared to the coefficient compensated for higher GBW. Overall, only a drop of 2dB in SQNR can be seen in a GBW variation range of [90%, 130%], meaning for a robust design, a slightly over-compensation is recommended.

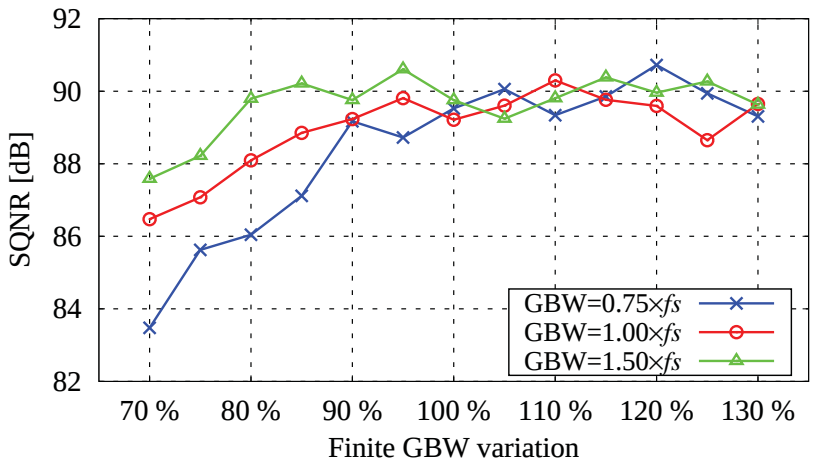


Figure 6.6: Simulated the compensated modulator under the influence of finite GBW variation

6.2 Improvement of Op-amps

Based on the pie graph in Fig. 4.35, one could plainly see that half of the modulator power is consumed by the op-amps. Therefore, these op-amps have been redesigned to improve their power efficiency. During the redesign process, the current flowing through the emitter followers has been minimized while maintaining the frequency requirement of the op-amps. As shown in Table 6.2, the power consumption of

the op-amps has been reduced by approximately 50% without degrading the SNDR performance of the $\Delta\Sigma$ modulator. It should be noted that for the first op-amp, high linearity requirements have to be satisfied; therefore its power could not be reduced significantly. In contrast, the redesigned second op-amp dissipates the lowest power since it drives the smallest load and its nonlinearity is suppressed by the preceding filter. Lastly, the third op-amp consumes more power than the second one since it has to feature sufficient slew rate, as discussed in Section 3.5.4.

Table 6.2: Power consumption of the designed op-amps

Power (mV)	**Op-amp1**	**Op-amp2**	**Op-amp3**
Old design	30.3	30.3	30.7
New design	23.9	13.8	15.1

The loop gain method outlined in 4.1.1 was utilized to simulate the performance of the redesigned op-amps. The simulated loop response with and without the integration capacitors is shown in Fig. 6.7, Fig. 6.9 and Fig. 6.11, respectively. In these figures the DC gain, GBW and PM are identified. The GBW and PM are determined when including the integration capacitor in the feedback, while the DC gain of the op-amp is derived by shorting out the integration capacitor. Table 6.3 shows a summary of the simulated DC gain, GBW and PM for the redesigned op-amps. When referring to the op-amps' requirements derived in Section 3.5.5, these redesigned op-amps satisfy the constraints with margin.

Table 6.3: Performance summary of the redesigned op-amps

Parameter	**Op-amp1**	**Op-amp2**	**Op-amp3**
DC gain (dB)	65.5	66.2	62.8
GBW (GHz)	3.1	2.9	3.2
PM (°)	72.2	64.7	73.3

In addition, Monte Carlo simulations with 500 runs have been performed for these redesigned op-amps, and the simulated histograms are given in Fig. 6.8, Fig. 6.10 and Fig. 6.12, respectively. Apparently, all these op-amps achieve reasonable robustness against process variation and mismatch.

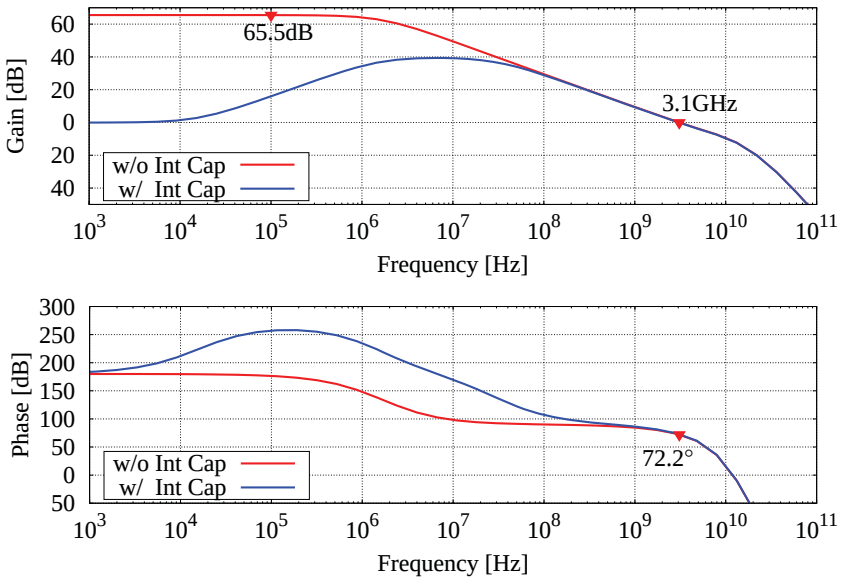


Figure 6.7: Simulated frequency response of the redesigned op-amp1

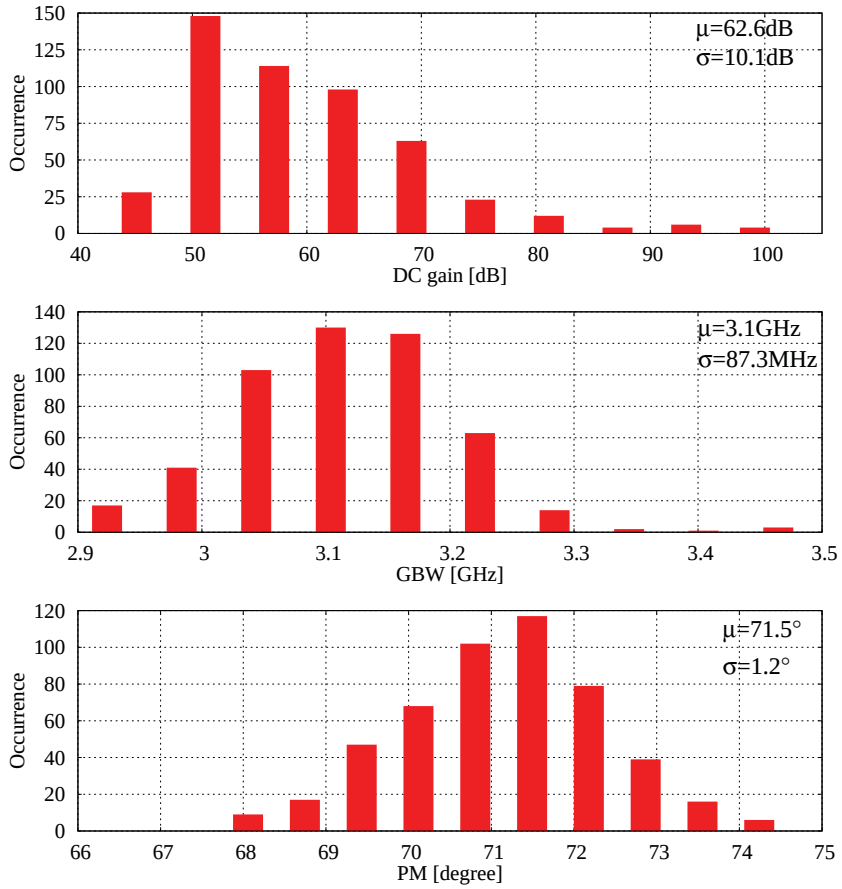


Figure 6.8: Monte Carlo simulation results of the redesigned op-amp1 (500 runs)

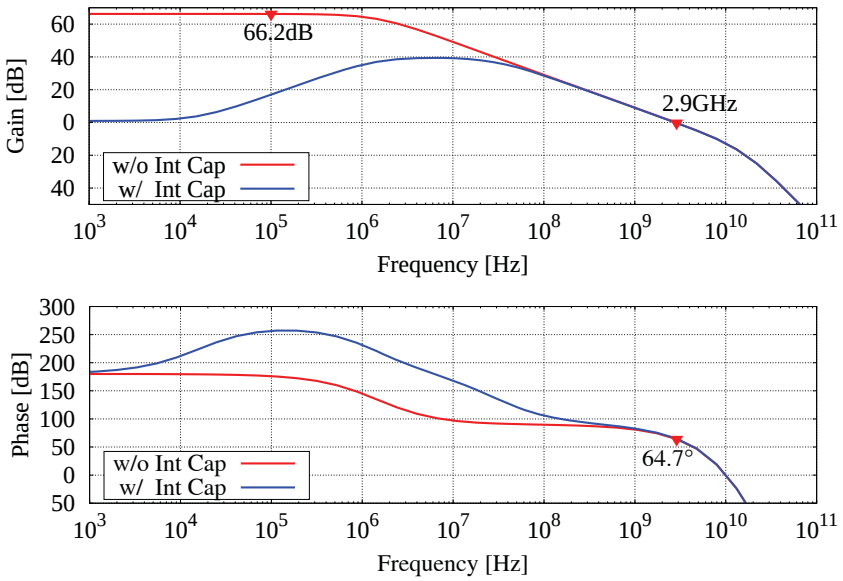


Figure 6.9: Simulated frequency response of the redesigned op-amp2

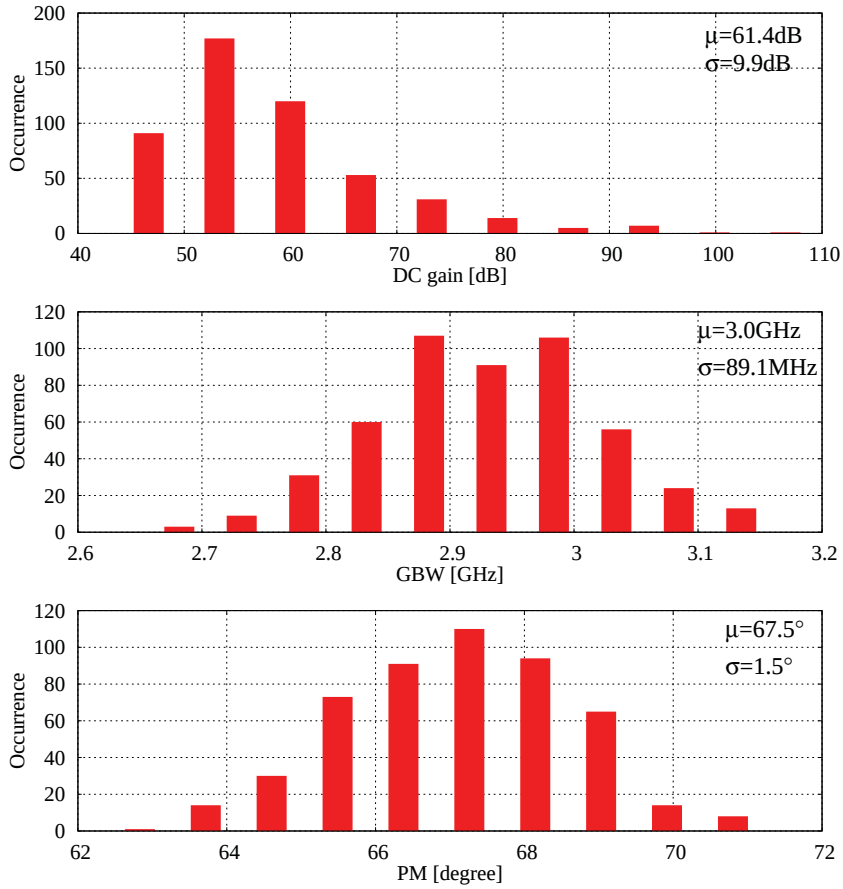


Figure 6.10: Monte Carlo simulation results of the redesigned op-amp2 (500 runs)

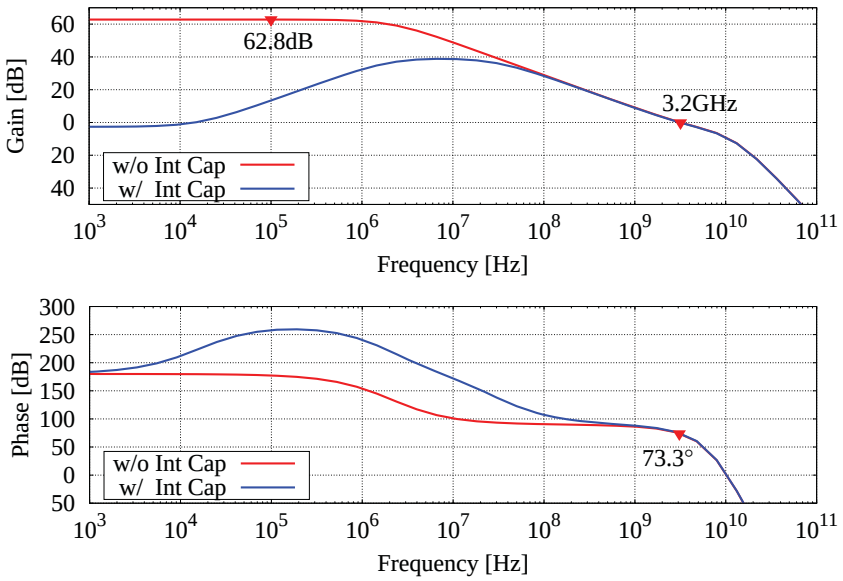


Figure 6.11: Simulated frequency response of the redesigned op-amp3

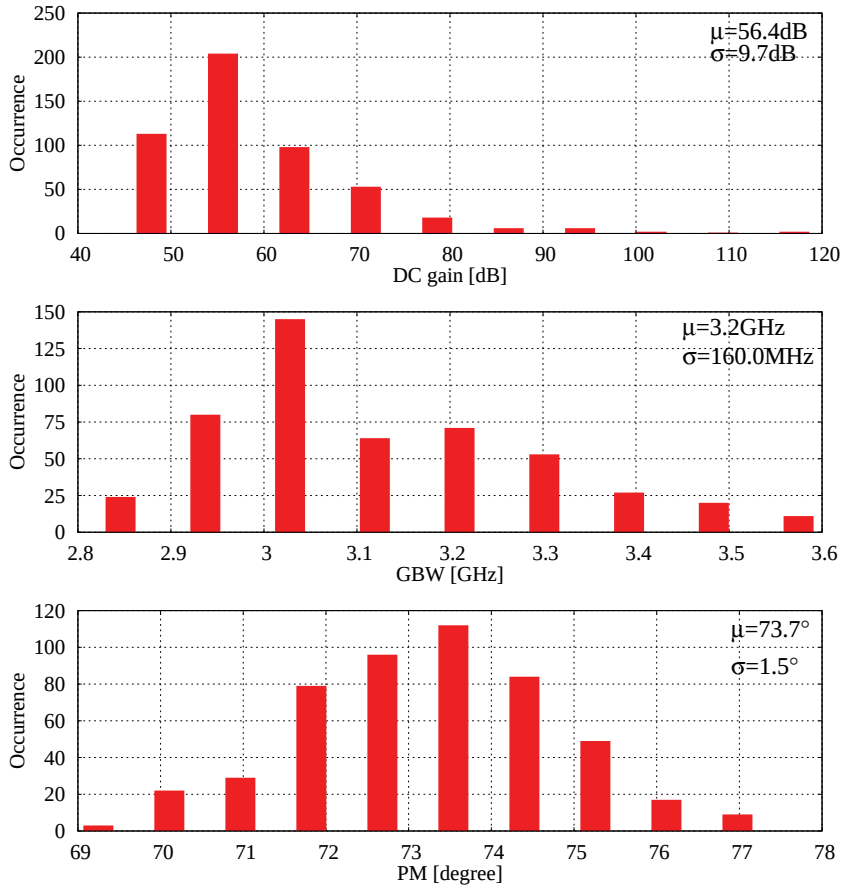


Figure 6.12: Monte Carlo simulation results of the redesigned op-amp3 (500 runs)

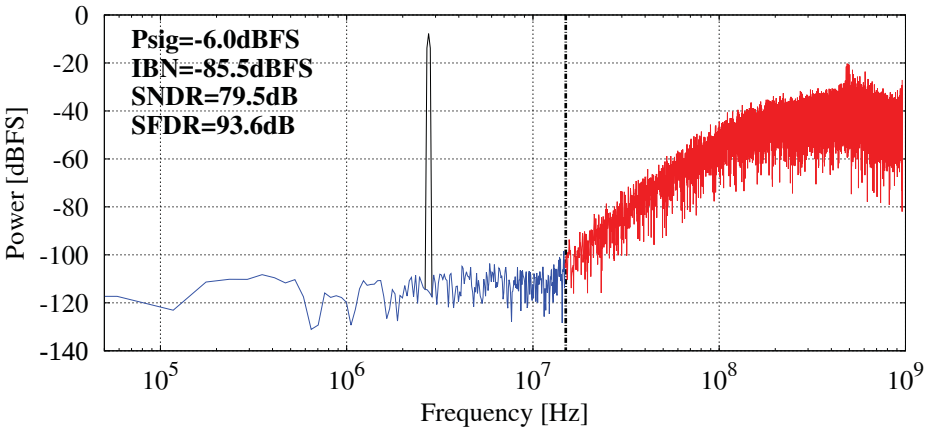


Figure 6.13: Simulated spectrum of behavioral model including three redesigned op-amps with a -6dBFS input signal at 2.75MHz (2^{15} points using a Hann window)

In order to verify whether the redesigned op-amps fit into the system environment, transient simulation was performed for a modulator with three redesigned transistor-level op-amps while the other building blocks were ideal Verilog-A models. The ELD was set to $50\%T_s$, while the finite GBW of op-amps was compensated by using the proposed method described in Section 6.1.2. In this simulation the transient noise was activated, and the modulator was fed with a -6dBFS sine wave at 2.75MHz. Fig. 6.13 shows the simulated spectrum, indicating that the modulator achieves an SNDR of 79.5dB. Note that the previously designed op-amps limited the modulator performance to 79.3dB, as shown in Table 4.3. Therefore, the redesign of these op-amps is successful and approximately 50% power consumption can be saved without degrading the modulator performance.

6.3 Improvement of the Single-bit Quantizer

As discussed in Section 4.5, an SNDR of 76.4dB is achieved when only the transistor-level quantizer and the sin2rec clock buffer are included in the behavioral modulator while the other building blocks are Verilog-A based ideal components. In this simulation the transient noise was activated so that only the non-idealities of the quantizer and the noise from resistors degraded the ideal SNDR. Since the SNDR is limited to

83dB due to the resistor noise, the quantizer is the main source of SNDR degradation and should be redesigned.

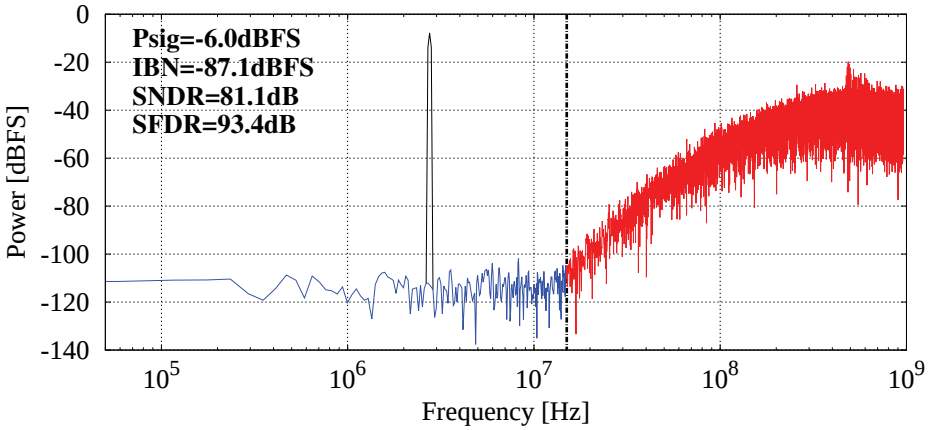


Figure 6.14: Simulated spectrum of behavioral model including the new designed quantizer with -6dBFS input signal at 2.75MHz (2^{15} points using a Hann window)

After a careful examination and inspection, it was found that the emitter follower at the sin2rec clock buffer is not capable to drive the three latches in the quantizer at such a high frequency of 1.92GHz. Therefore, more emitter followers are inserted at the sin2rec clock buffer output and each latch is driven by one individual emitter follower. In addition, the biasing of the HBT transistors has been increased to 1.2 times maximum f_T current density, so that the gain of each latch is increased, leading to reduced metastability errors.

Fig. 4.1 illustrates the simulated spectrum when the redesigned quantizer is included in the behavioral modulator model while the other building blocks are Verilog-A based ideal components. The modulator achieves 81.1dB SNDR as well as 93.4dB SFDR for a -6dBFS input at 2.75MHz. Note that the SNDR is limited to 83dB due to the resistor noise, as discussed in Section 4.5, therefore the non-idealities of the quantizer only results in a 2dB loss in SNDR, which has been significantly improved compared to the original design with an SNDR of 76.4dB.

Chapter 7

Nonlinearity of the First Op-amp in CT $\Delta\Sigma$ Modulators

In this chapter, the nonlinear effect of the first op-amp in an exemplary CT third-order $\Delta\Sigma$ modulator has been studied when the finite GBW compensation technique is adopted in the loop filter design. In order to approximate the nonlinear characteristic of the op-amp, a behavioral model employing a hyperbolic tangent expression has been developed and verified. Under the influence of op-amp's nonlinearity, the performance of the CT single-bit $\Delta\Sigma$ modulator compensated for different GBWs has been investigated, indicating that more stringent linearity requirement on the first op-amp must be satisfied if the modulator is compensated for lower GBW [8]. Additionally, two approaches have been proposed to address this issue, one method is to increase the op-amp's DC gain, and the other is to incorporate the mixed FF/FB architecture which reduces the output swing of the op-amp.

7.1 Introduction

As described in Section 3.4, the finite GBW compensation technique [1] [31] provides an approach which allows the GBW of internal op-amps to be chosen even below the sampling frequency while maintaining the original noise shaping performance of the modulator. Since the current flowing in HBT op-amps is proportional to GBW, a power-efficient modulator can be achieved taking advantage of this technique.

However, the effectiveness of this compensation technique is questionable and must be compromised under the influence of the op-amp's nonlinearity.

7.2 Exemplary ΔΣ Modulator

The CT 15MHz third-order single-bit ΔΣ modulator discussed in the previous chapters has been reused to study the nonlinear effect of the first op-amp when the finite GBW compensation technique is adopted in the modulator design. The block diagram of the ΔΣ modulator is given in Fig. 7.1, while active *RC*-integrators are chosen to implement the modulator. It is based on the CIFB topology, and the sampling frequency is 1.92GHz with an OSR of 64. Since the input stage is the most critical building block in a CT ΔΣ modulator, in this work only the non-idealities of the first op-amp, such as finite GBW and nonlinearity, are taken into account. Additionally, the ELD is set to half a sampling period, and the mixed-signal differentiator technique for ELD compensation has been extended to counteract the effect of the finite GBW of the first op-amp [7].

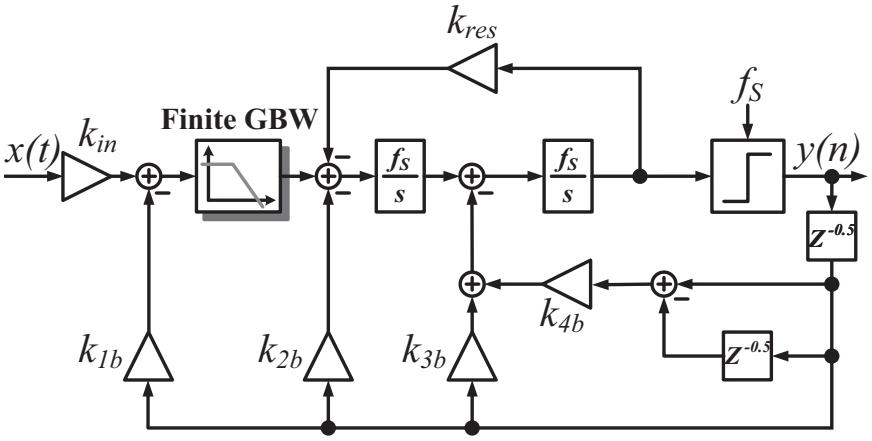


Figure 7.1: Architecture of the third-order single-bit CIFB modulator

Since there is no preceding loop filter to suppress the nonlinearity of the input stage, it is worthwhile to carry out simulations to check the signal at the virtual ground node of the first op-amp if the modulator employs finite GBW compensation. In these simulations, the DC gain of the first op-amp is fixed to a reasonable value of 60dB; in contrast, its finite GBW is swept for different values but the effect of the

finite GBW has been counteracted by coefficient tuning. Consequently, the modulators employing op-amp1 with different GBWs feature the identical noise shaping performance.

Fig. 7.2 shows the simulated spectra at the virtual ground node of the first op-amp for a modulator input signal of -9dBFS while the transient noise is deactivated. For the almost ideal GBW1 of $50\times f_S$, the signal power at the virtual ground node P_{sin} is equal to -74.7dBFS. As the modulator is compensated for lower GBW, P_{sin} increases and higher residual voltage fluctuations can be observed at the virtual ground node; this is clear as the op-amp is not fast enough anymore to keep the virtual ground node stable. Consequently, together with non-linearities, more distortion can be expected at the output of the op-amp, as well as the modulator output.

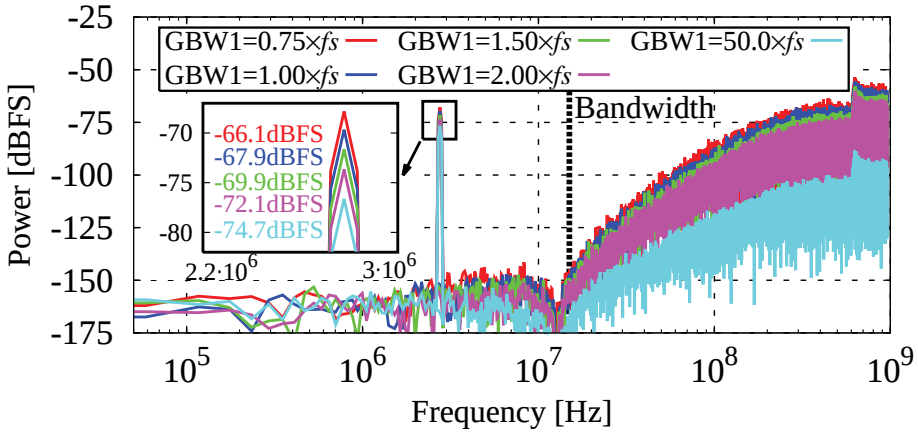


Figure 7.2: Spectra at the virtual ground node of the first op-amp

7.3 Nonlinear Op-amp Modeling

In order to approximate the op-amp nonlinear characteristics, a behavioral op-amp model has been developed, in addition to the op-amp's typical specifications such as GBW, slew rate and DC gain. The nonlinear input/output characteristic of op-amps can be approximated with a simple hyperbolic tangent by [66]

$$V_{out} = f(V_{in}) = a \cdot tanh(b \cdot V_{in}) \tag{7.1}$$

In order to reasonably fit the actual characteristics of transistor-level op-amps by using Eq.(7.1), the parameters a and b should be selected according to the following equations:

$$a \cdot b = \frac{d}{dV_{in}} f(V_{in})|_{V_{in}=0} = Gain|_{V_{in}=0} \tag{7.2}$$

$$a \cdot tanh(\pm bV_{in,max}) = f(\pm V_{in,max}) \tag{7.3}$$

The nonlinear op-amp model is realized in Verilog-A, and parameters of this model include GBW, slew rate as well as small-signal DC gain $Gain|_{V_{in}=0}$. Note the op-amp nonlinear gain in the Verilog-A model can be viewed as a variation with the input signal level. Calculating a from Eq.(7.1) and substituting in Eq.(7.2), this results in the op-amp nonlinear gain:

$$Gain_{nonlinear} = \frac{Gain|_{V_{in}=0} \cdot tanh(b \cdot V_{in})}{b \cdot V_{in}} \tag{7.4}$$

where the nonlinearity coefficient b can be treated as a metric for quantifying the extent of nonlinearity [8].

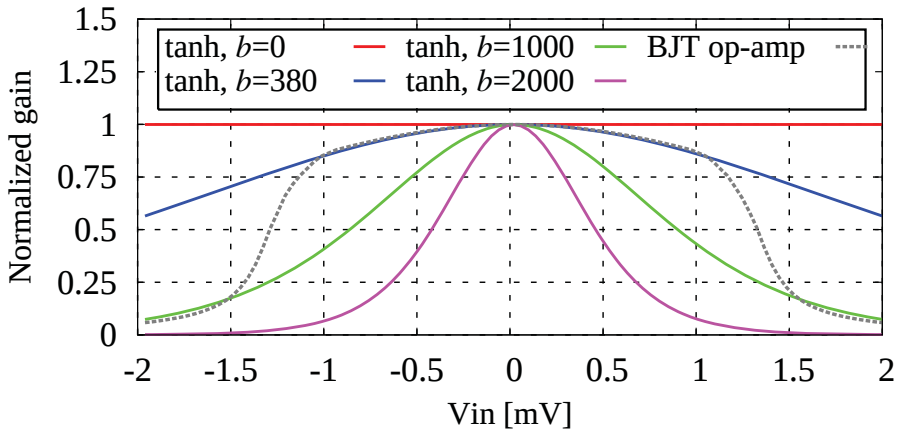


Figure 7.3: Normalized op-amp gain versus Vin

Fig. 7.3 exhibits the simulated model input/output characteristics for different nonlinearity coefficients b. The input range of the op-amp is limited to $[-2\text{mV}, 2\text{mV}]$, which is reasonable for an op-amp with a small-signal DC gain of 60dB as well as a

output swing of 1V. In addition, the op-amp gain is normalized to the small-signal DC gain in Fig. 7.3; therefore a straight line of unity can be observed for $b = 0$ since in this case there is no nonlinearity. For extremely small input swing, the nonlinear effect is negligible, and obviously all normalized non-linear gains are approximately unity which are independent of the nonlinearity coefficient b. As the input signal increases, in the nonlinear model the op-amp gain starts to drop due to nonlinearity. Furthermore, more severe deviation of the gain can be seen as b increases. As a consequence, the nonlinearity coefficient b in Eq.(7.4) can be used as a variable to investigate the nonlinear effect of the first op-amp in CT $\Delta\Sigma$ modulators.

In addition, the input/output transfer curve of a transistor-level implemented two-stage Miller-compensated op-amp1 discussed in Section 4.1.1 is also depicted in Fig. 7.3. In a reasonably small input range of [-1mV, 1mV], the gain of tanh model for b=380 is in good agreement with that of the transistor-level op-amp.

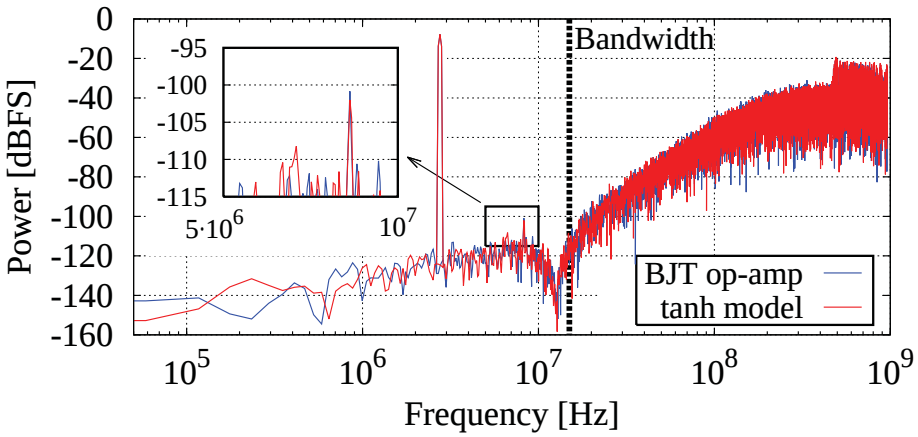


Figure 7.4: Simulated spectra of the CT $\Delta\Sigma$ modulator with nonlinearity in the first op-amp, comparing transistor-level and tanh model

In order to further verify the accuracy of the nonlinear model in the CT $\Delta\Sigma$ modulator, transient simulations were carried out with noise deactivated. Fig. 7.4 shows the output spectra of the modulator when the first integrator is implemented with the transistor-level op-amp or the tanh model with b=380, respectively. In this simulation, the tanh model features a GBW of $1.5\times f_S$ and a small signal DC-gain of 62dB, which are the same as the transistor-level op-amp1 discussed in Section 4.1.1. As shown in Fig. 7.4, the modulator with tanh model op-amp exhibits the same noise shaping property as the one implemented with transistor-level op-amp1.

Analyzing the nonlinearity, the simulated SFDR is approximately 95dB. Note the difference in the visible third-order harmonic distortion is only 1.5dB, indicating that the nonlinear model works well with reasonable accuracy.

7.4 Simulation Results of the CIFB Modulator

Since the tanh model reasonably fits the actual characteristics of transistor-level op-amp, the nonlinear effect of the first op-amp can be investigated in CT modulators which adopt finite GBW compensation. Behavioral simulations have been performed without transient noise. The first op-amp features different GBW, but the influence of the finite GBW has been compensated in the loop filter design. Thanks to the finite GBW compensation, all the modulators achieve the same NTF as the ideal one with no finite GBW non-idealities. In order to make an unbiased comparison, all the modulators have the same input scaling coefficient k_{in} and k_{1b}, while the other coefficients have been tuned to perform the GBW compensation. The feedback DACs have a NRZ scheme, while the small-signal DC gain of the first op-amp is set to a common value of 60dB in all simulations.

7.4.1 Single-Tone Test

Single-tone simulations have been carried out first. In these simulations, the input signal frequency is 2.75MHz to include the majority of harmonics in the 15MHz bandwidth. Additionally, the modulator input signal has a reasonably large value of -9dBFS to guarantee the stability, since the maximum stable amplitude is -6dBFS.

Fig. 7.5 shows the simulated spectra over the nonlinearity coefficient b of the first op-amp in the modulator compensated for GBW1=$0.75\times f_S$. Obviously, the performance degradation of the modulator becomes more significant as the nonlinearity of the first op-amp increases. More harmonic distortion appears at the modulator output for higher nonlinearity coefficient b, and therefore the SFDR deteriorates. In addition, the noise floor rises as the nonlinearity of the first op-amp becomes more severe, since the op-amp nonlinearity causes the high-frequency quantization noise

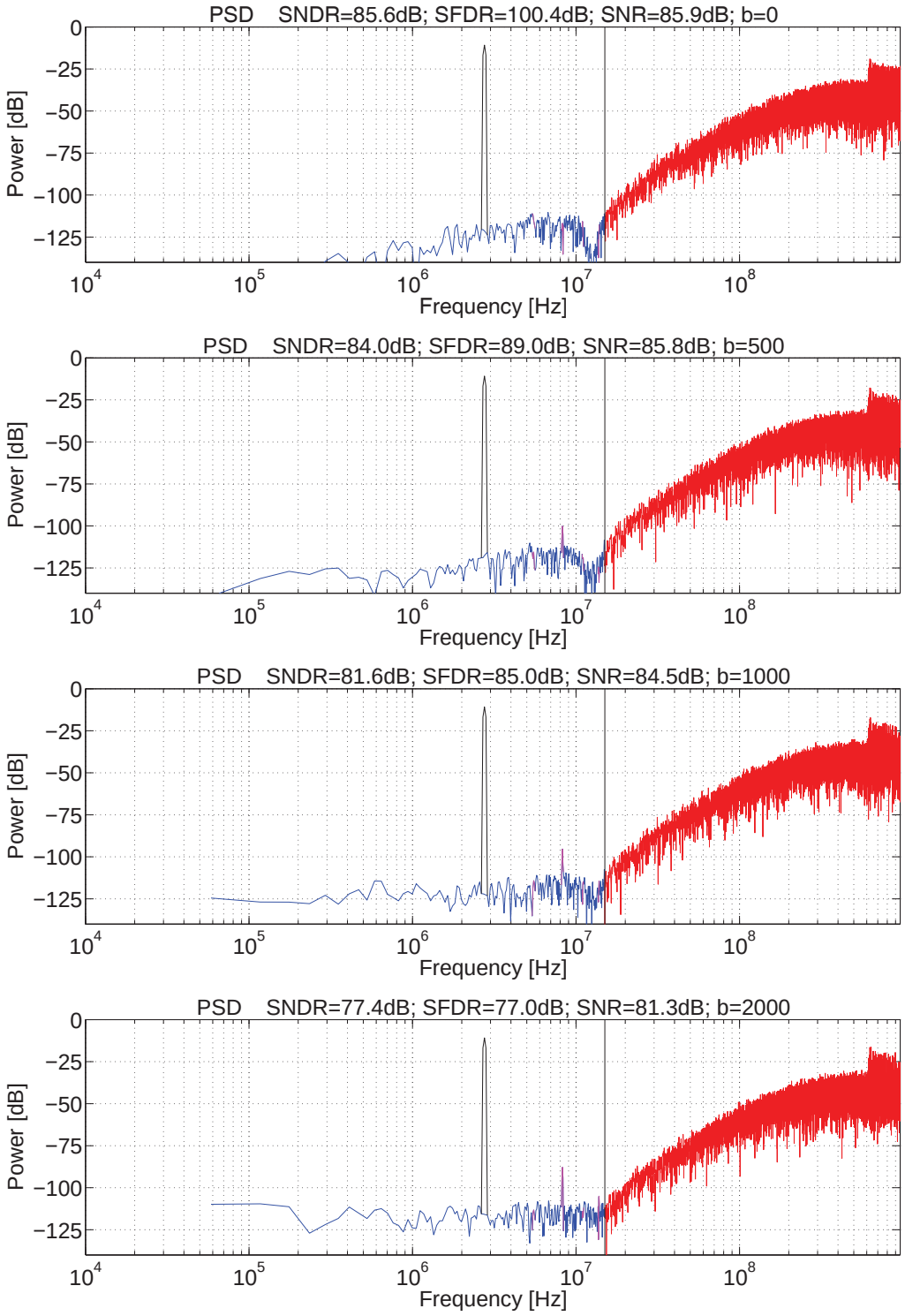


Figure 7.5: Simulated spectra over the nonlinearity coefficient b of the first op-amp. GBW1=$0.75\times f_S$, P_{sig}=-9dBFS

to inter-modulate and then fold back into baseband frequency [67]. Consequently, the combined effect of the raised noise floor and the increased distortion result in a degradation of the SNDR.

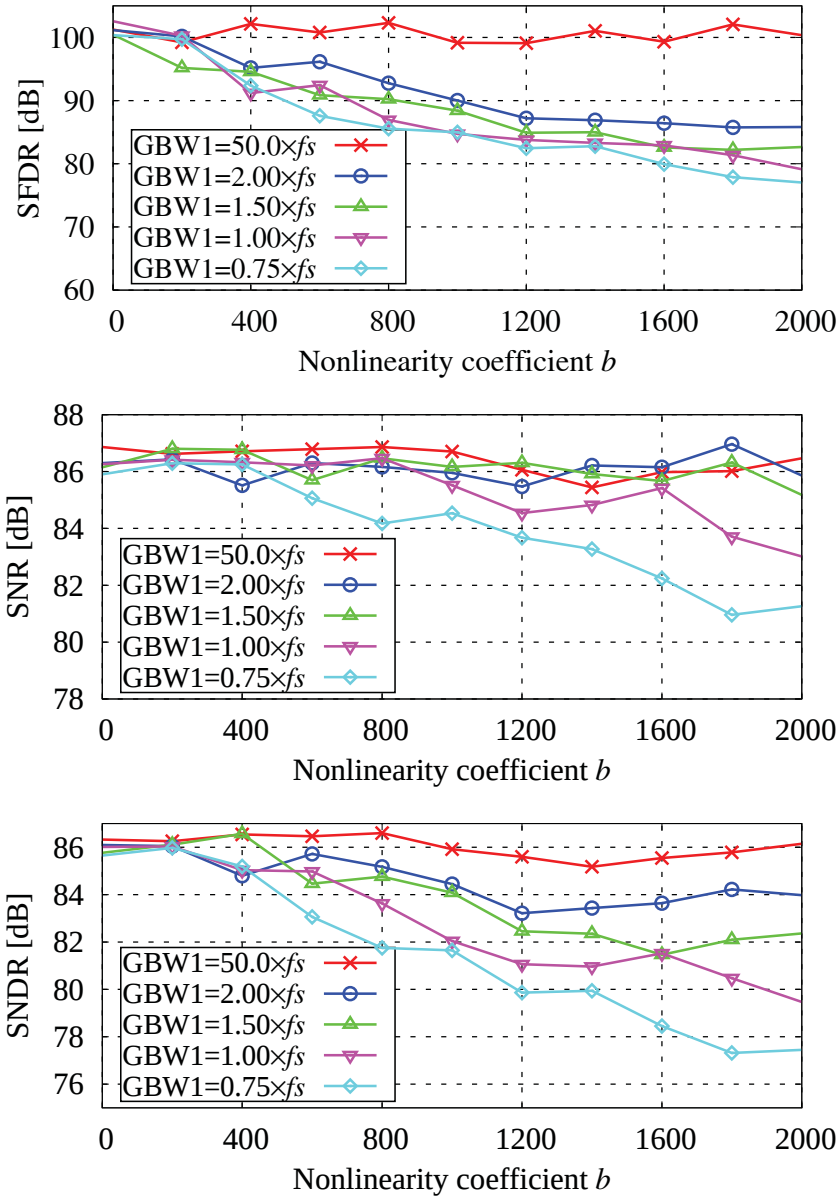


Figure 7.6: Output SFDR, SNR and SNDR versus the nonlinearity coefficient b of the first op-amp in modulators compensated for different GBWs. P_{sig}=-9dBFS at 2.75MHz, Adc=60dB

Furthermore, Fig. 7.6 presents the simulated SFDR, SNR and SNDR versus the nonlinearity coefficient b of the first op-amp in modulators compensated for different GBWs. It can be seen that the modulator performance deteriorates due to

the increasing nonlinearity of the first op-amp. Note that more severe performance degradation is visible in modulators using slower op-amps, although the GBW compensation technique has been incorporated. Therefore, the employment of op-amps with lower GBW has to fulfill higher linearity requirements in order to avoid any performance degradation.

7.4.2 Two-Tone Test

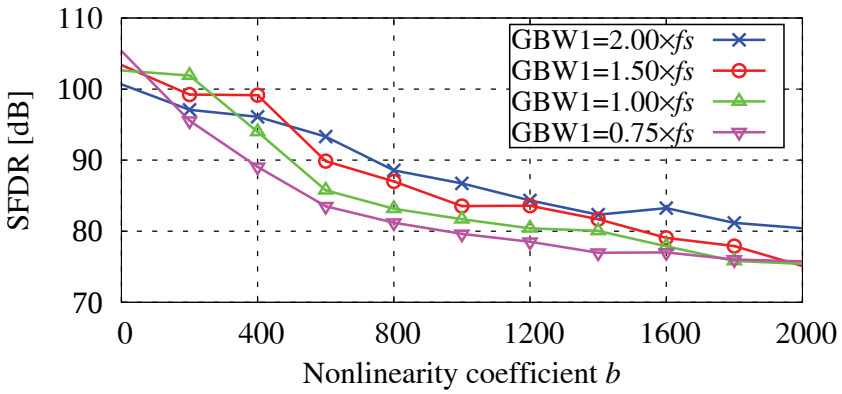


Figure 7.7: Simulated SFDR as a function of the nonlinearity coefficient b of the first op-amp for two-tone simulations. Two -12dBFS input tones at 12MHz and 14MHz are applied

In addition, two-tone simulations were also performed to examine the distortion caused by the first op-amp in modulators compensated for different GBWs. In these simulations, two input signals of -12dBFS at 12MHz and 14MHz have been fed into the modulator; consequently, the inter-modulation components locate at the band edge. The simulated SFDR over nonlinearity coefficient b is depicted in Fig. 7.7. For the same nonlinearity coefficient b, more significant degradation in SFDR can be seen in the modulator compensated for lower GBW. Therefore, more stringent linearity requirements on the first op-amp should be satisfied in the modulator compensated for lower GBW.

Furthermore, the SFDR in two-tone simulations is degraded more severely compared to the single-tone simulation results shown in Fig. 7.6, since for the same input amplitude, the third inter-modulation distortion component is theoretically 3 times as high as the third order harmonic distortion of single-tone simulation [68].

7.5 Methods to Reduce the Op-amp Linearity Requirements

Since the modulator compensated for lower GBW shows a higher sensitivity to the op-amp nonlinearity, methods to reduce the linearity requirements have been studied. Two approaches are proposed to address this issue, one method is to increase the op-amp's DC gain, and the other is to incorporate the mixed FF/FB architecture which reduces the output swing of the op-amp.

7.5.1 The DC gain Effect on the Linearity Requirement

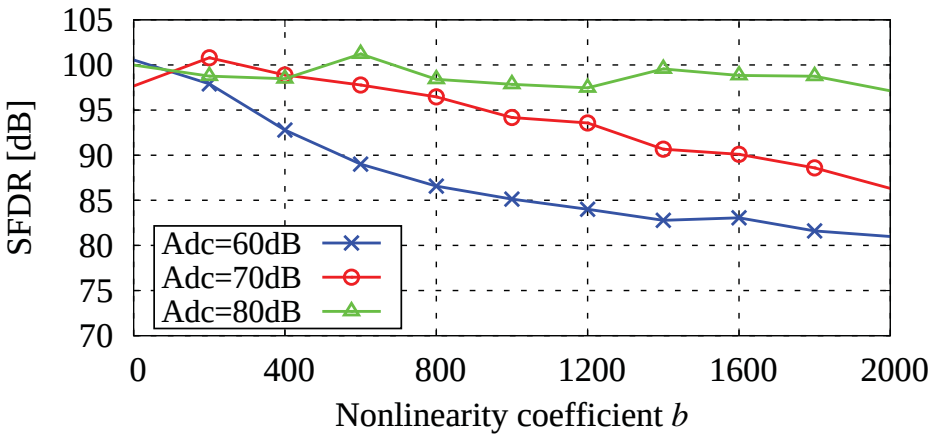


Figure 7.8: Simulated SFDR vs. different DC gain of the first op-amp in the CIFB modulator compensated for GBW1=0.75×f_S. P_{sig}=-9dBFS at 0.18MHz

One common method used to reduce the linearity requirements on the op-amp is to increase the DC gain. Although in a single loop modulator, a DC gain in the range of the OSR is sufficient to minimize the non-ideal effect from the leaky integration [1] [10], more DC gain is normally required to suppress the nonlinear distortion. For the CIFB modulator in Fig. 7.1 compensated for GBW1=0.75×f_S, transient simulations have been performed to verify the DC gain effect on the nonlinearity. As shown in Fig. 7.8, modulators implemented with higher DC gain op-amps are less sensitive to nonlinearity. A higher than 95dB SFDR can be guaranteed by increasing the op-amp DC gain to 80dB, even for a significantly large nonlinearity of $b = 2000$.

However, an increase of DC gain normally can be achieved at a cost of more power consumption due to the demand of more gain stages.

In addition, it should be noted that this method is only effective for signals within the bandwidth of the op-amp. Fig. 7.8 shows the simulated SFDR for f_{sig} = 2.7MHz. Note the op-amp GBW is fixed at 0.75×f_S; thus, the op-amp features the same gain at 2.7MHz when sweeping Adc from 60dB to 80dB. Consequently, the achieved SFDR of the modulator is approximately the same for different DC gains, as shown in Fig. 7.9.

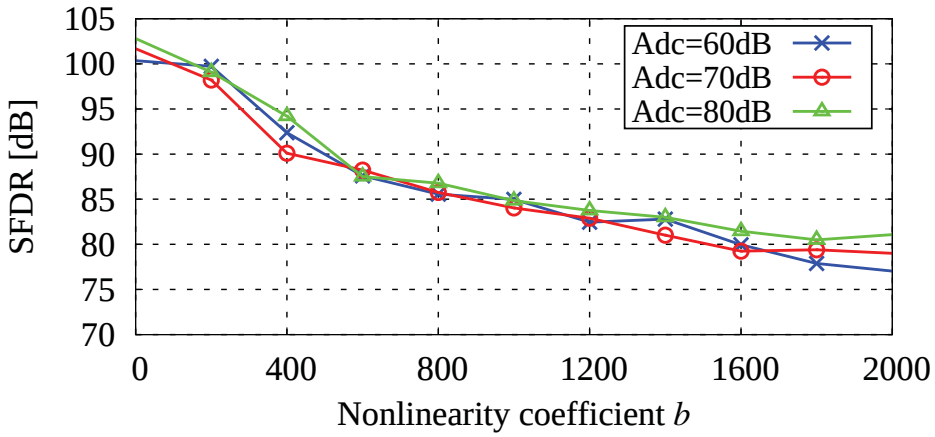


Figure 7.9: Simulated SFDR vs. different DC gain of the first op-amp in the CIFB modulator compensated for GBW1=0.75×f_S. P_{sig}=-9dBFS at 2.7MHz

7.5.2 Nonlinearity in the Mixed FF/FB Modulator

In the CIFB architecture in Fig. 7.1, the output swing of the first integrator is relatively large due to the presence of a significant amount of the input signal. Therefore, a stringent requirement on the linearity should be satisfied. In order to overcome this effect, the DAC2 in this modulator can be removed while adding a feed-forward path k_{2ff} across the second integrator. Consequently, a mixed FF/FB topology featuring the same NTF can be obtained, as illustrated in Fig. 7.10. One major advantage of this architecture is that the first op-amp output swing is significantly reduced, and therefore lower sensitivity to nonlinearity can be expected. However, this topology suffers from an aggravated STF peaking at high frequencies, which is induced by the feed-forward path.

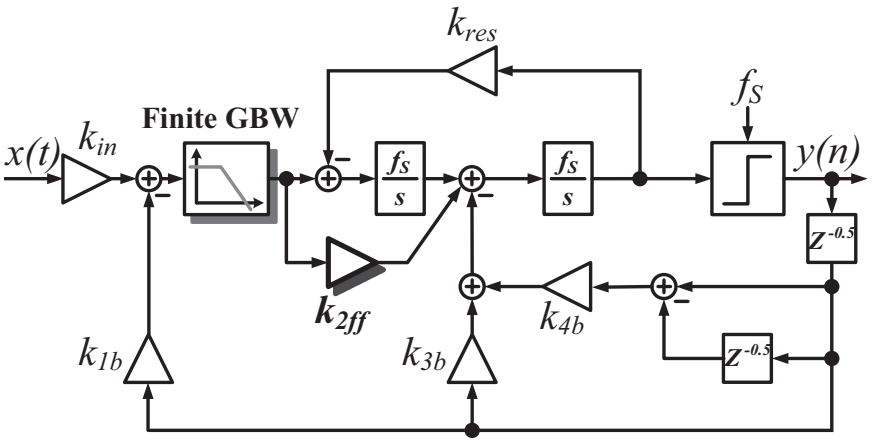


Figure 7.10: Architecture of the third-order mixed FF/FB modulator

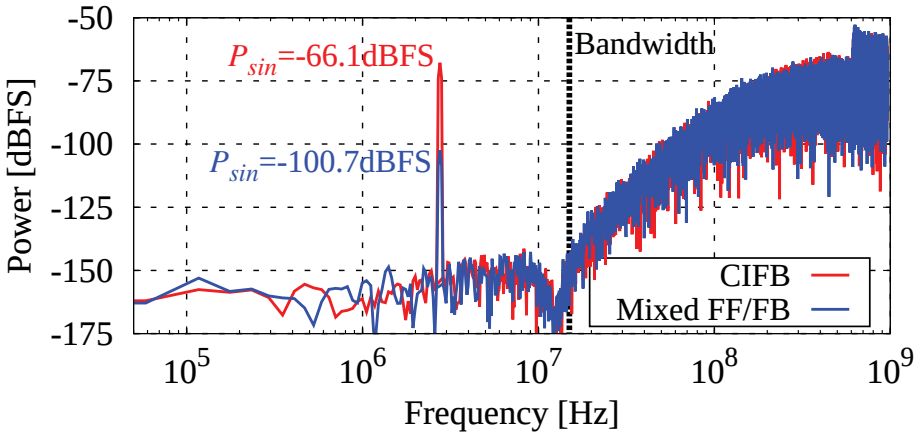


Figure 7.11: Spectrum of the first op-amp input signal in the mixed FF/FB modulator. GBW1=0.75×f_S, P_{sig}=-9dBFS, Adc=60dB

The mixed FF/FB modulator also adopts finite GBW compensation, and effect of the limited GBW1 of 0.75×f_S has been counteracted by the differentiating path. The same input scaling coefficient k_{in} and k_{1b} are used as the ones used in the CIFB topology, and identical NTF can be achieved by both topologies. For the mixed FF/FB modulator, behavioral simulation was performed to check the virtual ground of the first op-amp, and the simulated spectrum is displayed in Fig. 7.11 with a reference of the CIFB modulator compensated for the same GBW1. Clearly, the signal power of the input tone is -100.7dBFS at the virtual ground of the first op-amp in the mixed FF/FB modulator, which is 33.4dB smaller than the one in the CIFB topology in the shown simulation example. Therefore, it can be expected that the mixed FF/FB modulator should offer a much higher tolerance to the nonlinearity of

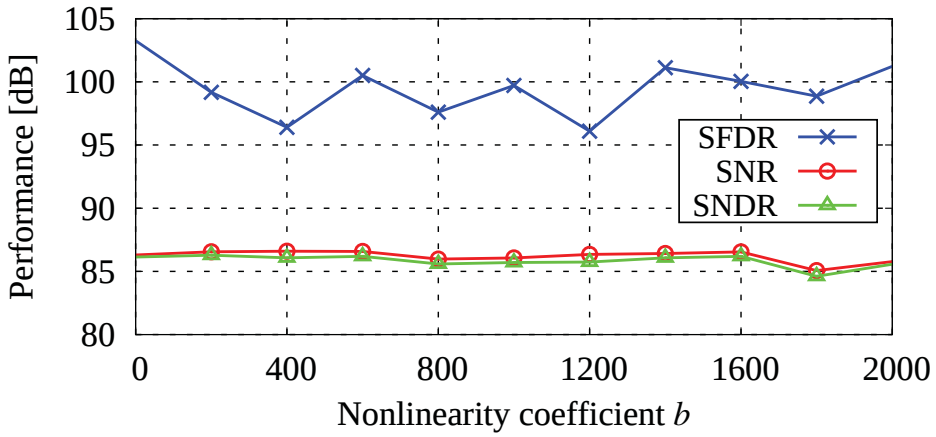


Figure 7.12: Simulation results of the mixed FF/FB modulator vs. nonlinearity coefficient b. GBW1=0.75×f_S, P_{sig}=-9dBFS, Adc=60dB

the first op-amp, and this has been proved by further simulations. Fig. 7.12 shows the performance of the mixed FF/FB modulator over the nonlinearity coefficient b, and there is negligible performance degradation even for a large b of 2000. Note in these simulations the op-amp features a DC gain of 60dB. Compared to the CIFB architecture, the linearity requirement of the first op-amp is significantly relaxed in the mixed FF/FB modulator with finite GBW compensation.

7.6 Conclusion

Although the finite GBW compensation technique provides an approach to reduce op-amp GBW while maintaining the original NTF performance of the modulator, this advantage is alleviated when taking the nonlinear effect of the op-amp into account. Modulators compensated for lower GBW suffer more severely from the nonlinearity of the first op-amp, compared to modulators compensated for higher GBW. Therefore, the op-amp linearity requirement should be satisfied when adopting the GBW compensation technique. This can be achieved by increasing the DC gain, or by reducing the output swing of the op-amp through incorporating the mixed FF/FB architecture.

Chapter 8

Conclusion and Outlook

This work demonstrates the implementation of a high linearity third-order CT low-pass $\Delta\Sigma$ modulator for a high input frequency (>5GHz) RF receiver SoC. Fabricated in a low-cost 0.25µm SiGe BiCMOS process, the prototype modulator achieves a 70dB dynamic range in a 15MHz signal bandwidth. Clocked at 1.92GHz, the modulator achieves 78.1dB SFDR by employing a single-bit internal quantizer which is inherently linear, and thus no digital DAC linearization technique is required. The modulator dissipates 215.9mW and occupies an active area of 0.4mm^2.

Additionally, the ELD compensation technique using a mixed-signal differentiator has been extended to counteract the effect of the finite GBW of the op-amps. A RZ DAC is incorporated to realize a fast compensation path from the quantizer output to the input of the last integrator. After proper tuning of the scaling coefficients, the original NTF of the ideal modulator can be restored.

The final contribution of this thesis involved the analysis on the nonlinear effect of the first op-amp in a single-bit CT $\Delta\Sigma$ modulator with finite GBW compensation. A behavioral op-amp model employing a hyperbolic tangent expression has been created and verified to approximate the op-amp nonlinear characteristics. In analyzing transient simulations of $\Delta\Sigma$ modulators compensated for different GBWs, the influence of the first op-amp nonlinearity has been studied, indicating that more stringent linearity requirements on the first op-amp must be satisfied in the modulator compensated for lower GBW. This issue can be addressed by increasing the op-amp DC gain, or by employing a mixed feed-forward/feedback architecture.

8.1 Future Work

Although the experimental results of the designed $\Delta\Sigma$ modulator meet our design requirements, there still exists areas for continued development. To improve the performance of this work, several issues need to be considered:

- The technique to reduce the clock jitter sensitivity is required for the chosen CT single-bit architecture. One possible solution is to use the non-rectangular, e.g., exponentially decaying, feedback pulses [69]. The clock jitter influence could be alleviated by using a mixed-signal finite impulse response (FIR) filter which smoothes out the feedback waveform by attenuating the high-frequency quantization noise [70] [71].

- Although there is no power consumption limit for the receiver, the power optimization of the designed modulator is another field where further research is required. Methods to minimize the power dissipation should be investigated while maintaining the modulator's performance.

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List of Author Publications

During his work the author has done studies, theoretical analysis, simulations, implementations and measurements on systems and circuits. These are mainly in the field of $\Delta\Sigma$ modulators, but also in analog circuit design and signal processing. A list of therefore resulting publications in leading international conferences and journals, as well as patents, is given below.

- **C. Chu**, J. Wagner, A. Al Marashli, J. Chi, J. Anders, and M. Ortmanns, "A Study on Op-amp Nonlinearity in a Single-bit CT Delta Sigma Modulator Employing GBW Compensation," 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Lisbon, Portugal, Jun 2016.

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