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High Linearity Sigma-Delta-Enhanced SAR ADCs

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Signed: Ahmad AlMarashli

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Abstract

SAR ADCs recorded the highest power efficiency in the last decade, while employing a simple architecture and making a perfect use of the advanced digital capabilities in modern deeply-scaled CMOS technologies. Recently, there is an increased importance of high-resolution high-linearity Nyquist-rate ADCs with multiplexing capabilities, in areas like environmental and medical applications. Simultaneously, high power efficiency and low-area consumption are essential features to enable efficient implementations in battery-powered and/or hand-held devices. The state-of-the-art for high-linearity ADCs is dominated by oversampling ADCs, which do not allow multiplexing. On the other hand, available high-linearity Nyquist-rate ADCs require high-power and large chip area for matching enhancement, linearization and calibration techniques. Additionally, these ADCs prefer older technologies for advantageous analog processing. Also, highly-efficient SAR ADCs currently present limited linearity and resolution. This work aims to introduce novel concepts for SAR ADCs, which enable high-linearity A/D conversion with reliance neither on extensive digital linearization nor on large chip area. Instead, the proposed concept makes use of an intrinsically linear Sigma Delta DAC, to enhance the linearity of the SAR ADC. To implement this proposal, two system architectures are introduced and compared to available solutions in the state-of-the-art. Also, system-level design choices are discussed with pros and cons. A prototype in a 40 nm CMOS technology was implemented and measured to validate the proposed technique. The measured linearity of the prototype competes the state-of-the-art for high-linearity power-efficient Nyquist-rate ADCs, while occupying the smallest active chip area, with good stability over PVT variations. The proposed concept, with silicon-validated performance, advances the state-of-the-art for high-linearity, scaling-friendly, simple and power-efficient Nyquist-rate ADCs.

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List of Abbreviations

AAF	Anti Aliasing Filter
A/D	Analog/Digital Interface
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
BS-switch	Bootstrap switch
CDAC	Capacitive Digital-to-Analog Converter
CDF	Cumulative Distribution Function
CM	Common Mode
CoI	Cascade of Integrators
CSR	Capacitor-Swapping Reset
CT	Continuous Time
D/A	Digital/Analog Interface
DAC	Digital-to-Analog Converter
DFF	D-type Flip-Flop
DT	Discrete Time
DUT	Device Under Test
dB	Decibel
dBc	Decibel to carrier
ENOB	Effective Number Of Bits
FIR	Finite Impulse Response
FOM$_W$	Walden Figure Of Merit

FOM$_S$	Schreier Figure Of Merit
IIR	Infinite Impulse Response
IO	Input-Output
IoT	Internet of Things
I-ΣΔM	Incremental Sigma Delta Modulator
LPF	Low-Pass Filter
LSB	Least Significant Bit
LVDS	Low Voltage Differential Switching
MASH	Multi-stAge noise SHaping
MSB	Most Significant Bit
NS	Noise Shaping
NTF	Noise Transfer Function
OS	Over Sampling
OSR	Over Sampling Ratio
PD	Phase Detector
PDF	Probability Density Function
PSD	Power Spectral Density
PSS	Periodic Steady-State
PVT	Process-Voltage-Temperature
R$_{ON}$	ON resistance
RMS	Root-Mean-Square
S&H	Sample and Hold
SAR	Successive Approximation Register
SC	Switched Capacitor
ΣΔM	Sigma Delta Modulator
SFDR	Spurious Free Dynamic Range

SNDR/SINAD	Signal to Noise and distortion Ratio
SNR	Signal to Noise Ratio
SoA	State-of-the-Art
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
T&H	Track and Hold
THD	Total Harmonic Distortion
TI	Time Interleaving
VCO	Voltage-Controlled Oscillator
$\mathbf{V}_{CM}$	Common Mode Voltage

Chapter 1

Introduction

1.1 ADCs for digital life

Major technology trends currently involve advanced digital processing capabilities to provide novel and improved services for better human life. The current trend list includes Internet-of-things (IoT) and smart home, machine learning and artificial intelligence (AI), autonomous driving/flying, automated or digital-assisted medical care and many more. Despite the diversity of the list items, at least two things are common to all these trends: First, they increasingly demand for complex digital processing. Second, they need to interface with humans or with the surrounding environment, and they increasingly need to read and sense this "analog" environment faster and more accurately.

Recently, the digital capabilities have achieved big improvements, using deeply scaled CMOS technologies for increased speed and decreased area and power consumption. However, the design bottleneck in many applications has moved to the interface that translates the analog signals into the digital domain, which is the analog-to-digital converter (ADC). Unlike digital circuitry, the analog circuits did not similarly benefit from technology scaling, but instead, conventional – analog – ADCs preferred older technologies for higher accuracy. With increased integration complexity, typical applications, potentially battery-powered, require the ADC(s) to quantize several (even tens/hundreds) signals, which puts a stringent requirements on ADC power and area, also, this creates a strong demand for multiplexed use of a single ADC on a group of signal sources, at the same time.

Many applications require high-linearity ADCs, which can detect weak signals in highly noisy environment, like digital lock-in detection or neural recorders. Conventional solutions for high-linearity and high-resolution are dominated by oversampling ADCs, which average the quantized signals and do not allow for multiplexing, also these ADCs are dominated with analog circuitry which is not scaling friendly. Also, high-linearity Nyquist-rate ADCs, which allow for multiplexing, suffer from high power and area consumption; additionally, they require costly techniques with sophisticated post-manufacturing trimming and calibration to achieve high linearity. On the other hand, high-efficiency Nyquist rate ADCs are dominated by successive approximation register (SAR) ADCs. Those, benefit from major digital part to provide a simple and scaling friendly design, which achieved best power efficiency with close to minimum area consumption. Therefore, a great demand and big challenge are present, to research and develop high-resolution high-linearity high-efficiency and scaling-friendly Nyquist rate ADCs.

1.2 ADC concept and characteristics

The ADC is a system/device that transfers analog signals at its input into the digital domain; examples of analog signals could be sound, image or electromagnetic waves. A representation of each of these signals by a voltage or a current signal, is usually present at the ADC input; this signal could be generated by a microphone, a sensor or an antenna. Figure 1.1 shows a basic ADC concept; the analog signal at the input, which is continuous in time and value, is converted into digital streams representing quantized values of the input signal at specific points in time.



Figure 1.1: ADC concept

1.2.1 Sampling

In order to convert the analog signal to the digital domain, a time quantization is required. Therefore, the ADC samples the signal periodically in time. This sampling action takes place either in front of the ADC or internally within the ADC structure. Figure 1.2 presents an example of ideal sampling of an arbitrary signal (in black). The time interval between two consecutive sampling instances is the sampling time, T_S in Fig. 1.2, while the sampling frequency f_S is equal to the inverse of T_S. Assuming the analog input signal to be limited

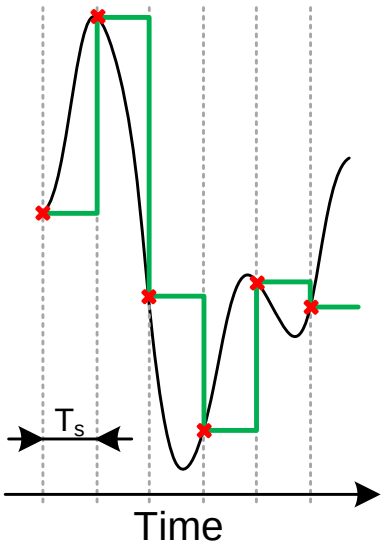


Figure 1.2: Sample and hold example

in frequency up to a frequency f_B, a minimum sampling frequency ($f_{S,min}$) is required, in order to allow the sampled signal to capture all the information in the analog input.

$$f_S \geq f_{S,min} = 2 \cdot f_B \tag{1.1}$$

Sampling the analog signal with a sampling frequency of f_S is equivalent to repeating the analog signal frequency components periodically over a period of f_S, as illustrated in Fig 1.3. Therefore, if the sampling frequency satisfies (1.1), an exact copy of the analog signal can be reconstructed by applying a low pass filter on the sampled signal, as illustrated by an exemplary brickwall filter in Fig. 1.3 (b). On the other hand, when the minimum required sampling frequency ,in (1.1), is not respected, an overlapping in frequency domain will

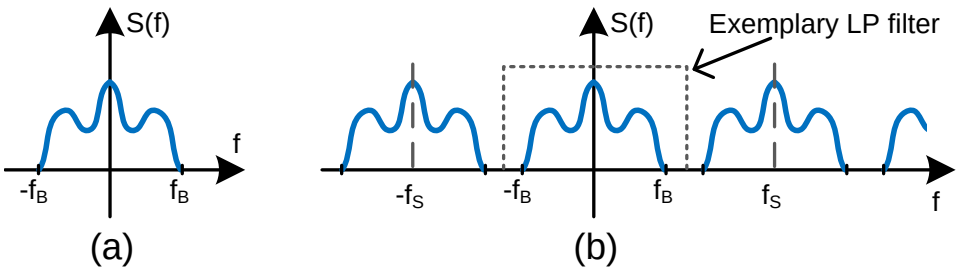


Figure 1.3: Sampling effect in frequency domain. (a) Analog signal. (b) Sampled signal with $f_S > 2 \cdot f_B$

occur between the fundamental signal components around zero Hz and the components at higher bands, which is called aliasing.

1.2.2 Quantization and ADC static features

In addition to sampling, the ADC quantizes the analog signal, which has an unlimited number of levels, into a finite number of levels, which are the quantization levels of the ADC. In Fig. 1.4, the sampled signal is quantized into 8 levels, and 3-bit digital outputs are respectively generated. Unlike the sampling process, which is fully invertible, the quantization process is not invertible. Because, based on the finite quantization bits/levels, a quantization error is

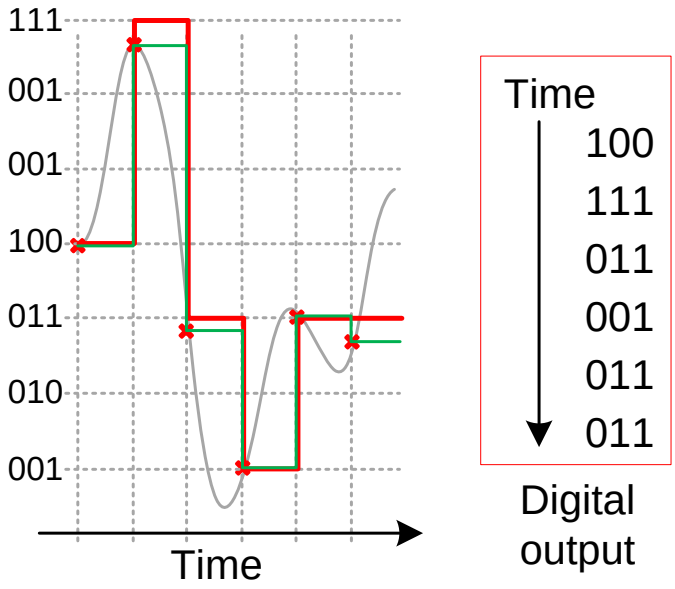


Figure 1.4: 3-bit quantization example

added to the input signal, and different analog values within one quantization interval will be represented by equal values after quantization. The quantization error is defined as the difference between sampled signal and its quantized form (the output of the quantization process).

1.2.2.1 ADC resolution

The accuracy of the ADC is represented by its resolution, which is determined by the number of quantization levels. The ADC nominal resolution is defined as the bit-width used to represent the digital output or equivalently the quantization levels. Also, the quantization step Δ, which is the distance between two neighboring quantization levels, is related to the ADC full scale voltage V_{FS} and the ADC resolution b as in (1.2):

$$\Delta = \frac{V_{FS}}{2^b - 1} \tag{1.2}$$

1.2.2.2 ADC transfer characteristics

The static (DC) specifications of the ADC are represented by its transfer characteristic curve. Figure 1.5 (a) shows an ideal 3-bit transfer characteristic, and the related quantization error (b). When the ADC input is limited below $V_{FS} - \Delta$, the ideal quantization error is limited within $\pm\Delta/2$. The transfer characteristics can also be represented by the line connecting the end points of the characteristic curve steps or the mid-step points (or code centers) as included in Fig. 1.5 (a). In this case, this line has a zero offset (crosses the (0,'000') point) and a slope (gain) of '1000'/V_{FS}.

1.2.2.3 Static nonidealities

Gain and offset errors: The gain error is represented on the ADC transfer curve as a slope change of the mid-step line compared to the ideal slope, while the offset error is a constant shift of the whole curve. Figure 1.6 shows two examples of gain and offset errors in (a) and (b) respectively. Under gain and offset errors, the ADC transfer curve is still represented by a straight line (mid-step line), therefore a linear input-output relation is maintained. This together

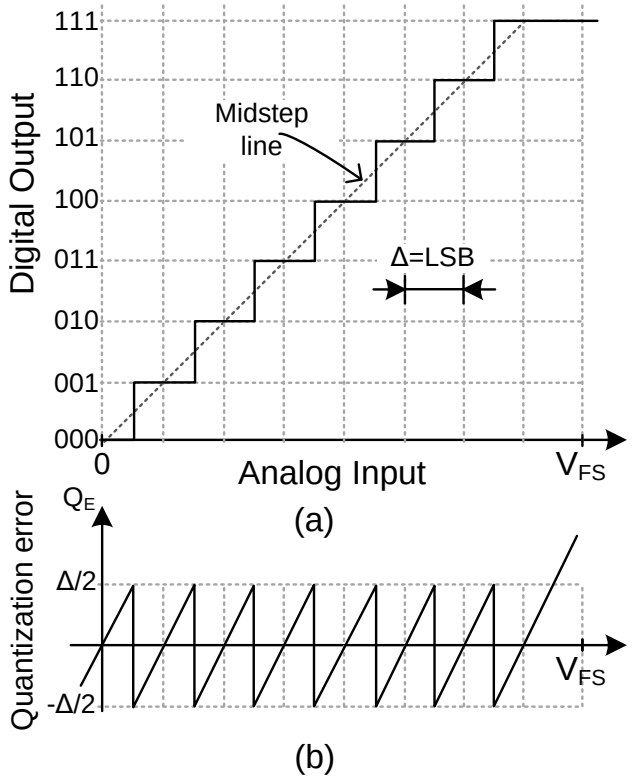


Figure 1.5: Ideal 3-bit transfer characteristics (a), and the respective quantization error curve (b).

with the fact that gain and offset errors are usually easy to correct for, makes the gain and offset errors, for many applications, of no major importance. However, big gain and offset errors can cause limitations on the input range. In the case of the example in Fig. 1.6(a); the input range is limited approximately between [0,5/8·V_{FS}], and between [2/8·V_{FS},V_{FS}] in the case of Fig. 1.6(b).

Static non-linearities: The main reason for a nonlinear ADC transfer curve is having irregular steps between the quantization levels, which is caused by a non-ideal matching in the ADC circuit implementation. The most common measures for static non-linearity are differential non-linearity (DNL) and integral non-linearity (INL). **DNL** is the deviation of the step size (in the real transfer curve) of its ideal size Δ [1]. For a b-bit ADC, assuming $\Delta(k)$ ($k = 1 \ldots 2^b - 1$) to be the step sizes of the ADC transfer curve, the DNL can then be calculated as in (1.3) [1].

$$DNL(k) = \frac{\Delta(k) - \Delta}{\Delta} : k = 1 \ldots 2^b - 1. \tag{1.3}$$

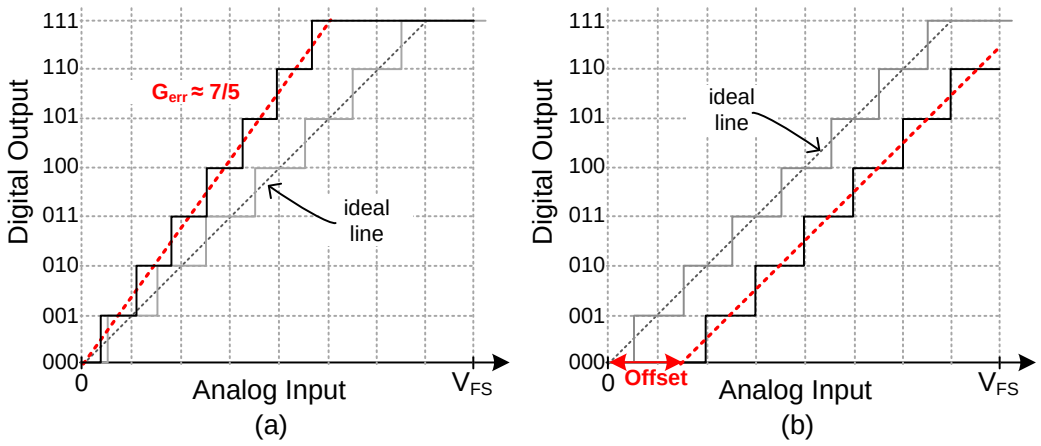


Figure 1.6: 3-bit ADC transfer characteristics with: (a) gain error, (b) offset error.

INL is the real transfer curve deviation, at each quantization level, of the ideal curve. INL is calculated as a running sum of the DNL as in (1.4) [1]. INL is usually calculated after correction for gain error (sometimes also for offset error), which is not relevant for input harmonic distortion.

$$INL(k) = \sum_{i=1}^{k} DNL(i) : k = 1 \ldots 2^b - 1. \tag{1.4}$$

Figure 1.7 shows a non-linear ADC characteristic curve with an example estimation for DNL and INL.

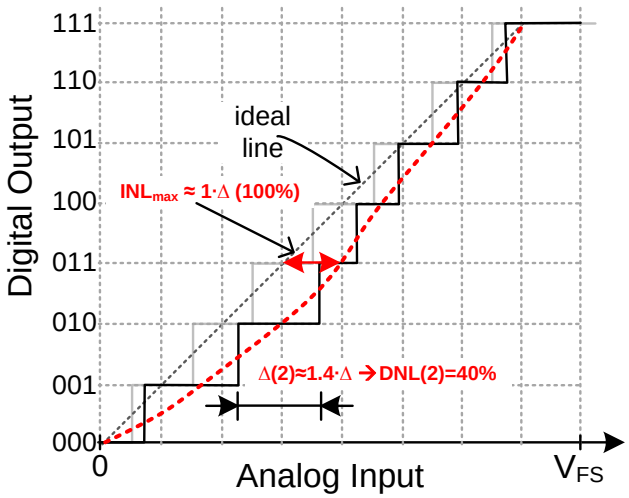


Figure 1.7: Non-ideal 3-bit ADC characteristic curve, with example DNL and INL estimations.

1.2.3 ADC dynamic features

Examining the ADC features on static or low speed signals does not provide sufficient evaluation for most applications. Therefore, a dynamic or AC evaluation of the ADC is usually required to include the frequency response and speed of the ADC components. In the following, the most relevant dynamic features, addressed in this work, are listed and briefly discussed.

Quantization noise model: The A/D conversion process can be modeled as an addition of the quantization error (equivalently called quantization noise). For an ideal ADC with a rapidly changing input signal, the quantization noise can be approximated as a white noise process [2, 3]. Based on this approximation, the quantization noise process is uncorrelated and distributes uniformly over the range $[-\Delta/2, \Delta/2]$, also the power spectral density of this process is flat over the input frequencies $[-f_S/2, f_S/2]$. The probability density function (pdf) of the quantization noise equals to $1/\Delta$ within $[-\Delta/2, \Delta/2]$ and zero elsewhere. Thereby, the mean square value of the quantization noise (total power) can be calculated as (1.5). Also, based on the ADC sampling frequency (f_S), the power spectral density is given by (1.6).

$$\overline{Q_E^2} = \int_{-\Delta/2}^{\Delta/2} Q_E^2 \cdot dQ_E = \frac{\Delta^2}{12}. \tag{1.5}$$

$$S_{Q_E}(f) = \frac{\Delta^2}{12}\frac{1}{f_S}, \quad f \in [-f_S/2\ ,\ f_S/2]. \tag{1.6}$$

Signal to quantization noise ratio (SQNR): The ideal value of SQNR can be calculated based on ADC testing with a full-scale sinewave input. Assuming an ideal b-bit ADC, the full scale approximately equals to $[2^b \cdot \Delta]$. Therefore, a full-scale sinewave has an amplitude of $[2^b \cdot \Delta/2]$ and a root-mean-square (rms) value of $[2^b * \Delta/(2\sqrt{2})]$. The SQNR value in decibels (dB) is calculated as in (1.7,1.8) [4].

$$SQNR = 20\,log_{10}\frac{rms\ value\ of\ input}{rms\ value\ of\ Q_E} = 20\,log_{10}\frac{2^b * \Delta/(2\sqrt{2})}{\Delta/\sqrt{12}} \tag{1.7}$$

$$SQNR = 6.02 \cdot b + 1.76\ (dB) \tag{1.8}$$

Signal to noise ratio (SNR): The SNR is the ratio between the signal power and the total noise at the output of the ADC, which includes both the quantization noise and the circuit noise generated within the ADC (e.g. thermal and flicker noise). The noise power is integrated on the complete Nyquist bandwidth of the ADC.

Dynamic range (DR): DR is the amplitude range between the ADC full scale and the minimum detectable signal (at SNR = 0 dB). This is usually used for ADCs that do not reach their maximum SNR with full-scale input [1].

Signal to noise and distortion ratio (SNDR or SINAD): The SNDR measure includes all non-idealities in the ADC implementation. It is estimated by integrating the complete ADC output power spectrum over the whole Nyquist bandwidth. Therefore, not only noise power is included ($P_{Q_E} + P_n$), but also all distortions (P_{dist}) due to static nonlinearities and also dynamic performance drop at high speed operation.

$$SNDR = 10\,log_{10}\frac{P_{sig}}{P_{Q_E} + P_n + P_{dist}} \tag{1.9}$$

Effective number of bits (ENOB): The ENOB measure represents the effective resolution of the ADC, which includes the effect of ADC implementation non-idealities and performance degradation over input frequencies. The ENOB is calculated based on the SNDR value as in (1.10), in a similar manner to (1.8), which relates the nominal resolution b with the ideal SQNR value.

$$ENOB = \frac{SNDR\,(dB) - 1.76}{6.02} \tag{1.10}$$

Total harmonic distortion (THD): In a single tone test (sinewave input to the ADC), the THD value in dBc (decibels below carrier) is the ratio between the rms value of the fundamental signal to the rms value of all harmonics components including aliased terms. Normally, only the first five (or sometimes ten) harmonics are significant for THD calculation.

Spurious free dynamic range (SFDR) is an important measure of the dynamic linearity of the ADC, especially for communication applications. The SFDR is the ratio of the rms value of the fundamental signal to the rms

value of the peak spurious spectral component measured over the bandwidth of interest.

Aperture jitter refers to the sampling clock jitter at the input of the ADC. Considering the same single tone test as before, the sampling clock jitter leads to a variation of the sampling time instance, which can cause a distortion on the sampled sinewave and limit the measured SNDR. For a full scale signal at frequency f, the signal to aperture-jitter noise ratio for a clock time jitter of t_j is given by SNR_{ap} in (1.11) [4].

$$SNR_{ap} = 20\, log_{10} \frac{1}{2\pi f t_j} \tag{1.11}$$

1.3 ADC types and input-output relations

The ADCs can be classified in different types based on their conversion algorithms. This classification may focus on different features or specifications in different application areas. However, ADCs are generally distributed in two main types, which are Nyquist-rate and oversampling (OS) ADCs. In the following, the main features and differences between the two types are discussed. Then the noise shaping ADCs, as a special kind of the OS ADCs, are also addressed. Finally, the relationship between ADC input and output is discussed with focus on multiplexing capability.

1.3.1 Nyquist ADCs – general concept

The main feature that identifies a Nyquist ADC is that the input signal bandwidth is close or identical to the sampling Nyquist-bandwidth of $f_S/2$, where f_S is the sampling frequency. Also, the Nyquist ADC usually process individual input samples independently, therefore, a Nyquist ADC does not introduce inter-symbol memory.

Figure 1.8 includes a block diagram of the general chain for a Nyquist A/D conversion. In order to prevent aliasing from higher frequencies (above $f_S/2$), due to the sampling action (as discussed in chapter 1.2.1), an anti-aliasing filter (AAF) is required. Also, the existence of signal components close to

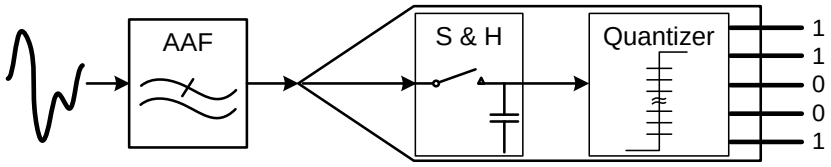


Figure 1.8: General block diagram of a Nyquist ADC.

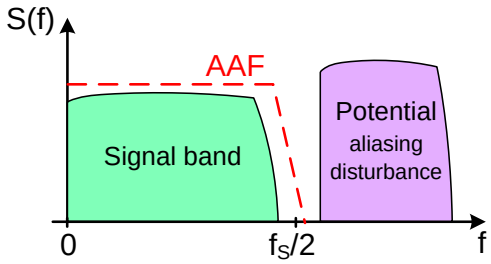


Figure 1.9: Anti-aliasing filter requirement in Nyquist ADCs.

the Nyquist-bandwidth, puts strict requirements on the AAF, including for example a tight transition band as presented in Fig. 1.9.

A sample-and-hold (S&H) block is usually the first block within the Nyquist ADC. This block samples the input signal once per ADC conversion cycle, therefore, the sampling rate/frequency equals the ADC conversion rate or the digital-output rate. After a complete conversion of the sampled input to the digital domain, a new sampling action is triggered after resetting the ADC to the same initial states, which avoids memory effect in this ADC type.

1.3.2 Oversampling ADCs

Unlike Nyquist ADCs, the signal bandwidth in OS ADCs occupies only small fraction of the Nyquist frequency range ($f_B << f_S/2$), which widely relaxes the AAF requirements, as sketched in Fig. 1.10. The oversampling ratio (OSR) is defined as the ratio between the sampling frequency and double the signal bandwidth (the minimum required sampling frequency), $OSR = f_S/(2 \cdot f_B)$.

The major advantage for OS ADCs is the reduction of ADC quantization noise in the signal bandwidth. Based on (1.6), the quantization noise power spectral density is inversely proportional to f_S, therefore, the integrated

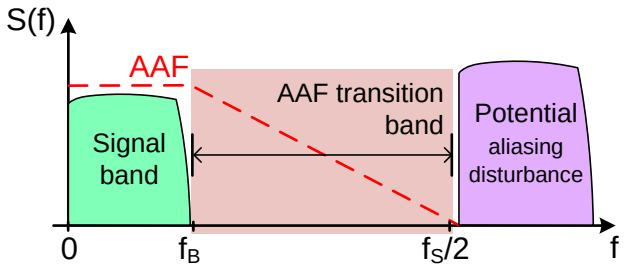


Figure 1.10: Anti-aliasing filter requirement in OS ADCs.

noise power within the signal band is a factor OSR lower than the equivalent Nyquist-rate noise power (integrated up to f_S), as presented in Fig. 1.11. Also, this equivalently applies for the ADC thermal noise (especially sampling noise), which is also distributed over the full f_S frequency band, therefore, the SNR is improved by factor OSR as in (1.12).

$$SNR_{OS} = 6.02 \cdot b + 10\, log_{10}\, OSR + 1.76\ (dB) \tag{1.12}$$

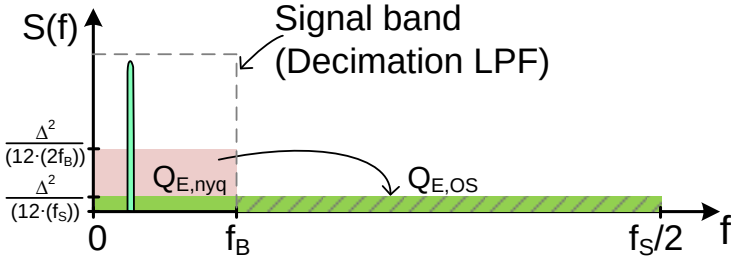


Figure 1.11: The quantization noise power over frequency in OS ADCs.

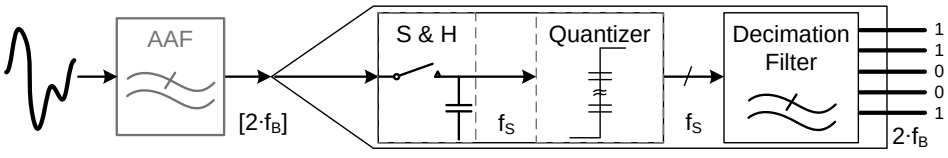


Figure 1.12: General block diagram of an oversampling ADC.

Figure 1.12 shows a block diagram of an OS ADC. The main blocks in the OS architecture seem similar to the Nyquist ADCs, however, their specifications and operation frequencies can be very much different. Both the S&H and

quantizer blocks operate at f_S, which is a factor OSR higher than the minimum required sampling rate. Also, these two blocks can be mixed in one block, which does not employ an explicit sampler at its front-end, this is usually the case for continuous-time ΣΔ ADCs (CT-ΣΔ). Finally, the major architectural difference for an OS ADC is the required digital decimation filter after the quantizer. This filter performs two functionalities; a removal or attenuation of ADC noise beyond the signal band, and a down-sampling of the high speed quantizer output at f_S into $2 \cdot f_B$.

1.3.3 Noise shaping ADCs

The noise-shaping (NS) ADC is a special case of an OS ADC, which not only makes use of the reduced in-band noise by OS, but also shapes the quantization noise and concentrates it out of the signal frequency band, to further reduce the in-band noise, as illustrated in Fig. 1.13. By doing that, a very small fraction of the internal quantization noise is seen in the signal band, which allows the use of a very coarse quantizer (even a 1-bit) to achieve high resolution.

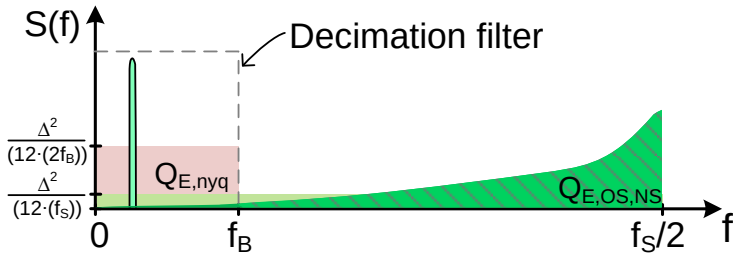


Figure 1.13: The quantization noise power over frequency in NS ADCs.

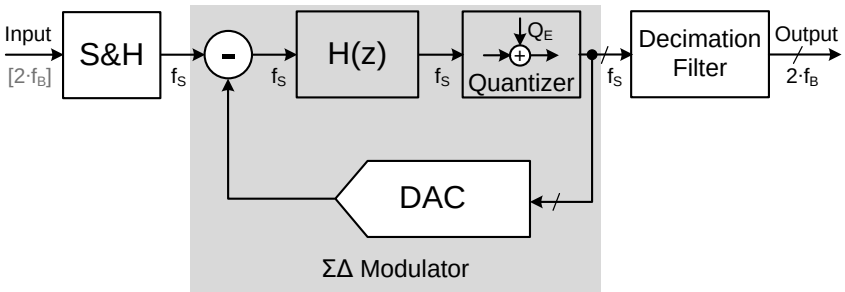


Figure 1.14: Block diagram of a DT ΣΔ ADC.

The most common examples of NS ADCs are ΣΔ ADCs. Figure 1.14 shows an exemplary implementation of a discrete-time (DT) ΣΔ ADC [2]. Unlike the OS ADC diagram in Fig. 1.12, here, the coarse quantizer (internal ADC) is placed in the ΣΔ modulator (ΣΔM) loop, to allow one to shape its quantization noise Q_E out of the signal band. The DAC uses a similar resolution to the quantizer to form the feedback path from the digital output to the analog input of the modulator. Commonly, for a low-pass implementation of the ΣΔM, the filter H(z) features a low pass characteristic, for example a cascade of integrators (COI). Thereby, the ΣΔM features a low-pass signal transfer function (STF) for the signal path from modulator input to the output. Also, the ΣΔM introduces a high-pass noise transfer function (NTF) for the quantization noise Q_E path to the output. The order of H(z) defines the modulator order and also the NTF order, which is equivalent to the NS order, therefore, it determines the overall effective resolution. Thereby, the higher the modulator order, the better the NS is and the higher the effective resolution. Equation (1.13) shows the improvement in SNR as a function of OSR for a first order modulator [2].

$$SNR_{sdm1} \approx 10\,log_{10}\,OSR^3\ (dB) \tag{1.13}$$

The NS ADC architecture allows for a very high-resolution ADC implementation without dependence on a highly linear quantizer. This diminishes the effect of quantizer static nonlinearity, which relies on analog element matching. Therefore, NS ADC concept breaks the conventional dependency of high-resolution ADCs on highly matched element arrays. This is achieved at the cost of OS, higher speed operation and additional components as the loop filter and the digital decimation filtering. Moreover, the NS process requires handling a complete input signal, instead of quantizing individual input samples as the Nyquist ADC.

1.3.4 ADC in-out relation and multiplexing

An important feature of the ADC architecture is the multiplexing capability, which may be a determining factor to select the suitable ADC for an intended application. Figure 1.15 shows a multiplexing concept of an ADC over N chan-

nels. The ADC is operated at N times faster rate than the individual channels require, therefore, in a time frame equal to $1/f_{ch}$ the ADC converts N samples in total, and during this time, each input channel is visited once and each output channel receives one output, at its required sample rate.

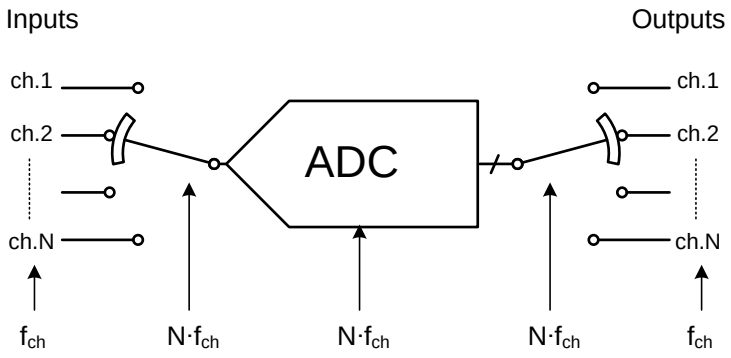


Figure 1.15: Multiplexing a single ADC over N channels.

In order to allow this multiplexing operation, the ADC has to provide a one-to-one relation between input and output samples. This feature is guaranteed in a Nyquist ADC, which converts individual input samples and resets to the same initial conditions, before each conversion.

In OS ADCs without NS, the multiplexing capability depends on the ADC implementation. The OS concept does not – by default – prevent multiplexing, as each multiplexed channel can be oversampled with a factor OSR without introducing inter-channel memory. However, a free running decimation filter, which conventionally uses an infinite-impulse-response (IIR) architecture, performs an averaging operation on the whole quantizer output stream. Consequently, the filter/ADC output is dependent on previous inputs and an inter-channel memory is introduced. Therefore, a sample-sample relation is not guaranteed between input and output, which prevents correct ADC multiplexing. However, if the decimation filter is periodically reset at the ADC conversion rate (which can degrade the filter efficiency), or equivalently if an finite-impulse-response (FIR) filter architecture is used (with order smaller than ADC OSR), a memory free operation can be achieved to enable ADC multiplexing. On the other hand, in NS ADCs, the quantization noise shaping operation depends on a steady-state NTF, therefore, a reset action is not

possible. The NS ADC has an implicit memory, as it averages the input signal and does not allow multiplexing operation.

1.4 ADC performance measures

The ADC evaluation is an important aspect to conduct efficient comparison between various ADC types and architectures, and to achieve good balance between cost and performance. In the following, the common measures for ADC evaluation are discussed, in addition to the mostly used figure of merits (FOMs). Also, few other ADC features are addressed, which – despite their importance – are usually not included in common FOMs.

1.4.1 Performance measures and FOMs

Three features are commonly considered for a general ADC evaluation, those are ADC speed, resolution and power.

ADC speed is represented by the ADC sampling frequency f_S for a Nyquist ADC, while for an OS ADC the Nyquist frequency is considered which is f_S/OSR. The ADC speed is sometimes represented by the input bandwidth, for example when the ADC is used in a sub-sampling mode, extending its bandwidth beyond f_S.

ADC resolution is reported by ENOB or equivalently by SNDR as an effective resolution, since the nominal resolution does not provide fair evaluation of the performance limitation due to ADC implementation. Also, the SNDR (or ENOB) has to be reported over the whole signal bandwidth, as the performance typically drops gradually with increased input frequencies (specially for Nyquist ADCs).

ADC power is the total power consumed by the ADC statically and dynamically. For ADCs, which features major dynamic circuit parts, the power can also be reported over different sampling frequencies, which presents the trade-off between power and speed. In different application areas and depending on the ADC architectures, special blocks are usually excluded or additional supporting blocks are added to the ADC power consumption. Typical examples are $\Sigma\Delta$ ADCs excluding the decimation filter power, or SAR ADCs excluding

the power consumption of the – usually external – reference generator and/or input buffer.

Walden FOM (FOM_W) combines the three above mentioned measures, to present the trade-off between power (P) and speed. This FOM provides good evaluation of power efficiency for moderate to low resolution ADCs, where the resolution is usually not thermal noise limited especially for high speed ADCs. $\mathrm{FOM_W}$ (in J/conversion-step) is given by (1.14), and a lower $\mathrm{FOM_W}$ value indicates a better power efficiency.

$$FOM_W = \frac{P}{2^{ENOB} \cdot f_S} \quad (J/conv. - stp) \tag{1.14}$$

Schreier FOM (FOM_S) is usually used for high-resolution ADCs. It provides similar evaluation as $\mathrm{FOM_W}$, however, it signifies the effective resolution, compared to P and f_S, since, for noise-limited high resolution ADCs, an additional resolution bit is not obtained by factor x2 but x4 more power. The general form of $\mathrm{FOM_S}$ (in dB) is given in (1.15), where f_B is the input signal bandwidth. Some ADC publications replace SNDR by DR in (1.15), which provides a noise-based evaluation excluding the dynamic distortion.

$$FOM_S = SNDR + 10 \cdot log_{10}[\frac{f_B}{P}] \quad (dB) \tag{1.15}$$

1.4.2 Additional measures

In order to focus on high resolution low energy ADCs in a SoA comparison, the energy plot ($E = P/f_S$) over SNDR is often used [5]. Moreover, there are additional measures that are less addressed in SoA FOM comparison, although, they can be of a major importance for specific applications. For example the **ADC chip area**, as an essential aspect for production cost and efficient design integration. Also, the ADC **technology node** is an important feature; since the digital post-processing, which mostly uses the same node as the ADC, would benefit from recent technologies, it is highly desired to have the ADC implemented in a recent technology and to have a scaling-friendly implementation to ease the migration into new technologies.

1.5 Thesis contribution and contents

In order to fill the SoA gap for high linearity high efficiency Nyquist-rate ADCs, this work presents a design study and implementation with a prototype validation of a novel architecture for high-linearity Nyquist-rate SAR ADC. The design employs a major digital part and benefits from incremental $\Sigma\Delta$ DAC and from advanced technology. For concept validation, a prototype is implemented in a 40 nm CMOS technology. The prototype measures an unprecedented linearity for Nyquist SAR ADCs in SoA.

The thesis is organized as follows: Chapter 2 presents the current ADC trends in SoA, then it dives into the available Nyquist ADC structures with special focus on SAR ADCs and their potential limitations towards high resolution implementations. Chapter 3 introduces the first proposal for high linearity SAR, which employs an incremental $\Sigma\Delta$ DAC. The system design choices and implementation details are discussed and followed by a design evaluation for this approach. The second proposal is presented in chapter 4, the concept and architecture are discussed and compared to the previous proposal. In chapter 5, a SAR ADC tool-set for high linearity is developed, including techniques for calibration and redundancy within the proposed architecture. The circuit implementation details for the complete SAR ADC are presented in chapter 6. The final prototype implementation, fabrication and measurements are discussed in chapter 7, in addition to a comparison to the latest SoA publications. The thesis objective and results are summarized and concluded in chapter 8.

Chapter 2

ADCs Trends and State of the Art SAR and Nyquist rate ADCs for high resolution

In this chapter, the current SoA ADC trends are presented. Then, SoA Nyquist ADCs are discussed with few details about the available architectures, while the main intention is focused on candidates for high linearity conversion. SAR ADCs, as the best candidates for power efficiency, are addressed in more details; their limitations and challenges for a high linearity are also discussed.

2.1 ADC trends and common comparison plots

2.1.1 General trends in SoA of ADCs

The most common ADC comparison includes FOM_W or FOM_S plots over speed, as shown in Figures 2.1 and 2.2 respectively, which include SoA ADC publications from the ADC survey in [5]. To present the time trends, Figures 2.1 and 2.2 include the publication years. In Fig. 2.1, the general trend is to reduce FOM_W toward the current limit at 1 fJ/conv.-step at low frequencies, while this limit linearly increases with frequency for high speed ADCs (above 1 GS/s). One also notices that the trend line moved down approximately by factor 10 over the last ten years, also the increase at high frequencies shifted by a factor 10 in frequency with latest ADC publications. Similar facts can be seen in Fig. 2.2 with FOM_S, as only ADCs from the latest seven years are located within the last 10 dB range of the current trend.

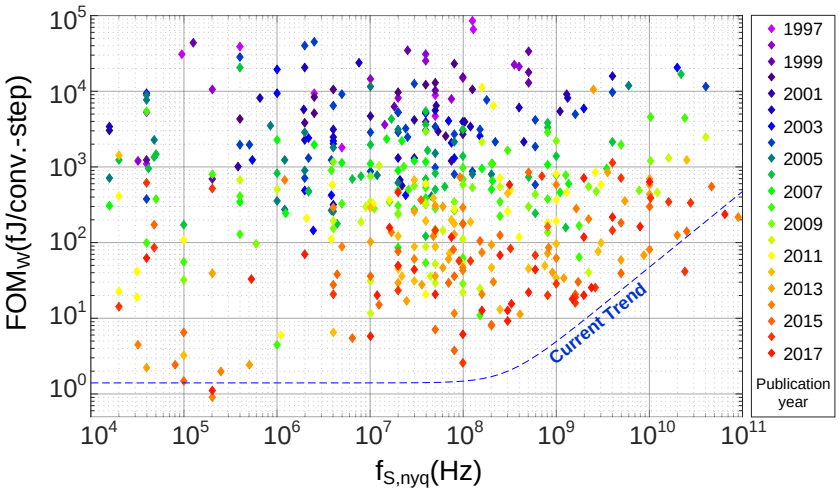


Figure 2.1: ADC comparison of $\mathrm{FOM_W}$ over speed and publication year [5].

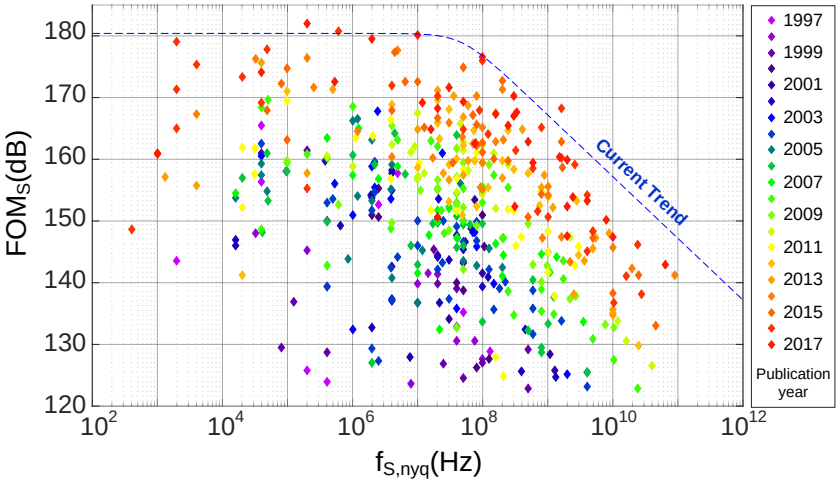


Figure 2.2: ADC comparison of $\mathrm{FOM_S}$ over speed and publication year [5].

Although, the two FOM plots provide an evaluation for power efficiency over speed, they lack the information required for effective comparison at high resolutions, since the power efficiency is further limited there. This information can be better explored in the energy plot over SNDR in Fig. 2.3. The ADCs generally reach the high efficiency trend, shown by the two constant FOM lines, around moderate resolutions (SNDR $\approx$ [50-70] dB), while this becomes very challenging at high resolutions (similarly at very low resolutions).

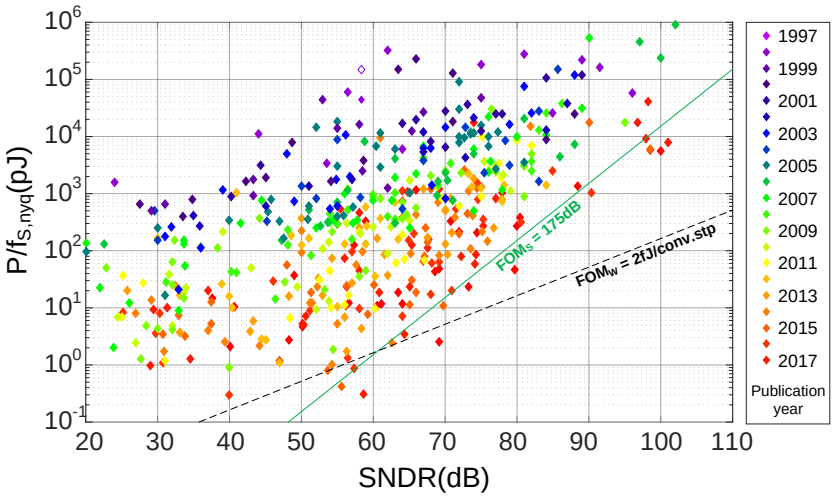


Figure 2.3: ADC energy comparison over SNDR and publication year [5].

ADC trends over Technologies: As discussed in 1.4.1, the used technology node in the ADC is an important feature and an implementation using latest (scaled) technologies is very much desired. Figure 2.4 shows also the energy plot over SNDR, but with ADCs classified for technology node size. Thereby, the major benefit of modern deeply scaled technologies is seen for moderate to low resolution, which is primarily related to the speed advantage with recent technologies. On the other hand, the high resolution region does not present similar advantage, and it is generally dominated by older technol-

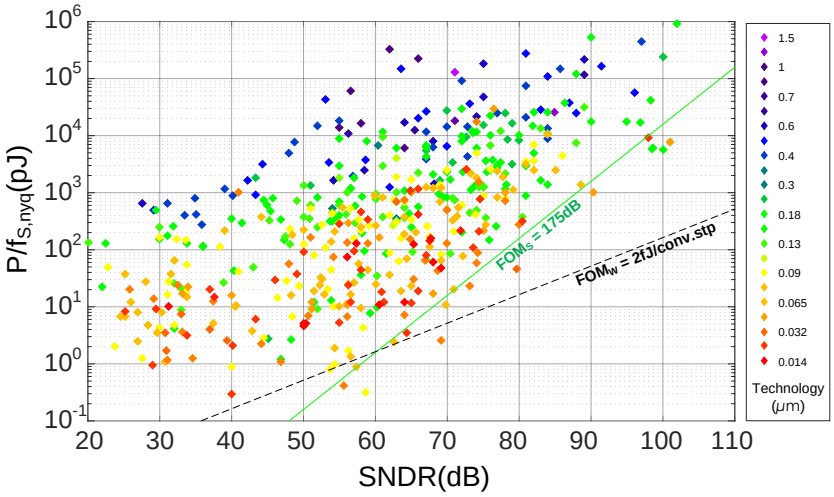


Figure 2.4: ADC energy comparison over SNDR and technology node [5].

ogy nodes, mainly, due to better analog capabilities at higher power supplies and wider input ranges.

2.1.2 ADC trends for high resolution

This work mainly focuses on the implementation of high-efficiency high-resolution ADCs for multiplexed applications. Therefor, further investigations are made on SoA ADC performance in the high-resolution range. Figure 2.5 includes –similar to Fig 2.4– the energy plot, but it identifies the ADC types as OS and Nyquist ADCs, thereby, the following remarks can be pointed out:

- The SoA high-resolution ADCs (SNDR > 75 dB) region is mainly dominated by OS ADCs.
- The efficiency of Nyquist ADCs drops of the optimum FOM lines; and the higher the effective resolution, the farther the drop is.
- The high-resolution Nyquist ADCs are almost exclusively developed with old technology nodes, which makes them less desired for integration in recent complex applications.

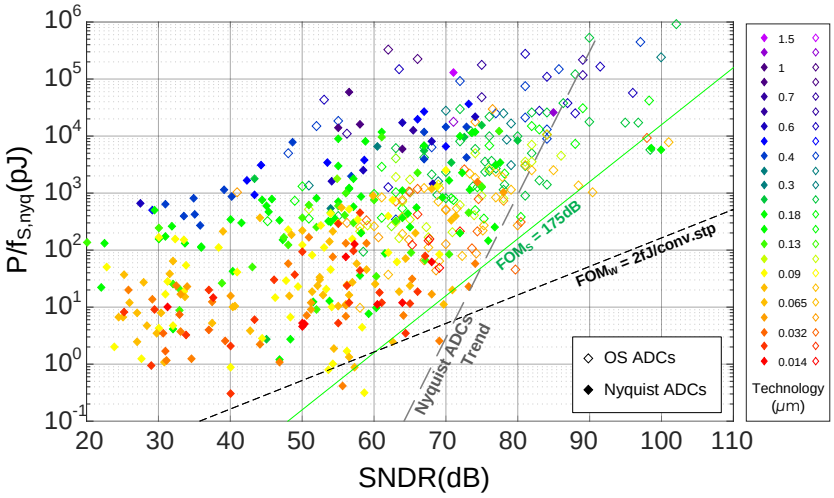


Figure 2.5: SoA energy plot for different ADC types.

As discussed in section 1.3.4, OS ADCs generally do not allow efficient multiplexing, therefore, Nyquist ADCs are required for a high-resolution multiplexed A/D interfaces. And specially by considering the current SoA, high motivation arises for the development of power and area efficient high-resolution

and linearity ADCs, which feature scaling-friendly architectures and benefit from recent technology nodes, potentially by employing major digital capabilities.

2.2 Nyquist ADCs - quantization concept

The Nyquist ADC processes individual input samples captured by a S&H block, which is introduced directly at the analog input, as shown in Fig. 1.8. After sampling, the quantization process takes place, which is equivalent to selecting the ADC quantization level that best matches the fixed input sample. Therefore, every Nyquist ADC implementation involves a circuitry for quantization levels generation. For that, the ADC usually employs an array (or arrays) of analog elements, which are combined in different ways, based on the ADC algorithm, to generate a proper analog scaling for the quantization levels. This analog scaling is done in voltage, current, charge or time domain. Thereby, a major source of non-idealities in Nyquist ADCs is the non-ideal scales of the analog elements after manufacturing, which is referred to as element mismatch. The effect of element mismatch and how it affects the ADC performance, strongly depend on the used algorithm and the ADC architecture.

2.3 Architectural overview

2.3.1 Flash ADC

Flash ADCs are the fastest ADCs, because the quantization operation is performed in one time step (one comparator decision time). They are also called parallel ADCs, because they rely on parallel decisions from many comparators. Despite the speed advantage of the flash ADC structure, the exponential growth of the implementation hardware limits flash ADC implementations to a maximum nominal resolution around 8 bits.

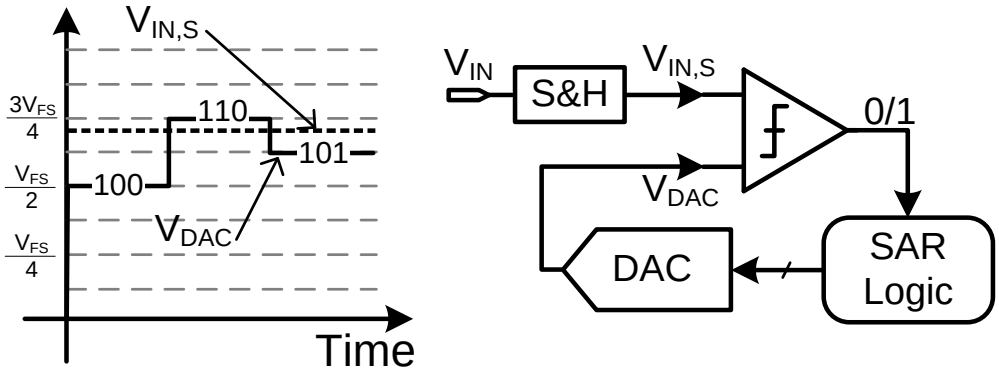


Figure 2.6: SAR ADC basics.

2.3.2 Successive approximation ADC

SAR ADCs perform A/D conversion through the binary search algorithm, as indicated in Fig. 2.6. The conversion algorithm simplifies the required circuit complexity; it employs only one comparator with a DAC in the feedback. Thereby, a relaxed circuitry is achieved at the cost of extended operation time, since a complete conversion requires a series of n comparator decisions, which results generally in a speed limitation in SAR ADCs. On the other hand, the SAR ADC can achieve resolutions much higher than flash ADCs, however, due to limitations in the DAC implementations, it is very challenging to implement a SAR ADC with very high resolutions (above 14 bit), as detailed in section 2.6.

2.3.3 Time-interleaved ADCs

Time-interleaved (TI) ADC architecture increases the ADC conversion rate by using multiple of identical ADCs in a parallel fashion, as shown in Fig. 2.7. TI ADCs allow to achieve much faster conversion rates than those allowed by the individual ADC conversion time, therefore, they present the fastest ADC architecture. However, non-idealities due to mismatch between the internal ADCs and a non-ideal clock generation, limit TI ADC applications for moderate- to low-resolution conversion.

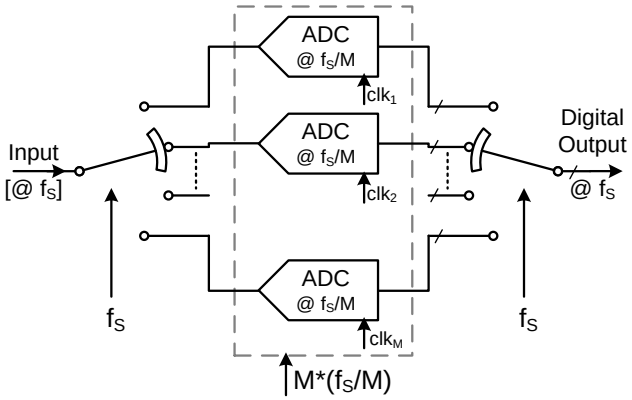


Figure 2.7: Time-interleaved ADC concept.

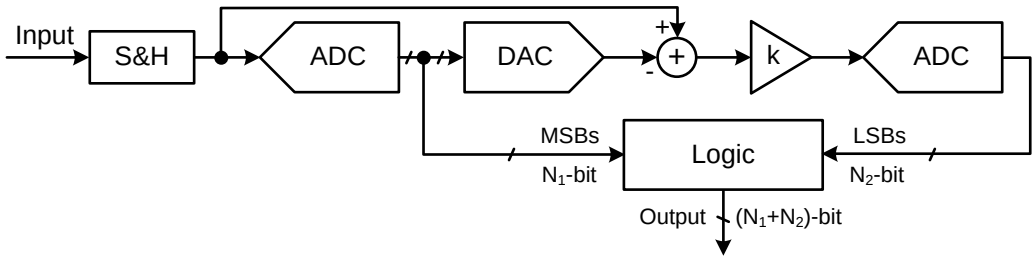


Figure 2.8: Two-step sub-ranging ADC example.

2.3.4 Sub-ranging and pipelined ADC

In order to allow higher resolution than allowed by an individual ADC, or to have a better speed-resolution trade-off, a sub-ranging or two step ADC is used [1]. Sub-ranging ADC combines two or more sub-ADCs in a serial fashion; the later ADC converts a scaled-up copy of the residual error of the previous ADC, as shown in the example of Fig. 2.8. Pipelined ADCs employ the sub-ranging concept with additional S&H at the input of each sub-ADC, to enable higher conversion rates at the cost of delayed ADC outputs. In SoA publications, both architectures are recently more often referred to as pipelined ADCs.

2.3.5 Other architectures

The architectures discussed above have recently dominated SoA publication, because they filled the trend edges for high power efficiency, high-speed, and

high-resolution Nyquist ADCs. However, there are many more ADC architectures, which are less used in SoA, either due to degraded design efficiency, and/or because they provide application-specific features like elimination of AAF, intrinsic monotonicity, miniaturized size and fully digital structures. Examples of those include the following:

- **Folding ADCs:** employ sub-ranging after folding the analog input into two or more smaler ranges to be converted by a sub-ADC.
- **Counting and integrating ADCs:** including for example charge rundown, ramp-up and tracking ADC [4]. Those, usually provide high-resolution conversion at very low conversion rates.
- ADCs based on **voltage to frequency converters** and **time to digital converters (TDC)**, which are attracting more attention due to mostly digital structures.

2.3.6 Performance overview

In order to explore the advantages of each converter architecture and its application ranges, SoA Nyquist ADC FOMs are compared for different architectures. Figure 2.9 (a,b) shows plots of $\mathrm{FOM_W}$ and energy, while marking the four discussed architectures.

- **Flash ADCs:** are almost exclusively designed for very high speed and very low resolution.
- **TI ADCs:** allow one to go for a higher speed, therefore they dominantly shape the high speed high efficiency trend, in Fig. 2.9(b). Moreover, by TI other architectures than the flash ADC, they also move to the moderate resolution range.
- **Pipelined ADCs:** mainly dominate the high-resolution range, and combined with TI they go into high speed range.
- **SAR ADCs:** provide the best power efficiency, especially for moderate resolution and low to moderate speed. Also, while moving to higher resolution, a rapid drop in power efficiency is generally reported. However, due to the superior power efficiency and simple design of SAR ADCs,

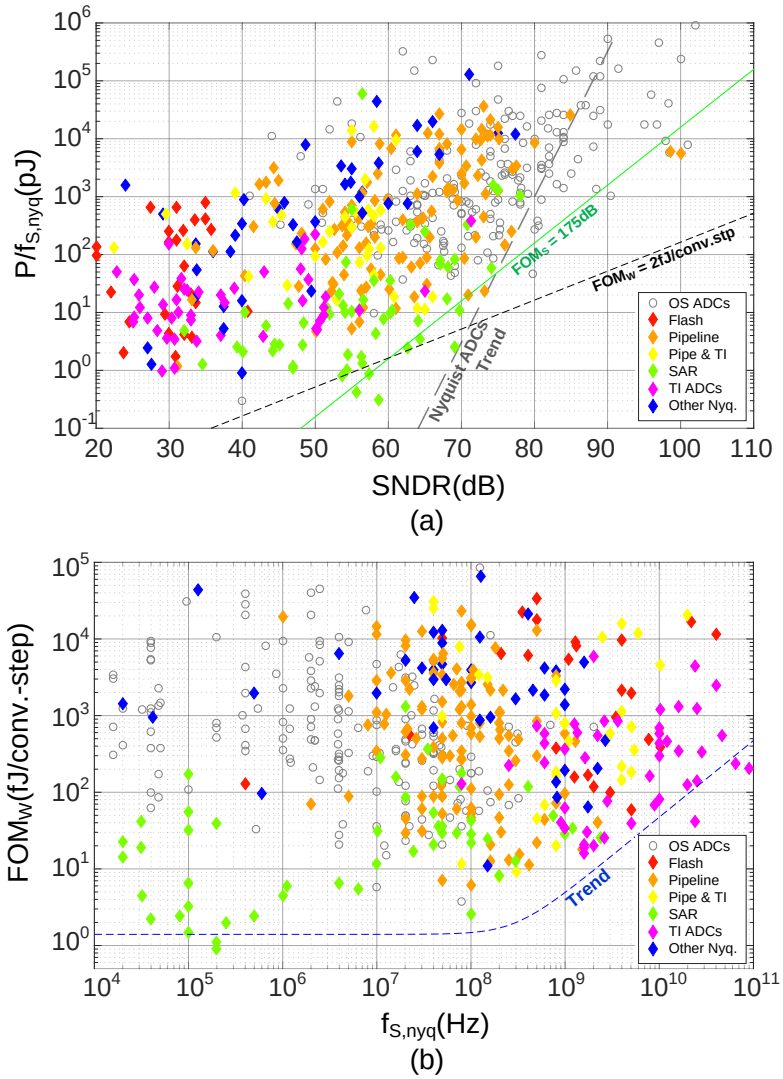


Figure 2.9: SoA energy plot (a), FOM_W plot (b), for different Nyquist ADC architectures (1997 - 2017).

the current trend is to employ them in Pipelined ADCs and TI ADCs for higher resolutions and speeds respectively.

2.4 SAR ADCs working principle

The SAR ADC structure and implementation details are discussed in this section, in order to clarify its advantages as a candidate for high-efficiency Nyquist-rate ADC implementation.

2.4.1 SAR algorithm and building blocks

An N-bit conversion in a SAR ADC is usually performed over an N-step binary search algorithm. The conventional algorithm is presented by the flow-chart in Fig. 2.10, and the transient signals in the SAR ADC are shown in Fig. 2.11.

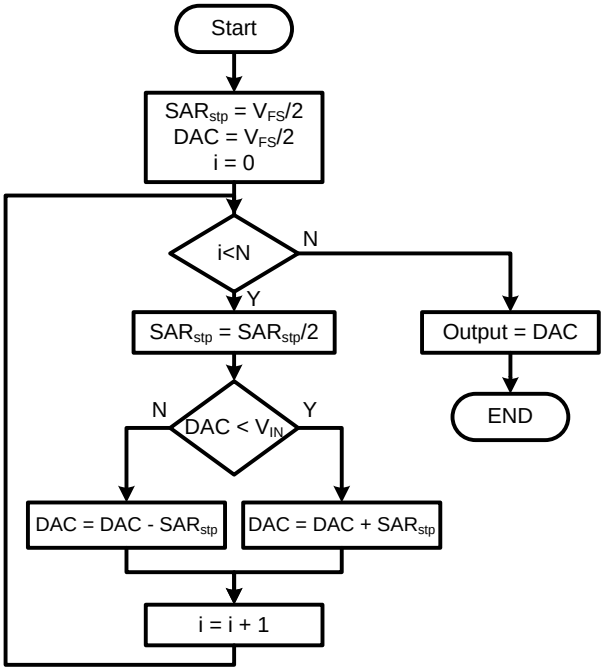


Figure 2.10: Binary search algorithm used in an N-bit SAR ADC.

At each new step through the binary search, the search scope is split into two halves, and the algorithm decides to which half the input belongs. Splitting the search scope is done by generating a DAC output at the middle of this scope, and the decision is obtained by a comparator, which receives the sampled input and the DAC output at its two inputs. Based on the comparator decision, one output bit is decided, and the next search scope is defined, which is half-sized compared to the previous scope. Therefore, after N steps, the search scope is reduced by factor 2^{-N} relative to the first scope, which equals the input full-scale; this results in a search accuracy equivalent to the LSB size of an N-bit ADC.

The SAR output is obtained either by collecting the serial comparator outputs, or equivalently by the digital logic output, which forms the DAC input. However, the later has to consider the last comparator decision to update the DAC input, which is not required to be converted by the DAC anymore.

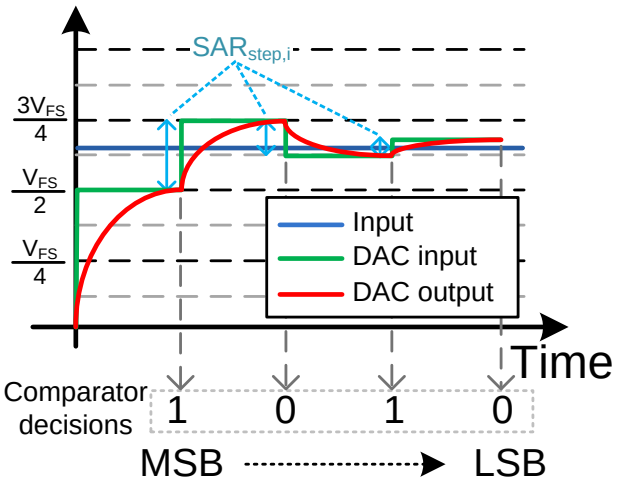


Figure 2.11: 4-bit SAR ADC transients.

Main building blocks

- **SAR logic:** An important feature of the SAR architecture is the employment of a major digital part, which made it specially attractive for implementation in modern technology nodes. The SAR logic is the main controller of the search algorithm; it controls the algorithm flow, triggers or enables each block in the ADC, reads and interprets the comparator output, updates the DAC input and generates/stores the ADC output.

- Similar to every Nyquist ADC, the SAR uses a **S&H** block – or track and hold (T&H) – to sample the analog input. This block determines the accuracy of the sampled signal, which forms the quantization process input. Therefore, the speed and accuracy of the S&H block have to be at least equivalent to required ADC speed and accuracy. Also, the sampling noise should be kept below (or equal) to the ADC required effective resolution.

- **The comparator** is an important and a design-critical block in the SAR. The comparator performance is a main limitation of the ADC performance. Usually, comparator noise determines the overall ADC noise level; this makes the comparator design a major challenge for high-resolution ADC implementation. The comparator offset leads to an equivalent offset on the ADC characteristics. Finally, comparator hysteresis leads to ADC memory effects and potentially dynamic linearity degradation.

- **The DAC** builds up the feedback path by converting the digital SAR output, which successively tracks the sampled input, into an analog value at the comparator input. The DAC linearity determines the overall ADC linearity, which makes the DAC design the main challenge for high-linearity ADC implementation.

2.4.2 Conventional circuitry

Most SoA SAR ADCs employ a capacitive DAC (CDAC), which performs the D/A conversion through the charge redistribution concept. The CDAC conventionally employs a binary weighted capacitor array, which is switched between two (or more) reference voltages, as shown in Fig. 2.12.

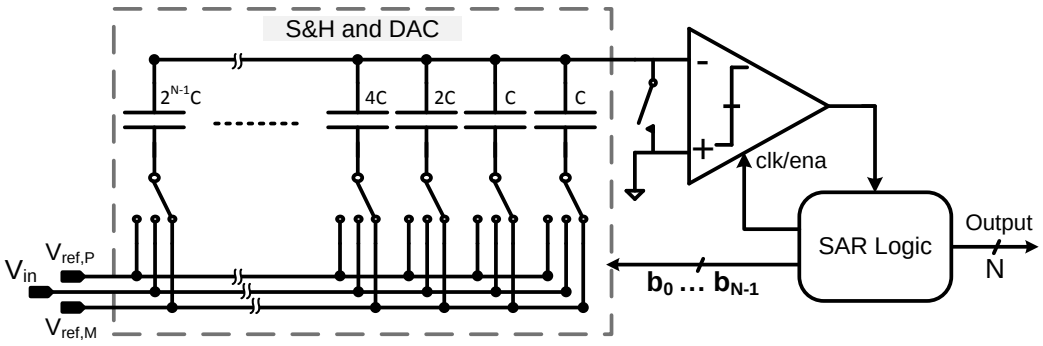


Figure 2.12: A conventional N-bit SAR ADC with capacitive charge redistribution DAC.

An important advantage of CDAC implementation in SAR is the shared S&H, which is embedded in the CDAC structure. This excludes the need for a dedicated S&H, which eliminates a significant area consumption by the sampling capacitor. Thereby, the input sampling takes place on the same capacitor array of the CDAC. On the other hand, the charge redistribution is controlled through the digital control signals $(b_0, b_1, ..., b_{N-1})$ generated by the SAR logic; these signals switch the bottom plates of the CDAC in Fig. 2.12, and an equivalent voltage to the charge redistribution appears at the comparator input.

Figure 2.13 shows an exemplary switching scheme in a 4-bit SAR ADC with charge redistribution binary weighted CDAC. This scheme moves through six switching phases [6], as follows:

(a) Sampling phase: All capacitors are connected at bottom plate to the input and the comparator inputs are shorted to allows charging the capacitor array to V_{in}.

(b) Hold phase: The sampling (or tracking) phases ends by disconnecting the two comparator inputs, then, V_{in} is held on the capacitor array. Before the CDAC switching starts, all the bottom plates are switched to ground (the negative reference), and the comparator differential input equals -V_{in}, due to charge conservation on the top plates.

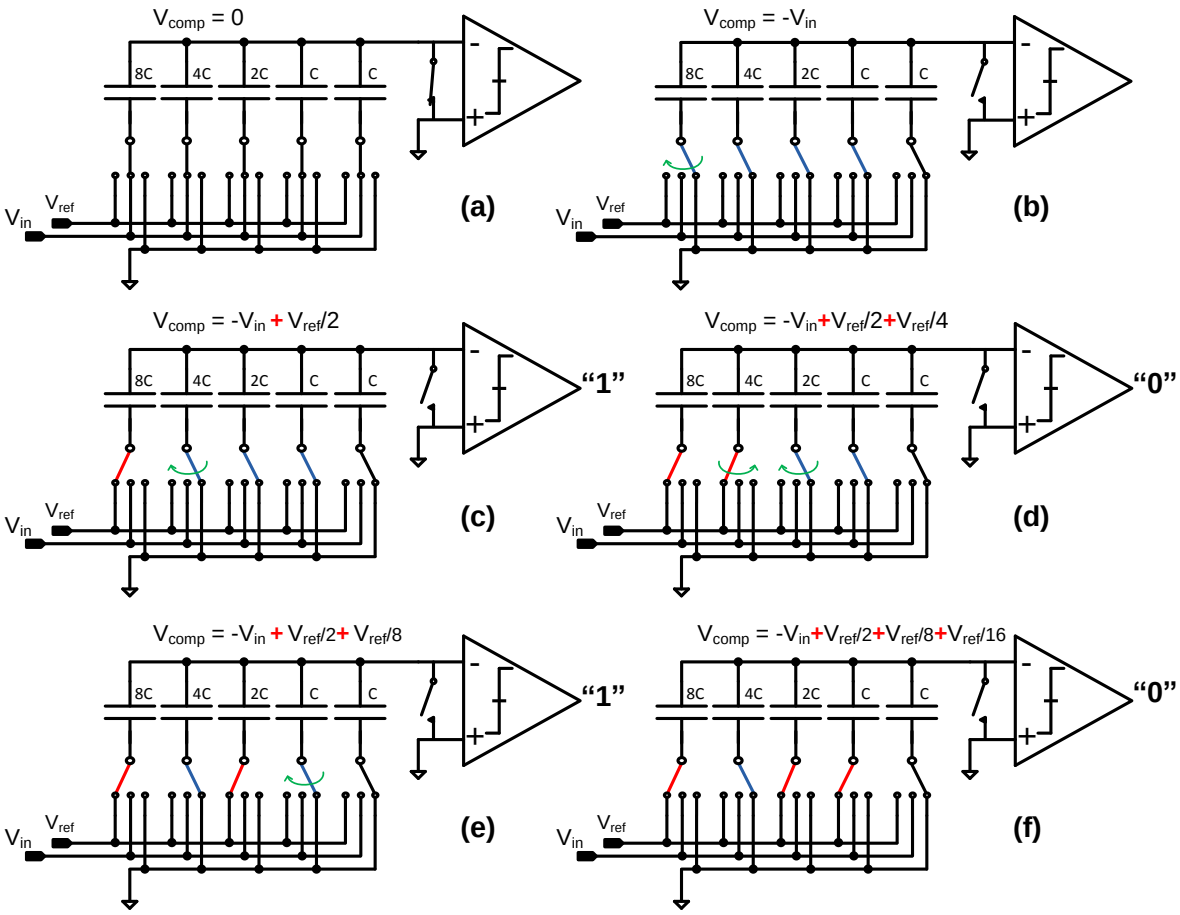


Figure 2.13: An exemplary switching scheme of a 4-bit CDAC in the SAR, in accordance with the example in Fig.2.11.

(c) MSB bit trial: The DAC conversion starts with the most significant bit (MSB). In order to generate a half full scale step ($V_{ref}/2$), a complete V_{ref} is applied at the bottom plate of the MSB capacitor, which forms half the capacitor array (8 C in Fig. 2.13). In this case, the CDAC array forms a voltage divider between two equal capacitors, therefore, the top plate voltage is increased by $V_{ref}/2$. Now, the comparator decision of "1" interprets that $V_{in} > V_{ref}/2$, therefore MSB = "1", and the MSB capacitor connection is kept for later trials. But for a "0" comparator decision the MSB capacitor bottom plate should be connected back to ground for later bit trials.

(d..f) Next bit trials: In Fig. 2.13 (d), a similar procedure is carried on the second MSB capacitor (4 C), while the equivalent voltage divider involves two capacitors with sizing ($3\,C_{total}/4, C_{total}/4$), therefore, the voltage shift at top plate equals $V_{ref}/4$. Due to a "0" comparator decision (in accordance with the exemplar V_{in} of Fig. 2.11), the bottom plate is switched back to ground before the next bit trial is performed. The bit trials ends after switching the least significant bit (LSB) capacitor (C), and the last comparator output generates the LSB value.

Differential implementation: Although, Fig. 2.13 includes – for simplification – a single-ended implementation of the charge redistribution CDAC, the SAR ADC usually implements a differential structure (similar to any ADC) to suppress common mode and even order distortions and to double the input range to $[-V_{ref}, +V_{ref}]$. The differential implementation follows the same concept as described above, but with two CDAC arrays to sample the two differential input respectively, and the two CDACs are switched fully symmetrically during the conversion phases (by exchanging the V_{ref} and ground connections).

2.4.3 Advantages and limitations

The SAR ADC implementation with charge redistribution CDAC has proven an excellent efficiency among SoA. This implementation, initially excluding the comparator, employs major digital part and fully-dynamic CDAC; thus, it introduces a scaling friendly structure and allows for an efficient trade-off between power and speed, while employing a relatively low area consumption and a simple design.

On the other hand, the conventional implementation suffers from few limitations, which motivated further investigations and improvements. High resolution implementations of this structure led to exponential growth of CDAC array and C_{max}/C_{min} ratio. Also, increased sizing is usually required to guarantee element matching and to avoid parasitic effects, therefore it becomes more challenging and less efficient, hence, a non-practical implementation. Moreover, the conventional switching scheme includes high power consumption by switching all the binary weighted CDAC elements to the full-scale reference voltage with more (wasted) power at the reverted decisions (switched back). Finally, conventional comparators with static preamplification included two drawbacks; they limit the benefit of scaled technology, as they rely on good analog processing (e.g. for high differential gain), and they require high power, especially for high-resolution implementations, consequently, they prevent an efficient power and speed trade-off.

2.5 SoA SAR techniques

2.5.1 Switching Schemes

A major part of the research on SAR ADCs in the last decade involved developing improved and more efficient CDAC switching schemes. Two main objectives drove this development: lower power consumption and decreased number of unit elements in the CDAC, which determined its area consumption at a fixed unit capacitor size based on technology and parasitics. Many SoA publications reported new and modified schemes; in the following, few of these schemes are discussed, to show the major improvement steps achieved by SoA designs.

Capacitor splitting: Based on a similar conversion algorithm and CDAC structure as in section 2.4.2 and [6], the work in [7] focused on reducing the reference power dissipation at step-down decisions (reverted switching), in cases similar to Fig. 2.13 (d). This power can be reduced by performing two step switching (in Fig. 2.13 (d): switching 2C high then 4C down), or by sharing the charges between the two capacitors (parallel connection for 4C and 2C), before switching 4C down. Moreover, this dissipation can be completely avoided

by capacitor splitting; thereby, the capacitor 4C is split into two 2C capacitors and only one half is stepped down, while original 2C capacitor is left on ground. To perform this for all elements, [7] suggested splitting the MSB capacitor to an exact copy of the left elements of the CDAC, and a step down at bit (i) is done by leaving the capacitor (C_i) unaltered, while switching down its copy in the MSB array. Therefore, no extra reference power is consumed at step-down. The number of capacitors in CDAC is kept the same as required by the conventional structure.

Monotonic switching: A CDAC with monotonic switching scheme was introduced in [8]. The scheme does not require step-back or reverted switching; every CDAC element is switched once at most, which further reduces the switching energy. Moreover, the major improvement with this proposal is the reduced number of elements, because the first decision (MSB) is obtained directly after sampling without CDAC switching. Therefore, the MSB element is excluded and the total unit elements is reduced by factor 2. Figure 2.14 shows an example switching procedure of a 4-bit monotonic-switching CDAC, which employs only 3-bit arrays. The sampling action (Fig. 2.14 (a)) takes place at the CDAC top plates directly at comparator inputs, while all bottom plates are connected to V_{ref}. Therefor, after input holding (opening the sampling switch) as in (b), the comparator detects the input polarity (c), which generates the MSB value. For an MSB = "1" (/"0"), the 4C MSB capacitor of the positive (/negative) CDAC array is switched to ground. The same procedure is carried out for the next MSBs down to the LSB (f), without any step-back action. This scheme suffers from two drawbacks: Due to the monotonic switching, the comparator common-mode voltage (V_{CM}) changes during conversion steps, which potentially leads to output distortion due to a dynamic offset variation. Also, the monotonic switching does not allow efficient reduction of common mode and even-order harmonic distortion as fully differential ADCs.

V_{CM}-based switching: The V_{CM}-based CDAC in [9] employs an additional reference voltage (V_{CM}), to implement a differential switching. Thereby, during the sampling phase (CDAC reset), all capacitors bottom plates connect to V_{CM}. After top-plate sampling, the comparator detects the input sign, which equals MSB value (similar to monotonic switching). Then the two MSB capacitors (in the positive and negative arrays) are switched differentially to either V_{ref} or ground respectively, based on the MSB value; the same applies

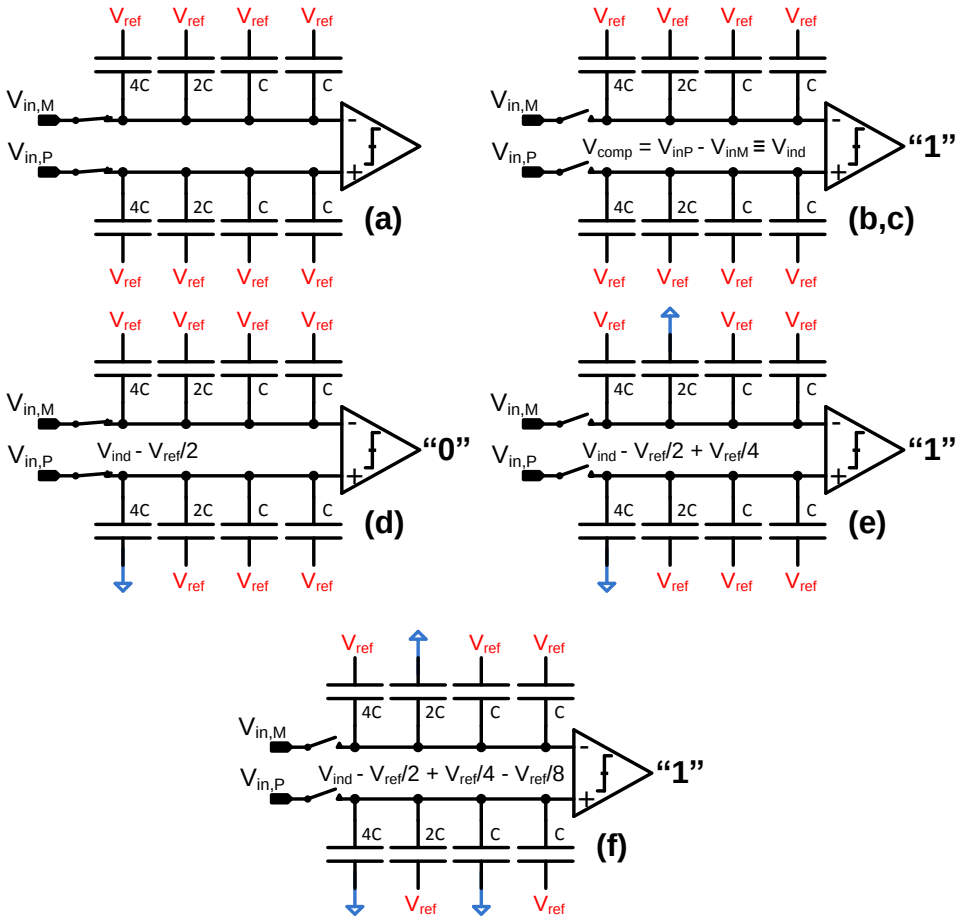


Figure 2.14: 4-bit CDAC in the SAR with monotonic switching, in accordance with the example in Fig.2.11.

for the later capacitors in the CDAC. Compared to monotonic switching, this structure reduces the average switching energy by about 33%, while using the same CDAC array size, additionally, it allows for differential switching to reduce common mode distortion. However, this scheme requires an additional reference voltage and a more complex switching logic. Nonetheless, V_{CM} variations in this scheme leads to common mode variation; they do not limit the conversion linearity, because the CDAC is completely disconnected of V_{CM} at the end of the conversion.

Tri-level CDAC: A tri-level CDAC switching scheme also requires an additional reference voltage, similar to V_{CM}-based scheme [10]. However, based on an accurately scaled V_{CM} as half of V_{ref}, this reduces the number of CDAC elements by another factor 2. This is achieved by allowing each CDAC capacitor

(or capacitor group) to have one of two weights that represents either a full size or half size, by switching the bottom plate(s) to V_{ref} or to $V_{CM} = V_{ref}/2$ respectively. Therefore, after MSB decision (sign detection), only one of the two CDAC sides will be switched using the tri-level concept, which also leads to a varying common mode voltage. Due to decreased CDAC size a significant reduction of switching energy is achieved at the cost of a second high-accurate reference (V_{CM}) generation.

More schemes: Many other schemes were introduced based on one of these schemes or merging some of these concepts together, like the **V_{CM}-based monotonic switching** in [11], which adapt the CDAC sides reference after MSB decision, then it proceeds with a monotonic switching using V_{CM}. Further improvements on switching schemes involved mainly modifications on the initial CDAC states and the switching algorithms, to further decrease the switching energy, which was not accompanied with further decrease in CDAC size [12, 13]. Also, recent publication addressed the **reset energy saving**, additional to the switching energy, which is required to switch the CDAC back to the initial phase required by the switching algorithm [14, 15]. The **semi-resting CDAC** is reported in [16], which presented one of the best power efficient SAR ADCs with $FOM_W = 0.44\,fJ/conv.step$. The semi-resting DAC uses a concept close to the V_{CM}-based CDAC without the need for V_{CM} generation, as V_{CM} is generated by connecting all the CDAC bottom plates together after the sampling phase, in which only half the CDAC was connected to V_{ref}.

Comparison and limitations: Table 2.1 includes a comparison of some CDAC switching schemes, which cover the major reduction steps in switching energy. For a reasonable comparison, the numbers in Table 2.1 represents the application of each scheme in a 10-bit SAR ADC with a fixed unit capacitor, as the unit capacitor is limited with a minimum size based on the used technology and / or estimated parasitics. Therefore area reduction is represented by reduced number of unit elements; the average energy reduction is shown with and without the reset energy, which is required only for the switching schemes that reset the CDAC bottom plates to different voltages before sampling.

Although Table 2.1 shows the advantage of advanced switching scheme for power and area reduction, a complete fair comparison is not possible at the bases of these few measures. For example, V_{CM} generation can be more costly for the structure both in energy and area, when compared to one scheme

advantage. The power consumption of the digital circuitry to implement the switching scheme is not considered, while it potentially reaches levels comparable to the power advantage. Also, the energy estimation varies significantly with increased parasitics. On the other hand, other measures like common mode rejection or comparator common mode variation may be of major importance. Finally, when the CDAC unit capacitor is determined by matching or noise requirements, instead of the minimum C limitation, then all numbers in Table 2.1 need to be recalculated for a reasonable comparison.

Table 2.1: Comparison of CDAC switching schemes.

Scheme	CDAC Area (C)	Area reduction	Average switch energy ($C \cdot V^2$)	energy reduction	Reset Energy ($C \cdot V^2$)	Total energy reduction	V_{CM} sensitivity
Conventional [6]	2048	ref.	1363.3	ref	0	ref	no V_{CM}
Split capacitor [7]	2048	0 %	852.3	37.5 %	0	37.5 %	no V_{CM}
Monotonic switching [8]	1024	50 %	255.5	81.3 %	0	81.3 %	no V_{CM}
V_{CM}-based [9]	1024	50 %	170.2	87.5 %	0	87.5 %	low
Switch-back [17]	1024	50 %	127.5	90.6 %	255.5	71.9 %	no V_{CM}
Tri-level [10]	512	75 %	42.4	96.9 %	0*	96.9 %*	high
V_{CM} monotonic [11]	512	75 %	31.9	97.7 %	0*	97.7 %*	high
[12]	512	75 %	25.1	98.2 %	127.8*	88.8 %*	high
[13]	512	75 %	15.8	98.8 %	127.8	89.5 %	high
[14] w/o CSR	512	75 %	10.5	99.2 %	127.8	89.9 %	high
[14] w/ CSR	512	75 %	10.5	99.2 %	0	99.2 %	high

* Estimated numbers not provided in the references.

2.5.2 Other DAC architectures

The charge redistribution CDAC with binary-weighted capacitor array is the most common implementation within SAR ADCs. Due to its simplicity, it has been preferred over other DAC architectures, specially, in low resolution ADCs. However, due to the exponentially growing capacitor array size and limitations related to parasitics and area constraints, a full resolution binary-scaled capacitor array is not a practical solution for higher resolutions. Also, a reduced total capacitance is very much desired for moderate and high speed. Therefore, two main approaches are introduced to ease the DAC implementation with reduced total C.

The split CDAC splits the capacitor array into a most-significant-bits (MSBs) array and one or more sub-arrays connected via a series bridge capacitor(s). Thereby, all arrays can share the same unit capacitor size, which saves chip area and relaxes the mentioned layout limitations [18] [19]. Figure 2.15

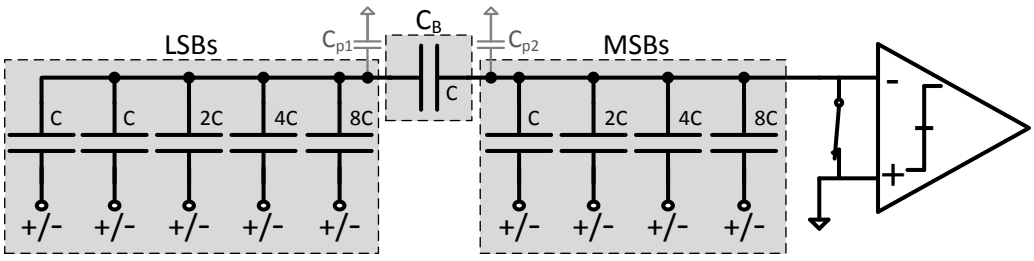


Figure 2.15: Example of an 8-bit split CDAC with two sections.

shows an example of a two-section split CDAC; each of the two sections features a 4-bit array, therefore a total of 8 bits is obtained with a total of $2{\cdot}2^4 = 32$ unit C instead of $2^8 = 256$ unit C. Due to the serial bridge capacitor C_B, the elements in the LSBs part of the CDAC in Fig. 2.15 will be additionally weighted by C_B. Hence, switching the complete LSBs part (in one direction) is equivalent to switching an LSB or a unit element (C) in the MSBs part; while switching the individual elements of the LSBs part provides the fine steps within one unit element size of the MSB array. This architecture provides a good solution to reduce the total CDAC size and area consumption. However, the split CDAC structure is very sensitive to parasitics related to

the bridge capacitor(s), and the whole DAC needs to be calibrated to the full resolution [55].

Hybrid R-C DAC: The second approach uses a hybrid architecture combining both conventional capacitive charge redistribution and resistive voltage scaling DACs [20] [21]. This approach employs a coarse resolution with a coarse CDAC for MSBs; while an additional resistive DAC (R-DAC) connected to the LSB capacitor generates the LSB part. Therefore, this approach also relaxes the DAC design with a reduced C_{max}/C_{min} ratio, which leads to a reduced area. Similar concept was applied in [22], where a ramp generator replaced the resistive DAC to produce the LSB part after the coarse CDAC [21].

In fact, both approaches are useful to reduce the overall DAC capacitance and therefore enhance the speed for moderate resolution ADCs. However, they both require a large calibration and/or linearization effort, which makes them have worse area and power efficiency for high-resolution ADCs. Therefore, the most power-efficient SAR ADCs employ CDACs at moderate to low speed [16]-[23] and moderate to low resolution. Some use a sub-fF unit capacitor with a custom layout in [23], which was similarly applied in [16], bringing the design close to the kT/C noise limit.

Current-mode SAR: Few SoA SAR ADC implementations replaced the voltage domain charge redistribution CDACs by current mode DACs, as in [24] [25]. These were beneficial mainly for moderate resolution and high speed implementations. Thereby, a current steering DAC improves the ADC speed by reducing the DAC settling time during bit trials by excluding voltage settling delay, as in CDAC; it also relaxes the input driving power because it allows for reduction of the sampling capacitor size down to the kT/C noise limit. This is usually achieved at the cost of high power (potentially with more area) consumption in the DAC current arrays.

2.5.3 Comparator trends

The comparator is a very important block in the SAR ADC structure; it is called the last analog block within the mostly digital/dynamic SAR structure. The comparator parameters determine several SAR ADC performance measures. For example, the comparator offset determines the overall ADC offset;

the input-referred comparator noise is usually the dominant noise contribution in the SAR ADC.

Conventional comparators: Figure 2.16 includes a basic comparator structure, which includes three blocks: The first block is the differential preamplifier, it provides signal amplification and mainly determines the noise performance, it also attenuates the distortion (kick-back), which is fed from the dynamic circuitry afterwards back to the input; thereby, a simple differential amplifier stage was conventionally used [17, 26]. The second block is the decision circuitry, which practically amplifies the differential input into a full-rail (full-VDD) decision; positive feedback load with a reset control is usually employed in the decision circuit [26], also a strong-arm latch is widely used as a decision circuit [17, 27]. The final block is the output storage unit, which is mostly combined with the SAR logic in recent implementations; it records the decision outputs before the decision circuit is reset.

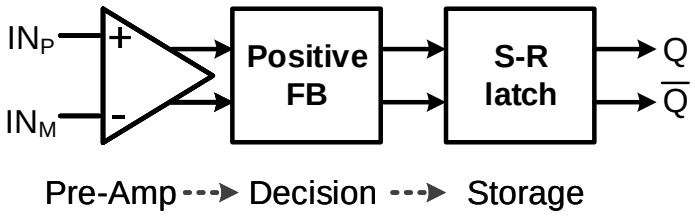


Figure 2.16: Conventional comparator structure.

Fully dynamic comparators: A fully dynamic SAR ADC implementation is very desirable, because it excludes static power consumption and allows one to scale the power consumption with the ADC sampling rate. Therefore, dynamic comparators, also referred to as latch-type voltage sense amplifiers, are widely used in SoA [28]. Also, most recent SAR implementations, with superior power efficiency, employed fully dynamic comparators [16, 23, 29].

The double tail dynamic comparator is a very efficient comparator implementation [30, 31], which has been increasingly used in SAR ADCs [29, 32, 33]. Figure 2.17 shows a circuit schematic of the double tail dynamic comparator [30]. It includes a dynamic preamplifier followed by a latch circuit; the comparator is activated at the rising clock (clk) edge, and it consumes power only then; it is reset during the low clock level (clk : low, clkB : high), therefore it does not consume any static power. At the rising clock edge, $M_{l,7}$

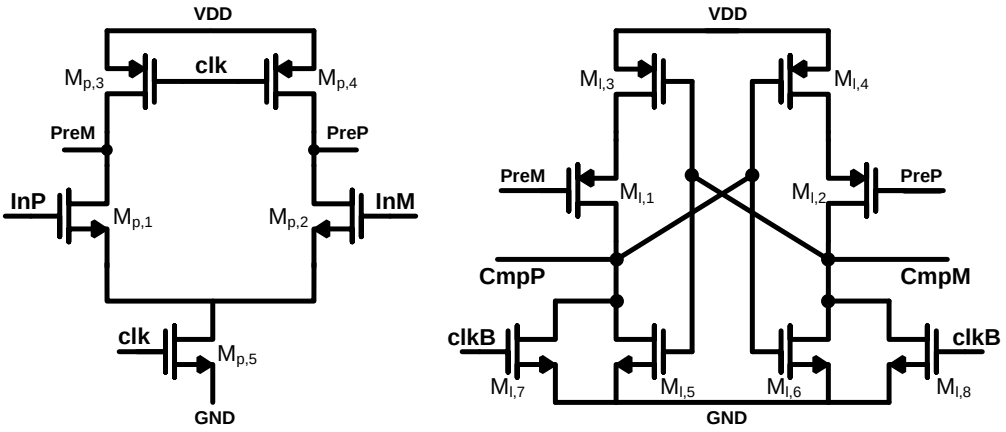


Figure 2.17: Schematic of the double tail dynamic comparator [30].

and $M_{l,8}$ release the latch outputs, while the latch regeneration only starts when PreP and PreM are pulled low in different speeds (after reset to VDD), based on the differential input, which leads to the final latched outputs.

Comparator with voting decisions: In order to reduce noise in dynamic comparators without further increasing the transistor sizing and hence the power consumption, a majority voting for comparator decisions was proposed in [34]. It also aimed to optimize the comparator power consumption through the SAR bit trials, since the comparator receive large input (beyond noise levels) in most bit trials, and it is required to resolve small inputs only in few steps. Therefore, [32,34] suggested techniques to detect critical comparator decisions and activate the majority voting accordingly. During majority voting the comparator is activated repeatedly for N times with a fixed input; the final decision is based on voting over the collected N decisions.
Similarly, other SAR ADC implementations employed techniques with repeated decisions to resolve an LSB below the comparator noise levels by decisions averaging [35], statistical estimation noise reduction [36], or LSB repeats and comparator zero detection [37]. All these techniques aimed for a high comparison precision, at increased power, only around LSB range, while operating at low power during MSBs.

Comparator power scaling and VCO-based comparators: In addition to voting and repeated LSB decisions, more techniques were developed to scale the comparator power over SAR decisions; these include for example

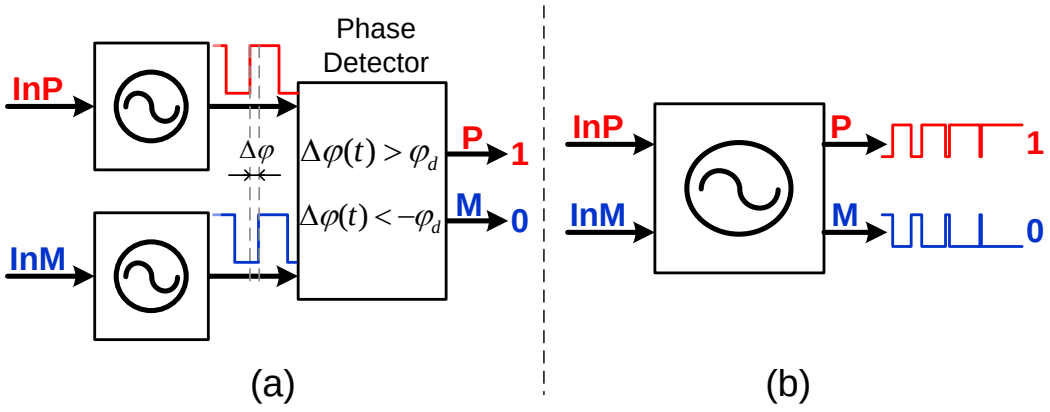


Figure 2.18: Basic principles of: (a) the eye-opening and (b) the oscillator-collapse comparators.

subranging using fine and coarse ADCs in [29] and multiple parallel comparators [38]. Two drawbacks are common for all these power scaling schemes: a complex design overhead altering the SAR simplicity and a limited power scale (in most cases two levels: coarse and fine).

Recently, oscillator-based comparator architectures were proposed for automatic power scaling; this allowed the comparator power consumption to smoothly scale with the overdrive levels without a need for additional sensing circuitry. An eye-opening VCO based comparator was introduced in [39], cf. Fig. 2.18(a), and an oscillator collapse comparator was presented in [40], cf. Fig. 2.18(b). These two comparators operate fully dynamically and consume power only during a limited time window; the width of this window is inversely dependent on the overdrive voltage. In [39], the overdrive voltage is represented by a frequency drift between two internal oscillators; their adjacent edges form an eye-opening which incrementally opens at a speed dependent on the overdrive voltage. Therefore, high overdrive voltage leads rapidly to an open eye, which is detected by a phase detector (PD) in a short time, thus at low power consumption. But at low overdrive voltage, the eye-opening requires longer oscillation time to open, which leads to more power consumption. In [40] a non-zero overdrive voltage gradually drifts the duty cycle of a single VCO either to 0% or to 100% (collapsed oscillation); the collapse speed dependency on overdrive voltage leads to similar power scaling as the eye-opening comparator [39].

2.6 SAR Challenges for high resolution

SAR ADC presented an attractive architecture that recently dominated the research on Nyquist ADC design; most recent Nyquist ADCs either are SAR ADCs or employ internal sub-ADCs using SAR, to achieve high efficiency and/or high speed A/D conversion. However, SAR ADCs were not able to reach the high-resolution range as discussed in section 2.3.6. The comparator design is a major challenge for higher resolution implementations, however, with a compromised power consumption, SoA comparator designs can be extended to the high-resolution range. On the other hand, the high-resolution DAC represented the main obstacle, which prevents high-resolution SAR ADC implementation or greatly degrades its efficiency and needs an excessive calibration effort.

2.6.1 High linearity DAC for SAR ADC

Several SoA designs aimed to implement SAR ADCs with resolutions above 12 bit, but effective resolutions always deteriorated due to limited DAC element matching, which resulted in limited linearity and significant harmonic distortion at ADC outputs. Several techniques were introduced to enable high-resolution DAC implementations. In [41] 3-section split CDAC is used for a 16-bit ADC, which allowed for large unit capacitor sizing; this together with huge calibration units led to a significant increase in power consumption. A 14-bit implementation is introduced in [42]; to achieve a high effective resolution, the ADC is operated in oversampling mode with thermometer coded DAC elements combined with dynamic element matching (DEM). In [43], also a 14-bit implementation is presented; three MSB capacitors are switched by a thermometer coded flash output, also foreground calibration is used, however, the effective resolution is limited below 12 bits. Both [39, 44] presented 13-bit ADCs, which employ non-binary CDACs to facilitate error detection and corrections, despite the employed calibration, both effective resolutions were below 11 bits. The 14-bit implementation in [45] employs a "half-split" technique for a triple split CDAC structure, by splitting each capacitor into two halves to allow the calibration logic to benefit from more possible capacitor combinations. The reported ENOB is also below 12 bits. Finally, in [46],

a uniform split CDAC with sub-radix-2 is implemented for a 14-bit resolution resulting in about 12.5-bit ENOB.

The SAR ADCs reported above showed a limited linearity mainly due to a limited calibration accuracy. This problem is not limited to SAR ADCs, but it is common to most Nyquist ADCs, which rely on matching between weighted elements to achieve high resolutions. Therefore, similar degradation of the effective resolutions – compared to nominals – is reported for high-resolution Nyquist converters, which are recently almost exclusively implemented as pipelined SAR ADCs [47–49]. These ADCs require extensive calibration to achieve high resolutions and are usually limited to the available calibration capabilities.

2.6.2 Calibration and linearization techniques

Calibration of the CDAC is required for any SAR ADC with above moderate resolution, to remedy the CDAC mismatch effect on ADC linearity. The calibration is often performed by first performing mismatch estimation for CDAC elements. This is followed by correction or compensation for this mismatch, either in the analog domain (through a compensation DAC) or in the digital domain (in the SAR logic). The mismatch estimation is performed either in foreground by taking the ADC off-line, once at startup or repeatedly in time, or in the background during ADC operation. In order to improve the limited calibration accuracy, it is often accompanied by mismatch shaping, dithering or other linearization techniques [32, 35, 50, 51].

Conventional Calibration: In [52] an error cancellation scheme is introduced to calibrate a 14-bit ADC; resistor strings (resistive DACs) are used with voltage buffers at the bottom plate of a capacitor in parallel to the CDAC, in order to estimate the mismatch errors and generate compensation voltages. The two designs in [53] and [54] also use RDACs similarly for calibration in parallel to hybrid RC DACs. In [53] a calibration DAC is additionally used during conversion to get two further bits, this design presented very good linearity but at a limited speed (signal bandwidth $= 50\,\text{Hz}$). The design in [54] allowed higher speed ($167\,\text{kS/s}$) but with poor linearity (THD $= 85\,\text{dB}$). These three designs perform a foreground error estimation, then a background analog error compensation, which requires a fast operation for the calibration DACs

and relatively high power consumption. An extensive calibration is performed in [55], for a 16-bit ADC, due to availability of an on-chip micro-controller. To calibrate 13 capacitors in a three-section split CDAC, 13 additional capacitor arrays are added with 12% of the CDAC size and with LSB/4 resolution. This design reports a THD = 101 dB for 100-kHz input frequency.

Self Calibration: A common approach for calibration uses the CDAC to perform a self-calibration, by using the LSBs to measure the MSBs. This usually provides only coarse improvement due to a limited calibration accuracy (unless mismatch errors are very much higher than CDAC resolution). In [56], a self calibration is employed with an additional half LSB capacitor to prevent missing codes of an 11-bit split CDAC. The design reports an SFDR = 77.5 dB for 555-kHz input frequency. A 13-bit ADC is introduced in [44]; each of the 5 MSB capacitors are calibrated by a comparison to a redundant representation (by the same CDAC) using the array of smaller capacitors; thereby, two additional CDAC elements are added to provide the redundancy. This calibration is performed in the background during an additional (16th) SAR step; it caused about a 4 dB improvement in SFDR to 82 dB. The 14-bit ADC in [45] uses a "half-split" CDAC with self calibration by splitting each CDAC capacitor into two halves in addition to a 4-bit sub DAC for extended calibration accuracy to 1/16 LSB, thereby, an SFDR = 92 dB at f_{in} = 1.1 kHz is reported.

Linearization techniques: To improve the calibration accuracy beyond the limited calibration device (e.g. the RDAC or sub-CDAC), many designs employ dynamic linearization techniques, either to exclude additional calibration elements (at moderate resolutions) or to extend calibration accuracy (at high resolutions). In [35], a 13-bit ADC is introduced without calibration by applying a "Noise-Shaped-Uniform dither" to the DAC input. This randomizes the mismatch effect and shapes it to high frequencies, which allows it to be further reduced by a low-pass CDAC characteristic (by additional capacitors); an SFDR = 85 dB is reported at f_{in} = 2.3 MHz. Both [39, 57] employ perturbation-based calibration by error estimation through digital post-processing (LMS algorithm), which is enabled by injecting a perturbation signal into the redundant CDAC output; the two designs report SFDRs of 85 dB and 95 dB at 64 kHz and 1 MHz input frequencies respectively. To achieve high effective resolution and linearity in the pipelined SAR ADCs [47–49], careful design and layout are combined with startup foreground calibration for error cor-

rection, in addition to dither injection for improved DNL and INL. Thereby, SFDRs above 100 dB are reported at low frequencies (below 100 kHz), with rapid degradation at increased input frequencies. The additional analog and digital logic blocks for calibration and linearization led to increased power and area consumption which degraded the overall efficiency.

2.7 SoA gap and design target

Introducing high-resolution Nyquist ADCs is accompanied with several challenges. With low-cost simple calibration, highly efficient SAR ADCs showed limited effective resolutions, while highly sophisticated calibration and linearization techniques rendered less efficient ADCs. As Fig 2.19 shows, despite the increased interest for high-efficiency high-resolution SAR ADCs, those were generally limited below SNDR = 76 dB [32,40,58,59]. On the other hand, high-resolution Nyquist ADCs showed degraded power efficiency. Only few exceptions recently presented good power efficiency [47,49]; nonetheless, those rely on analog residual amplification in older technologies. This together with extensive calibration and large area requirements made them less attractive solutions for scaling to small CMOS nodes.

This work aims to produce novel techniques for SAR ADCs, which allow high-resolution Nyquist conversion in the simple SAR architecture by employing a scaling friendly design with low or no additional calibration cost and good power efficiency. The target design is intended to fill the gap between the current trend of high-resolution Nyquist ADCs – as in Fig 2.19 – and the general trend of high-efficiency ADCs.

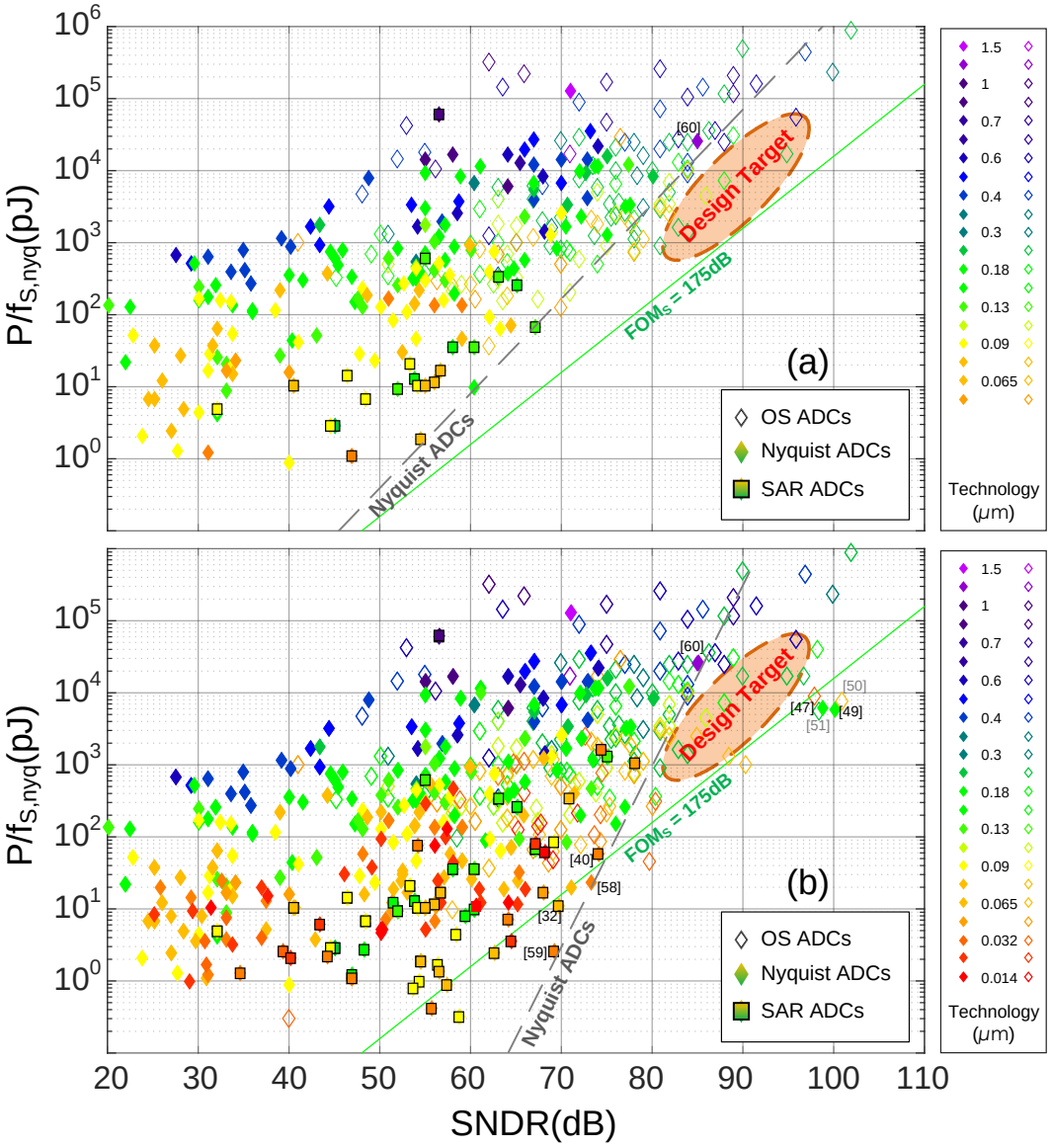


Figure 2.19: SoA energy plot and design target: before thesis start (a) and in 2018 (b).

Chapter 3

Sigma-Delta DAC for SAR ADC

Recent research on SAR ADCs led to improved conversion speeds and unprecedented power efficiency FOMs; however, these improvements were achieved only up to moderate resolutions. This is mostly caused by the limited accuracy of the common CDAC implementations. To counteract this limitation, the following chapter presents a novel approach to build the internal DAC in SAR ADCs as an incremental-ΣΔ DAC [61, 62].

3.1 SAR concept with ΣΔ DAC

In symmetry to NS ΣΔ ADCs, ΣΔ DACs achieve high-resolution D/A conversion without dependence on strict element matching, but on oversampling and noise-shaping. Therefore, ΣΔ DACs can replace CDACs in SAR ADC to achieve high linearity and high effective resolution.

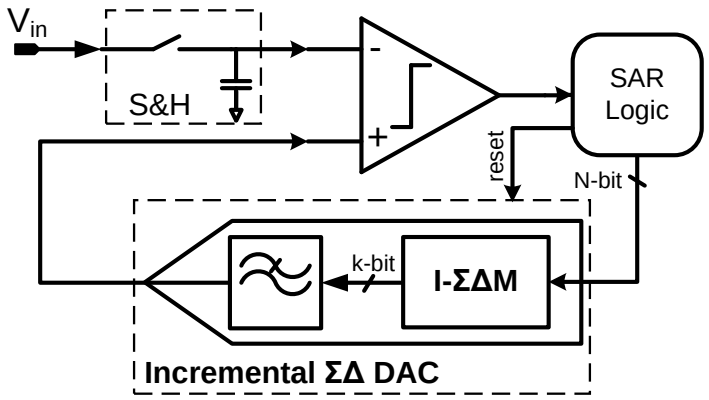


Figure 3.1: I-ΣΔ DAC in an N-bit SAR ADC.

Figure 3.1 shows the basic structure of a SAR ADC with an I-ΣΔ DAC. In order to perform the binary search algorithm in the ADC, the DAC output tracks the sampled input over N SAR cycles (for N-bit conversion), as in Fig. 3.2 with N = 8. Each SAR cycle involves one D/A conversion and a comparator decision, after which the SAR digital output is updated accordingly. Then, the next cycle and D/A conversion take place until the digital word finally equals the analog input within the intended accuracy, when the last bit in the SAR digital output is defined. Hence, the DAC requires both a resolution equal to the overall SAR resolution and a sample-to-sample correspondence between its input and output. If the DAC is to be realized using a ΣΔM, an incremental operation is required for the ΣΔ DAC to be integrated in the SAR loop. This is because a free running ΣΔM has a memory and is thus not suitable for Nyquist operation.

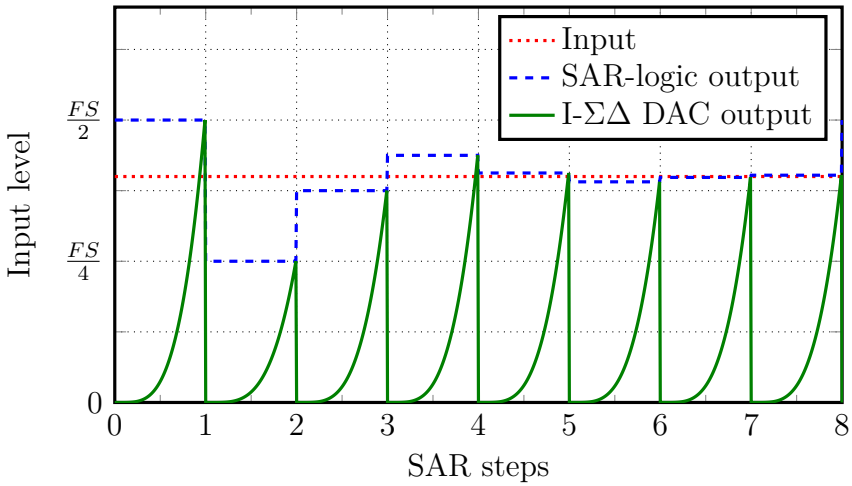


Figure 3.2: Transient response of an 8-bit I-ΣΔ based SAR ADC [61] ©2014 IEEE.

3.2 I-ΣΔ DAC structure

3.2.1 The Incremental ΣΔ Modulator

The first part of the ΣΔ DAC is the digital ΣΔM, which is responsible for converting the full-resolution (N-bit) digital word from the SAR logic into a coarsely quantized output (k-bit in Fig. 3.1). Here, a single bit output is particularly attractive due to the intrinsically linear behavior of the corresponding

DAC. The quantization error of the coarsely quantized output, which is commonly modeled as quantization noise, is spectrally shaped to high frequencies. The objective of the analog post filter is the removal of this quantization noise while leaving the signal untouched. At this point, it should be noted that the filter following an I-ΣΔM is different from a common decimation filter, because its design is guided by time-domain rather than frequency domain requirements, when striving for minimum residual quantization noise [63].

The incremental or cyclic operation of the ΣΔM is governed by a reset signal, cf. Fig. 3.1. This reset arrives together with the new digital input value, before the ΣΔM operates for a fixed number of clock cycles M. Thus, the single digital value at the modulator's input is finally represented by a sequence of M values at the output of the modulator, which are passed to the analog reconstruction filter. Through this incremental conversion in the modulator and the analog reconstruction filter, the averaging nature of classical ΣΔ-based converters is broken and a sample-to-sample conversion is achieved.

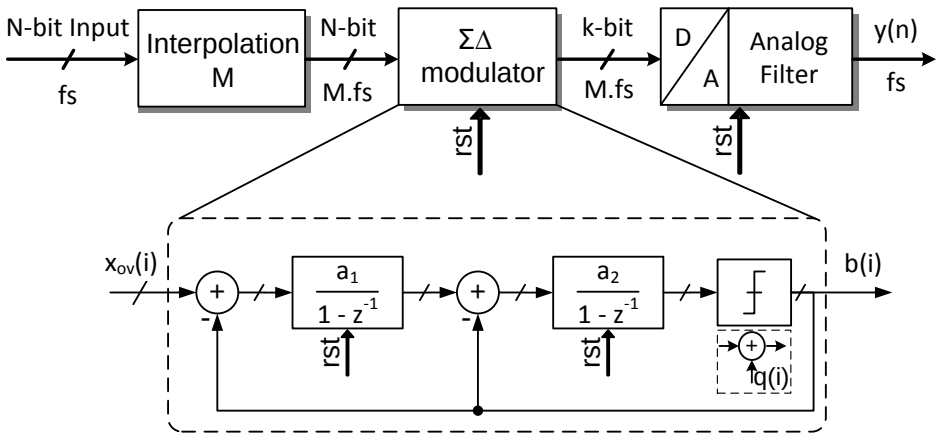


Figure 3.3: Basic block diagram of the I-ΣΔ DAC with an exemplary second order ΣΔM implementation [61] © 2014 IEEE.

The performance of the ΣΔM is commonly defined by its order, OSR = M and internal bit width. In Fig. 3.3, an example of the ΣΔ DAC is presented incorporating a second-order single-bit ΣΔM. The digital implementation of the ΣΔM in the DAC allows for a trade-off between speed and complexity, and introduces the possibility of a digitally reconfigurable design, i.e. a SAR ADC architecture with a variable resolution.

3.2.2 Analog Reconstruction Filter

3.2.2.1 D/A interface

The analog reconstruction filter receives the coarsely quantized serial data from the ΣΔM, from which it generates a high accuracy analog output. Therefore, the filter is in fact a semi-digital filter. Also, due to the periodic reset every M samples, the reconstruction filter behaves as a finite-impulse-response filter (FIR), with a maximum order of M. The conventional structure of a semi-digital FIR filter, as shown in Fig. 3.4, includes a shift register fed by the ΣΔM digital output $b(n)$, an array of coefficients a_i, e.g. realized as a capacitor array, and a summing node to generate the final output, which satisfies the FIR filter equation (3.1).

$$y(n) = \sum_{i=0}^{M-1} a_i \cdot b(n-i) \tag{3.1}$$

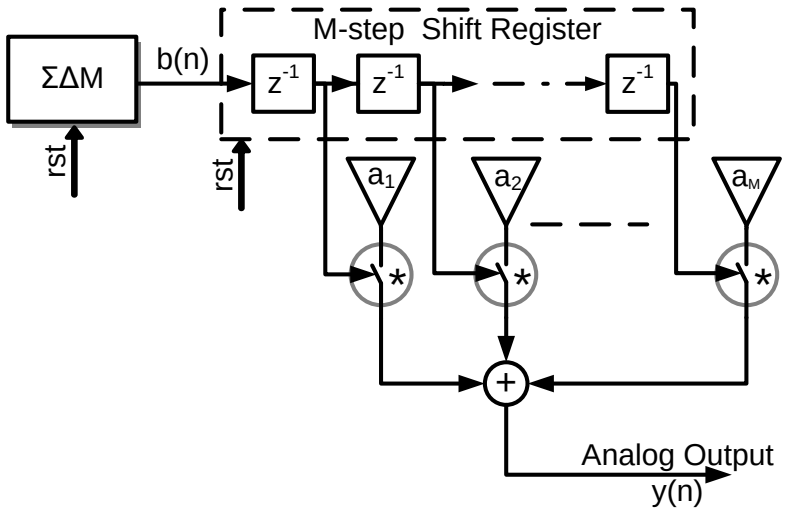


Figure 3.4: M-order semi-digital FIR filter with binary input.

Each multiplication between an analog coefficient and a single bit output of the shift register ($a_i \cdot b(n-i)$) is produced with a switched element controlled by the output of a shift register. A similar switching scheme is applied using switched-C (SC) array in the oversampling DAC of [64], while in [65] an array of scaled current sources implements the coefficients a_i.

The main advantage of this semi-digital FIR structure is that errors in the filter coefficients do not lead to nonlinearity in the DAC output, because the digital input is shifted over all coefficients. Therefore, errors introduced by mismatch are averaged at the output leading to a minor degradation of the filter response, which manifests itself as less attenuation of the quantization noise [65].

3.2.2.2 Optimal filter design

In conventional oversampling DACs, the FIR filter coefficients are chosen according to the intended frequency response of the filter, which describes the filter's steady-state behavior. However, this is not valid for the incremental DAC. Here, due to the reset action after each conversion, the filter never reaches steady-state but always works in transient mode. Hence, the steady state of the filter represented by its frequency response is of minor importance, and the reconstruction filter must be designed through an analytical optimization of its impulse response (IR), using the removal of quantization noise as optimization criterion as proposed in [66].

The output of the filter $y(n)$ at the end of the nth cycle is given by an M-point convolution between the filter impulse response h and the ΣΔM output (during the nth cycle) $b(i)_{|i=(n-1)\cdot M \ldots n\cdot M-1}$ according to (3.2).

$$y(n) = h * b\ (n) = \sum_{i=(n-1)\cdot M}^{n\cdot M-1} h([n \cdot M - 1] - i) \cdot b(i) \tag{3.2}$$

Due to the reset action, only the first M values of the filter IR appear in the output of (3.2), and it suffices to characterize the filter by these M values only. The output of the ΣΔM $b(i)_{|i=(n-1)\cdot M \ldots n\cdot M-1}$ can be decomposed into two terms, one corresponding to an oversampled (interpolated) version of the SAR digital input, $x_{\mathrm{ov}}(i)_{|i=(n-1)\cdot M \ldots n\cdot M-1}$, convolved with the STF impulse response, and a second term corresponding to the quantization noise, $q(i)_{|i=(n-1)\cdot M \ldots n\cdot M-1}$, shaped by the ΣΔM's NTF, as included in (3.3).

$$b(i) = \mathrm{stf} * x_{\mathrm{ov}}\ (i) + \mathrm{ntf} * q\ (i) \tag{3.3}$$

In the case of an I-ΣΔ ADC (with a digital decimation filter) a third term would appear in (3.3) due to the input referred circuit noise of the modulator. This term vanishes for the DAC case, since the modulator is implemented in the digital domain. In (3.3) both convolution terms are again M-point, due to the M-step periodic reset. Thus, both STF and NTF need to be represented in FIR forms only with the first M values of their corresponding IRs.

Designing the filter for optimum signal-to-noise ratio (SNR) is equivalent to designing its impulse response for optimum suppression of the shaped quantization noise at its output. According to [66] this M-point optimum IR can be obtained analytically using the Lagrange Method and is given by

$$h_{\text{opt}} = \frac{\mathbf{K}^{-1} \cdot e}{e^T \cdot \mathbf{K}^{-1} \cdot e} \ , \quad \text{with } \mathbf{K} = \mathbf{N}^T \cdot \mathbf{N} \ , \ e = [1 \ 1 \ \ldots \ 1]^T, \tag{3.4}$$

where $\boldsymbol{N}$ is the noise transfer matrix of the ΣΔM and e is an M-element vector of ones. The analog reconstruction filter should ideally implement this optimum IR. However, an efficient analog implementation requires the use of suboptimal approximations for the filter as will be discussed in section 3.4.

3.3 System level simulations for the I-ΣΔ DAC

In this section, a systematic study of the I-ΣΔ DAC performance is presented. This study covers ΣΔMs of second to fourth order. The used ΣΔM topologies and internal coefficients are similar to those in [67], with modifications on some coefficients to match a binary representation, which simplifies a digital implementation. These modifications are performed by a simulation based optimization. As performance measure, the maximum SQNR obtained at the output of the optimal FIR filter according to (3.4) is used, when applying a sinusoidal signal at the modulator input.

Table 3.1 lists the simulated SQNRs and the ENOBs of the various modulator structures, for different number of steps M of the I-ΣΔM. This number of steps is equal to the number of FIR filter coefficients and the length of the optimal impulse response. Hence, the higher the number of samples, the better the filter performance and the quantization noise shaping are, as well as

Table 3.1: I-ΣΔ DAC system simulation results

ΣΔM	#Samples: M	SQNR(dB)	ENOB(bit)	Quantizer
2nd order	80	74	12.0	1-bit
	128	84	13.7	
3rd order	64	79	12.8	1-bit
	80	86	14.0	
	128	100	16.4	
4th order	64	86	14.1	1-bit
	80	95	15.5	
2nd order	80	85	13.7	2-bit
	128	95	15.5	
3rd order	64	95	15.5	2-bit
	80	102	16.7	
	128	116	19.0	
4th order	64	102	16.7	2-bit
	80	111	18.1	

the achievable performance. Increasing the modulator order also leads to better quantization noise shaping, thus a higher SQNR when combined with the optimal analog filter. Nevertheless, the challenges associated with an analog implementation of the optimal filter increases with increasing modulator order. Fig. 3.5 shows the optimum filter impulse responses for the three exemplary modulator structures of Table 3.1 (M=80). According to Fig 3.5, the higher the modulator order, the wider the coefficients spread is, which leads to a more difficult matching of the analog representation of these optimal coefficients.

Increasing the internal resolution of the ΣΔM leads to a decreased level of quantization noise resulting in an improved performance. In addition to that, the modulator stability is relaxed especially for higher order ΣΔMs, which in turn allows for a more aggressive coefficient scaling and a higher SQNR. Table 3.1 shows that for a fixed number of conversion steps M a performance gain between 11 and 16 dB is possible, when moving from a single bit to a two-bit internal quantizer. Alternatively, a significantly decreased number of samples has to be implemented to obtain the same performance with a two-bit ΣΔM, leading to faster conversion cycles. However, the multi-bit operation is prone to mismatch, which now not only results in a sub-optimal filter response, but also

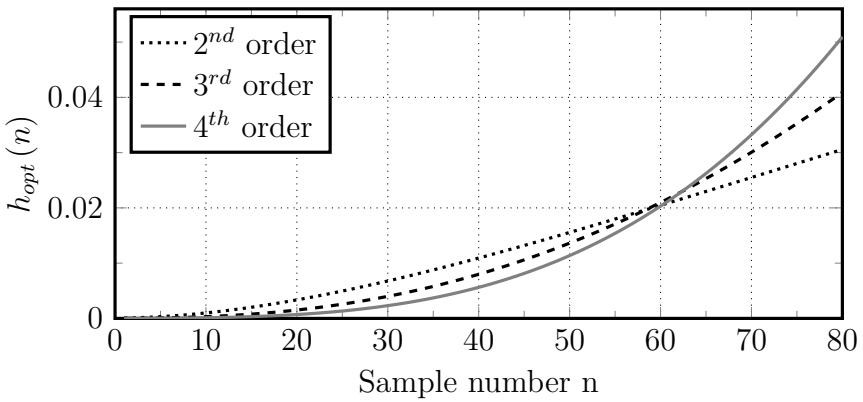


Figure 3.5: 80-sample impulse response h_{opt} of the optimal reconstruction filter for 2nd, 3rd and 4th order ΣΔMs.

introduces non-linearity, which would need to be calibrated using additional circuitry. Thus, a single-bit ΣΔM is chosen for the proposed DAC.

3.4 Optimal reconstruction filter approximation

On system level, designing the filter after an I-ΣΔM can be similarly adressed for DAC as for ADC implementations. However, in the design of the optimal decimation filter for an I-ΣΔ ADC according to (3.4), apart from arithmetic operations, the main cost to be considered is the digital representation of the optimal filter coefficients. Therein, a binary representation with a bit-width equal to or greater than the overall ADC accuracy is conventionally used [68]. On the other hand, for the analog reconstruction filter implementation inside the intended I-ΣΔ DAC, a 15..16-bit accuracy of the FIR coefficients is not affordable with any analog representation. Thus, an approach for approximation of the optimal filter is mandatory to render it realizable.

For the I-ΣΔ DAC design study in the next sections, we consider a fixed structure for the ΣΔM in order to validate the proposed architecture with an example implementation. The proposed design target is to achieve a dynamic range above 90 dB, while keeping the design complexity and the number of conversion steps in the I-ΣΔM tolerable. To this end, a third order single bit ΣΔM is used with a cycle length of 128 samples, which can achieve an ideal SQNR of 100 dB.

3.4.1 Cascade of integrators

A Cascade of Integrators (CoI) can be used in the digital domain, in order to simplify the decimation filter for the I-ΣΔ ADC. This structure provides a very good approximation of the IR of the optimal filter when it is of the same order as the ΣΔM, cf. Fig. 3.6, [63,68,69]. In an analog implementation, the CoI structure has the attractive feature that it removes any matching requirements on the analog elements. It uses the one-bit output of the ΣΔM as the input of the first integrator, hence an intrinsic DAC linearity is guaranteed. System simulation for the exemplary case shows that the CoI approximation provides an SQNR of 96 dB, which corresponds to a 4 dB drop compared to the optimal filter performance. However, the main draw-backs of this structure in the analog domain are a relatively high power consumption together with stringent noise requirements on the active stages, because it requires three active stages operating at the high speed rate of the ΣΔM output.

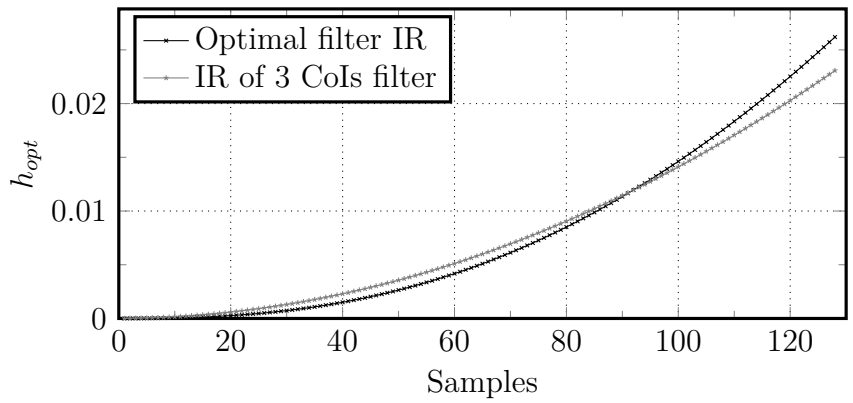


Figure 3.6: 128-sample IR of the optimal reconstruction filter for 3rd order ΣΔM and the filter IR as a cascade of 3 integrators [61] © 2014 IEEE.

In order to combine the advantages of a semi-digital FIR structure and a CoI approximation of the optimal filter, two structures were investigated as reconstruction filters for the 3rd order I-ΣΔM. The first structure includes a semi-digital FIR filter followed by one integrator, as shown in Fig. 3.7. Therefore, the FIR coefficients are scaled as $a_i = i \;:\; i = 1..M$. The second structure is shown in Fig 3.8. It includes an FIR array followed by two integrators. The two structures are selected to realize the CoI filter with efficient implementation, which makes use of the semi-digital FIR filter to relax the

active stage requirements and replace at least one active stage, at the same time, they do not implement a full (stand alone) FIR filter, which requires a strict element matching. The advantages and disadvantages of the two structures with proposed implementations are discussed in sections 3.4.2 and 3.4.3 respectively.

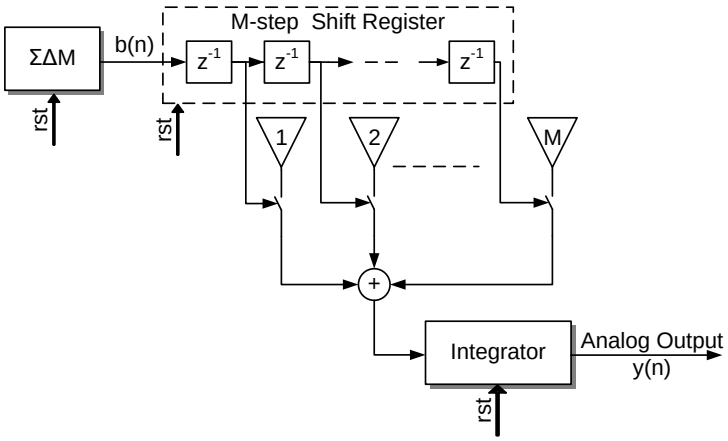


Figure 3.7: Block diagram of the filter approximation as a semi-digital FIR filter with one integrator.

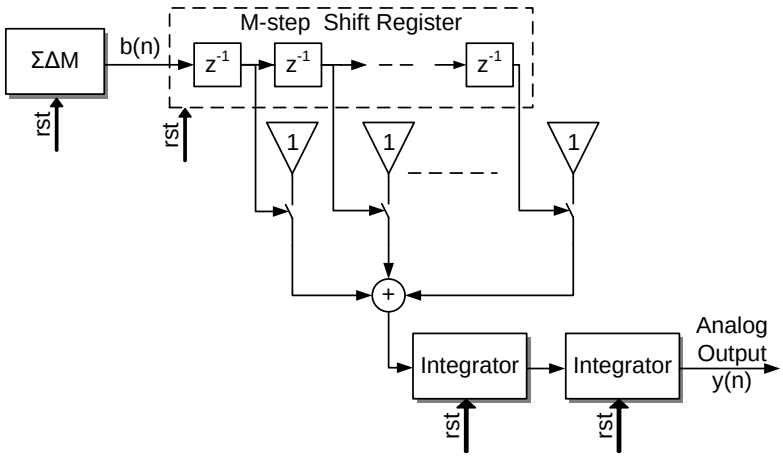


Figure 3.8: Block diagram of the filter approximation as a semi-digital FIR filter with two integrators.

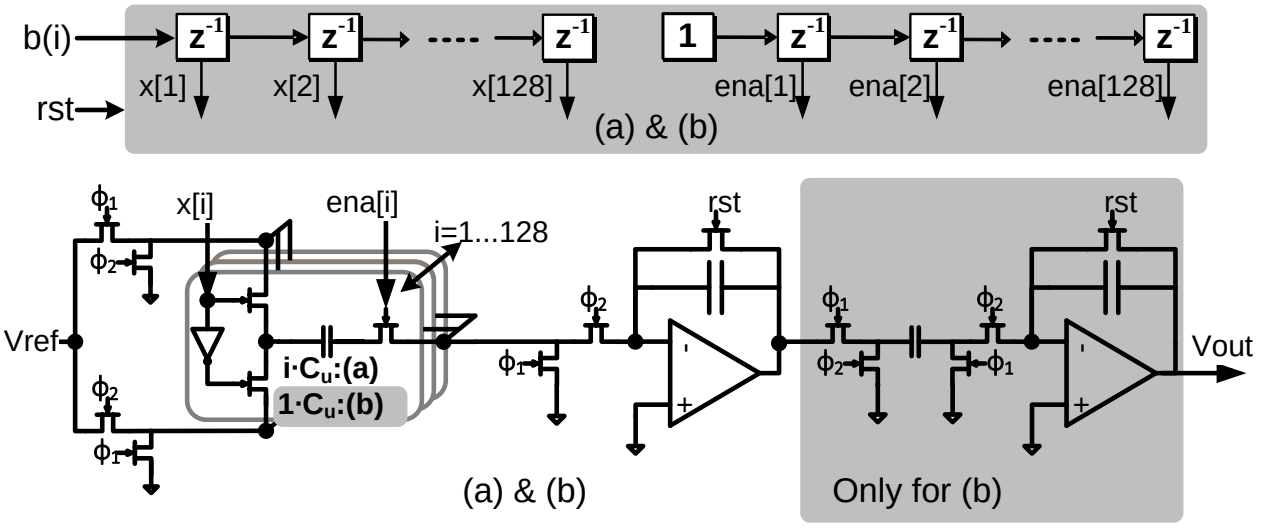


Figure 3.9: Illustration of the analog reconstruction filter implementation using a capacitor array followed by one integrator (a) or two integrators (b).

3.4.2 SC-integrator with a scaled capacitor array

To implement the structure of Fig. 3.7, a switched capacitor (SC) integrator is used with an array of scaled capacitors summed up at the integrator input (virtual ground). Fig. 3.9 (a) shows the circuit diagram of the proposed structure. A similar system was used in [64] to build the analog reconstruction filter for a conventional $\Sigma\Delta$ DAC, where the semi-digital FIR filter was combined with an infinite impulse response (IIR) filter. In the proposed structure the IIR part is now replaced with a resetting integrator and the FIR filter operates in an incremental fashion, using a reset signal in addition to a vector of enable signals from a resetting shift register.

The detailed filter operation in Fig. 3.9 (a) is as follows: The $\Sigma\Delta$M output is incrementally fed into a 128-element shift register, which is reset together with the $\Sigma\Delta$M by the reset signal (rst). The 128 outputs of the shift register control the charging/discharging phases of the capacitor array at the input of the SC-integrator. Hence, a logic '1' in the shift register connects the top plate of the respective capacitor to V_{ref} during the first phase ϕ_1 and to the common mode during the second phase ϕ_2 leading to a positive charge transfer into the output. On the contrary, a logic '0' controls the switching in an inverse fashion during the two phases ϕ_1/ϕ_2 leading to a negative charge transfer.

Additionally, since the shift register is filled in a sequential fashion, 128 enable signals are used to disable the not-yet-active taps of the FIR, reflecting the incremental nature of this conversion.

The capacitor array is scaled to match the impulse response of a cascade of two integrators i.e. a ramp. Therefore, the capacitors in the array have sizes of $\{1, 2, 3, \ldots, 128\} \cdot C_{\text{unit}}$. Hence, together with the third integrator, a 7-bit representation of the element array is capable of providing a 96 dB SQNR with a single active integrator.

3.4.3 Two-stage structure with a unity capacitor array

Alternatively, a second structure is proposed in Fig. 3.9 (b), in which the capacitor array is followed by a cascade of two active integrators. Thus, the capacitor array together with the shift register represent the impulse response of a single integrator, i.e. a unit step function, corresponding to equally sized capacitors in the array, in order to perform the optimal filter approximation corresponding to a 3rd order CoI. This structure has two major advantages. Firstly, the overall size of the capacitor array decreases from $\sum_1^{128} i \cdot C_{\text{unit}} = 8256 \cdot C_{\text{unit}}$ for the structure of Fig. 3.9 (a) to only $128 \cdot C_{\text{unit}}$. Also, since the feedback capacitor of the first active integrator scales with the total capacitance of the capacitor array, the capacitive load of this structure is lowered, which in turn leads to a significant power saving.

3.4.4 DAC mismatch simulation

A statistical mismatch study to determine the required matching between the array elements was performed. Fig. 3.10 shows the effect of array element mismatch on the SQNR obtained with the two structures in Fig. 3.9 (a) and (b), in comparison to the optimal semi-digital FIR filter. For the direct semi-digital implementation using a FIR filter without any integration stage, a relative mismatch with a standard deviation below 10^{-4} is needed, in order to keep the average SQNR above 90 dB. Using the element array with one integrator of Fig. 3.9 (a) relaxes the matching requirement to around 0.6%. The modified structure with two integrators in Fig. 3.9 (b) relaxes the matching requirement of the capacitor array even further, due to both the equally sized capacitors

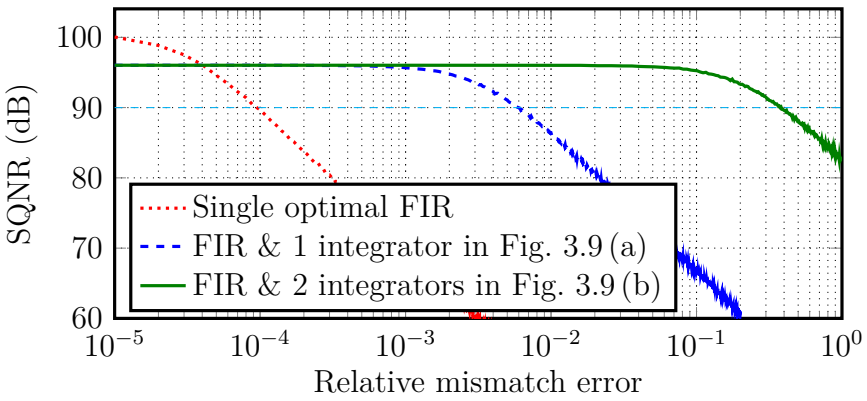


Figure 3.10: Comparison of element mismatch effect on DAC performance, between a FIR filter with optimal coefficients and approximations using FIR filter followed by one integrator or two integrators.

and the additional smoothing performed by the two integration steps. Fig. 3.10 shows that the mismatch in the 2 integrators case can be as large as 40%, while keeping the average SQNR above 90 dB. Figure 3.11 shows three histograms for 100-run mismatch simulations on this structure for three values of standard deviation (σ). Thereby, with $\sigma = 25\%$ for the element mismatch, an SNDR above

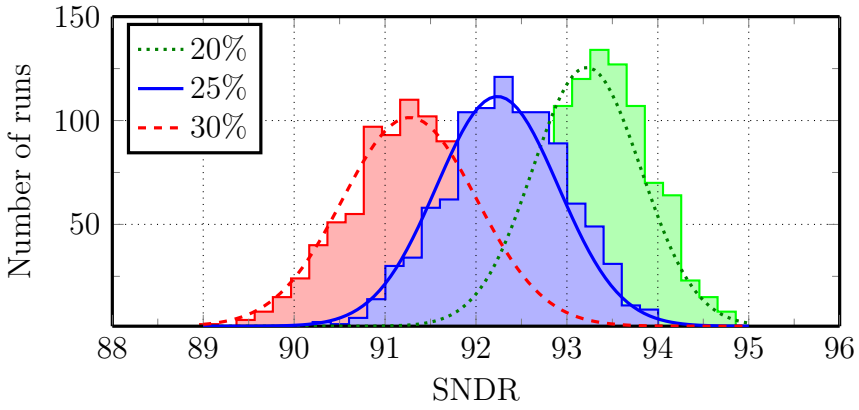


Figure 3.11: Capacitor array mismatch effect on the DAC performance, for FIR & 2 integrators structure from Fig. 3.9 (b).

90 dB is achievable with 3-σ yield. Therefore, with the modified structure, the total capacitance size decreases, matching requirements are very low, with the disadvantage of a required second active integrator.

3.4.5 System simulation using the I-ΣΔ DAC

In order to evaluate the proposed structure, the requirements on the op-amps were estimated. To this end, system-level simulations and circuit simulations with VerilogA models were performed on the proposed structure. The simulations show that the slew rate (SR) requirement on the Op-Amps is relatively relaxed, due to the incrementally slow output settling shown in Fig. 3.2, which causes the output not to change with the fast internal sampling frequency (f_s) but with the slow conversion frequency: $SR \propto f_s/128$. Furthermore, the required gain-bandwidth (GB) product, which influences the internal power consumption of the Op-Amp, was found to be low with values of $GB < 2 \cdot f_s$ already resulting in near optimal performance. Finally, the only challenging requirement is a high DC-Gain $> 80\,\text{dB}$ needed to achieve the required linearity in the filter.

A Spectre simulation using VerilogA models for the Op-Amps incorporating the mentioned non-idealities is shown in Fig. 3.12, proving that the I-ΣΔ DAC achieves ENOB>15 bit within a bandwidth of 250 kHz, allowing its use within the intended 16 bit SAR ADC.

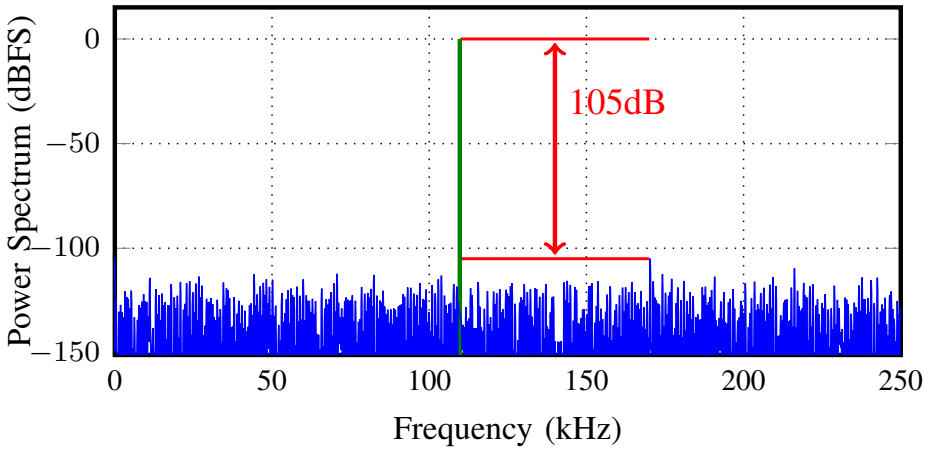


Figure 3.12: Power spectrum at the output of the I-ΣΔ DAC (4096 point), with VerilogA-based simulation, $f_{in} = 109.9\,\text{kHz}$, $f_{S,DAC} = 0.5\,\text{MHz}$: SNDR = 95.1 dB, SFDR = 105.0 dB, ENOB = 15.5 bit, modified from [61] © 2014 IEEE.

3.5 Transistor-level design of the original I-ΣΔ DAC enhanced SAR ADC

To validate the original approach of an I-ΣΔ DAC in a SAR ADC, a partial implementation for the I-ΣΔ DAC on transistor level was performed. The focus of this implementation was to evaluate the requirements on the analog part of the DAC, which poses the main challenge concerning noise and linearity. The digital part of the filter was simulated in Verilog, while the comparator of the SAR ADC was simulated in Verilog-A. The feasibility study was performed in TSMC 40 nm CMOS technology, with a 1.1 V supply.

3.5.1 Reconstruction filter structure

Fig. 3.13 shows the single ended circuit implementation of the designed analog reconstruction filter, which implements the architecture introduced in section 3.4.3, with few more modifications to allow for more efficient implementation: The circuit includes a switched capacitor array summed up at node X, which is the input of an active integrator, followed by a second SC-integrator. The input of the filter is the one-bit ΣΔM output, which feeds a shift register with M delay elements. The outputs of this register control the charging/discharging phases of the equally sized capacitor array elements during ϕ_1, ϕ_2 to the output of the first integrator, which implements the D/A interface of the filter. Instead of a 128-tap capacitor array in Fig. 3.9, where the shift register outputs x[1:128] control its switching, the FIR taps count is halved into 64 by merging each two consecutive taps in one. Each FIR tap i $\{i = 1 : 64\}$ includes one capacitor switched to V_{ref+} or V_{ref-} with a logic block controlled by (x[2i-1], x[2i], ena[i]) during phases ϕ_1, ϕ_2. The 64 signals ena[1:64] control the tap activation to satisfy the incremental operation, i.e. they are reset to logic '0' initially and then incrementally set to logic '1' by a shift register, which is clocked with half the ΣΔM clock frequency.

Therefore, the objective of the logic block is as follows: if the selected tap[i] is enabled (ena[i]='1'), then if x[2i-1]=x[2i]='1' the related capacitor bottom plate is switched to V_{ref+}/V_{ref-} during phases ϕ_1/ϕ_2 respectively, leading to a positive charge transfer to the output. In contrast, if the tap is enabled and

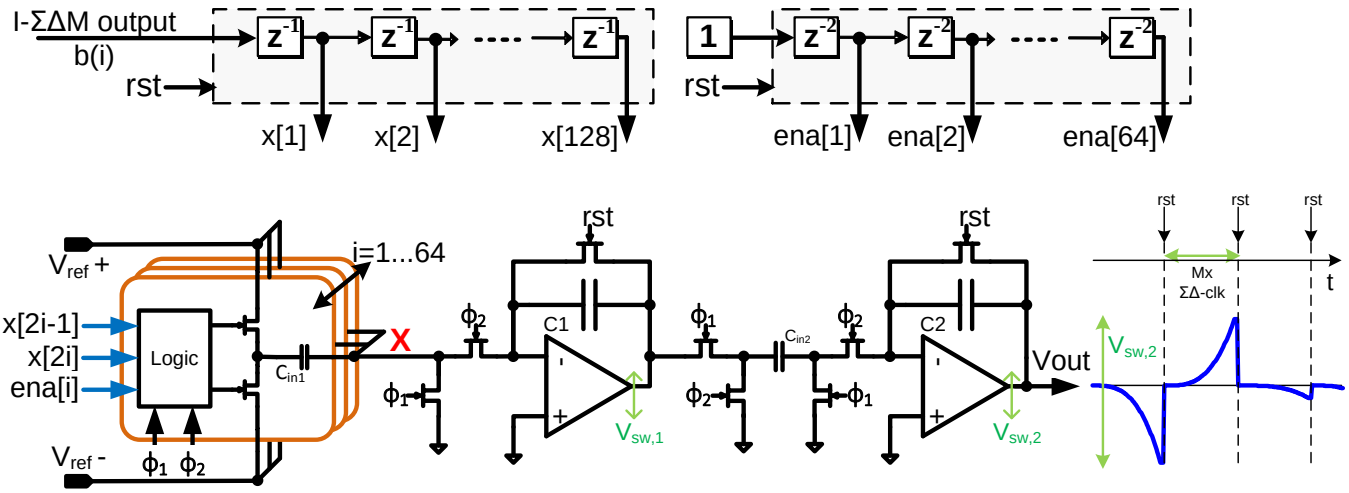


Figure 3.13: Schematic view of the implementation circuit of the reconstruction filter, approximating a 3rd-order CoI, modified from [62] © 2015 IEEE.

x[2i-1]=x[2i]='0', then the capacitor is switched in an inverse fashion during ϕ_1, ϕ_2, leading to a negative charge transfer. Finally, if the tap is not yet enabled (ena[i]='0') or the bits x[2i-1] and x[2i] are different, the capacitor's bottom plate is connected in both phases to V_{ref-}, leading to zero charge transfer to the output.

3.5.2 Capacitor sizing

The capacitor size is determined from three requirements: Firstly, the matching requirement on the capacitor array, which is of low importance for this architecture (as discussed in section 3.4.3). Also, mismatch between the capacitor array and the integration capacitor, as well as the capacitors in the second stage, only lead to a linear gain error, which does not deteriorate the output linearity. Secondly, the ratios of the input and output capacitors used in each of the two integrator stages define their voltage gains, which define the voltage swings at the two op-amp's outputs. It is beneficial to maximize the output voltage swing, which is equal to the SAR-ADC input voltage range. Also, for the first integrator it is useful to maximize the signal component at its output, where it is compared to the op-amp output noise and the sampled noise at C_{in2}. Therefore, the voltage output swing is set to 700 mV around a

common mode of VDD/2. To achieve this, the input to output capacitor ratios in the two stages ($\frac{C_{in1}}{C_1}$, $\frac{C_{in2}}{C_2}$) were chosen accordingly.

Finally, the main aspect to consider for the absolute capacitor sizing is the effect of thermal switch and opamp noise. To estimate the generated noise and the related degradation on the DAC performance, it is useful to consider the noise contribution at the DAC output and compare it to the signal power at this point. The noise of an SC-integrator is addressed in [70] and split into two noise sources: the first source is present at the input, which is accumulated in the integrator, and an output referred op-amp noise, which is usually less dominant. Following a similar procedure, a thermal noise source is defined for each of the 64 taps, which has a mean square power of

$$\overline{v_{n,tap}^2} = \frac{kT}{C_{in1}}. \tag{3.5}$$

If the maximum noise contribution from all FIR taps is considered, the estimated total charge introduced into the first integrator capacitor C_1, including an estimate of the op-amp input referred noise [70], yields

$$\overline{q_{n,out1}^2} = 2\,kT \cdot \sum_{1}^{64} C_{in1} = 128\,kT \cdot C_{in1}. \tag{3.6}$$

This is accumulated at every integration step at C_1, thus assuming uncorrelated noise samples, the total noise power at the first integrator output after m integration steps is given by

$$\overline{\Delta V_{n,out1}^2} = m \cdot 128\,\frac{kT}{C_{in1}} \cdot \frac{C_{in1}^2}{C_1^2} = m \cdot 128\,kT \cdot \frac{C_{in1}}{C_1^2}. \tag{3.7}$$

This represents a worst case estimation, since the 64 array elements do not generate independent noise sources, but they are most of the time connected in parallel as two groups to the reference voltages. Therefore, for a 50% duty-cycle ΣΔM output, the capacitor array is split into two equal capacitors of size $32 \cdot C_{in1}$, hence the total noise power after the first integrator is

$$\overline{\Delta V_{n,out1,\ 50\%}^2} = m \cdot 2\ \frac{2\,kT}{32 C_{in1}} \cdot \frac{C_{in1}^2}{C_1^2} = \frac{m}{8}\ kT \cdot \frac{C_{in1}}{C_1^2}. \tag{3.8}$$

The estimated noise contribution from the first stage is added to the kT/C_{in2}

noise and is injected into the second integrator. Therefore, it is beneficial to decrease the ratio $\frac{C_{in1}}{C_1}$ with increasing reference voltage to keep a constant signal transfer function, then being able to ignore the noise contribution from the first integrator against the noise source at C_{in2}[1]. Through a similar derivation for the second integrator with a single input capacitor, the output noise power, due to sampling over C_{in2}, is found after 128 integration steps to be

$$\overline{\Delta V_{n,out2}^2} = 128 \cdot 2kT \cdot \frac{C_{in2}}{C_2^2}. \tag{3.9}$$

Therefore, the capacitor absolute sizing is directly determined by the maximum allowed noise power at the DAC output, which in turn is determined by the required SNR. Hence, with the defined capacitor ratio, picking $C_2 = 64\,\text{pF}$ leads to an output noise power of approximately $-94\,\text{dBV}$, hence a differential noise power of $-91\,\text{dBV}$, which compared to a $-6\,\text{dBV}$ signal power gives an output SNR of 85 dB.

3.5.3 Amplifier design

As discussed in section 3.4.5, the system level simulations revealed relatively relaxed speed requirements on the op-amps including low gain bandwidth product (GB) and slew rate (SR). However, the op-amps require relatively high power consumption to drive the huge load capacitors, which is required for noise performance. On the other hand, high dc-gain is required to attenuate the op-amps nonlinearities. Therefore, the op-ams are designed with a three stage positive feedback compensation shown in Fig. 3.14 [71, 79].

A PMOS input stage with increased transistor sizes was used for better low frequency noise performance. The common mode feedback circuit, which is not shown in Fig. 3.14, includes a replica of the first stage with diode connected NMOS load. The bias voltages are generated with a beta-multiplier circuitry. The first op-amp consumes 3 mA of current from a 1.1 V supply. Unusually, the current has to be increased to around three times in the second op-amp,

[1] Reducing C_{in1}/C_1 at constant signal transfer function, leads to a linear increase of the sampled noise but with square-fashion decrease in noise gain, hence a reduced output noise. Moreover, due to the parallel group connection of the C_{in1} array, and the very low C_{in1}/C_1 ratio, the total noise (from first integrator) is negligible compared to the sampled noise at the small capacitor C_{in2}

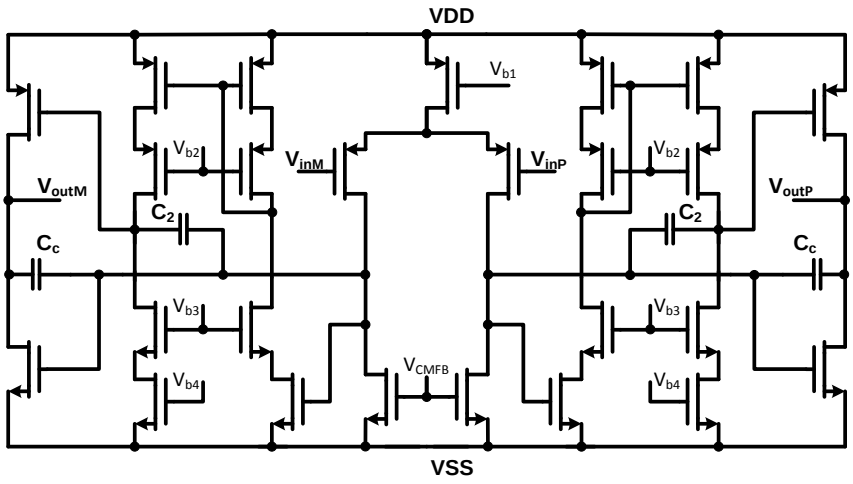


Figure 3.14: Three stage amplifier design with positive feedback compensation [62] © 2015 IEEE.

due to more stringent noise requirements on the second integrator as a result of the high pass transfer characteristic from the input of the second op-amp to the DAC output.

3.5.4 Simulation Results

The transistor level simulation of the design presents a big challenge due to the incremental nature of the internal analog voltages, occupying wide dynamic range, in addition to the mixed signal interfaces, which have to be simulated accurately to precisely estimate the DAC and ADC performance, which results in a slow simulation speed. Therefore, the design is simulated in two steps. The first step is to validate the DAC linearity, which is reflected on the ADC performance. Hence the DAC is simulated as a stand alone Nyquist-rate DAC. Then, in the second step the DAC is inserted into the 16-bit SAR ADC and simulated to validate the proposed concept. The ΣΔM is clocked at a frequency of 64 MHz, which for M = 128 leads to a DAC conversion rate of 500 kS/s.

Fig. 3.15 shows the power spectrum at the output of the DAC, after applying a digital sinusoidal signal to its input with $f_{in} = 207.5$ kHz; the noise is turned off for these simulations, in order to estimate the DAC linearity. The output spectrum presents a very good DAC linearity with SFDR > 100 dB and SNDR ≈ 94 dB, the analog signal power is around −6 dBV.

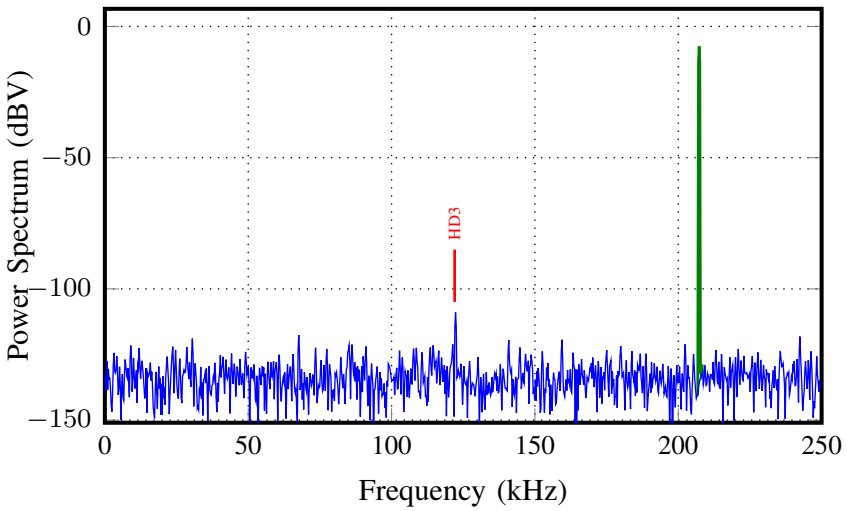


Figure 3.15: Noiseless simulation of the I-ΣΔ DAC with a sinusoidal input (2048-point fft), $f_{in} = 207.5\,\text{kHz}$, $f_{DAC} = 0.5\,\text{MS/s}$: SNDR = 94.0 dB, SFDR = 101.3 dB [62] © 2015 IEEE.

Fig. 3.16 shows the simulation results over the whole input frequency range including the SNDR and SFDR. According to Fig. 3.16, the performance does not change significantly with varying input frequencies due to the incremental (resetting) conversion. The output noise of the DAC is simulated by applying a fixed digital input and calculating the output power excluding the DC signal. Using this method, a noise power of $\approx -88\,\text{dBV}$ is found, which is 3 dB larger than the estimated noise power from section 3.5.2, which does not include op-amp noise and the non-dominant noise contribution of the first stage.

Finally the complete SAR ADC is simulated using the designed I-ΣΔ DAC on transistor level including transient noise, with Verilog-A models for the rest of the SAR loop. The SAR ADC sampling frequency is 34.18 kS/s. Fig. 3.17 shows the ADC output spectrum, for a fully-differential sinusoidal input signal with 0.7 V amplitude (−6 dBV) at 16.76 kHz. The ADC performance is dominated by DAC thermal noise, with SNDR = 83.5 dB, while the harmonic distortion is almost covered by the noise floor with SFDR > 96 dB.

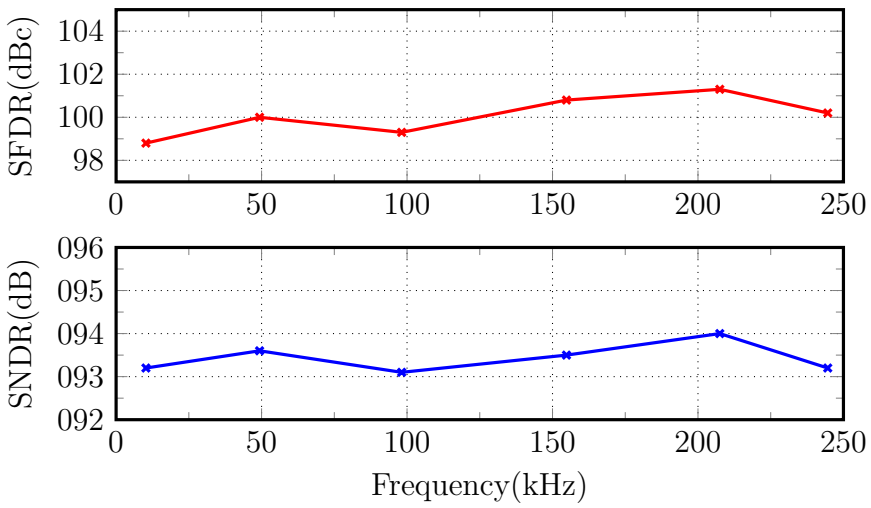


Figure 3.16: I-ΣΔ DAC performance over input frequency without thermal noise [62] © 2015 IEEE.

3.6 Design evaluation

The simulation results present a concept validation for the use of I-ΣΔ DACs in SAR ADCs to allow for a very high linearity conversion. However, the realization of the complete SAR DAC as a single I-ΣΔ DAC with optimized analog filter comes mainly with the following drawbacks:

- The I-ΣΔ DAC provides unnecessarily a full resolution output at the SAR logic rate –rather than the overall ADC Nyquist rate–, which puts stringent requirements on the power and area of the reconstruction filter. This is in contrast to an efficient SAR design, which does not require full resolution over all its steps, but only at the critical steps, thus requiring a high resolution DAC only at one or few steps during each ADC conversion cycle.

- By using the optimized filter, the DAC output is available only at a specific time step and does not smoothly settle over time; besides requiring accurate timing, this does not allow one to trade off between speed and redundancy, which is a mandatory feature in SAR to relax DAC speed and resolution, but at the same time contradicts the nature of the optimized filter.

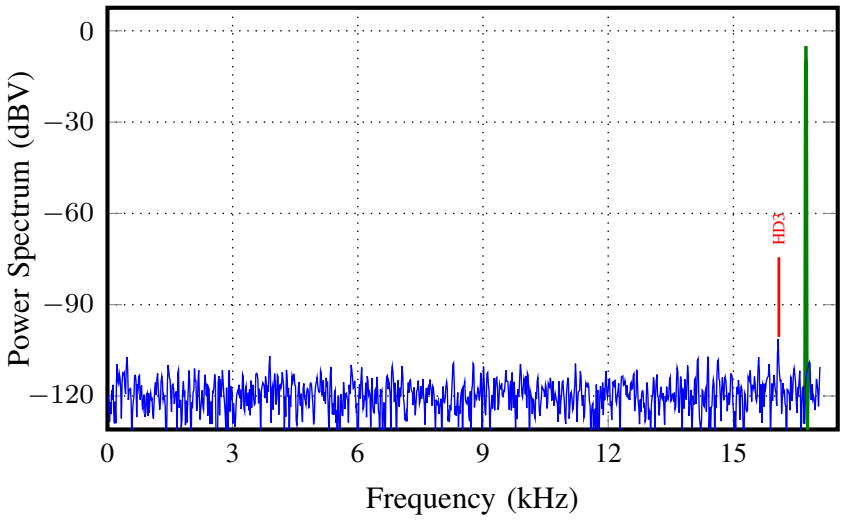


Figure 3.17: Power spectrum at the output of the SAR ADC (1024-point) for a sinusoidal input signal at 16.76 kHz frequency with a sampling frequency of 34.18 kHz including noise. SNDR = 83.5 dB, SFDR = 96.2 dB [62] © 2015 IEEE.

- To achieve good noise performance, this implementation required large capacitors for both input sampling and for a full-scale DAC and analog reconstruction filter (unlike the CDAC with shared sampling C), besides the high power required for the high-speed full-resolution DAC.
- All these together increased the implementation cost and degraded the design FOM, which made this proposal less attractive both in area and power consumption.

On the other hand, despite the degraded power FOMs, this novel design could still provide a feasible solution for specific applications, which require high resolution Nyquist conversion. The design provides intrinsic linearity for the SAR ADCs without any additional circuitry, also without the need for calibration neither in foreground nor background. This feature is not available in any Nyquist rate ADC in SoA, to the best of the author's knowledge.

Chapter 4

High linearity SAR employing hybrid DAC – Architecture

This chapter introduces a new concept to build a high linearity SAR ADC by employing I-ΣΔ DACs. The new design aims to get rid of the drawbacks accompanied the original proposal in chapter 3, without degrading the achieved linearity. Also, the complete SAR ADC architecture is discussed with several features to enable a superior ADC performance [72, 73].

4.1 Hybrid DAC for SAR ADC

The charge redistribution CDAC is a very efficient structure. It has proven a very high efficiency because of simple design and dynamic nature, which made it the dominant DAC structure for SAR ADCs with highest efficiency. In chapter 3, the introduced I-ΣΔ DAC provided a solution for high linearity that is not readily available with the plain CDAC; however, the I-ΣΔ DAC implementation drifted the design power efficiency far from expectations for highly efficient SAR ADCs.

Therefore, to benefit from the CDAC simplicity and the I-ΣΔ DAC intrinsic linearity, the proposed DAC introduces a hybrid structure of the two DACs. This allows a high resolution conversion, while depending neither on strict element matching in the CDAC nor on a demanding optimized analog filter for a full-resolution Nyquist rate I-ΣΔ DAC [62]. Fig. 4.1 shows a basic diagram of the proposed hybrid DAC, which combines two parts. The first one is an n-bit binary-weighted capacitor array switched on a common reference voltage V_{ref} to perform the coarse MSB steps of the SAR search. The second

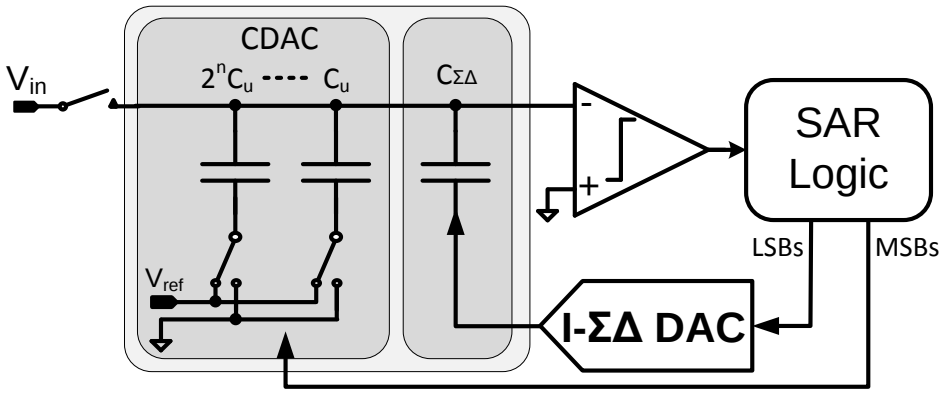


Figure 4.1: Conceptual diagram of the hybrid DAC for an N-bit SAR ADC [73] © 2018 IEEE.

part uses a single capacitor (C_{LSB}) with its bottom plate connected to the output of a ΣΔ DAC for the subsequent LSB (least significant bit) steps. These steps are achieved by applying scaled voltages at the LSB capacitor bottom plate instead of the scaled capacitors. Similar concepts were applied in former hybrid R-C DACs [21], where the LSB part was achieved with a resistive DAC connected to the bottom plate of the smallest capacitor in the CDAC; similarly, a ramp generator was used in [22]. However, the use of the proposed I-ΣΔ DAC comes with two major advantages: flexibility for bit scaling and intrinsic linearity. Together, they both allow for a remarkable extension of the DAC resolution and linearity.

The sampling capacitor in Fig. 4.1 is formed by both DAC parts, which are connected together at the top sampling plate. Therefore, equivalent to a conventional (one-step) SAR ADC, the successive search takes place via charge redistribution on the capacitors' top plates throughout the two DAC phases. Scaling $C_{\Sigma\Delta}$ in Fig. 4.1 against the CDAC unit capacitor size C_u, allows one to match the ΣΔ DAC output full scale with the CDAC LSB size, and it optionally defines an additional redundancy between the two DAC parts. The proposed architecture introduces the following advantages compared to conventional SAR ADCs [73]:

1. The sampling capacitor size, which is here shared (for sampling and DAC), can be solely chosen to fulfill kT/C noise limits, without upscaling due to C_{min} or due to matching requirements.

2. The CDAC design is highly relaxed since the sampling capacitor is split into fewer fractions, allowing much larger unit capacitor size compared to pure high resolution CDAC designs.

3. No matching critical bridge capacitor is needed, which is required for all high resolution split CDACs [19].

4. With 1 or 1.5-bit output, the ΣΔ DAC linearity is not affected by component mismatch. Thus, calibration is only needed for the coarse CDAC array, and the mismatch between the two parts represents only a gain error on the ADC fine bits, which is easily calibrated.

5. The ΣΔ DAC benefits from a noise-free scaling through ($C_{\Sigma\Delta}$ / C_{total}); therefore, also its own output can have rather coarse resolution, which is not required to satisfy the noise performance corresponding to the full ADC resolution.

6. The ΣΔ DAC input is defined by the digital word from the SAR logic; this introduces great flexibility in defining the SAR search steps and/or adding selective redundancy, while these steps are conventionally fixed and hard coded during the CDAC design.

7. Also, the ADC resolution is digitally defined and traded off for speed, where the ΣΔ DAC allows a reduced or extended resolution by readjustments of the SAR steps and number of ΣΔM averaged samples.

8. The self calibration of the CDAC using the ΣΔ DAC, as will be detailed in section 5, allows linearization beyond the nominal resolution of the SAR ADC.

In summary, the proposed DAC receives the advantages of the two DAC structures, including CDAC simplicity and cost efficiency, in addition to the ΣΔ DAC linearity and digital reconfigurability. It further introduces advantages by co-operation of the two DACs for calibration and redundancy. On the other hand, the design avoids the drawbacks of the two DACs, including high resolution parasitic critical CDAC in addition to high cost and limited range from a full resolution ΣΔ DAC.

4.2 High linearity SAR with hybrid DAC

Fig. 4.2 shows a block diagram of the hybrid capacitive and incremental ΣΔ DAC within the proposed SAR ADC architecture. The target nominal resolution is 16 bit. Several features are introduced into the ADC to improve its performance and efficiency, which push the design into higher effective resolutions: dual supply is used by sampling in the 2.5 V domain, whereas the backend runs from 1.1 V. A dual comparator structure is employed for the coarse and fine phase. A mixed switching scheme is used in the both phases. These are outlined next.

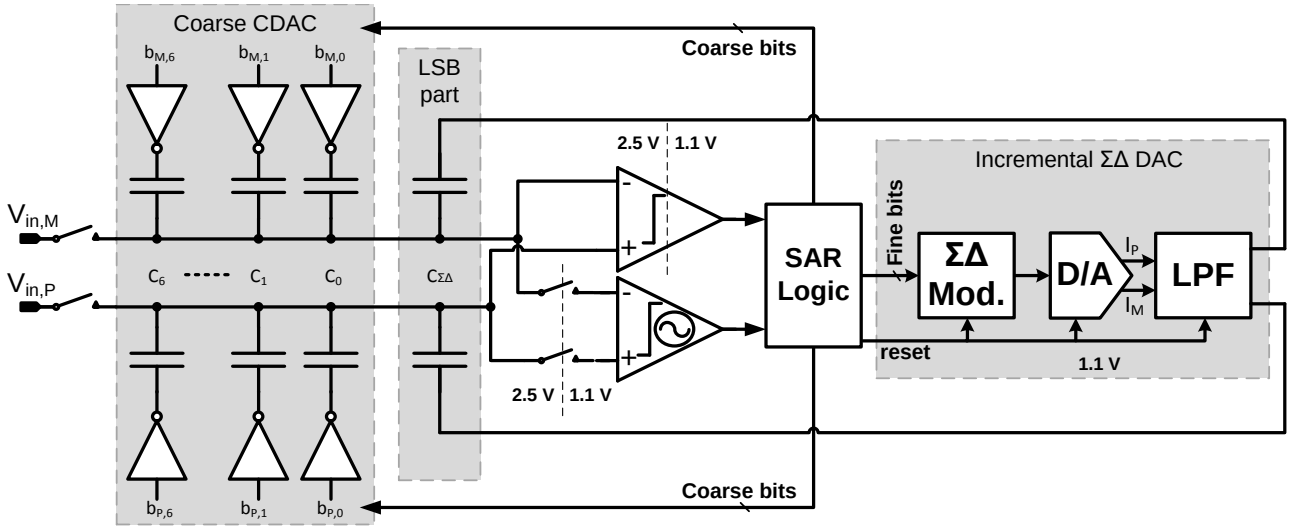


Figure 4.2: I-ΣΔ DAC enhanced SAR ADC architecture [73] © 2018 IEEE.

4.2.1 Mixed monotonic and differential conversion

The CDAC features a top-plate sampling directly at the coarse comparator inputs, which allows for a sign detection after sampling and before DAC switching. This, together with a monotonically switching CDAC, halves the required DAC unit elements without the need for a second reference in the CDAC [8], as outlined in section 2.5.1. The monotonic switching scheme is chosen here because it provides the most power and area saving at single voltage reference, without complicated switching logic and at zero reset energy, as shown in Table 2.1.

The monotonic switching scheme is though only used for the coarse CDAC, while the following LSBs are differentially applied by the ΣΔ DAC; this avoids any even order harmonics observed by a purely monotonic switching DAC [8], while the monotonic switching scheme advantageously reduces the common mode voltage from 2.5 V domain into the 1.1 V domain during the coarse phase of the SAR search. Thereby, the hybrid DAC benefits from the signal-independent common mode shift by the monotonic switching scheme, without suffering from distortion due to the varying comparator offset[1], by adding a redundancy range after the coarse phase (chapter 5). Fig. 4.3 shows the transient response of the SAR ADC comparator input voltages in Fig. 4.2, exposing the two switching phases within one conversion cycle after input sampling.

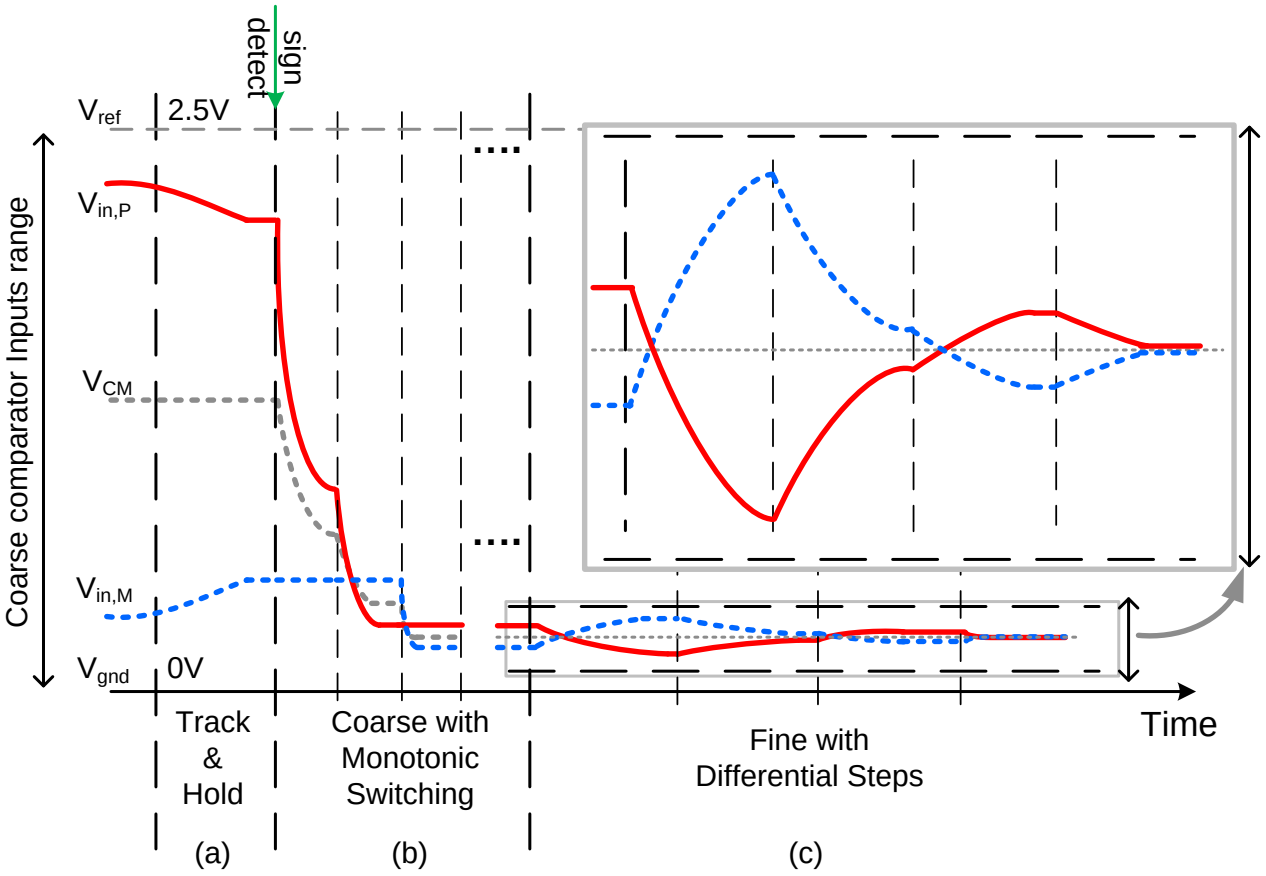


Figure 4.3: SAR ADC transient response at comparator inputs during: (a) sampling, (b) CDAC switching and (c) fine phases, modified from [73] © 2018 IEEE.

[1] In conventional monotonic switching scheme, despite the signal independent CM changes, a redundancy-free SAR suffers from varying CM; because DAC errors would be signal dependent and happen only when the input is close to the varying comparator offset.

At which position the nominal ADC resolution is split between the two DAC parts represents a design choice, which allows one to balance the complexity of the CDAC against the speed limitation at increased resolution in the ΣΔ DAC, which obviously needs oversampling for operation. The CDAC is not required to satisfy the ADC full resolution but only its own coarse resolution. Therefore, increasing the CDAC resolution moves it from a rather simple layout and design with advantageous matching due to large unit devices, gradually into a more complex design with significant overhead and critical matching. On the other hand, a higher resolution in the ΣΔ DAC requires longer conversion cycles and stronger filtering after the ΣΔ DAC, both translating into slower conversion and increased power. In this design, a simple 7-bit CDAC implementation is used (whose layout could be almost fully automated), which leaves 9 bits plus redundancy for the ΣΔ DAC.

4.2.2 Dual comparator structure

Fully dynamic comparators have been used for low to moderate resolutions achieving remarkably low power levels [16], and combined with comparator noise averaging, they showed further resolution improvement [32, 35]. On the other hand, oscillator-based comparators like the edge-pursuit [40] and eye-opening comparators [39] introduced a more efficient comparator power scaling with reduced overdrive voltage for high resolution decisions. However, these oscillator based designs suffered from high sensitivity to common mode (CM) variations, which is especially critical during the monotonic switching in Fig 4.3, where the CM voltage significantly changes. Therefore, a dual-comparator structure is implemented in this design as shown in Fig. 4.2 [74].

This proposal includes a fully-dynamic comparator for the initial coarse CDAC phase with monotonic switching, where the CM varies significantly but monotonically, which is tolerated by the PMOS input dynamic comparator. Subsequently, an eye-opening comparator is used for the later, noise-critical comparisons. It works with differential input steps, a small input range and a fixed CM voltage as shown in Fig. 4.3, which when combined, significantly relaxes the LSB decisions. This allows for efficient designs of the two comparators. In the coarse phase, errors within the coarse resolution are tolerated, whether they originate from coarse CDAC or from coarse comparator, which

allows for a cost efficient dynamic comparator design. On the other hand, the critical fine comparator design is eased by limiting the input range and common mode variation to the small fine range with the I-ΣΔ DAC. Another advantage of the hybrid comparator structure is the reduced nonlinearity of comparator input parasitics. Especially for high resolution implementations, the nonlinear parasitic capacitors at comparator inputs cause input sampling distortion; while large input devices are usually required for low noise operation. Here, during the input sampling, only the small sized coarse comparator is connected, hence a minimal non-linear capacitor is present. While the low noise fine comparator is only connected during the limited-voltage-range fine steps, hence it contributes a minimal non-linearity.

However, the major disadvantage of the dual comparator structure is comparator offset mismatch. This is either corrected by the fine range, combined with coarse conversion errors, or when it exceeds the correction (redundancy) range, it is corrected in the background as discussed in detail in chapter 5.

4.2.3 The I-ΣΔ DAC

The DAC in Fig. 4.2 consists of the 7-bit capacitor array and an I-ΣΔ DAC. The third-order digital ΣΔ modulator truncates its output by a 1.5-bit quantizer and shapes the quantization noise to high frequencies. The 1.5-bit quantization guarantees an intrinsic linearity without dependence on element matching in the D/A interface following the modulator in Fig. 4.2. The last block of the ΣΔ DAC is an analog low-pass filter, which suppresses the shaped noise from the modulator and drives the bottom plate of the LSB capacitor ($C_{\Sigma\Delta}$) in Fig. 4.2. The ADC nominal resolution is digitally determined by the SAR logic and is only limited by the noise suppression in the analog filter, while featuring a reconfigurable ΣΔ modulator.

To prevent any memory effect in the ADC and ensure a Nyquist rate operation with a sample-to-sample input output conversion, the ΣΔ DAC is reset after every single SAR conversion, thus making the ΣΔ DAC operate incrementally. The ΣΔ DAC could also be reset after every fine bit decision during a SAR conversion, but this turned out to be disadvantageous: for a single conversion, the memory of the ΣΔ DAC successively tracks the actual input value, and does not lead to distortion but to an even faster settling, whereas

multiple resets would need the new value to be built up from zero, which would require more settling time. Therefore, the I-ΣΔ DAC incorporated in the proposed hybrid DAC differs majorly from the stand alone I-ΣΔ DAC originally proposed in chapter 3. It is not required to provide a Nyquist rate conversion at the SAR logic rate, it receives the reset signal only once during one ADC conversion instead of repeated reset pulses with each SAR logic output update, and it only provides a coarse resolution since it shares a partial resolution with the CDAC. Thanks to downscaling in the capacitor array, the coarse resolution provided by the I-ΣΔ DAC is translated into the fine resolution (LSBs) of the SAR ADC.

The analog reconstruction filter does not implement an optimal filter response as proposed in chapter 3, which provides a full-resolution DAC output that is valid only at a fixed point in time. Instead, this proposal uses a low-pass analog reconstruction filter after the free-running ΣΔM (w/o reset during one ADC conversion cycle). Hence, instead of the 3rd order CoI structure proposed in chapter 3 to approximate the optimal filter response, this DAC implements a low-pass filter of the same order as the ΣΔM, which smooths the ΣΔM output over time. This allows for an efficient implementation in an asynchronous SAR loop, which makes use of redundancy for decreased power and/or increased conversion speed.

4.2.4 Input sampling and dual supply operation

A major drawback of advanced scaled CMOS technologies is the reduced supply voltage. Although this is beneficial for digital circuitry, it strongly limits the analog processing capabilities; for instance, the input range is limited to a certain subrange within the supply voltage, which limits the dynamic range of the ADC. However, while the analog core processing is limited to the scaled supply, a higher input-output (IO) supply is usually used to interface the design off-chip with other circuitry. Although it is not beneficial to perform the analog processing on the high IO supply, using this supply for extended input range is of significant advantage, therefore this is applied in many high resolution Nyquist ADCs [24, 47, 49].

Therefore, a hybrid supply is used in this design; it allows to benefit from the two supply voltages. The input sampler, the 7-bit CDAC and the coarse

comparator operate at 2.5 V in Fig. 4.2, which allows one to increase the input full scale signal, which is sampled at the higher supply, and therefore reduces the required – noise limited – sampling capacitance. The fine comparator together with the $\Sigma\Delta$ DAC and the logic circuits operate at 1.1 V, which reduces their power consumption and implementation area by fully benefiting from transistor scaling.

Chapter 5

SAR error recovery: redundancy and calibration

High linearity A/D conversion requires immunity to conversion errors or circuit techniques to avoid and/or correct for these errors. In this chapter, the used SAR error recovery concept is briefly introduced, and different tools for error recovery including redundancy and self calibration are developed for the high linearity SAR ADC architecture proposed in chapter 4.

5.1 Conversion errors in SAR ADC

An error-free conversion in the SAR ADC requires two conditions at the end of conversion: a DAC output settled close (within LSB size) to the sampled analog input, or equivalently a zero (or $<$ LSB) comparator input[1], and correct digital representations of the DAC analog steps. Figure 5.1 (a) shows an exemplary correct DAC settling in a 4-bit SAR ADC.

Two main non-idealities prevent these conditions and hence an error-free conversion: The first non-ideality is a settling speed error (or non-complete settling) due to slow DAC output settling, which potentially leads to non-settled (to zero) comparator input, thus wrong decisions and digital outputs, as in the example of Fig. 5.1 (b). The second non-ideality is the DAC element mismatch, which is due to mismatch between DAC steps and their nominal digital representations. In Fig. 5.2, two settling examples for two inputs are shown; both include mismatched MSB elements with about -2·LSB and +2·LSB in

[1]This is valid for a comparator with zero offset, otherwise the comparator input settles to the comparator offset at the end of a correct conversion.

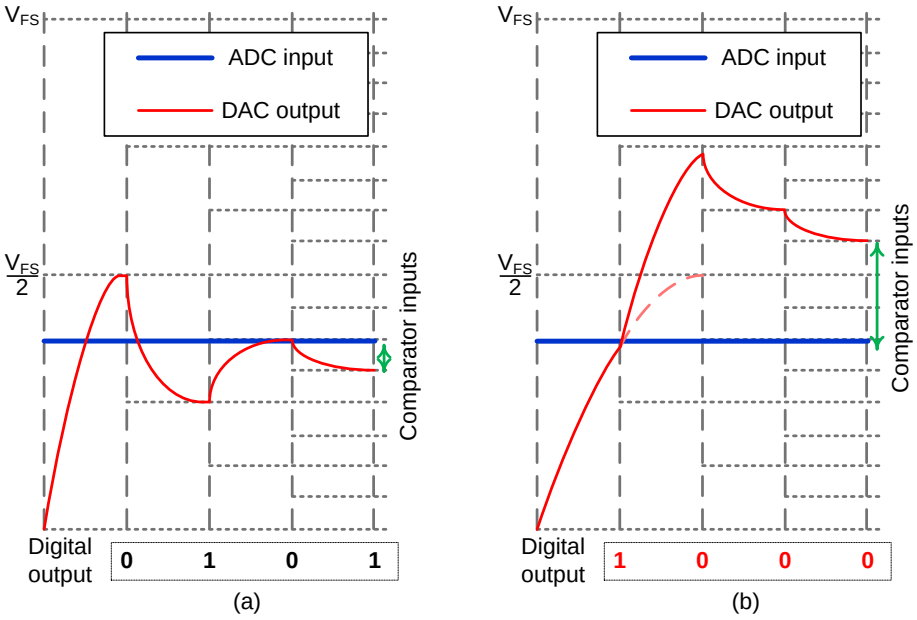


Figure 5.1: DAC settling in a 4-bit SAR ADC: (a) ideal, (b) with non-complete settling.

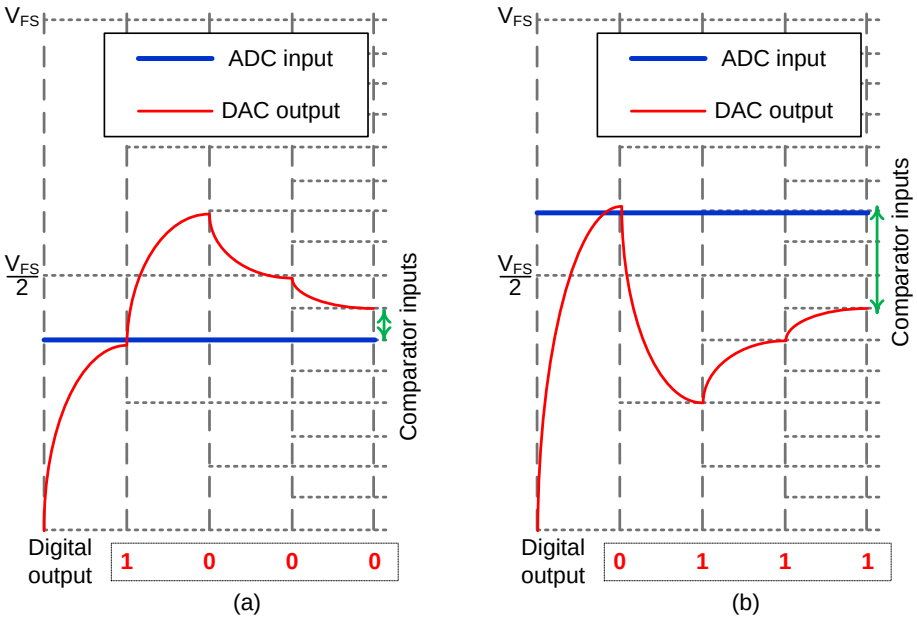


Figure 5.2: DAC settling in a 4-bit SAR ADC, with mismatched MSB element: (a) MSB = MSB_{ideal}-2 LSB, (b) MSB = MSB_{ideal}+2 LSB.

Figures 5.2 (a) and (b) respectively. The mismatch in Fig. 5.2 (a) results in a correct DAC settling but wrong digital representation, while in Fig. 5.2 (b) the conversion ended in wrong settling and wrong output.

5.2 Redundancy

5.2.1 Concept and usage

In a conventional SAR ADC the DAC steps are binary weighted, and the DAC output cannot return to a previous value during one conversion cycle. Therefore, an error during previous steps cannot be corrected by the later steps. This is because the size of any DAC step is larger than the sum of all later steps. In order to allow for later correction after one DAC step, one has to add redundancy step(s) or a redundancy range after this step, which makes the sum of the later steps larger than the actual step. One way to add redundancy is to repeat some DAC step(s), which requires the implementation of additional step(s), e.g. multiple elements with the same size.

The two examples in Figures 5.1 (b) and 5.2 (b) include errors at the MSB step, which ended in a final settling error of about 2·LSB (of the ideal value within input±LSB). In order to handle these errors, a redundancy of 2·LSB is added in Figures 5.3 (a) and (b) respectively. In both cases, correct settling is achieved at the conversion end by redundancy, and by knowing that the redundant step is of 2·LSB size, the 5-bit digital outputs can be easily corrected to get the correct 4-bit output. Enough redundancy can completely cure DAC settling errors, however, in the presence of mismatch, as in Fig. 5.2 (a), the redundancy cannot correct for output errors originating from the mismatch between DAC analog scales and digital nominal bit weights, i.e. non-linearity. Nonetheless, in the presence of mismatch, redundancy is necessary to ensure a correct DAC settling, as in the example of Fig. 5.3 (b), where the digital output can be correctly obtained (after including redundancy), because the mismatched element is not used in the final DAC output.

Besides repeated steps, redundancy can be added by changing individual step sizes or by using sub-2 radix, for example using a 1.9 radix, which means that N SAR steps are scaled as $[1/1.9^i : i = 1 : N]$ relative to full scale. Under

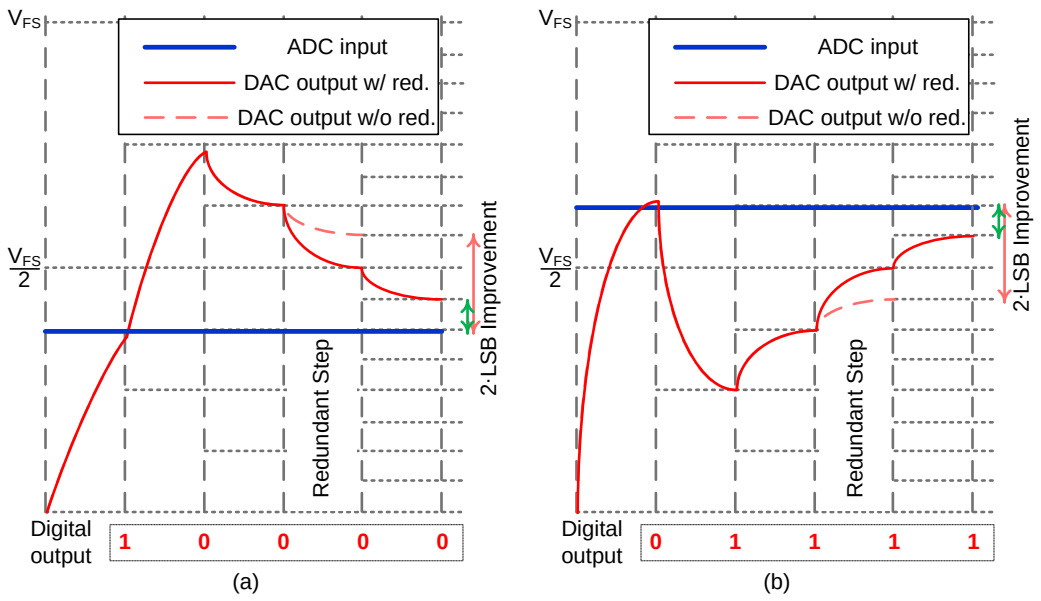


Figure 5.3: Redundant DAC settling in a 4-bit SAR ADC, with (a) non-complete settling, (b) mismatched MSB.

redundant DAC steps, additional SAR steps are required compared to the non-redundant case, in order to reach the same final precision (LSB sized final step). Therefore, also the redundant digital output uses a longer bit width, hence a correction logic is required.

5.2.2 Redundancy for hybrid SAR

Conventionally, redundancy is used to relax the DAC settling in SAR ADCs at high sampling frequencies. However, although the proposed ADC targets high resolution at relatively low conversion rates, redundancy within the SAR steps is essential for the proposed design. Three main aspects highlight the importance of the applied redundancy.

- **Coarse conversion errors** are allowed up to the coarse (CDAC) resolution. Therefore, mismatch in the CDAC and/or erroneous decisions in the coarse comparator may also result in non-complete conversion during the fine phase (saturated $\Sigma\Delta$ DAC output), which can be avoided by redundancy covering the maximum mismatch of the coarse CDAC and/or the inaccuracy of the coarse conversion.

- **Offset mismatch:** Due to the dual comparator structure, there will be an unavoidable offset mismatch between the two comparators, which may prevent a complete settling. Therefore, an appropriate redundancy also allows recovery of the offset mismatch at the hand-over point between the two comparators (coarse to fine phase).
- **DAC settling:** Within the fine switching phase using the I-ΣΔ DAC, redundancy free steps would require the analog filter to settle to full resolution at every DAC step, while with a small additional redundancy, the DAC settling is relaxed; hence its speed and power efficiency are improved.

Consequently, a redundancy bit is added at the beginning of the fine phase, which allows to recover all errors below the 7-bit CDAC accuracy in the coarse phase (offset, mismatch and erroneous decisions). Furthermore, sub-binary steps with 1.8 radix are used for the fine conversion with the ΣΔ DAC, as illustrated in the SAR transient response in Fig. 5.4. Advantageously, in the proposed architecture, the ΣΔ DAC redundancy can be digitally reconfigured and optimized; this is further explained with the implementation details in section 6.2.

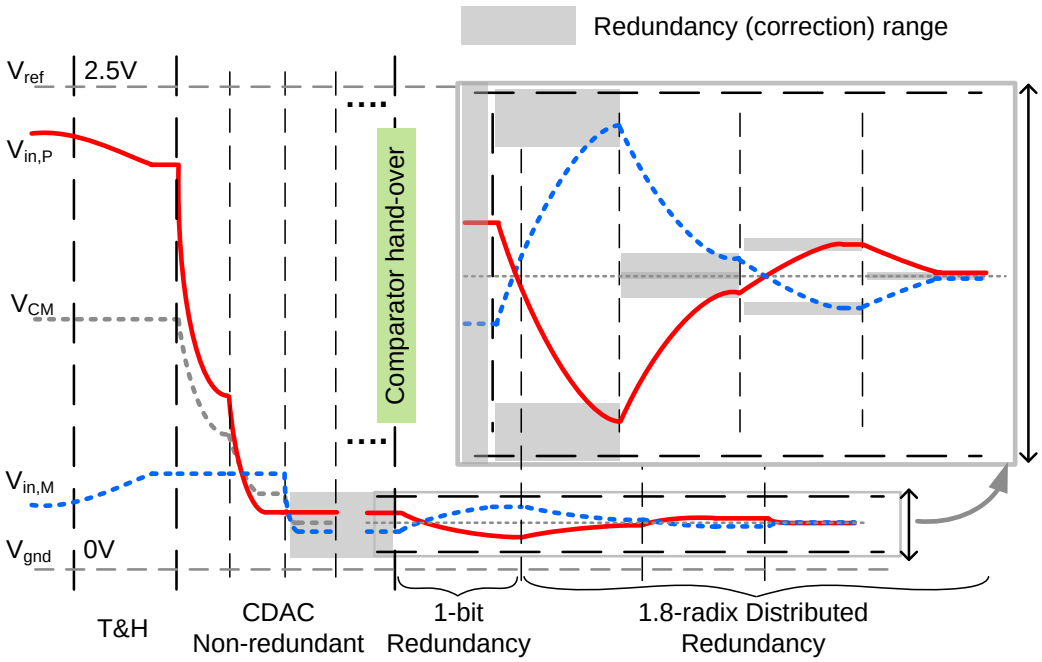


Figure 5.4: Redundancy ranges over SAR ADC transient response, modified from [73] © 2018 IEEE.

5.3 Self calibration

Calibration in SAR ADCs involves several procedures to handle manufacturing non-idealities and drifts of the nominal design specs. At high resolutions, the most common calibration techniques deal with CDAC mismatch by providing analog compensation for correct DAC settling and digital compensation for correct output representation. Two more procedures are relevant for the proposed hybrid ADC: comparator mismatch calibration and correction of the DAC scale mismatch between fine and coarse DACs. An efficient design allows for self calibration using the available analog components in the ADC, without a need for additional blocks or external calibration tools.

5.3.1 Calibration concept

5.3.1.1 CDAC linearity

The binary-weighted coarse CDAC will have a manufacturing related mismatch, which needs calibration. Thanks to the applied redundancy, a correct DAC settling is guaranteed without any analog calibration in background, even at the presence of element mismatch, if the CDAC mismatch is less than the redundancy range, equivalently, if CDAC linearity is better than its coarse resolution (7-bit). However, due to the CDAC mismatch, the coarse part of the digital output (resulting at the coarse CDAC phase) is potentially erroneous due to the differences between the actual mismatched capacitor sizes and their nominal values assumed by the digital logic. Therefore, in order to achieve an error free conversion, the actual sizes of the capacitors in the CDAC are estimated with at least the full ADC resolution, in order to digitally correct them. In the proposed hybrid DAC, the I-$\Sigma\Delta$ DAC is a suitable and efficient measurement tool for CDAC calibration. This is because the I-$\Sigma\Delta$ DAC is connected through the LSB capacitor to the same sampling node at the comparator input as all the CDAC capacitors, and it additionally features the full resolution of the SAR ADC, when handling a small input at the sampling node.

5.3.1.2 CDAC scale mismatch

The full scale range of the I-ΣΔ DAC has to be matched to the LSB size of the CDAC (considering redundancy). Otherwise, a gain error between the coarse and the fine digital outputs would appear. Therefore, besides measuring the mismatch on the individual CDAC capacitors, a gain correction factor is estimated.

5.3.1.3 Hybrid comparator offset

A large offset mismatch between the coarse and the fine comparator could cause the voltage range, into which the coarse conversion phase steers the CDAC voltages, to be outside the conversion range of the fine DAC as indicated in Fig. 5.4. An offset mismatch larger than the maximum input range of the fine DAC must be avoided, as illustrated in Fig. 5.5.

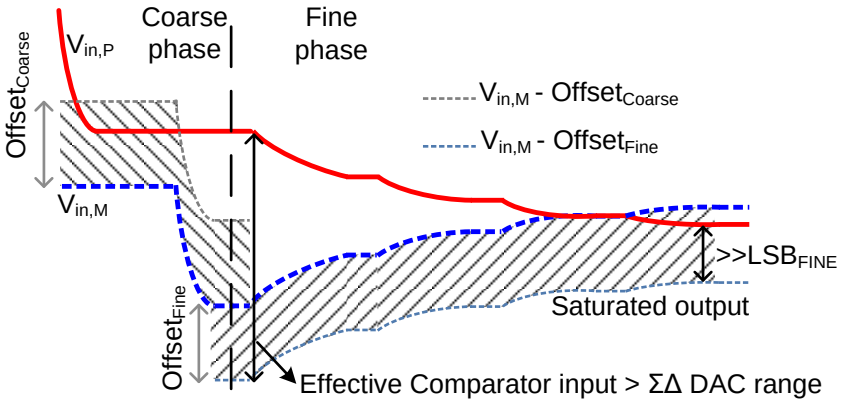


Figure 5.5: Saturated DAC output due to large comparator offset mismatch [73] © 2018 IEEE.

Thereby, the two comparator offsets are illustrated by voltage shifts on the negative comparator input $V_{in,M}$, to represent the effective input to an offset-free comparator. In Fig. 5.5, the two comparators have opposite sign offsets (negative for coarse and positive for fine comparator); due to the high offset mismatch, the effective comparator input at the hand-over point exceeds the ΣΔ DAC range, hence it leads to a saturated DAC output to the conversion end.

Since designing the redundancy for the worst case offset mismatch would lead to extended SAR conversion time, this was avoided by using an additional low resolution CDAC for offset compensation.

5.3.2 Calibration procedure

5.3.2.1 CDAC error estimation

The CDAC error estimation is based on the translation of the mismatch error of an individual capacitor C_i in the CDAC array into an equivalent voltage $V_{\mathrm{m,Ci}}$ [52, 53]. This voltage is digitized using the SAR ADC while operating only the fine loop, which includes the SAR logic, I-ΣΔ DAC and fine comparator. The equivalent mismatch voltage $V_{\mathrm{m,Ci}}$ is obtained by sampling a zero differential voltage at the CDAC, cf. Fig. 5.6 (1,2), then flipping the reference voltage connection at the bottom plate of the actual capacitor C_i under mismatch measurement, Fig. 5.6 (3). Based on charge redistribution, the voltage V_{Ci} on

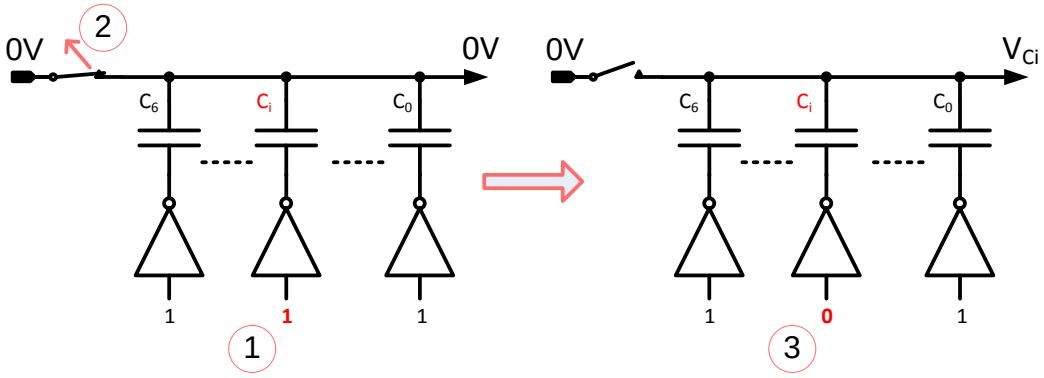


Figure 5.6: CDAC error estimation by charge redistribution

the CDAC top-plate (which is the comparator input), represents the actual weight of C_i ($\mathrm{C}_i/\mathrm{C}_{total}$), thus the digital correction value can be obtained by digitizing V_{Ci} through the fine loop, as applied in 5.3.2.2.

So as not to saturate the I-ΣΔ DAC output with the total capacitance estimation, which is represented by V_{Ci} in Fig. 5.6, only the capacitor mismatch is measured instead of the total capacitance. This is achieved by inversely switching an equally sized capacitance, which is in fact the group of all capacitors in the CDAC being smaller than C_i under investigation. To perform this, the CDAC binary array is completed with an additional reference capacitor C_r, which is of equal size to the CDAC unit capacitor, as shown in Fig. 5.7.

5.3.2.2 CDAC LSB calibration

The calibration starts with the CDAC LSB C_0, which is switched together with C_r as illustrated in Fig. 5.7; C_r is initially considered to be mismatch free. Firstly, a zero sampling takes place with C_0 and C_r having opposite control signals, c.f. Fig. 5.7 (a). After sampling, the switching controls for C_0 and C_r are swapped, which generates the mismatch voltage $V_{\mathrm{m,C0}}$, c.f. Fig. 5.7 (b). $V_{\mathrm{m,C0}}$ is calculated based on charge conservation as in (5.1), where C_{total} is the sum of all capacitors within the same side of the CDAC (the positive side in Fig. 5.7), while C is the ideal value of C_0, and $C_{0,Mism}$ is the absolute mismatch of C_0.

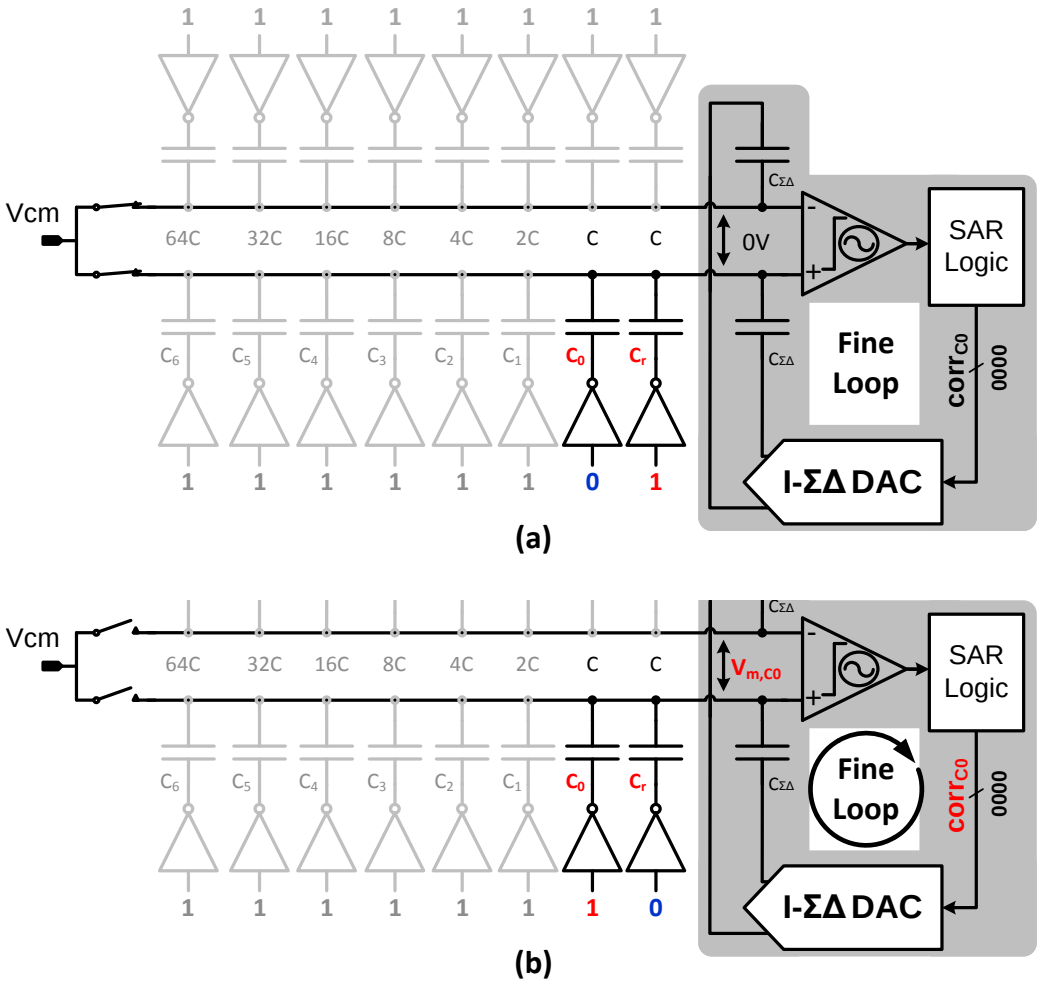


Figure 5.7: CDAC LSB mismatch estimation using I-ΣΔ DAC.

$$V_{m,C0} = \frac{C_0 - C_r}{C_{total}} \cdot V_{ref} \ , \quad C_0 = C + C_{0,Mism} \ , \quad C_r = C \tag{5.1}$$

$$V_{m,C0} = \frac{C_{0,Mism}}{C_{total}} \cdot V_{ref} \tag{5.2}$$

After the charge redistribution, the SAR operates with the fine loop (no change on the CDAC but only the I-ΣΔ DAC active) to convert $V_{\mathrm{m,C0}}$ to a digital word $\mathrm{D_{corr,0}}$, which is the digital correction value for C_0.

5.3.2.3 CDAC MSBs calibration

Calibration proceeds to the second LSB C_1 with similar procedure, but swapping the switching controls of C_1 with the group of C_0 and C_r, which leads to the mismatch voltage related to capacitor C_1:

$$V_{m,C1_0} = \frac{C_1 - (C_0 + C_r)}{C_{total}} \cdot V_{ref} \ , \quad C_1 = 2C + C_{1,Mism} \tag{5.3}$$

$$V_{m,C1_0} = \frac{C_{1,Mism} - C_{0,Mism}}{C_{total}} \cdot V_{ref} = V_{m,C1} - V_{m,C0} \ , \quad V_{m,C1} = \frac{C_{1,Mism}}{C_{total}} \cdot V_{ref} \tag{5.4}$$

As shown in (5.4), the voltage $V_{\mathrm{m,C1_0}}$ depends on the difference of the mismatches of C_1 and C_0. Therefore after digitizing $V_{\mathrm{m,C1_0}}$ with the fine loop, the result, which additionally includes the mismatch of C_0, is added to $\mathrm{D_{corr,0}}$ in order to obtain $\mathrm{D_{corr,1}}$, the digital correction for C_1. The same procedure is carried out to calibrate all CDAC capacitors up to the MSB capacitor C_6, as illustrated in Fig. 5.8. Thereby, after digitizing the mismatch voltage $V_{\mathrm{m,C6_0}}$, which includes the mismatch from all capacitors C_6 to C_0, into $D_{corr,6_0}$, the digital correction value of C_6 is given by

$$D_{corr,6} = D_{corr,6_0} + D_{corr,5} + D_{corr,4} + .. + D_{corr,0} \tag{5.5}$$

Here, $D_{\mathrm{corr,i}}$ are the respective digital correction words for the capacitors $C_i \,|\, i = 0..6$.

5.3.2.4 Mismatch of C_r

Since C_r represents the calibration reference, upon which $C_0 - C_6$ are calibrated, a mismatch in C_r does not affect the linearity of the CDAC. But

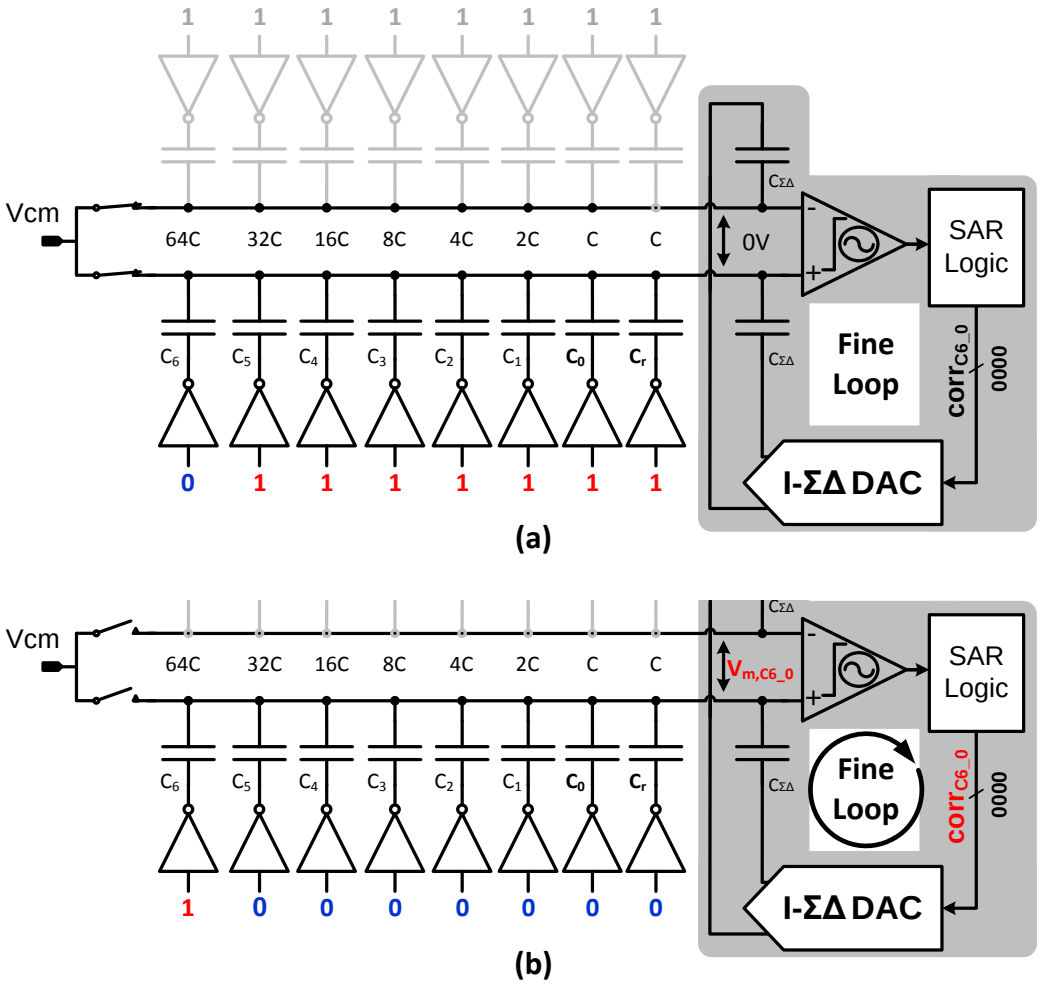


Figure 5.8: CDAC MSB mismatch estimation using I-ΣΔ DAC.

a mismatch of C_r still leads to a gain error between the CDAC and the I-ΣΔ DAC. Therefore, the actual digital representation of C_r is estimated using the same calibration concept, but without swapped switching with another CDAC capacitor. Therewith, a digital representation of the actual C_r is obtained relative to the I-ΣΔ DAC, which matches the gain error between the two DAC parts.

5.3.2.5 ADC output correction

Identical to the explanation above and as indicated in Figures 5.7 and 5.8 for the positive CDAC, the digital correction values are estimated for the negative

CDAC. This whole calibration is run once at startup, when the estimated digital correction values are stored, while the stored correction values are then operated continuously on the SAR ADC output. The output correction is performed by an arithmetic addition of the appropriate digital correction values to the ADC digital output.

5.3.2.6 Coarse offset compensation

A 4-bit capacitor array has been added to coarsely compensate for worst case offset mismatch. Once at startup, the two comparator offsets are estimated by the additional CDAC; during ADC operation, the two estimated offsets are compensated in the background during each of the two phases (coarse & fine) accordingly. In order not to change the common mode, the compensation DAC is switched differentially; also, due to its tiny size, its power consumption is negligible. An important aspect for using this compensation is that it neither requires calibration nor does it need to match the CDAC capacitors, which all makes it a quite affordable solution to safeguard excessive offset mismatch. For varying offsets over time and temperature changes, a background estimation is potentially required; however, offset changes within the redundancy range are tolerable and do not affect the ADC operation. Nonetheless, offset background estimation can be performed by allocating one cycle within the SAR steps to update the estimated offsets, which would lead only to negligible increase of the ADC conversion time.

5.3.3 Calibration beyond ADC resolution

Although the self calibration is achieved at almost no additional hardware cost, a usual drawback of it is the limited calibration resolution. This is because the calibration is limited to the resolution of the ADC itself, which is the measurement tool to estimate the non-linearity. However, the use of the I-$\Sigma\Delta$ DAC avoids this drawback and introduces an advantage for the calibration performance, which allows it to be performed beyond the ADC resolution. First, the calibration nominal resolution is improved by reducing the SAR LSB fine step below the one used for ADC normal operation, together with additional SAR steps, thanks to relaxed timing during the startup calibration.

This is easily achieved because the LSB size is digitally defined within the digital input of the I-ΣΔ DAC. Also, the I-ΣΔ modulator performance benefits from relaxed timing.

However, with the aforementioned modifications, the calibration output would be limited by random fluctuation due to noise. Nevertheless, this fluctuation together with (white) sampling noise is averaged out by repeated measurements during calibration at startup. Finally, the influence of the low-frequency noise within the SAR loop (mainly in the comparator) and the sampling distortion is also reduced. This is achieved by repeating the conversion in one calibration step, first on the zero sampled input, then after CDAC switching (including mismatch effect as described in section 5.3.2), and subtracting the two. This attenuates the low-frequency noise in a similar fashion to correlated double sampling (CDS [75]). Together, this allows one to perform the calibration beyond the SAR ADC resolution with no additional analog components.

Chapter 6

SAR ADC circuit implementation

This chapter presents a complete circuit implementation for the high linearity SAR ADC, with respect to the proposed hybrid architecture in chapter 4. In order to validate the proposed SAR ADC concept using a recent CMOS technology, the circuit implementation is based on TSMC 40 nm technology. The design specifications include a nominal resolution of 16 bit at a conversion speed of 80 kS/s, which enables potential ADC application in multiplexed sensor arrays, e.g. with tens of sensors at individual bandwidths of about 1 kHz.

6.1 Input sampling and capacitor array

The ADC features top-plate sampling of the analog inputs using a pair of bootstrap switches operating at 2.5 V. The sampling switches receive the sampling clock after buffering and boosting it close to double the supply voltage. Each switch is connected to one of the two common top-plates of the CDAC arrays, which are also connected to the two comparator inputs, respectively, as shown in Fig. 6.1. Due to the hybrid DAC structure, there is basically no matching related requirement on the unit capacitor size, as it forms only a 7-bit array. Therefore, the sampling capacitance (C_S) is solely sized for a 16-bit kT/C noise level, which yields $C_S = 16\,\text{pF}$ as the sampling capacitance for each CDAC side for an approximate $4\,V_{p-p}$ differential input voltage.

6.1.1 Bootstrap switch

A high linearity sampling is mandatory in front of the high linearity ADC. In order to get-rid of (or attenuate) the nonlinearity of the MOS switch, a

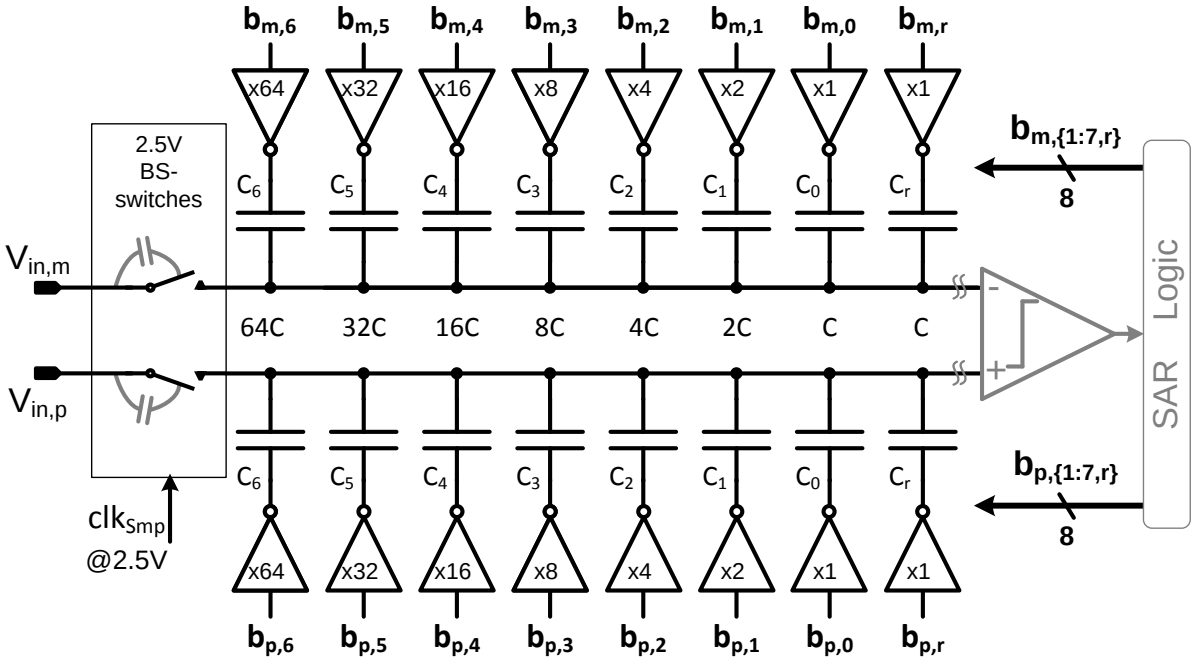


Figure 6.1: The 7-bit CDAC with input sampling

bootstrap-switch is implemented in this design similar to [76]. The switch circuit is shown in Fig. 6.2: to reduce the nonlinearity of the sampling switch (M_0 in Fig. 6.2), an almost fixed control voltage is applied between the switch gate and source terminals during the conduction (ON) phase, despite the varying input at source (T1). This is done using the floating capacitor C_{BS}, which is precharged to VDD.

To guarantee a fast and complete charging of C_{BS} a clock boosting circuit is implemented (M_1, M_2, C_1, C_2), which boosts the sampling clock close to double the supply. The switches M_7 and M_8 connect/break the connection between the floating capacitor and M_0 during the ON/OFF phases respectively. For a S&H (or a T&H) switch, the hold (OFF) edge defines the sampling time instance, therefore the speed of this edge is critical for sampling linearity. The transistors M_9, M_{10} feature increased sizes (width) for lower on-resistances (R_{ON}) and faster hold edges. The charges on capacitor C_{BS} are redistributed and shared during the ON phase with the switch parasitics dominated by the main switch M_0, which features increased size for faster sampling settling. Therefore, in order not to degrade the switch control voltage (V_{GS} of M_0),

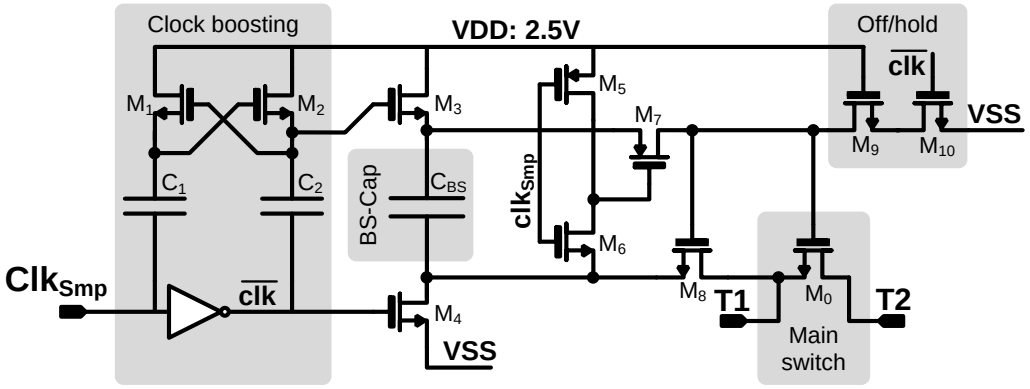


Figure 6.2: The bootstrap switch circuit, derived from [76].

C_{BS} has to be much larger than the expected parasitics. $C_{BS} = 200\,fF$ is used in this design.

6.1.2 CDAC array

The low linearity requirements, the relaxed switching speed of the CDAC and the added redundancy at the end of the coarse conversion phase allow for a standard binary-weighted implementation of the C-array, without a need for extra redundant steps within the CDAC and/or a non-binary array, which would lead to more complex design. The CDAC is implemented using MOM (metal-oxide-metal) capacitors with a unit capacitance $C = 127.6\,fF$ ($\approx C_S/128$). This comparably large unit capacitor highly relaxes the CDAC layout. To maximally reduce the layout-induced CDAC mismatch effect, elements of the CDAC array are implemented using a unit element, which includes a unit capacitor, a unit switch-pair and a driving buffer, as in Fig. 6.3. This enables binary weighting not only on the capacitors but also on their driving strength through the "cap-switch-buffer" unit. This is easily doable by the relaxed CDAC unit-element size.

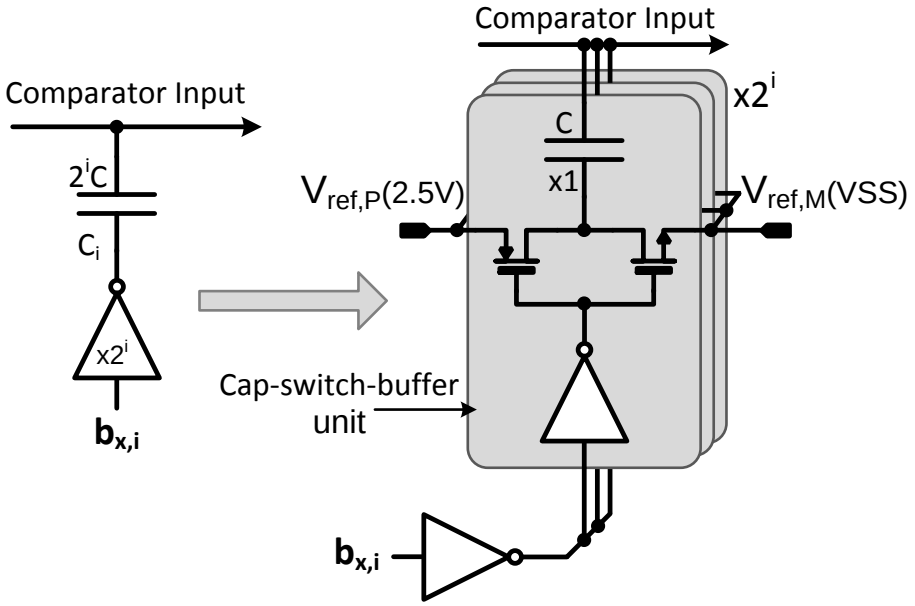


Figure 6.3: The ith CDAC array element with unit-element implementation.

6.2 Incremental ΣΔ DAC with analog reconstruction filter

The I-ΣΔ DAC generates the ADC fine steps (LSBs) by controlling the bottom plate of $C_{\Sigma\Delta}$, which is connected with the CDAC at top-plates, as shown in Fig. 4.2. The ratio between $C_{\Sigma\Delta}$ and the CDAC unit element (C) defines the nominal scaling between the I-ΣΔ DAC full-scale and CDAC LSB step-size (considering redundancy). The I-ΣΔ DAC provides a 9.5-bit resolution including a nominal redundancy of 1 bit after the coarse CDAC; accordingly, $C_{\Sigma\Delta}$ is scaled at a nominal size of 6·C, as detailed in 6.2.2. Therefore, the I-ΣΔ DAC output features a passive attenuation to the comparator inputs, which is equal to $C_{\Sigma\Delta}/C_{total}$, where C_{total} is the total sampling capacitance dominated by the single sided CDAC[1].

6.2.1 Structure and general specifications

Fig. 6.4 shows the block diagram of the I-ΣΔ DAC in the proposed architecture. The digital ΣΔ modulator receives a reset signal, which always brings

[1]Additionally, C_{total} includes $C_{\Sigma\Delta}$ and the offset compensation CDAC (C_{off}).

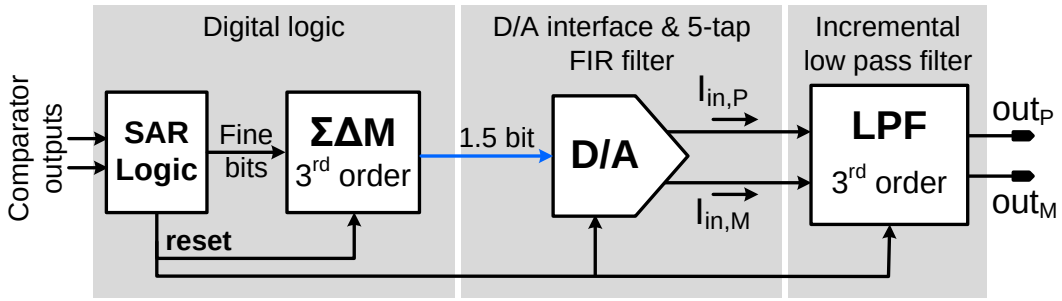


Figure 6.4: I-ΣΔ DAC block diagram.

the DAC to the same initial state before a new ADC conversion. The same reset signal also nullifies the state of the analog reconstruction filter. Within one ADC cycle, both the ΣΔ modulator and the LP-filter do not see the reset signal and feature a transfer function as a normal LP ΣΔ DAC. The digital ΣΔ modulator receives the fine bits as a digital input from the SAR logic. In this prototype, the digital part comprising the SAR logic and the ΣΔ modulator were implemented on an FPGA for the sake of debugging, reconfigurability and testing flexibility. The three-level output of the ΣΔ modulator is converted to the analog domain by a current mode FIR filter, which feeds an active RC followed by two passive RC low-pass stages to obtain an overall third-order low-pass reconstruction filter of the I-ΣΔ modulator, as shown in Fig. 6.5.

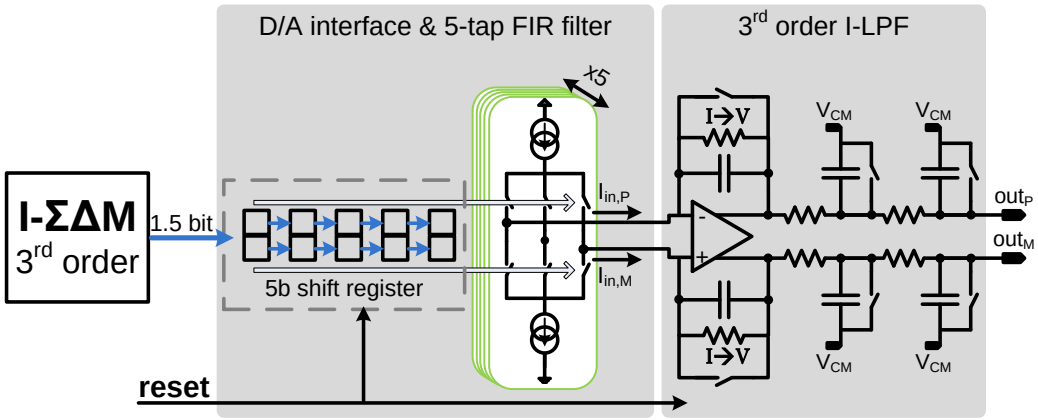


Figure 6.5: The analog reconstruction filter after I-ΣΔM.

Unlike the optimal filter approximation in chapter 3, which requires three high-speed stages (at ΣΔM-rate) to implement the CoI structure, the analog reconstruction filter features here a low-pass characteristic to suppress the ΣΔM quantization noise. A mostly passive structure is favored for reduced power consumption, therefore only one active stage is used to enable the D/A interface. Additionally, a simple FIR-filter is employed not to replace one filter stage, which would complicate its implementation and requirements, but to relax the active stage requirements. The filter details are outlined in section 6.2.2.

The filter noise defines the overall DAC noise, therefore it should satisfy the ADC resolution. Thanks to the noiseless scaling, the filter noise is relaxed by a factor $C_{\Sigma\Delta}/C_{total} \approx 6/138$ ($C_{total} = CDAC + C_{\Sigma\Delta} + C_{off} = 138\,C$), hence for a 90-dB SNR the filter noise is required to be below -63 dBFS (referred to the ADC input full-scale at 2.5-V reference). Also, the filter linearity defines the overall ADC linearity. Similar to the filter noise, the linearity is relaxed due to downscaling with single element ($C_{\Sigma\Delta}$). Thereby, for an ADC linearity beyond 110 dB, a filter linearity better than 83 dB is required. Moreover, better linearity in the DAC allows one to acquire a better calibration beyond the ADC limits (effective resolution), since during calibration, the thermal noise limited resolution can be improved by averaging, whereas the linearity would not benefit at all.

6.2.2 ΣΔ DAC steps and filter output settling

The last SAR step using the coarse CDAC is about 18 mV, due to binary scaling of the 2.5 V reference and the additional attenuation due to $C_{\Sigma\Delta}$ and the offset compensation CDAC. To achieve one bit redundancy, the ΣΔ DAC full-scale step at the comparator input equals 2*18 mV; therefore, the ΣΔ DAC full-scale is about $FS_{\Sigma\Delta} = 0.8$ V, due to scaling by ($C_{total}/C_{\Sigma\Delta}$). Instead of conventional binary scaling, the ΣΔ DAC uses redundancy through non-binary 1.8-radix steps, to relax the output settling as illustrated in Fig. 6.6. Therefore, the output is scaled with weights of $FS_{\Sigma\Delta}/1.8^n$, and the complete fine phase output

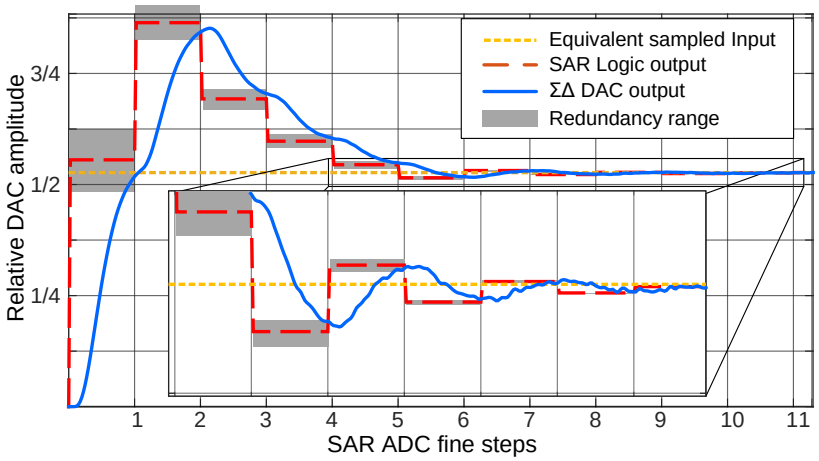


Figure 6.6: Transient response of the I-ΣΔ DAC output in SAR [73] ©2018 IEEE.

is represented by Out_{fine} in (6.1), where $c_i = \pm 1$ is the ith comparator decision during the fine phase.

$$Out_{fine} = \sum_{1}^{12} c_i \cdot FS_{\Sigma\Delta}/1.8^i \tag{6.1}$$

This non-binary scaling is achieved with no change in the analog circuitry, but by respectively scaling the digital input of the ΣΔ DAC, which is generated in the SAR logic. This redundancy allows errors up to 5% during the intermediate steps (less than 5-bit accuracy), instead of 0.1% which would be required for 10-bit settling. Therefore, the required settling time is reduced from $7\,\tau$ (10-bit) to $3.5\,\tau$ (5-bit), where τ is the reconstruction filter time constant.

The filter characteristics are determined by system level simulation, which provides a trade-off between the filter cut-off frequency and the output settling time (equivalent to ΣΔM OSR) to reach the required output accuracy. Thereby, both the settling time and the filter cut-off frequency are defined relative to ΣΔM output rate. Therefore, to define the filter parameters and hence the DAC speed, a realistic ΣΔM clock rate of $f_{\Sigma\Delta} = 150\,\text{MHz}$ is used, which is achievable for the used technology (w/o excessive power consumption) and reasonable for the board implementation (especially for the off-chip interface of ΣΔM output). Thereby, the filter is designed with a cut-off at 800 kHz, and the values of R and C satisfying this cut-off are chosen to have a similar area consumption for a better layout; thanks to the relaxed noise, which requires much smaller capacitors.

6.2.3 The digital modulator

Fig. 6.7 shows the implemented ΣΔ modulator; it is a single loop third-order 1.5-bit ΣΔ modulator. A 1.5-bit architecture was selected to avoid a multi-bit

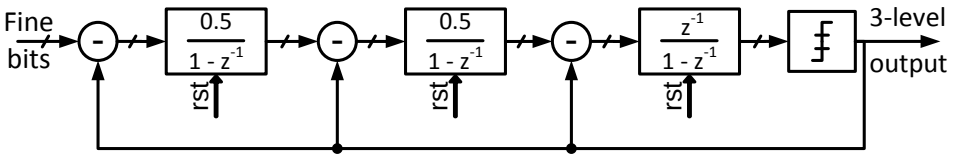


Figure 6.7: The third order ΣΔM [73] © 2018 IEEE.

DAC with its own non-linearity. A MASH (multi-stage noise shaping) structure is not used to avoid matching problems in the reconstruction filter. A third-order architecture was chosen as a compromise between reconstruction filter complexity and reasonable sampling frequency. The three-level quantizer and the incremental operation allow for more aggressive scaling of the coefficients compared to free-running ΣΔMs [77]. Usually, coefficient values as (0.2, 0.5, 0.5) would be used, especially for analog modulator with limited swings; while for the digital ΣΔM, increased swings are allowed by wider bit representation. Therefore, the optimal scaling from [77] was further optimized in Matlab in a constrained fashion for high SQNR and for using only binary-weighted scaling, which can be implemented using binary shifts in order to avoid digital multipliers in the implementation. This results in close to optimal scaling and does not limit the DAC performance.

The ΣΔ modulator operates at 150 MHz and the I-ΣΔ DAC uses 100 samples per conversion for a 9.5-bit Nyquist rate resolution, which allows an overall ADC sampling rate of 80 kS/s[2]. This was based on the ΣΔ DAC system simulation including filter settling; thereby the DAC cycle length is mainly limited by the filter output settling. Fig. 6.8 includes an illustration of the SAR ADC time diagram showing the time allocated for each ADC step during one conversion at 80 kS/s.

Lowering the clock rate would be possible by going to higher order ΣΔ modulators, or more beneficially to a multibit D/A; but the latter would come with matching requirements in the D/A interface for linearity reasons (especially

[2] After considering the full-resolution ADC timing, including sampling, coarse phase and comparator delays.

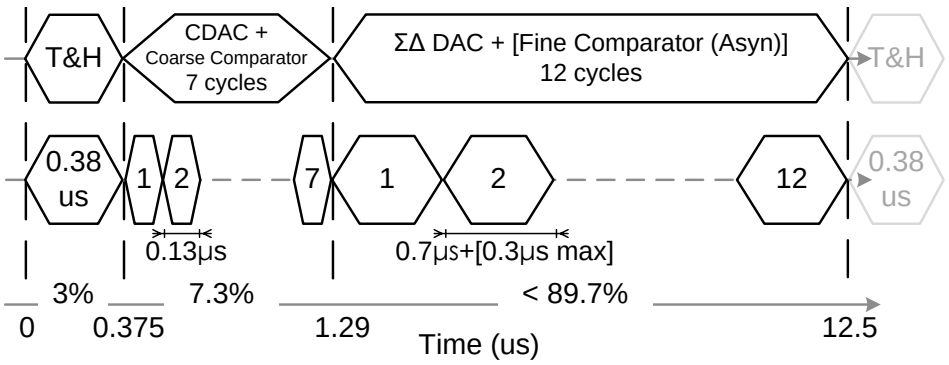


Figure 6.8: SAR ADC conversion time distribution for 80 kS/s operation.

considering the requirements outlined in 6.2.1). In this work, the aim was to achieve highest linearity and thus the higher clock rate was traded against the intrinsically linear 1.5-bit DAC. On the other hand, exploring other modulator architectures and orders with more sophisticated reconstruction filters could lead to improved performance as the analog reconstruction filter is the major power consumer in the presented design.

6.2.4 Current-mode FIR filter

The I-ΣΔM digital output has to be filtered by an analog reconstruction filter. Feeding the 1.5-bit output signal directly into an active RC filter would put stringent requirements on the operational amplifiers, since the 1.5-bit signal would include full-scale steps at the full rate of the digital modulator. On the other hand, decoding the ΣΔM output stream at lower rates using a binary weighted or even thermometer coded DAC would require element matching equivalent to the ΣΔ DAC accuracy; therefore, it would either consume big area and power, or require power hungry dynamic element matching techniques.

However, a semi-digital FIR filter stage performs the modulator output smoothing without putting high requirements on its element matching [65]. Hence, in the proposed implementation, the ΣΔ output is smoothed by a 5-tap current-mode FIR filter before being fed to the active RC filter, as shown in Fig. 6.5. Increasing the number of FIR taps would provide a smoother output and further relax the following active stage; however, this would increase the FIR array size and area, and its power consumption would be more significant.

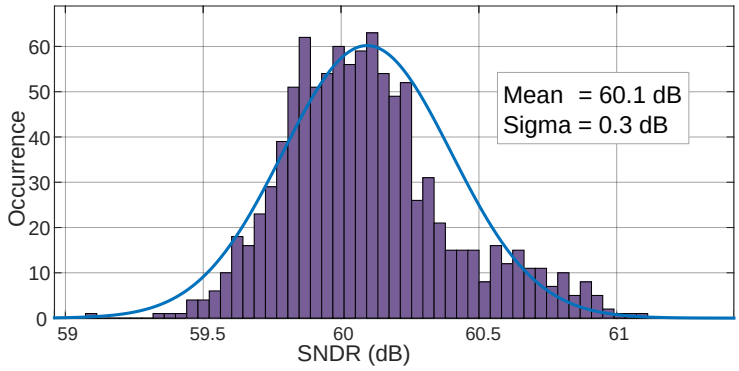


Figure 6.9: SNDR histogram of the ΣΔ DAC with 10% random mismatch on the FIR filter tap coefficients, in a behavioral simulation [73] ©2018 IEEE.

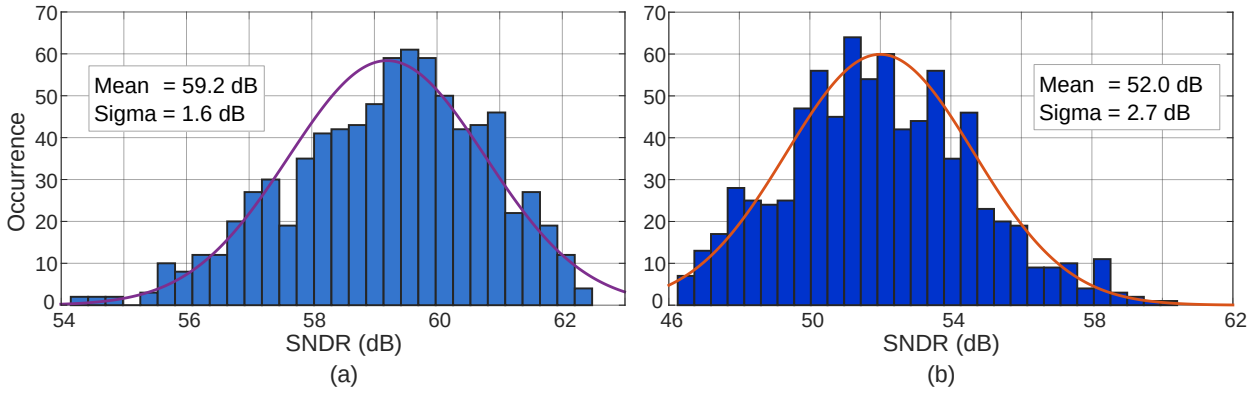


Figure 6.10: SNDR histograms of the ΣΔ DAC with 5-tap D/A interface (serial to parallel), including (a) 0.5%, and (b) 2% random mismatch on the D/A elements.

Also, having more taps requires higher switching and buffering complexity for the logic circuits operating at $f_{\Sigma\Delta}$, hence increases the disturbances to the nearby analog circuitry. On the other hand, by lowering the number of taps further, the FIR-filter advantage would almost vanish. Therefore, 5-tap array is used, as it provides relaxed steps to the active RC stage without large FIR array with significant area and power consumption.

Fig. 6.9 shows the behavioral model simulation results of the ΣΔ DAC including the D/A FIR and analog filter; thereby, the FIR filter coefficients include a random mismatch with 10% variance. The 1,000-point histogram shows that the SNDR remains within 1 dB of the nominal value, with a 3-σ yield; therefore, matching constraints on current elements are very relaxed.

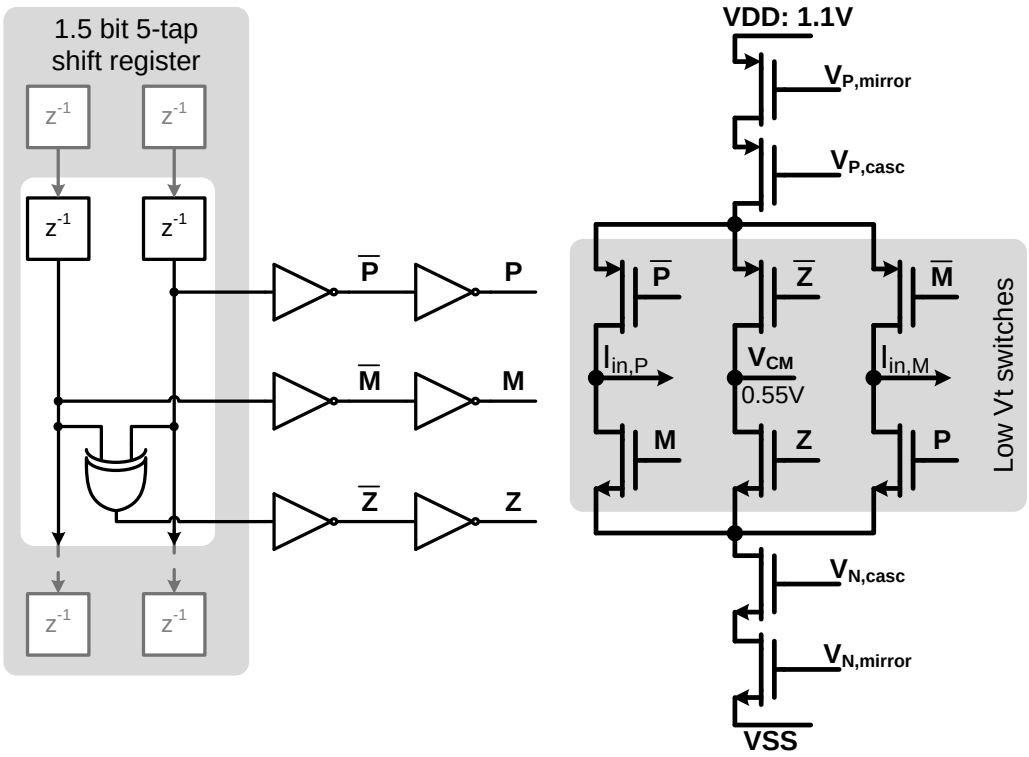


Figure 6.11: The 1.5-bit current tap of the FIR filter with switching control from the shift register [73] © 2018 IEEE.

For comparison, an equivalent mismatch simulation is performed on a 5-level DAC (serial to parallel converter), where the bit stream is not shifted over the DAC elements, as in FIR filter. Simulation results are shown in Fig. 6.10 for 0.5% and 2% mismatch standard deviations respectively, this yields worse results compared to 10% mismatched FIR array. Therefore, even at 20x more mismatch, the FIR filter results in a better SNDR. Moreover, under element mismatch, the effective resolution is limited by the SQNR for the FIR filter case; while for the DAC case, the mismatch leads to degraded linearity.

To generate the 1.5-bit output levels, a bipolar current tap is used with 2 µA unit current, as shown in Fig. 6.11. Despite the relaxed matching, lower unit current values were not used, because the small current array does not have a significant power consumption. Also, reducing the current unit would require an increased resistor value for the I-to-V converter (to keep a constant full-scale) in Fig. 6.5, which would require a significant area consumption. The intrinsically linear three-level current output is obtained by simultaneously

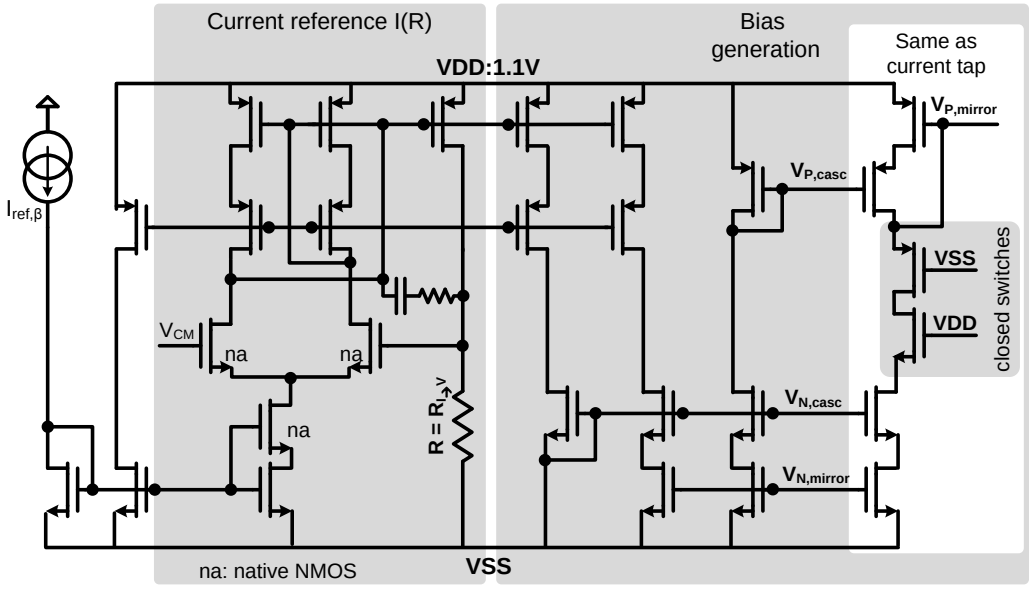


Figure 6.12: Bias generation for current taps with enhanced PVT sensitivity, derived from [78].

switching a single PMOS & NMOS current source per tap as p/m, m/p or z/z on the common mode voltage, where p is positive, m is negative and z is dump. The cascode transistors are biased in the sub-threshold region to provide a high output impedance and allow low voltage operation together with the switches, which use low threshold voltage transistors.

Due to process, voltage and temperature (PVT) variations, a high gain error at the I-to-V conversion through the active RC could potentially limit the DAC range. Therefore, a reference current is generated via V-I based biasing as shown in Fig. 6.12 [78]. This is achieved using a reference voltage (V_{CM}) regulated over a resistor (R) that has the same size and shape and is placed close to the resistor ($R_{I->V}$) performing the I-to-V conversion. Thereby, the biasing voltages of the current tap ($V_{P,mirror}$, $V_{P,casc}$, $V_{N,casc}$ and $V_{N,mirror}$) are generated by mirroring this reference current, which heavily reduces the impact of process and temperature related gain errors; the remaining gain error is digitally calibrated[3].

[3]While it is possible to fine tune the gain mismatch digitally, it would be very important to limit (or trim) an excessive gain mismatch, if is saturates the DAC output.

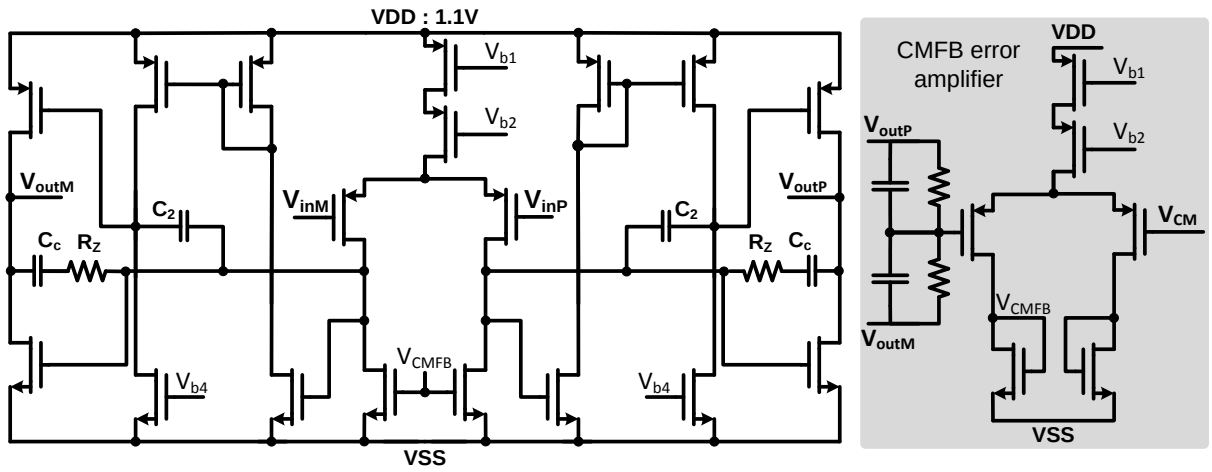


Figure 6.13: Three stage positive feedback compensation amplifier.

6.2.5 Amplifier design

From Fig. 6.5, the op-amp within the active RC filter drives two low-pass RC stages. Therefore, its output settling speed and stability are relatively relaxed compared to the fast ΣΔM clock. Also, a limited gain-bandwidth does not degrade the filter linearity, it even leads to a minor increase to the effective low-pass filtering. Nonetheless, the amplifier is required to stabilize the output of the preceding current sources fast enough to prevent any input dependent distortion at the D/A interface. Moreover, the op-amp must allow the DAC full-scale swing at its output and provide a dynamic current to drive the passive RC stages fast enough to not slow down the fine conversion loop.

The op-amp features a three stage positive feedback structure [71, 79], shown in Fig. 6.13. Beside the enhanced frequency response of this structure (compared to Nested-Miller), it also provides the flexibility to implement high dc-gain via the three stages, while at the same time it achieves good output driving. A class-AB output stage dynamically drives the load without major output swing limitation. The biasing voltages are generated with local current mirrors, which receive and regenerate a common reference current from an on-chip beta-multiplier circuitry. The relaxed load with series R-C connection (lower effective C load) allows for a small compensation capacitors; $C_C = 100\,\text{fF}$ and $C_2 = 50\,\text{fF}$ are used. However, this increases the effect of the parasitic capacitances on the op-amp speed. The common mode feedback

error amplifier is a replica of the first stage but with NMOS diode load; the output common mode is generated with a pair of parallel RCs. The op-amp has a gain-bandwidth (GBW) product of 62 MHz after RC-extraction, which is nominally designed for $f_{\Sigma\Delta}/2$ [4]. Although, the LP filter cut-off is much smaller than $f_{\Sigma\Delta}$, a much higher GBW (compared to cut-off) is required to stabilize the FIR output and prevent signal dependent distortion in the current array. Additionally, an overdesigned GBW is is allowed due to a relaxed load and non-significant power consumption at input stage.

6.2.6 ΣΔ DAC reconfigurability

Unlike conventional SAR designs, where the LSB size is physically fixed in the CDAC design, the LSB size in this design is defined by the digital word at the input of the ΣΔ DAC, its architecture and sampling rate. Therefore, the LSB size can be digitally readjusted, up to a limit allowed by the analog filter performance. Simulations show that about 3-bit increased performance (above nominal design) can be obtained by adjustments of the SAR steps and OSR without changing the analog filter.

This flexibility comes at a minor cost of extended digital signal representation and higher OSR of the ΣΔM, while both are associated with higher power when used, but it allows for reconfigurability after manufacturing. If only the reduced resolution is used, there is no extra power, because the additional bits would simply not be switched. This possibility of extending the nominal resolution can be beneficially used during calibration of the coarse CDAC with the fine ΣΔ DAC in order to extend the calibration accuracy and thus the achieved linearity; for that, an extended DAC SQNR is required, while the additional circuit noise is averaged (suppressed) during the startup calibration.

[4] Thanks to small compensation capacitors, non significant power is consumed at input stage, while the output stage dominates the op-amp power consumption.

6.3 Hybrid Comparator implementation

6.3.1 Dynamic comparator with dual supply

The coarse comparator resolves the seven MSB decisions based on the CDAC, which are followed by a redundancy decision within the fine conversion phase to recover errors below the seventh MSB size. The coarse comparator receives differential inputs with a varying CM, which is conceptually a drawback of the monotonic switching, as it may result in a varying comparator offset potentially leading to output distortion (chapter 4). However, the always decreasing and signal-independent CM voltage of the monotonic switching scheme is turned into an advantage for this design, as it allows one to move from the high supply used for input sampling to the low supply used in the fine comparator. Simultaneously, the errors due to CM changes do not exceed the 7-bit coarse accuracy. Therefore, they are covered by the redundancy and cured using the hybrid DAC and comparator concept.

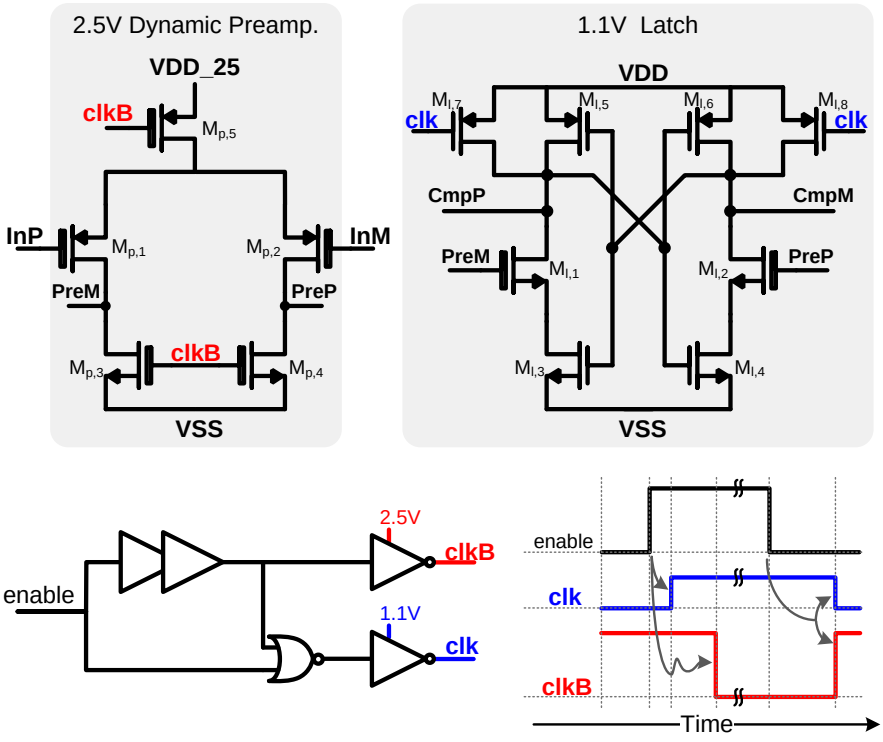


Figure 6.14: The dynamic coarse comparator with overlapping clock generation [73] © 2018 IEEE.

The coarse comparator operates from the 2.5 V supply to allow processing the full swing ADC input at 2.5 V, as shown in Fig. 6.14. It employs a fully dynamic two-stage structure similar to [32, 74]. The first stage is a dynamic preamplifier, which employs PMOS input transistors to manage the decreasing CM voltage. The transistor $M_{p,5}$ is sized such that the differential input pair operates in subthreshold for better voltage gain and noise performance [30]. A dynamic latch with reset follows the preamplifier [74]. It operates at the core 1.1 V supply, while having 2.5 V input transistors ($M_{l,1}$ and $M_{l,2}$) to translate the preamplifier differential voltage into a regeneration current difference, and shield the low voltage latch from the high voltage preamplifier.

The comparator operates dynamically at the rising edge of the enable signal, thereby a falling edge of "clkB" and a rising edge of "clk" (as in Fig. 6.14) are generated. Thereby, the two nodes PreP and PreM charge toward VDD with different speeds based on the comparator differential input. To generate the latch decision based on [PreP - PreM], its reset has to be released earlier, which requires an overlapping time between the high levels of "clkB" and "clk". Nonetheless, the overlapping period is not very critical. Figure 6.14 also includes the logic circuit implemented to generate the overlapping clocks at different supplies.

6.3.2 Comparator noise simulation

The comparator noise simulation aims to estimate the total noise contribution of the comparator circuitry and represent it as an input referred noise source in front of a noiseless comparator. Since the comparator is a nonlinear circuit the linearized noise simulation "AC noise" is not feasible, however, two approaches are used to estimate the comparator thermal noise, as follows.

Transient noise approach: In this approach a transient noise simulation is performed. The comparator input is fixed at voltage input (DC_{IN}) close to the expected noise levels [80]. The input referred noise at the comparator input has a probability density function (pdf) with shifted mean to DC_{IN}, as shown in Fig. 6.15 (b). By counting the '1' decisions at the comparator output a measure equivalent to the integrated blue area (in Fig. 6.15) is obtained, which represents the Gaussian cumulative distribution function (CDF). Therefore, by

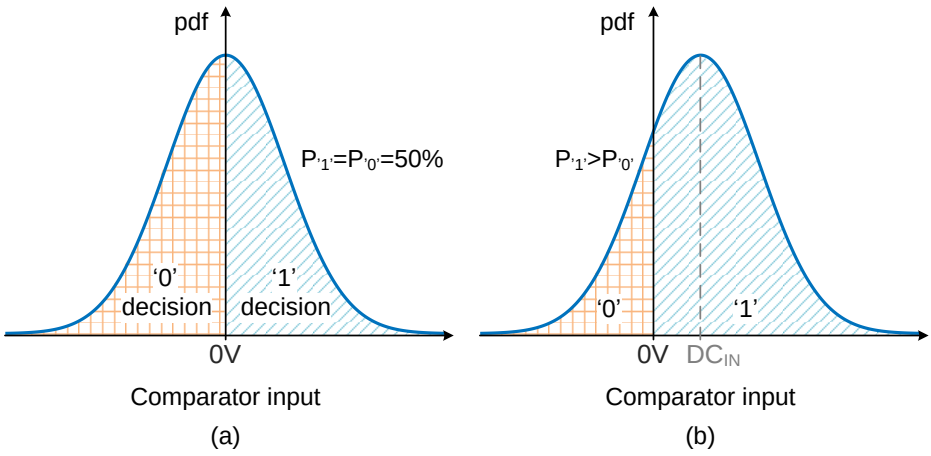


Figure 6.15: The probability density functions for noisy comparator inputs around: (a) 0 V and (b) fixed DC input.

comparing this measure to a Gaussian noise model, the equivalent root-mean-square (rms) noise is estimated, which is equivalent to the standard deviation of the Gaussian distribution. As this method performs a large signal simulation without linearized models, it provides an accurate measure of the comparator noise. However, for accurate estimation, a large count of comparator outputs is required, which leads to long simulation time.

PSS aproach: The periodic-steady state (PSS) simulation can be used to allow a linearized model of the dynamic comparators, which allows one to use a linearized noise simulation afterwards (Pnoise). This is achieved by periodically clocking the comparator and examining the output of the dynamic latch during the exponential increase [80], as shown in Fig. 6.16. Thereby, a linear input-output relation with fixed gain is guaranteed at a fixed point in time, within the exponential increase region. Hence, by examining the output noise with the linearized model at the fixed time instance, the input referred noise can be estimated.

The two methods are used to estimate the coarse comparator thermal noise. Two transient noise simulations are done by applying two fixed input voltages 0.5 mV and 1 mV, thereby the "1" decision rates were 71.1% and 86.9% respectively, which matches a Gaussian model CDF with $\sigma = 0.89$ mV. A third simulation with 1 mV input voltage is performed with 4-time scaled noise contribution, the simulation resulted 60.5% correct decision rate (1's), which also matches a Gaussian model with $\sigma = 4{*}0.89$ mV. On the other hand, the PSS

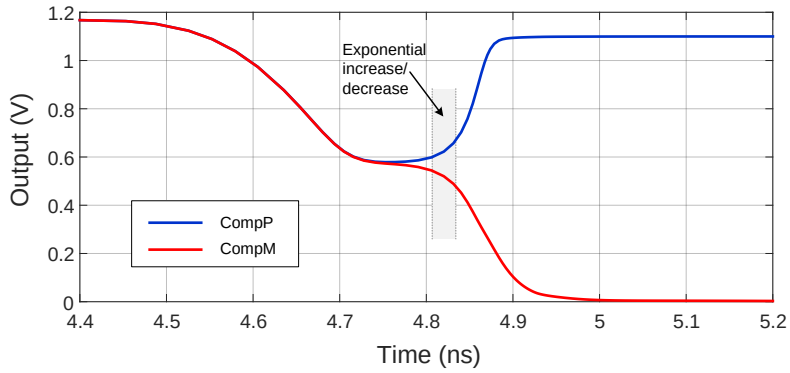


Figure 6.16: The transient comparator response at the outputs.

and Pnoise simulations resulted in an input referred rms noise of 0.97 mV, which is of an acceptable agreement with the transient simulations.

6.3.3 Eye-opening comparator implementation

A VCO-based eye-opening comparator is used for the fine decisions of the SAR ADC as in [39]. Conventional low-noise comparators consume high power during all SAR decisions, while comparators based on majority voting can step into a low-noise high-power mode (or use redundant decisions) based on additional logic for metastability sensing [32]. On the other hand, the eye-opening comparator smoothly scales the power consumption with its overdrive over SAR decisions without a need for additional sensing circuitry.

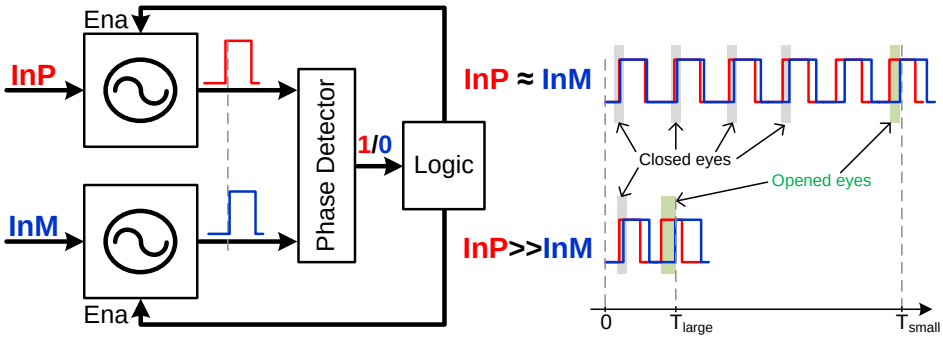


Figure 6.17: The eye-opening comparator concept.

The basic concept is that the differential input is fed into two competing VCOs, as shown in Fig. 6.17. Even with a small voltage difference, the VCOs develop a significant phase difference over time and a decision is made, when this phase difference is large enough. Thus, the "eye" is automatically opened for the decision, as illustrated in the two transients for large and small voltage inputs in Fig. 6.17. For a mostly digital implementation, the VCOs are implemented using current-starved inverter chains. The thermal noise is present as jitter at the inverter outputs and is accumulated over the inverter chains and integrated over time. Therefore, the thermal noise is averaged while the signal is integrated. The phase detector (PD) implements a dead zone, which prevents a latching decision due to jittery phase shifts. Therefore, the dead zone in the PD determines the noise level and the comparator delay by preventing fast decisions. The wider the dead zone the longer the decision time is, and the better the thermal noise rejection is.

Fig. 6.18 shows the schematic of the eye-opening comparator implementation. The limited input range – due to the proceeding monotonically switched coarse phase – allowed the exclusion of the time amplifier as in [39], by adaptation of the dead zone in the PD. The comparator receives an enable signal from the SAR logic, then it enables the internal VCOs. Thereafter, the VCOs automatically turn off after decision making to save their dynamic power, which is dominantly consumed in the two VCOs. To prevent erroneous decisions due to a wrongly re-latched disable edge (at the falling edge of $\mathrm{Ring}_{\mathrm{ena}}$ in Fig. 6.18), two flip-flops were added to store the PD decisions and provide the comparator output.

Each VCO is implemented with seven inverting stages, which include six inverters proceeded by a NAND cell to control the enable/disable comparator modes. Increasing the number of stages would increase the signal gain in the VCOs (more input contribution with more stages), it would also reduce the mismatch between the two VCOs, which is averaged over the stages. However, adding more stages leads to increased kick-back noise at the comparator input (over parasitic capacitors), which is very important aspect because of the required high resolution and the high speed VCO outputs. The VCOs feature a nominal oscillating frequency of around 370 MHz at 150 mV common mode. The phase detector is implemented using two rising-edge triggered D-type flip-flops (DFF) with reset. A dead zone of about 20 ps is generated by introducing

additional delay in the first stages of the two DFFs (devices with increased length).

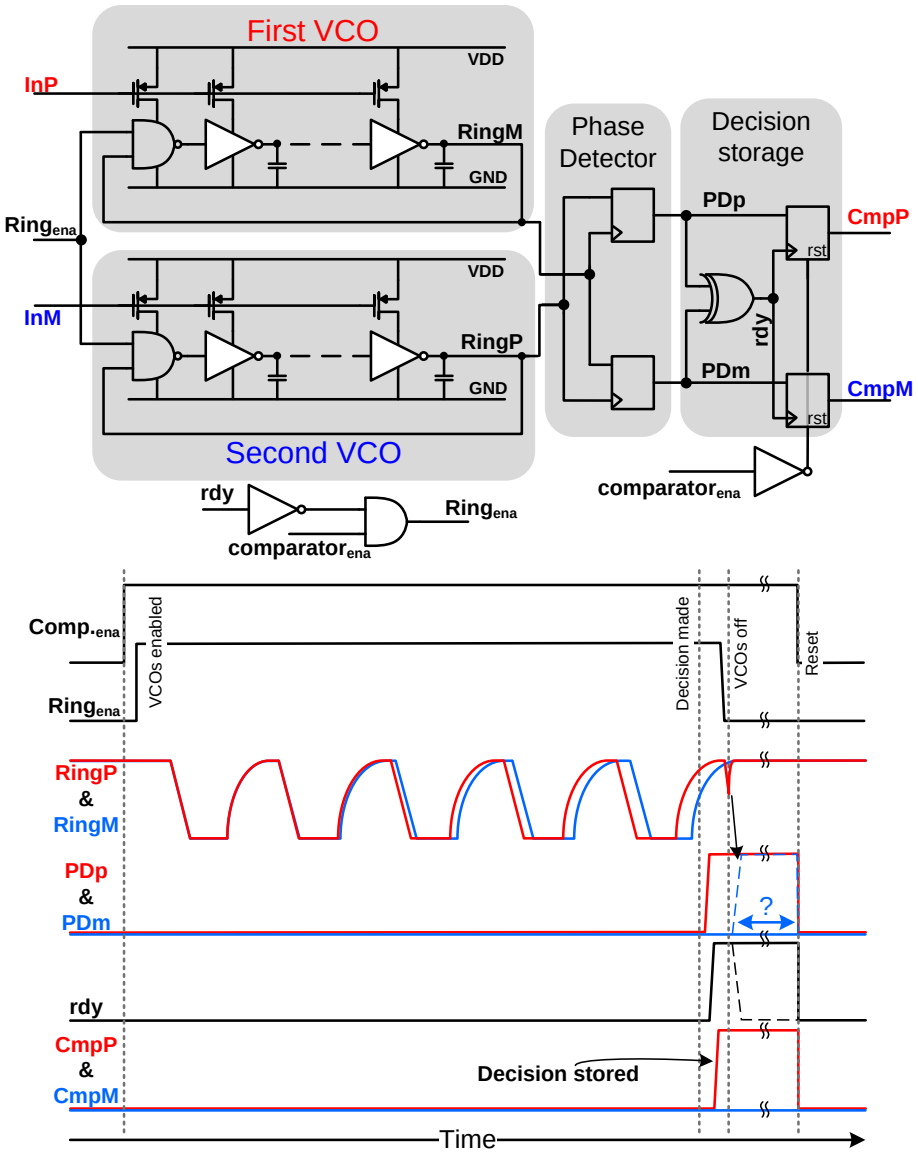


Figure 6.18: Schematic and transient responses of the eye-opening comparator, modified from [73] © 2018 IEEE.

6.3.3.1 V_{CM} sensitivity, power and delay

The eye-opening comparator features high sensitivity to input common mode voltage (V_{CM}) level, due to its effect on the VCO running frequencies. Due to the monotonically switching CDAC, V_{CM} drops close to VSS before the fine phase (nominally $V_{CM,Fine} \approx 100\,mV$). Increased V_{CM} leads to decreased

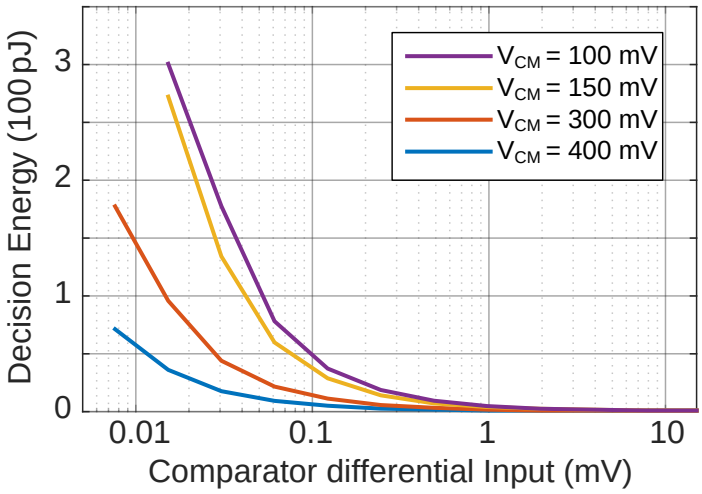


Figure 6.19: The scaled decision energy over comparator input voltage.

starving currents (at lower V_{GS} on the input transistors), which consequently decreases the oscillating frequencies of the two VCOs and simultaneously increases the gain of the input devices, which are further pushed from triode towards saturation region. Therefore, a shorter decision time and lower power results from higher V_{CM} (at a fixed PD), but due to faster decisions the thermal noise performance can be degraded, due to a decreased number of oscillations per decision (less effective averaging).

On the other hand, power scaling over overdrive voltage (comparator input) is a major advantage of the eye-opening comparator, which enables high power efficiency. Additionally, the scaled decision delay allows for increased ADC speed in an asynchronous SAR loop. Figures 6.19 and 6.20 show the scalings of the comparator energy consumptions and decision time delay, respectively, over input voltages for different common mode voltages V_{CM}.

6.3.3.2 Noise simulations

Unlike dynamic latch comparators, there is no linear relationship between input and output at the decision point (as in the exponential region for the latched comparators) in eye-opening comparators. This prevents to estimate the comparator noise in a linearized simulation (PSS & Pnoise), but allows it only through transient simulations. Due to decision time scaling over com-

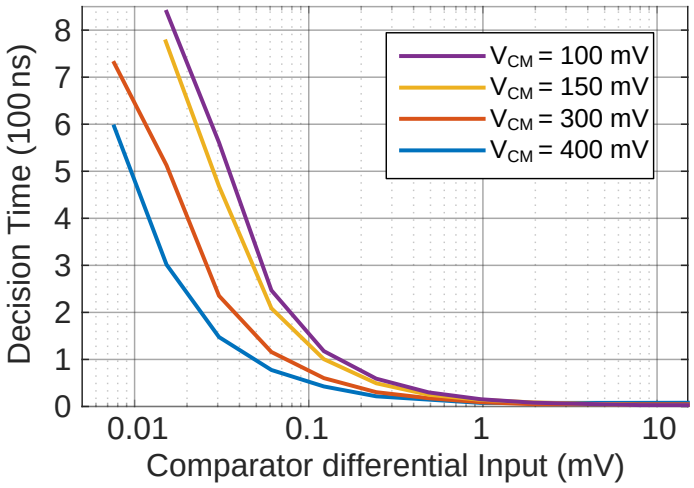


Figure 6.20: The scaled decision delay over comparator input voltage.

parator input, as shown in Fig. 6.20, the comparator features a minimum detectable input (without noise) based on a finite decision time window. This feature leads to a modification on the statistical noise simulation approach, as shown in Fig. 6.21, because the noise pdf range below the minimum detectable input is excluded from the CDF value. The accuracy of this noise estimation is generally degraded when the DC_{IN} is close to the minimum detectable input, and similarly when DC_{IN} is set too high compared to the noise rms value. Moreover, by increasing the maximum decision window, both the minimum detectable and the noise rms values decrease, which all make the result of this estimation less accurate and require longer simulation time (more outputs) for accurate estimation.

This approach is used to estimate the thermal noise contribution of the comparator with a decision window of 250 ns at $V_{CM} = 350$ mV. The estimated minimum detectable input – for the used decision window – is 27 µV, based on a noise-free simulation. Two positive inputs (50 µV and 40 µV) are applied to the comparator; thereby, the measured correct decision rates (ones rate) are 94% and 87%, respectively. Based on the Gaussian noise model, the estimated noise rms value is 15 µV. However, this result provides very coarse noise estimation, because the minimum detectable input is much higher than the estimated noise rms, and the '0' decision region almost vanishes, as shown in Fig. 6.22. Therefore, the final noise estimations are based on complete SAR ADC simulations as will be shown in section 6.4.2.2.

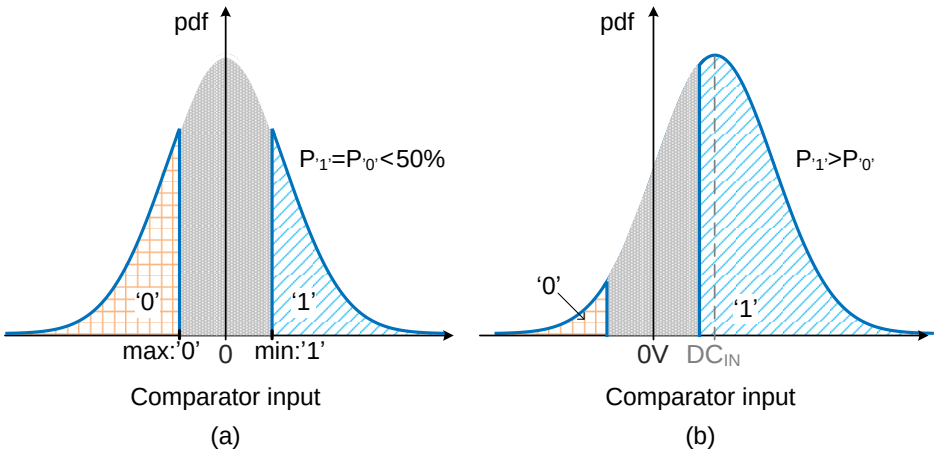


Figure 6.21: The noise pdfs at the input of the eye-opening comparator, around: (a) 0 V and (b) fixed DC input.

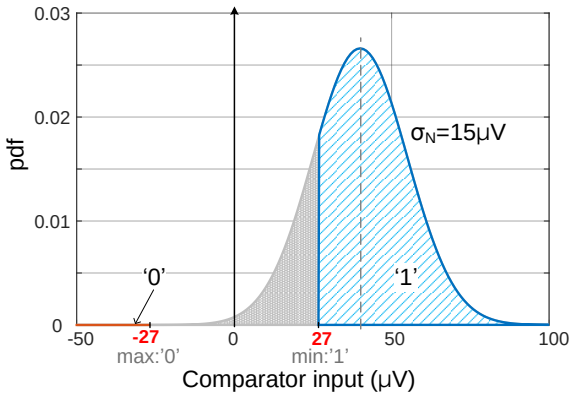


Figure 6.22: Simulated noise pdf of the eye-opening comparator with fixed input of 40 µV.

Low frequency noise: The statistical transient approach does not provide a valid estimation for a frequency dependent noise source. Therefore, flicker noise is also simulated within the complete SAR ADC loop. Conceptually, the incremental operation of the eye-opening comparator intrinsically attenuates the low-frequency noise contribution through the periodic reset, which cancels any memory within the comparator. However, due to the averaging effect over time, the thermal noise features high order averaging within one decision time, while low frequency noise is accumulated; effectively, this leads to shifting the noise corner frequency to high frequencies. Therefore, even if the noise corner frequency is below the comparator reset rate (which

is above 3.3 MHz), the comparator can experience flicker noise above its reset rate, because of strong averaging.

6.3.4 Coarse offset mismatch compensation

Based on the statistical mismatch simulations, cf. Fig. 6.23, the offset in the coarse comparator has a standard deviation of about 18 mV, which is relatively high due to close to minimum-size devices, and about 4 mV for the eye-opening comparator, with the expectation of some increase of the eye-opening comparator offset, due to non-available statistical models in the process design kit for the used "moscaps". Since designing the redundancy for the worst case offset

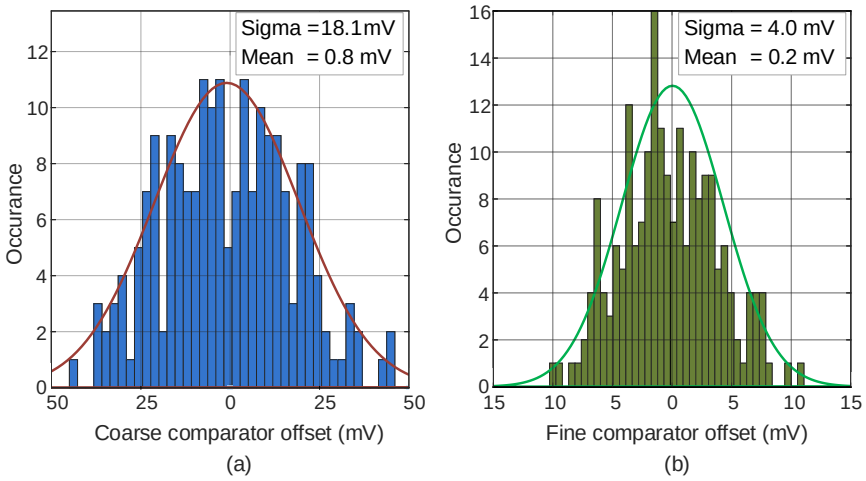


Figure 6.23: Comparator offset histograms via 200-run mismatch simulation.

mismatch would lead to extended conversion time, this was avoided by adding a small 4-bit CDAC for offset calibration. Therefore, the redundancy is designed to recover errors (including offset) within an LSB of the coarse CDAC, which is about 18 mV, which recovers a major part of the offset mismatch. On the other hand, the offset calibration CDAC is used to cover the worst case mismatch with a full scale of 68 mV.

The offset compensation CDAC is shown within the SAR ADC in Fig. 6.24. It comprises a 4-bit switched capacitor array, and it has an MSB size equal to $2\,C_{LSB}$ of the coarse CDAC. Therefore, it does not consume any mentionable

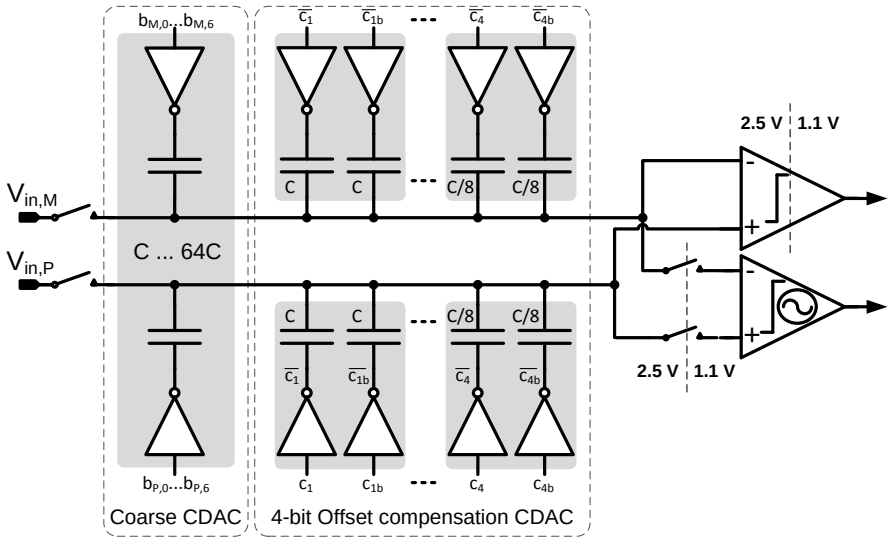


Figure 6.24: The Offset compensation DAC in the SAR ADC.

area. The differential structure is required to prevent common mode voltage changes due to offset compensation.

6.4 Toplevel SAR ADC simulations

To evaluate the dynamic ADC performance, a sinusoidal input signal with close to full-scale amplitude is typically applied, and the ADC digital output is examined after a discrete Fourier transform (dft/fft). On the output power spectral density (PSD) plot, the signal components are isolated of noise and distortion, to estimate the SNDR and SFDR. The complete SAR ADC is simulated on transistor level using the TSMC 40 nm design kit, while the digital part including the SAR logic and $\Sigma\Delta$M are implemented using verilog-A models.

6.4.1 Simulation challenges

Estimating the dynamic performance of high resolution ADCs is challenging, due to requiring long simulations to enable accurate PSD plots. At the same time, the simulator accuracy settings have to be strictly tightened, to allow

for accurate transients in the simulations, which all translate into very lengthy simulations[5]. Additionally, the merge between low sampling speeds (long periods) and fast switching internal nodes (e.g. the VCOs in fine comparator), or equivalently, the simultaneous simulation for high speed D/A interfaces (e.g. the FIR shift register) and the slow speed analog signals, both with the intended high accuracy, puts stringent requirements on simulation time steps and further extends the simulation time. Moreover, one of the most challenging simulations is the transient noise simulation including both thermal and colored (1/f) noise. That is because simulating low-frequency noise requires more strict accuracy, exclusively for the fine comparator, and especially at low V_{CM} and high noise averaging. At the same time, relatively long simulation time (at lease $1/f_{min}$) is required to evaluate the low frequency noise. Therefore, it is very challenging to combine these strict requirements for the colored noise with the extended time accuracy, accompanying the high frequency noise, in one long and accurate simulation.

All these reasons make it increasingly important to modify the simulation test-benches and develop tools to allow for faster ADC evaluation. Two approaches were developed during the design implementation, in order to allow for fast intermediate evaluations. One approach includes splitting one long transient into several small transients and distributing them over distributed processing units. Thanks to Nyquist operation, which enabled this technique, by allowing the ADC to process individual input samples independently. However, two drawbacks are related to this technique: an additional overhead to simulate enough overlapping time windows between the short simulation portions, and decreased capability to simulate low frequency noise and potential ADC memory effects (long-term). The second approach, which is very effective, is the SNDR estimation using the ADC quantization error (Q_E) power (including transient noise and distortion). Thereby, instead of the spectrum plot, which requires a predefined number of samples, evaluating Q_E relative to the signal power, can be done already with very few output samples; this directly gives a coarse estimation of the ADC performance, and the longer it runs the better the estimation is, without any predefined conditions on the sample numbers.

[5]These extend for days and even several weeks to accurately simulate the top-level design

6.4.2 Simulation results

The SAR ADC is simulated over time, initially using short periods or equivalently low number of samples (256 or 128) for coarse evaluations. The ADC is simulated in many scenarios to determine the limitation sources. An initial target is to maintain an approximate SNDR above 90 dB for the transistor-level simulations with transient noise. The ADC is simulated with close to 0-dBFS input signal power ($P_S > -1$ dBFS), and the output spectra are obtained after applying Hann window. To isolate the effect of quantization noise, a 16-bit quantization noise level is simulated in a noise-free test-bench as shown in the PSD plot of Fig. 6.25[6], which reports SNDR = 97.8 dB (quantization-noise only) at $f_S = 80$ kS/s. This performance is maintained at slightly higher sampling frequencies; Figure 6.26 shows the output spectrum using $f_S = 112$ kS/s, which reports SNDR = 97.5 dB.

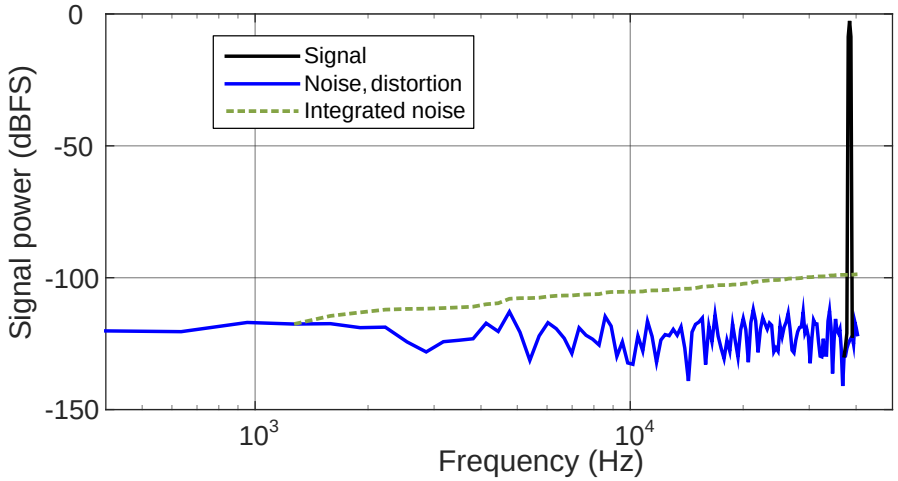


Figure 6.25: SAR ADC output spectrum (256-point fft) in a noise-free simulation with $f_S = 80$ kS/s, $f_{in} = 38$ kHz ($P_S = -0.9$ dBFS).

[6]Unless otherwise mentioned, all the reported transient simulation results are recorded at a fine comparator common mode of about 350 mV

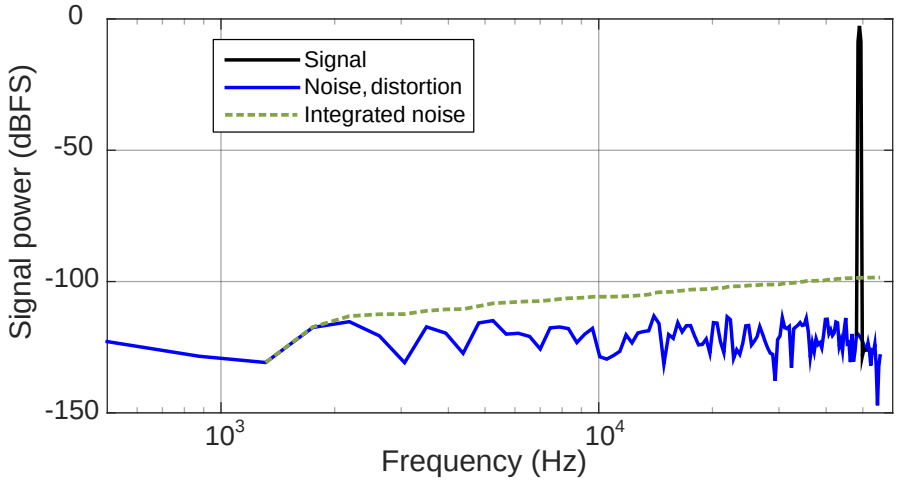


Figure 6.26: SAR ADC output spectrum (256-point fft) in a noise-free simulation with $f_S = 112\,\text{kS/s}$, $f_{in} = 49.5\,\text{kHz}$ ($P_S = -0.9\,\text{dBFS}$).

6.4.2.1 Corner simulations

In order to check for performance drop over process variation, the same noiseless simulation is performed over four available process corners [FF, SS, SF and FS], which all reported SNDR $> 95\,\text{dB}$, after tuning the gain mismatch between the full-scales of the fine and coarse DACs. The relative change in the full scale ratios for the four corners (FF, SS, SF and FS), compared to the typical corner, are (+6.1%, -4.4%, +0.3% and -0.4%) respectively.

6.4.2.2 Noise simulations

The SAR ADC is simulated including transient thermal noise. Figure 6.27 includes two output spectra at different common mode voltages: only a slight difference of thermal noise performance (1 dB) is seen between the two common modes. The common mode level mostly affects the performance of the fine comparator, as discussed in section 6.3.3.1, while other noise sources are mostly independent of common mode changes (e.g. sampling noise). Therefore, due to non-full dominance of the comparator thermal noise, the effect is only slight, and a degraded thermal noise at higher V_{CM} is related to faster operation and less averaging in the eye-opening comparator.

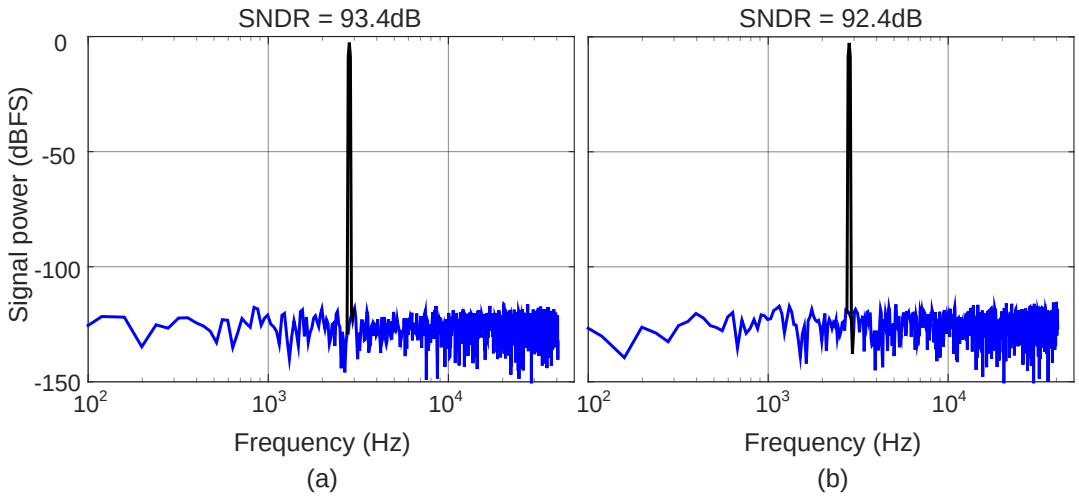


Figure 6.27: SAR ADC output spectra including thermal noise ($P_S = -0.9\,dBFS$), with fine comparator common modes of (a) 150 mV and (b) 450 mV.

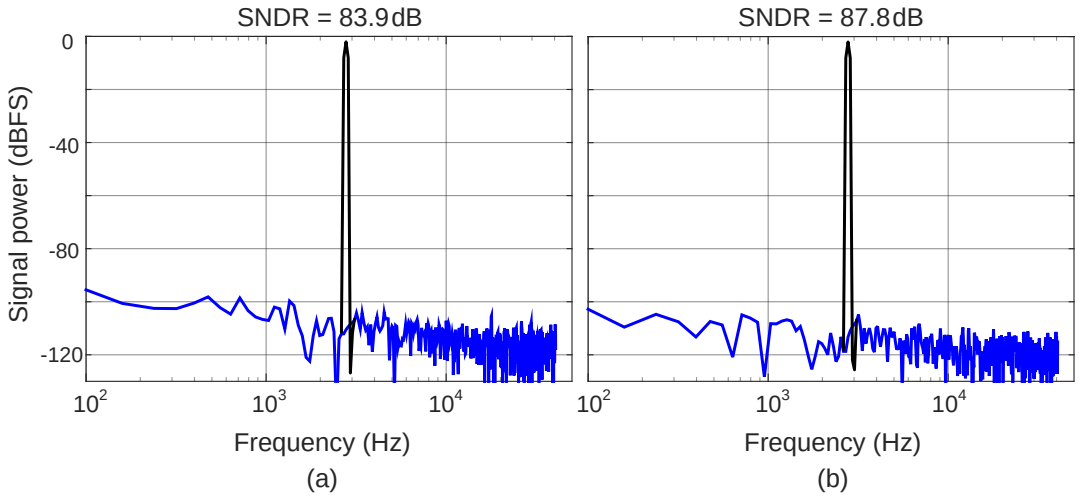


Figure 6.28: SAR ADC output spectra including thermal and flicker noise ($P_S = -0.9\,dBFS$), with fine comparator common modes of (a) 150 mV and (b) 450 mV.

Finally, the colored noise (frequency-shaped) including both thermal and flicker noise is included the transient simulation of Fig. 6.28. As discussed in section 6.3.3.1, the eye-opening comparator concept is immune to low frequency noise. Nonetheless, due to the high averaging factor (over VCO edges), the

noise corner frequency shifts to much higher frequencies. Simulations show that the effect of flicker noise is more significant at frequencies above 1 MHz, which can also be partly seen in the spectra in Fig. 6.28, where no clear 1/f slope is present, as the performance is dominated by shaped noise beyond the Nyquist-bandwidth, which is folded back in the spectra. Moreover, at higher V_{CM} values, lower averaging factors at shorter decision times are achieved, which leads to better low frequency noise performance.

6.4.2.3 Noise breakdown

In conventional SAR ADCs with CDACs, the ADC noise is mainly determined by the comparator noise besides the sampling noise. In the proposed design, the ΣΔ DAC is an additional noise source through the analog reconstruction filter. However, the ΣΔ DAC output benefits from noiseless scaling by $C_{\Sigma\Delta}/C_{total} = 6/138$, as shown in 6.2.1. Equivalently, the filter noise can be around 27 dB higher than the comparator noise, therefore it is very relaxed. Fig. 6.29 shows the ADC noise breakdown. In order to estimate the noise

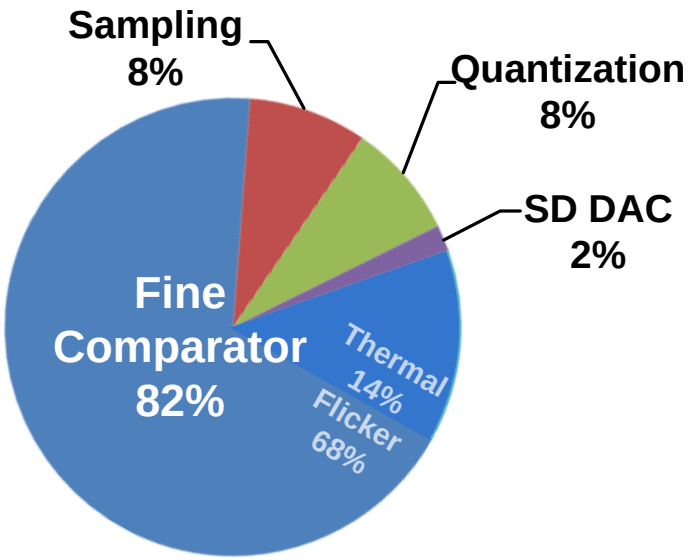


Figure 6.29: SAR ADC noise breakdown.

breakdown, the noise of each source (block) is enabled individually, using an additional upscaling factor (x4) to make the unavoidable share due to quantization and circuit distortion negligible. Based on Fig. 6.29, the ADC noise is

fully dominated by the comparator noise (1/f noise), while the filter noise in the ΣΔ DAC adds a non significant share of 2%.

6.4.2.4 Mismatch simulations

In order to simulate the SAR ADC with statistical mismatch variations, the calibration has to be employed to calibrate the CDAC mismatch. This, together with the required strict simulator accuracy settings, makes it not feasible to run many long simulations, at the same time limited transients prevent repeated averaging to improve the calibration performance. Nonetheless, several Monte Carlo runs proof that after CDAC calibration the performance is restored back to SNDR > 90 dB, excluding low frequency noise for a relaxed accuracy settings, as discussed in 6.4.1. Figure 6.30 includes two examples for SAR ADC output spectra with and without calibration. In the two examples in Fig 6.30 (a), (b), the reported SNDRs are 91 dB and 92 dB. Although, the SFDR estimation is an important calibration performance measure, it is not feasible using short transients: an accurate SFDR simulation would require at least an order of magnitude longer simulations than those reported in Fig 6.30, therefore, it is more accurately addressed in the ADC measurements, in chapter 7.

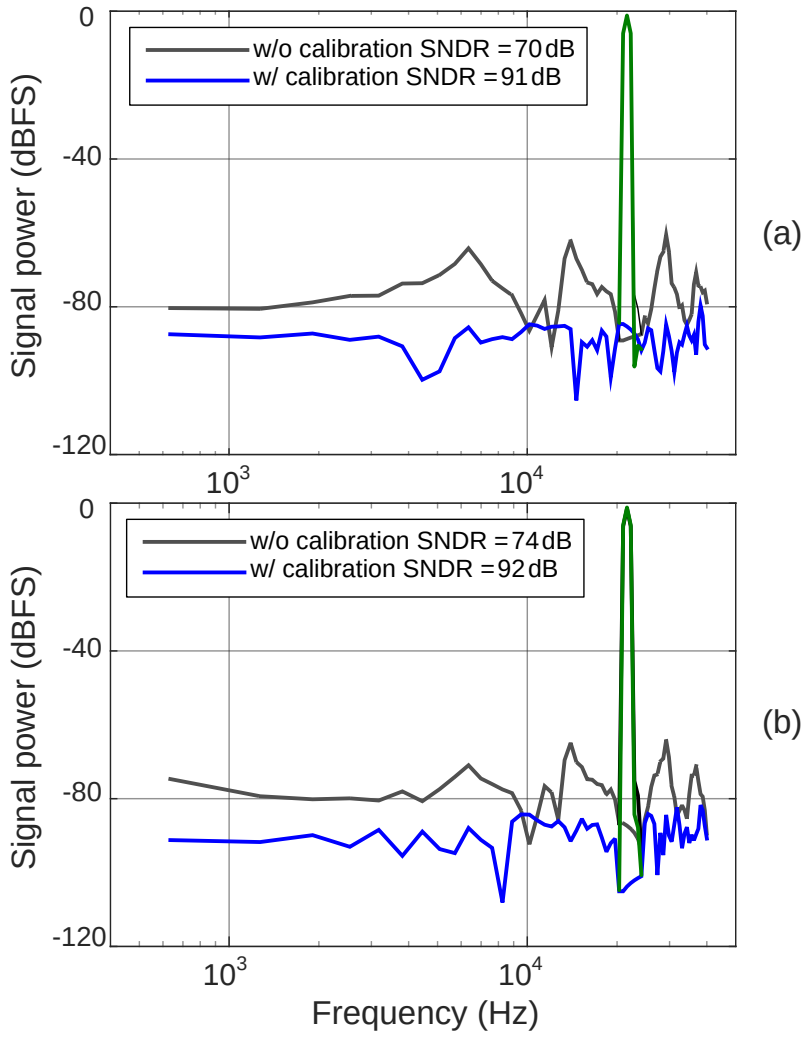


Figure 6.30: SAR ADC output spectra (128-fft) for two Monte Carlo simulations ($P_S = -0.1$ dBFS).

Chapter 7

Chip implementation, Measurements and Comparison

In this chapter, the system implementation is discussed, including critical blocks layout and chip area distribution, in addition to the chip measurement setup and board design. The measured ADC performance is also detailed and the design is compared to SoA publications.

7.1 Layout - Major milestones

High linearity ADC design conventionally requires very careful, sophisticated and large area layouts. However, one of the major objectives of the proposed concept is to allow the high linearity at low area and relatively simple layouts. Nonetheless, few design blocks require special care to guarantee the performance without expanding the area consumption.

7.1.1 CDAC layout

Although, the CDAC features a coarse resolution of only 7 bit, errors due to layout parasitics and mismatch should be lower than its coarse resolution, to allow for correction with the fine DAC. The unit cap-switch-buffer structure, introduced in 6.1.2, is combined with common centroid placement as shown in Fig. 7.1, to guarantee a post-layout matching beyond the coarse resolution.

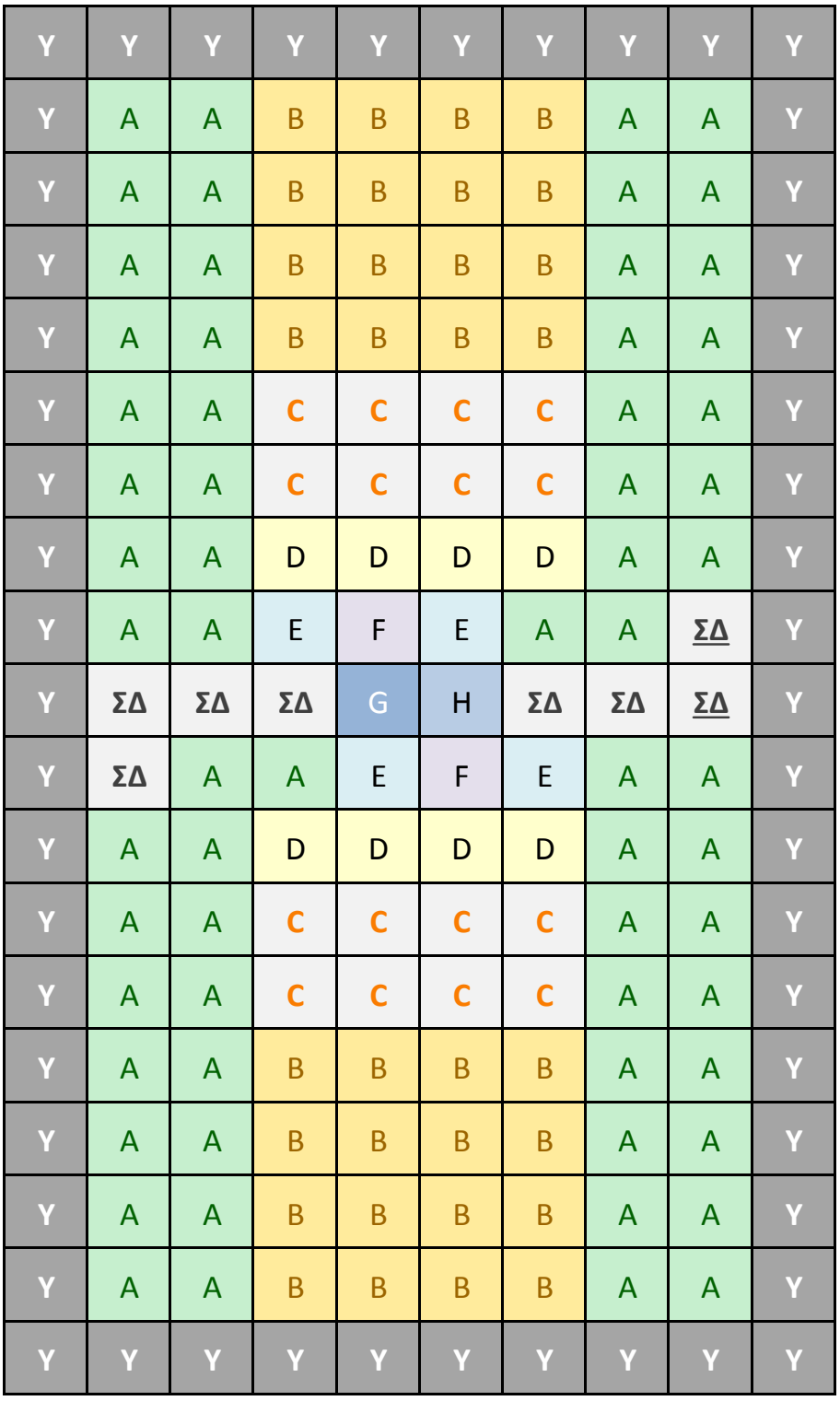


Figure 7.1: 7-bit CDAC layout pattern implementing common centroid concept.

Moreover, to allow fast/automated implementation with the pattern generator, a new concept for automated routing is developed, which is also based on routing unit cells. This is shown in Fig. 7.2, which includes the layout of the capacitor-buffer-switch-routing unit cell. The metal-oxide-metal (MOM)

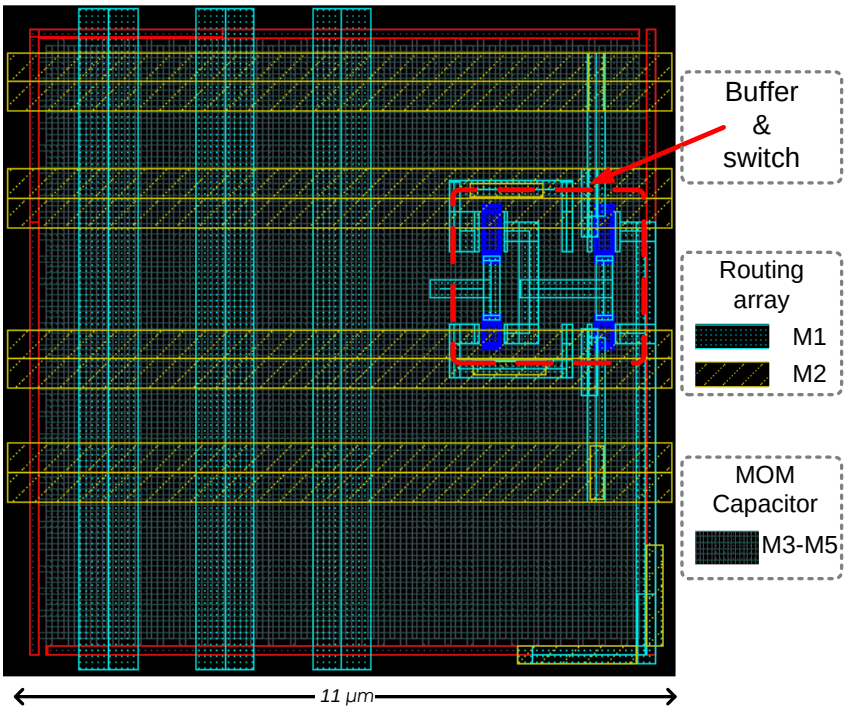


Figure 7.2: 127-fF CDAC unit cell including capacitor, switch, buffer, and routing elements.

capacitor is implemented using the metal layers M3, M4 and M5. Thanks to its relaxed unit size, the area underneath the capacitor is used to implement the local buffer and switch pair, the routing matrix uses vertical and horizontal lines of layers M1 and M2 respectively, while the layer above the MOM structures (M6) connects the capacitor top-plates. By using the pattern generator to place the unit cells (with respect to Fig. 7.1), the routing matrix is automatically connected by overlapping the routing metals of neighboring cells. Finally, to connect the cells within one CDAC group (belonging to one bit), selective vias are added between metals M1 and M2, accordingly. Therefore, the area consumption of the complete CDAC layout (cf. Fig. 7.3) is determined by the capacitors area without additional area for internal routing.

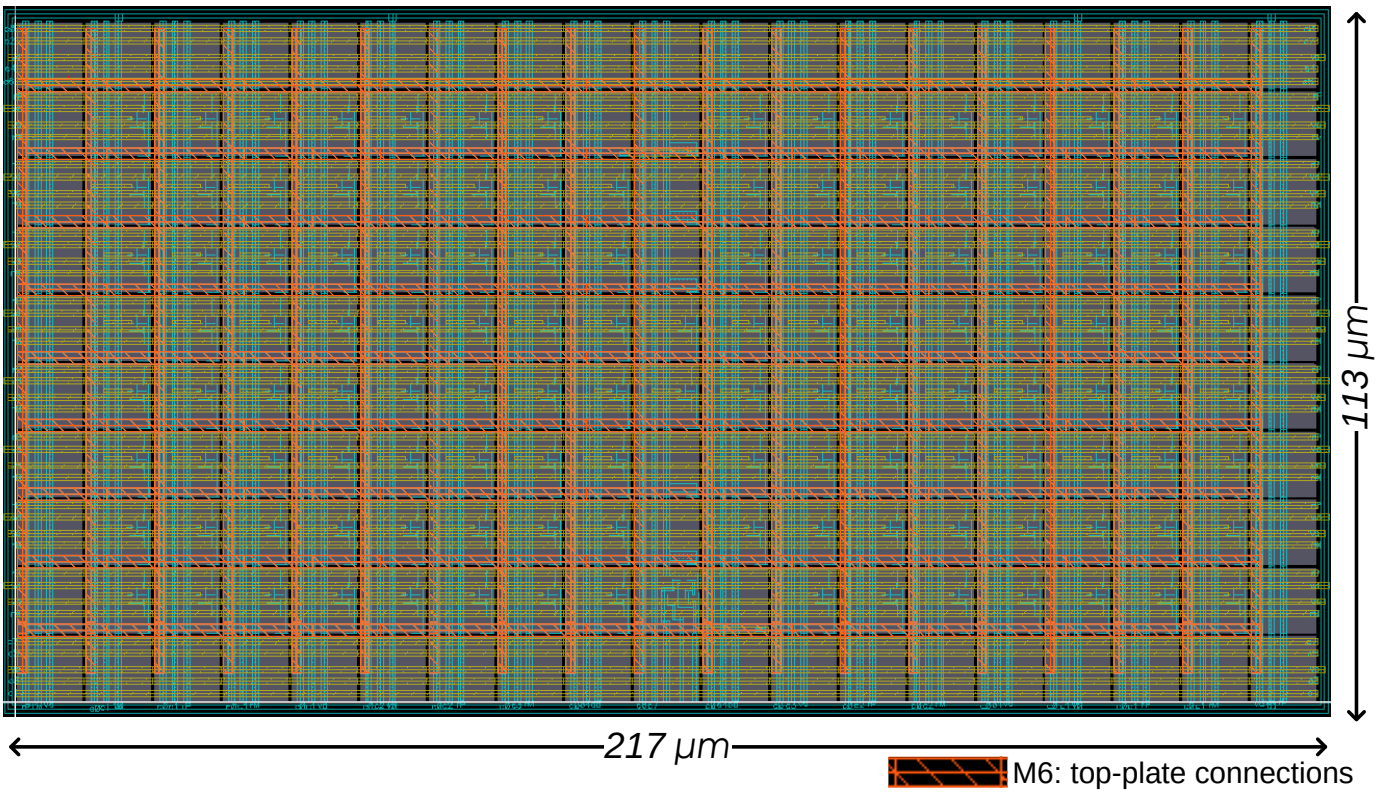


Figure 7.3: Single-sided CDAC layout.

7.1.2 Fine comparator

The comparator layout can potentially increase its offset and decision delay, which are of minor importance, especially for low speed ADC operation. However, the eye-opening comparator structure is highly sensitive to layout parasitics. This sensitivity affects two parameters in the comparator: the VCO oscillating frequencies and the phase detector (PD) dead-zone, which both affects the comparator performance.

Layout scheme: A differential layout is favored in differential structures, to reduce the mismatch and improve common mode rejection, and specially for comparator offset reduction. A differential layout concept of the fine comparator is illustrated in Fig. 7.4. Thereby, each VCO is split into seven cells (6x inverters and 1x NAND), each two identical cells from the two VCOs are merged in one differential cell cf. Fig. 7.4. This concept reduces the mismatch between two VCOs. However, it significantly increases the cross-talk between

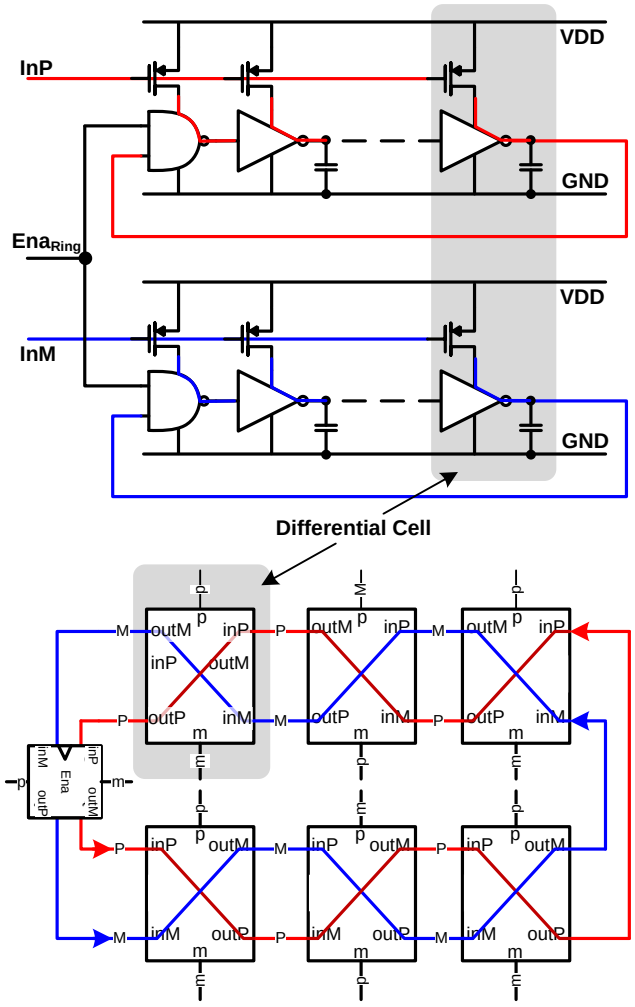


Figure 7.4: Fully differential layout concept of the fine comparator VCOs.

the two VCOs, thus it degrades the comparator performance. Thereby, for inputs smaller than 4·LSB, the comparator decisions are input independent and are dominated by the cross-talk effect[1]. To avoid this degradation, a non-differential layout was implemented for the two VCOs, and to attenuate the layout-related mismatch, the complete comparator is split into two identical chains (differential pair) cf. Fig. 7.5, each including a VCO and half PD (one DFF), and one layout is implemented once and copied for the two chains.

Layout parasitic: A concise layout is necessary for the fine comparator to limit the routing parasitics and to not drift the performance. Additionally, the nominal design is tuned to counteract parasitic effects. For instance, the

[1]This was evaluated through initial post-layout simulations.

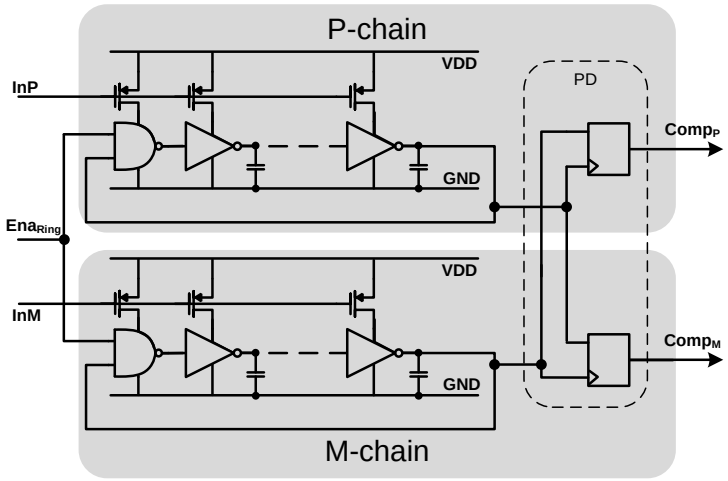


Figure 7.5: The fine comparator layout as two identical chains.

capacitor at the inverter outputs in Fig. 7.5, are reduced from about 40 fF nominal value to about 20 fF to account for parallel connected parasitic capacitances, in order to keep the nominal VCO oscillating frequency approximately unchanged after layout. Similarly, the DFF in the PD is redesigned after the parasitic extraction. Therein, additional DFF internal delays lead to increased dead-zone in the PD, as a countermeasure the transistor sizes (W) in the DFF are increased.

7.1.3 Floor-planning and shielding

Efficient floor planning and good positioning of different blocks are important aspects in mixed-signal chip layout, especially with the aim for a minimized area consumption. By considering the nature of the proposed design, which combines not only digital and analog blocks, but even the analog part includes both high speed switching (e.g. VCOs and FIR current array) and low speed high accuracy nodes (sampled input at CDAC top-plate), feasible block placement and shielding become highly demanded.

In order to allow for area saving by placing the different blocks within close proximity, double and triple grounded guard-rings are used as shields between different blocks. These guard-rings surround the critical analog blocks (CDAC, op-amp) and similarly the high speed / digital blocks (fine comparator, FIR shift registers). Additionally, the digital part is placed at the maximum

available distance from the sampling CDAC, then it is followed by the high speed VCOs. On the other hand, two power supplies at 1.1 V are routed independently, one is for the high speed switching blocks (digital and VCOs) and the other is for the 1.1 V analog parts, which suppresses disturbances through the power supply lines.

7.2 Chip area break-down

Figure 7.6 shows the chip die photograph after manufacturing in a TSMC 40 nm CMOS process. The ADC active area[2] is only 0.074 mm^2. The approximate area breakdown is shown in Fig. 7.7, and the full layout with area distribution

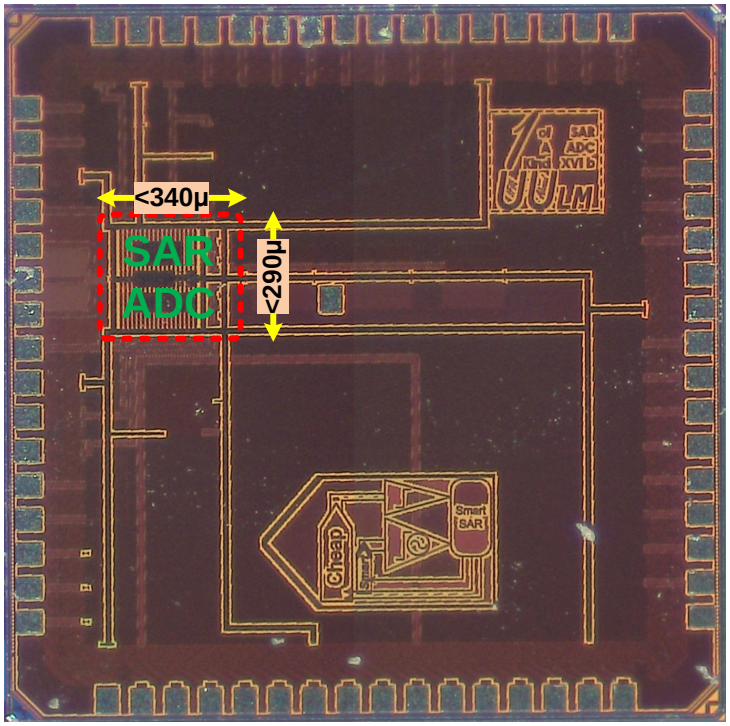


Figure 7.6: Chip photo.

is presented in Fig. 7.8. The active area is dominated and mainly determined by the sampling capacitor, concurrently forming the coarse CDAC array, which was scaled at the minimum requirements for 16 bit noise (kT/C) performance.

[2]The full chip area is fixed to 2*2 mm^2, in order to allow fabrication through the MPW (Multi project wafer) program runs.

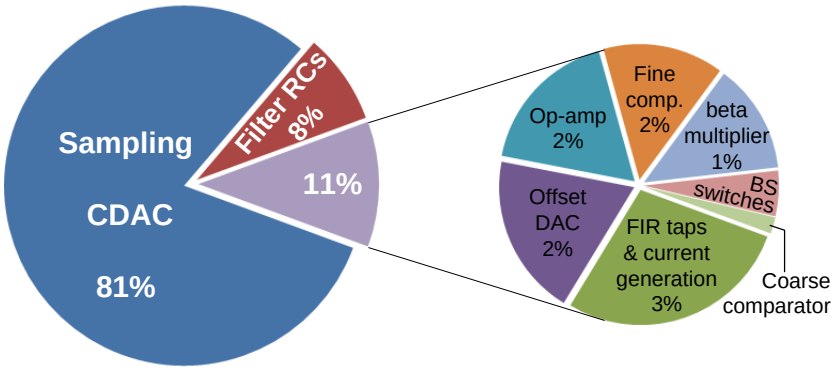
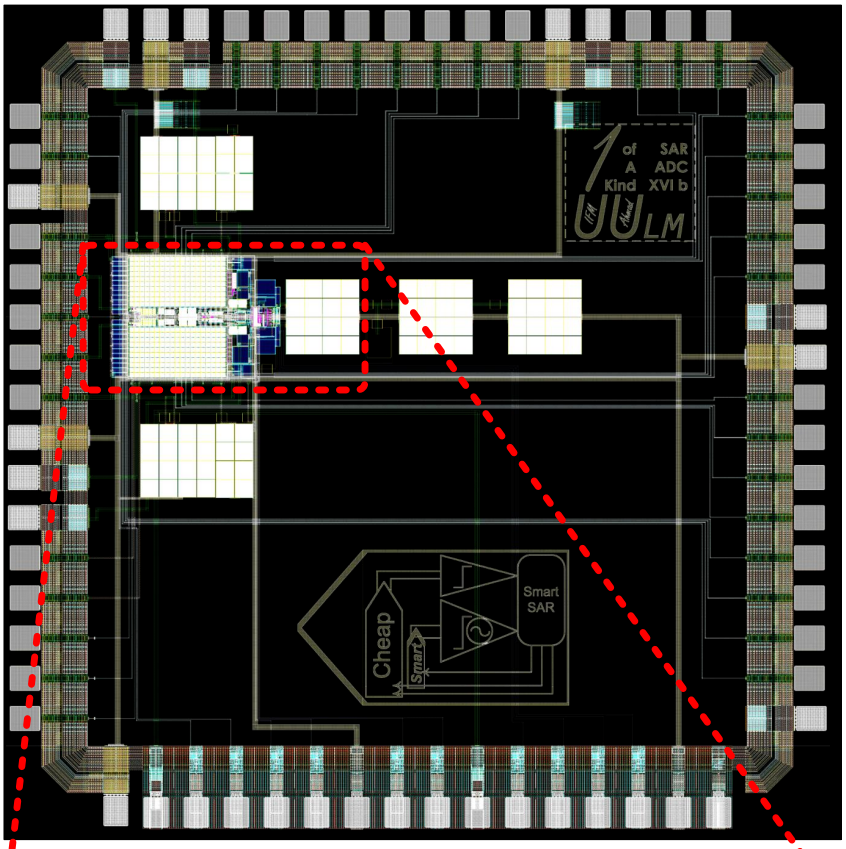
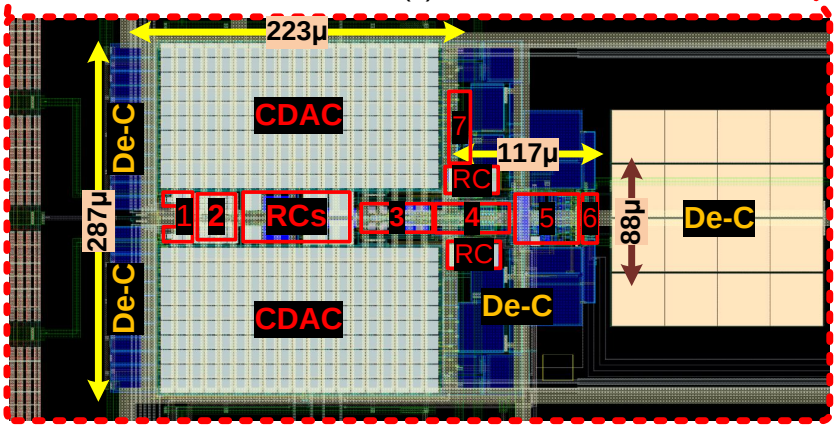


Figure 7.7: Chip active area breakdown [73] © 2018 IEEE.

Given the dominance of the CDAC area consumption, the advantage of the hybrid DAC using the ΣΔ modulator becomes very obvious. If a 16-bit CDAC would need to be scaled for matching, its size would be significantly larger, and thus it would produce a larger area consumption. The second dominant area consumption (though non-comparable to the CDAC) comes from the RC filters used in the analog low-pass filter in the ΣΔ DAC and the relatively big resistors used for biasing and reference current generation. Still, the RC filters only need 10% of the CDAC area. It is worth to mention that the additional offset compensation CDAC consumes a non-significant share with about 2% of the overall area. The fine comparator consumes about 1.6% of the total area due to symmetrical layout and multi-level guard-ring shielding, while the coarse comparator consumes only 0.2%.



(a)



1: BS-switches & 1st comparator, 2: CDAC-offset,
3: Op-amp, 4: Fine-comparator, 5: FIR Current sources,
6: FIR shift registers, 7: Current reference.

(b)

Figure 7.8: Full chip layout and active area distribution.

7.3 Measurement setup

In order to perform the ADC measurements on the fabricated chip, the SAR ADC loop is completed with the digital part implemented on an FPGA. A PCB is designed to condition the input signals and interface the chip with the signal generators and the additional FPGA board. Figure 7.9 shows the complete SAR ADC test structure including the manufactured chip, the digital blocks, the connections between the two and the ADC inputs and outputs.

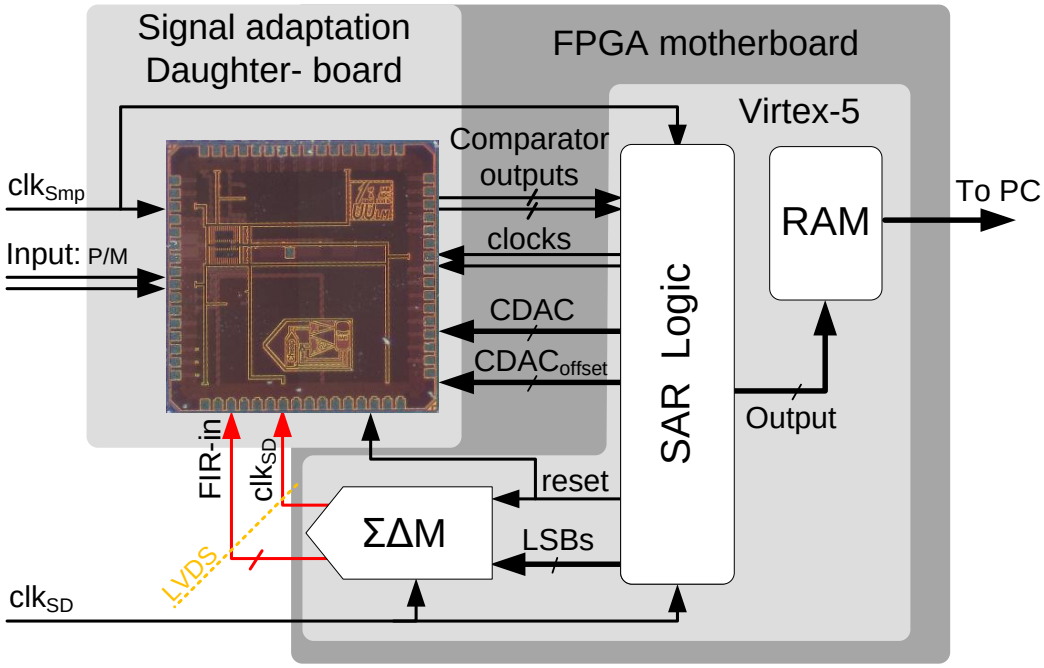


Figure 7.9: Complete SAR ADC diagram including logic blocks on FPGA.

7.3.1 Two-board setup

The signal conditioning board (daughter-board) interfaces the packaged chip, using a 64-pit QFN package holder. Additionally, a motherboard with embedded Xilinx Virtex-5 FPGA chip is used. The daughter-board is plugged into the FPGA motherboard using an available set of three 40-pin connectors, as shown in Fig. 7.10. The interface between the two boards introduces only slight delay for most connections, which are at low speeds (<10 MHz). However, few

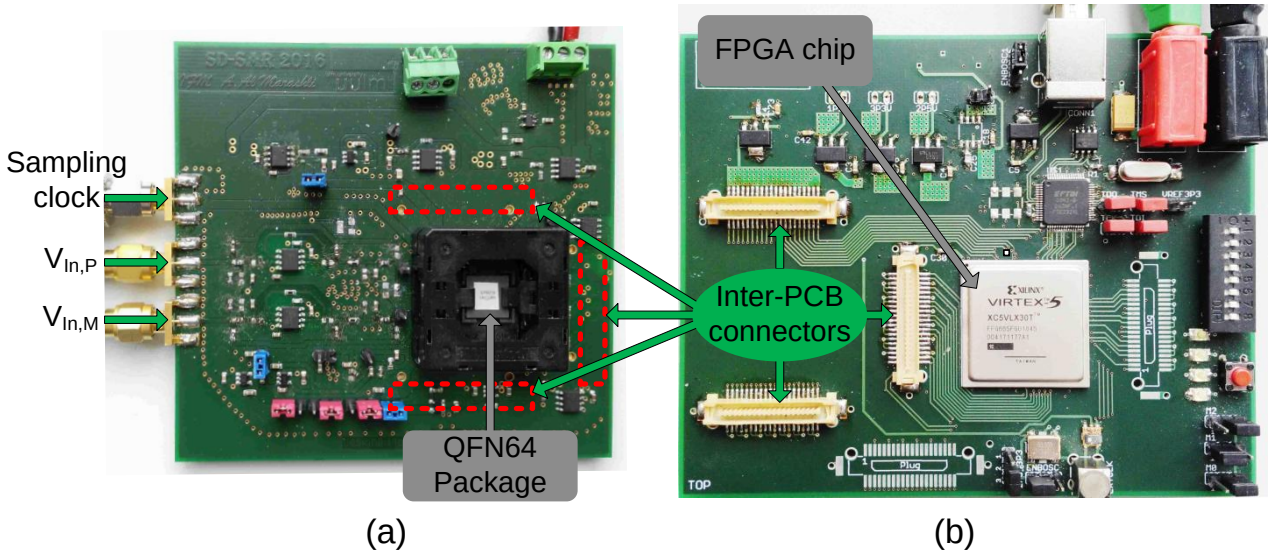


Figure 7.10: Two-board measurement setup: (a) daughter-board holding the packaged chip, (b) mother-board with FPGA chip.

connections operate at high speeds around 150 MHz ($\Sigma\Delta$M outputs and clock). Therefore, Low Voltage Differential Switching (LVDS) connections are used for these high speed interfaces.

7.3.2 Signal conditioning

The daughter-board implements four main functions, besides hosting and interfacing the manufactured chip. Those include power supply generation (2.5 V /1.1 V analog /digital), SAR reference voltage generation and buffering with decoupling capacitors close to chip pins, LVDS reception and transmission with on-board receivers and transmitters and differential input conditioning. The last function is the most critical, because it is of high resolution and linearity targets. The board implements a similar concept to the SAR ADC evaluation board in [81]. After generating the differential inputs using the low distortion signal generator (Stanford Research DS360), the daughter-board implements quasi-differential routing, low-pass filtering and optional buffering. A pair of low pass RC filters is used in front of the chip differential input pins to limit the inputs (and buffers) noise bandwidth, it also improves the aliasing rejection. However, it cannot replace the AAF, because its bandwidth has to be larger

than the Nyquist bandwidth to allow full resolution settling at the sampling capacitors [82, 83].

7.3.3 Digital blocks on FPGA

The digital logic implemented on the FPGA includes modules for the SAR logic and ΣΔM, which complete the SAR ADC loop. It also includes data storage, transmission and reception modules for communication with PC and a control unit, which controls the digital operations by enabling the individual blocks based on the received commands from a PC. As shown in Fig. 7.9, the FPGA receives the high speed clock (clk_{SD}), which synchronizes all digital modules, it also receives the low speed sampling clock (clk_{Smp}), which is used to synchronize ADC operation. Moreover, four modules are implemented for calibration procedures of CDAC elements and for coarse and fine comparator offset measurements and background compensation.

7.4 Measurement results

7.4.1 Main measurement steps

Initial meaurements: The ADC is measured initially without calibration over two steps: First, the coarse phase (only CDAC) is evaluated without the I-ΣΔ DAC. Two output spectra with different input frequencies are shown in Fig. 7.11 (red curves). Thereby, the measured SNDR is 47 dB (7.6 bit). The spurious tones are not dominated by the odd-order HDs; instead, common mode disturbances including 50-Hz and 100-Hz tones are significantly present, which is due to the monotonically switched CDAC. Then the fine output is enabled (with the I-ΣΔ DAC), and SNDR = 64 dB is measured, which is limited by the CDAC mismatch, hence the dominant tone is now located at $3{\cdot}f_{in}$ with SFDR = 69 dB, as in the two blue spectra in Fig. 7.11. Therefore, the CDAC features approximately an 11-bit linearity without calibration, which is comparable to the simulation results in section 6.4.2.4.

Calibration with system CDS: Figure 7.12, includes SAR ADC output spectra after enabling the calibration, as presented in chapter 5. Initial calibra-

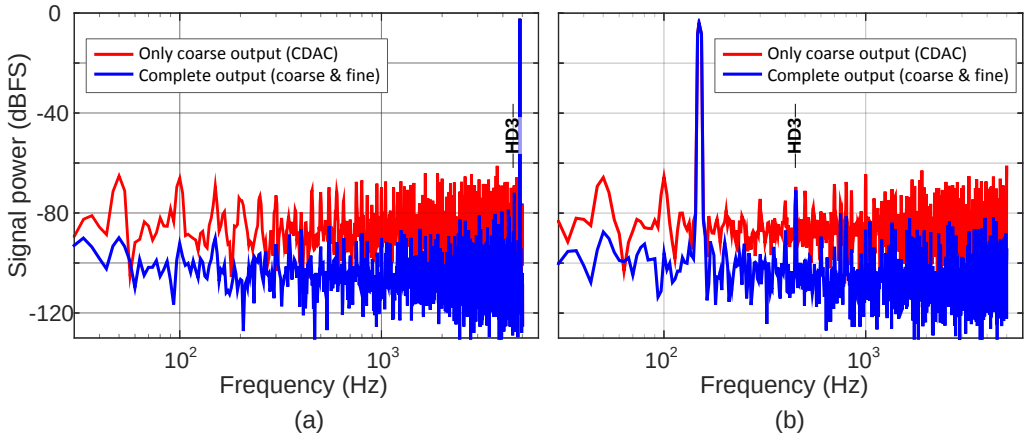


Figure 7.11: Uncalibrated SAR ADC output spectra (4000-point fft) at two input frequencies.

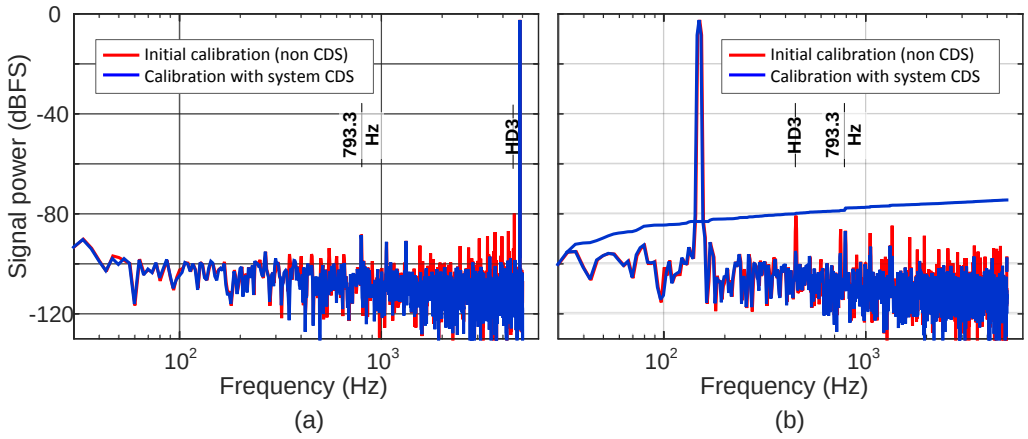


Figure 7.12: SAR ADC output spectra (4000-point fft) at two input frequencies, after initial calibration w/ and w/o system CDS.

tion does not include system-level CDS (red curves in Fig. 7.12). Thereby, an SFDR = 78 dB is measured. Next, system-level CDS is employed during calibration, to attenuate low frequency noise and sampling distortion (on the zero input to the calibration), which allows for an effective averaging for the CDAC estimation values (calibration output). Finally, an SFDR = 85 dB is obtained by CDS-enhanced calibration (blue curves in Fig. 7.12).

Digital interferance: After applying the CDS-enhanced calibration the SFDR is no more determined by input signal HDs. In the two examples of Fig. 7.12 (the blue curves), the dominant spurious tone is located at 793.3 Hz, and it is independent of input amplitude and frequency. However, its frequency

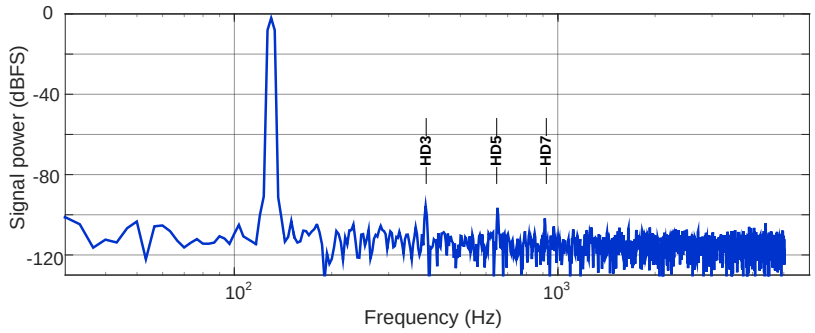


Figure 7.13: SAR ADC calibrated output spectrum (4000-point fft) after clock-gating for digital disturbance attenuation.

depends on the sampling clock frequency and also on the ΣΔM clock ($f_{\Sigma\Delta}$), which is routed from the FPGA-chip to the FIR logic array on-chip. To attenuate the distortion caused by the FIR logic, the ΣΔM clock is disabled during the input sampling time (sampling clock: high), which causes no functional change, as the digital part is normally in reset phase then. Figure 7.13 shows the ADC output spectrum after applying the clock-gating concept on the FIR digital part. Thereby, the spurious tones are dominated by odd-order HDs, and the SFDR is 94 dB.

Comparator CM and decision averaging: The fine comparator shows high sensitivity to the input common mode level (as discussed in section 6.3.3.1). Thereby, improved performance (SNDR) is measured at higher common mode (about nominal + 250 mV). This improvement is mainly related to increased signal gain, thus better immunity to distortion and low frequency noise, while thermal noise performance can be degraded at higher V_{CM} (see section 6.3.3.1). However, this is accompanied by higher speed and lower power consumption (with faster decisions). To compensate for this, thanks the faster operation, the comparator output is averaged for the last seven SAR steps, by applying voting decision similar to [32], with up to 12 votes. Figure 7.14 shows two ADC output spectra with and without averaging; the integrated noise is reduced between 2-4 dB using averaging.

Calibration beyond ADC resolution: As discussed in section 5.3.3 the calibration resolution is enhanced beyond the ADC effective resolution by averaging repeated calibration at extended nominal resolution. Therefore, at least 2^8-time oversampling is approximately required during the startup calibration,

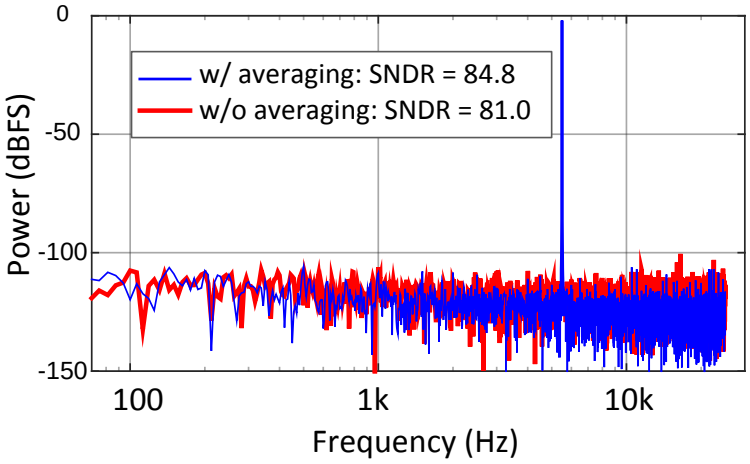


Figure 7.14: SAR ADC output spectra (8000-point fft) with and without comparator averaging.

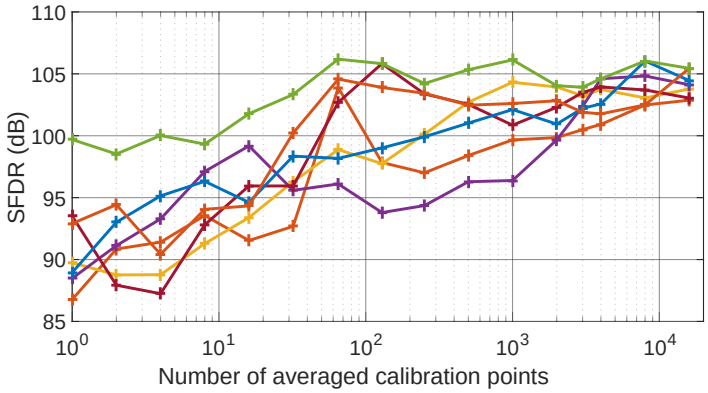


Figure 7.15: Calibration improvement over number of averaging points in seven different measurements of a single DUT.

to achieve a linearity above 105 dB, using an ADC effective resolution around 84 dB, in addition to the system CDS. Consequently, the calibration requires about 2^{13} Nyquist cycles for 2*8 capacitors in the CDAC. Figure 7.15 shows the calibration performance improvements (by SFDR) with increased averaging points (calibration oversampling), for different measurements of the same chip. While on average a 500-point averaging nominally allows for linearity over 100 dB, a statistically bad (noisy) measurement sample could require longer averaging (more estimations) to reach it. Finally, these techniques combined allow one to perform the calibration beyond the SAR ADC resolution with no additional analog components, within a relatively short time at startup.

7.4.2 ADC static evaluation - INL & DNL

Usually, high resolution Nyquist ADCs report the ADC linearity statically using INL and DNL measures. Those measures either replace dynamic linearity measurements (e.g. by SFDR), when it is not feasible to perform the dynamic measurement or to generate a high linearity dynamic input, or they are additionally provided, if the dynamic performance is significantly degraded compared to the DAC static linearity. Thereby, the DNL and INL exclude the dynamic distortion, hence they provide optimistic measures. The INL and DNL are commonly estimated by the histogram testing method [86], especially at high resolutions, when it becomes not feasible to provide a higher resolution DAC for static input generation.

To perform the histogram method (also called code density test), the ADC is usually operated with a sinusoidal input signal. The ADC outputs are stored into code bins, which represent the output codes, hence a 16-bit ADC requires 2^{16} code bins. The static linearity is calculated by comparing the resulting histogram values with the ideal probability density function of the input samples. This method requires fairly large data recordings to provide a sufficient confidence level. Based on [86], testing a 16-bit ADC with DNL error of 0.5 LSB and a 95% confidence level requires more than 1.5 million samples. For a lower DNL error or an increased confidence level, the required data size is significantly increased.

One the other hand, INL and DNL measures represent mainly the mismatch effect on the ADC element array (CDAC capacitors in SAR). Therefore, they are less relevant for the proposed hybrid DAC; thanks to the applied redundancy, the code transitions in the ADC characteristic curve represent changes of the I-$\Sigma\Delta$ DAC output, which employs an intrinsically linear 1.5-bit D/A and dose not switch in/out scaled analog elements. Therefore, typical mismatch-related DNL/INL errors are not expected in this design. Additionally, due to the limited storage size in the current measurement setup (in the implemented FPGA), it was not feasible to implement the static linearity test in the current setup. Therefore, the ADC linearity is reported using dynamic linearity, which includes both static and dynamic effects, as shown in the following sections.

7.4.3 ADC dynamic performance

The ADC is measured at $f_S = 80\,\mathrm{kS/s}$, with a full scale sinusoidal input. Fig. 7.16 shows ADC output spectra for three input frequencies.

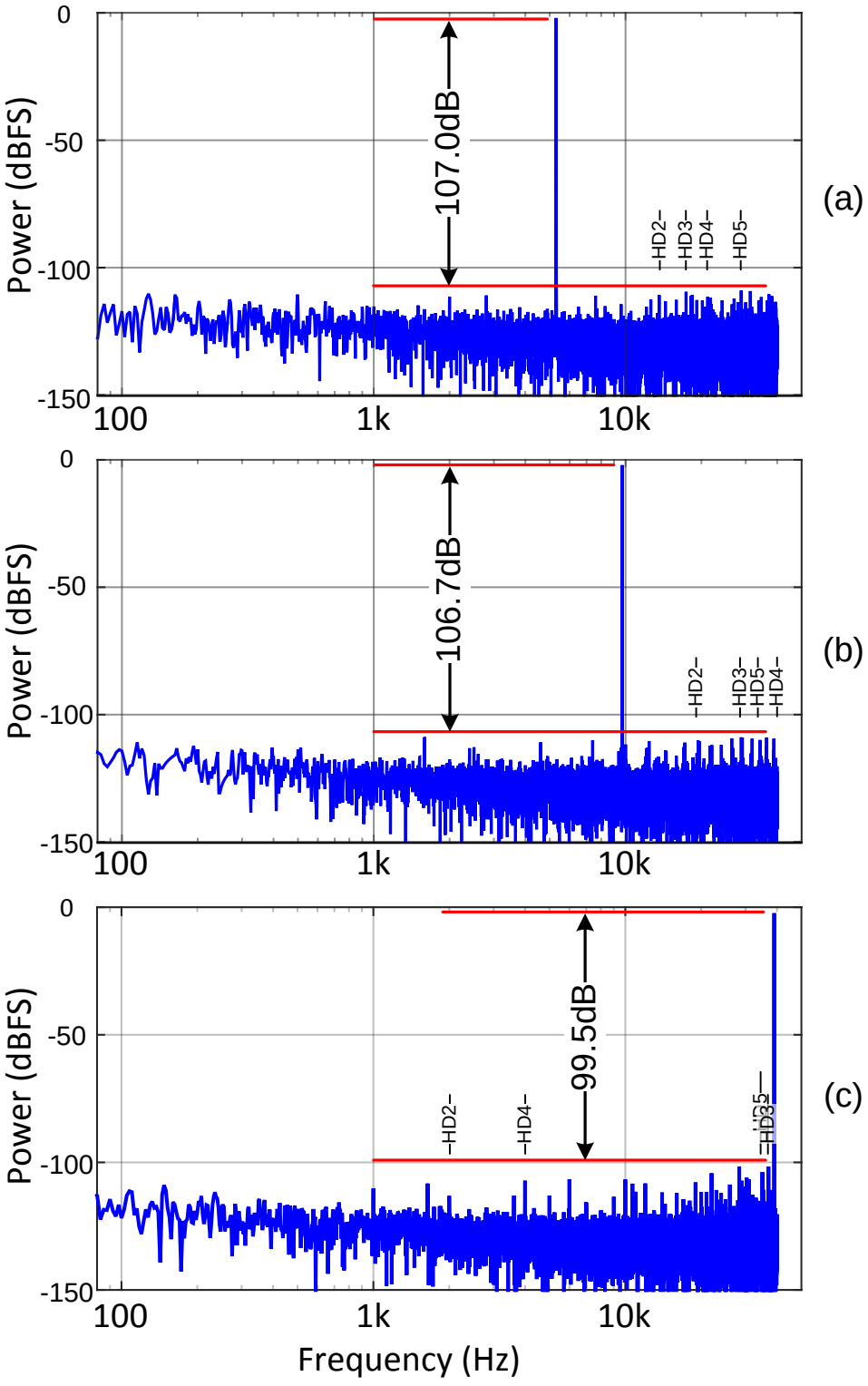


Figure 7.16: SAR ADC output spectra (32000-point fft) at (a) 5.3 kHz, (b) 9.7 kHz and (c) 39 kHz input frequencies [73] © 2018 IEEE.

Measurements over Nyquist bands: The measured peak SFDR is 107 dB, SFDR remains above 104 dB for input frequencies below $f_S/4$. Beyond $f_S/4$, the SFDR is limited by the quality of the used signal source (DS360). Fig. 7.17 shows the measured SNDR and SFDR over input frequencies of the presented prototype together with the measurements of an 18-bit commercial ADC [84] (applying the same signal range as that used for chip measurements), to determine the limitation of the source. The measured SNDR is 84.8 dB at

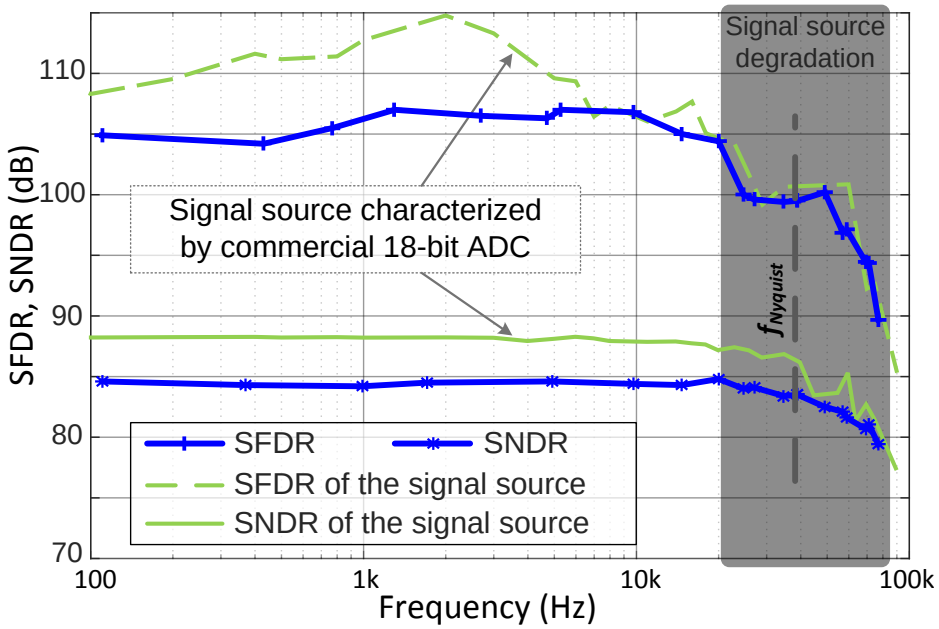


Figure 7.17: Measured SAR ADC performance over input frequency [73] © 2018 IEEE.

an input frequency of $f_S/4$, it remains above 83.5 dB for the entire Nyquist-bandwidth, which is about 10 dB above the state-of-the-art performance for Nyquist rate SAR ADCs [5]. The ADC is measured also in the second Nyquist-band, where the SNDR and SFDR are mainly limited by the signal source, nonetheless the measured SNDR and SFDR up to 71 kHz remain above 81 dB and 94 dB respectively.

Oversampled ADC: The oversampling performance is reported in Fig. 7.18. The ADC achieves an SNDR of 86.5 dB for a 20 kHz bandwidth with OSR = 2, and an SNDR above 90 dB for a 5 kHz bandwidth with OSR = 8. Thereby, the improvement is less than 3 dB per OSRx2, due to the dominance of 1/f noise, becoming more prominent the moment thermal noise is averaged by oversampling.

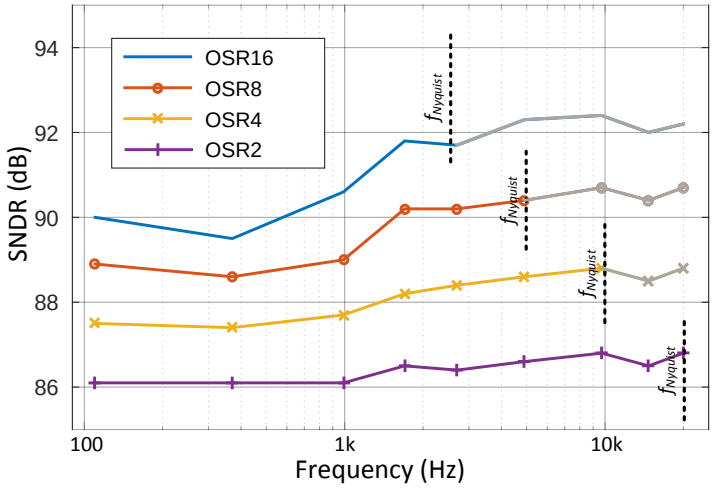


Figure 7.18: Measured SNDR of the SAR ADC in oversampling modes.

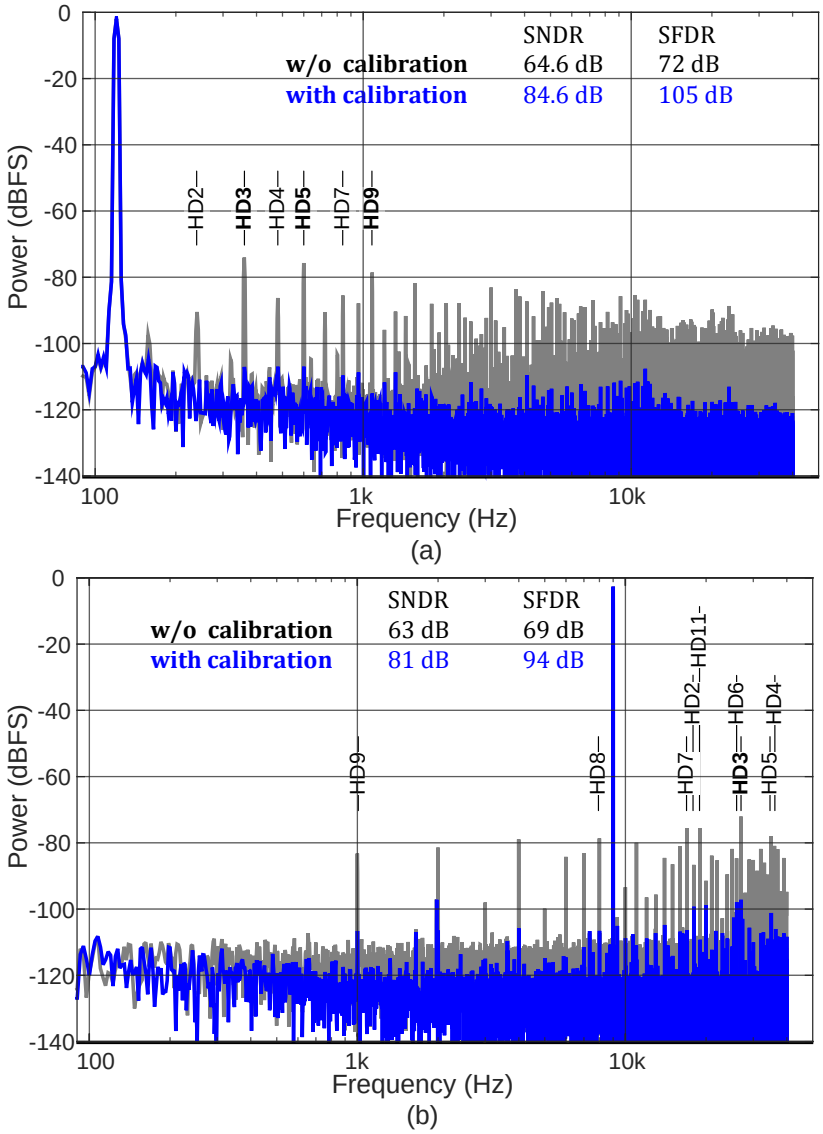


Figure 7.19: Calibration effect on SAR ADC output (32000-point fft) at 80 kS/s, (a) $f_{in} = 120$ Hz, (b) $f_{in} = 71$ kHz, modified from [73] © 2018 IEEE.

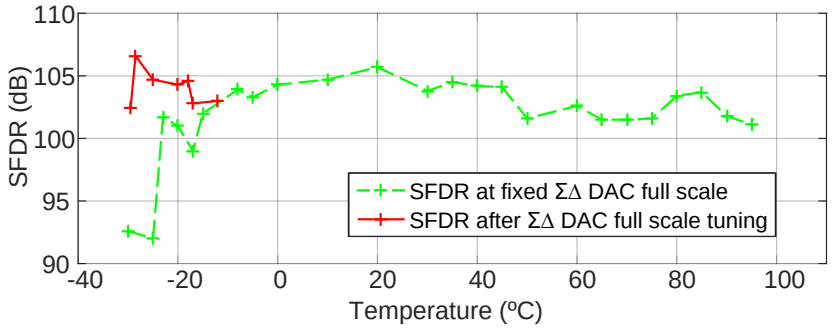


Figure 7.20: Measured SFDR over temperature variation [73] © 2018 IEEE.

Calibration effect: Fig. 7.19 shows two ADC output spectra before and after calibration, on two input frequencies near DC and near the end of the second Nyquist-band.

7.4.4 Measurements over temperature and voltage variations

Due to PVT variations, the scaling factor between the coarse and fine DAC outputs can drift from its nominal value. This is corrected by a digital calibration of the gain error between the two parts (one element calibration). This gain correction could be even integrated as a background calibration, for example, by dedicating one time slot per SAR conversion cycle, in a similar fashion to the background offset calibration in [85]. Fig. 7.20 shows the measured SFDR, which remains above 100 dB for the whole temperature range – except for very low temperatures, where the drop is mainly due to an excessively decreased full scale of the ΣΔ DAC leading to a saturated fine DAC output. To verify this, the solid red curve in Fig. 7.20 is measured after externally up-tuning the ΣΔ DAC full scale.

Also, supply voltage variations can affect the ADC performance. Especially as the fine comparator shows a sensitivity to common mode changes, it is equivalently affected by supply changes. In Fig. 7.21, the measurement results are shown over supply changes of the fine comparator. The solid curve shows the drop in performance due to a changing supply voltage. Even though almost ±10% supply variation is tolerated, while SFDR is above 100 dB, the performance drop is obvious. As a countermeasure, the red-dashed curve shows

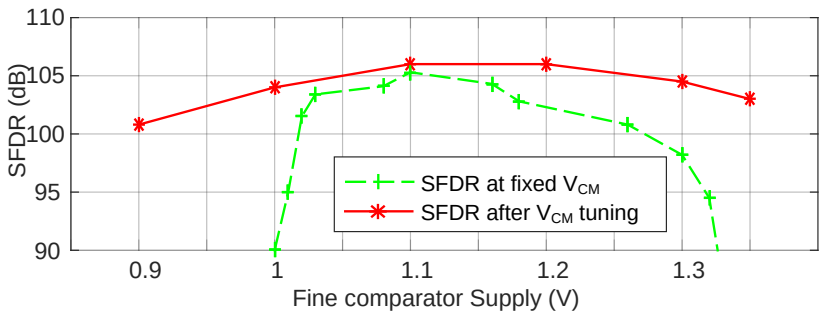


Figure 7.21: Measured SFDR over fine-comparator supply changes [73] © 2018 IEEE.

the same measurements over supply change, but with the common mode (V_{CM}) tuned to track the supply changes. This keeps the SFDR over 100 dB for supply voltages from 0.9 – 1.35 V. Advantageously, V_{CM} tuning could be implemented by readjusting the reset phase of the monotonically switched CDAC based on the supply voltage variation.

7.4.5 Power consumption

The ADC core power consumption was estimated from parasitic-extracted simulations to be 101 µW, while in the measurements, the analog filter and reference generation caused a 10% increase to approximately 110 µW. Fig. 7.22 shows the power consumption distribution. In this first prototype, the analog filter is the dominant power consumer, with more than three quarters of the

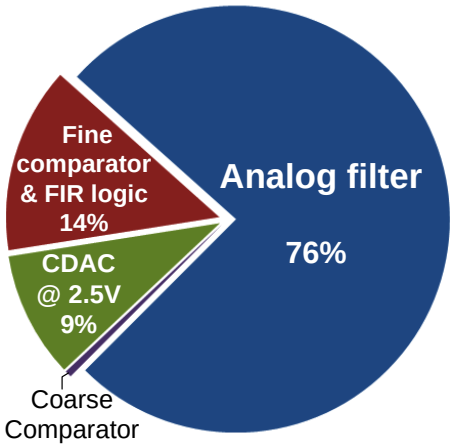


Figure 7.22: SAR ADC power consumption breakdown [73] © 2018 IEEE.

total consumption, which is mainly statically consumed from the 1.1 V power supply. On the other hand, only about 9% of the power is consumed from the 2.5 V CDAC reference, and less than 1% is consumed from the 2.5 V power supply. A synthesis of the digital part (currently implemented on an FPGA) in the same technology using Synopsys software occupied less than 5% of the reported area, and consumed about 30% of the reported power consumption. This shows that the area is insignificant, but the power consumption could be reduced in the next prototype by choosing a $\Sigma\Delta$ DAC with higher order, thus a lower sampling rate and using low power digital libraries.

7.4.6 Performance evaluation against SoA

Fig. 7.23 compares the ADCs SoA energy plots, showing the changes during the PhD duration, and comparing the reported performance to the current SoA. Although, a major advance towards high resolution Nyquist conversion has been reported in the last few years, compared to the measured performance, all other reported Nyquist rate ADCs are about one order of magnitude worse in either power efficiency or performance. Only [47] (and its recent applications in [49], [87]) reported higher Nyquist rate performance but measurements are reported only at a single input frequency of $f_{\text{in}} = f_S/5000$, without specifying dynamic linearity (SFDR). Also, [47] consumes about 75x higher core area than this design, in addition to the old technology node used (180 nm), which is required for good analog processing especially in the residual amplifier. Moreover, the recently published pipelined SAR ADC [87], in 180/500 nm technology, proposed a background calibration engine, which consumes an estimated power of 6.8 mW (besides 12.9 mW consumed in the ADC). It reports an SFDR above 130 dB around DC, which drops to 84 dB at Nyquist frequency. On the other hand, commercial ADCs reported higher performance as in [88]. Nonetheless, commercial datasheets often include very limited design information and no complete measurements to allow a fair comparison with SoA.

Table 7.1 presents a design summary and comparison to a selection of state-of-the-art Nyquist rate ADCs performing high-resolution, high-efficiency conversion. It is worth mentioning, that I-$\Sigma\Delta$ ADCs – despite oversampling the input – perform a Nyquist rate operation and provide very high resolution for relatively low conversion rates [89, 90]. Due to the DAC hybrid nature

in the proposed SAR ADC, the I-ΣΔ DAC provides only coarse resolution. Therefore, it features relaxed speed and noise requirements compared to I-ΣΔ ADCs, which makes it a better candidate especially for higher conversion rates. According to Table 7.1, the presented prototype competes the state-of-the-art in terms of linearity. In contrast to the state-of-the-art, this is achieved not at the cost of more area consumption, but even at the lowest reported area, and using the smallest technology node.

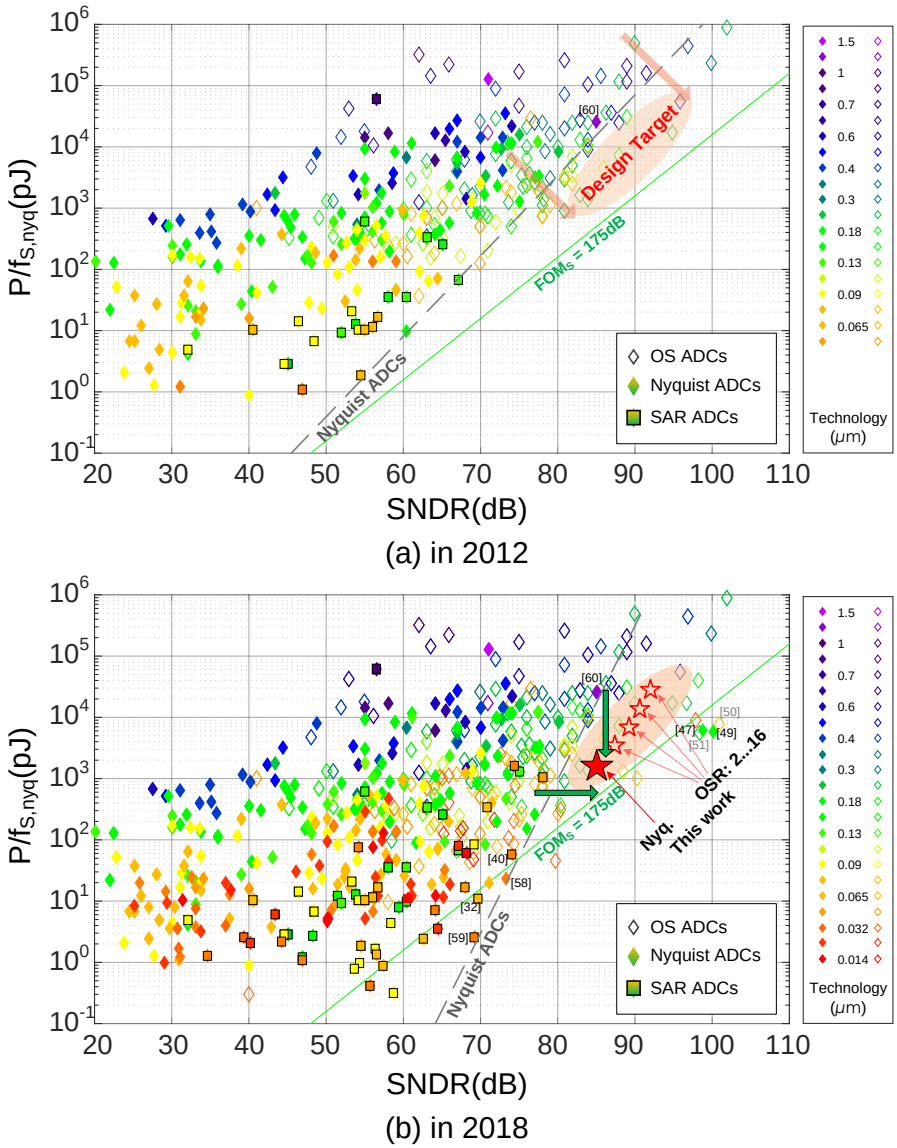


Figure 7.23: State of the art ADCs performance: Energy/Nyq.sample [5], (a) at PhD. start, (b) current.

Table 7.1: Performance Summary and Nyquist Rate ADCs Comparison

	Harpe [32] ISSCC'14	Bannon [47] VLSI'14	Xu [91] ISSCC'17	Krämer [24] JSSC'15	Shim [40] JSSC'17	Zhang [90] JSSC'17	Li [87] ISSCC'18	This work
Architecture	SAR	Pipe. SAR	Pipe. SAR	SAR	SAR	I-ΣΔ	Pipe. SAR	SAR
Technology	65 nm	180 nm	65 nm	40 nm	40 nm	180 nm	180/500 nm	**40 nm**
Resolution (bit)	14	18	14 (8+10-red.)	14	15	16	20	16
Area (mm^2)	0.18	5.74	0.342	0.236	0.315	0.5	3.78	**0.074**
Power Supply (V)	0.8	5 / 1.8	not rep.	2.5 / 1.2	not rep.	1.5	5 / 1.8	2.5 / 1.1
Power (μW)	0.35	30520	21800	54500	1.17	34.6	19700	110 + 30^{+}
$f_{s,nyq}$(kS/s)	32	5000*	35000	35000	20	2	1000	80
$SNDR_{nyq}$ (dB)	69.7	98.6*	75.1	74.4	74.1	96.1**	84 (101.5) xx	**83.5**x **- 84.8**
SFDR (dB)	78.5	not rep.	90-103.1	90-99	78-95.1	not rep.	84-133	**99.5**x **- 107**
FOM_S (dB)	176.3	177.7*	164.2	159.5	173.4	170.7**	158 (175.5) xx	168.1x - 169.4

* Reported for single input at $f_{in} = f_s/5000$. x limited by the accuracy of the signal generator cf.7.17 xx DC performance.

** Reported at $f_{in} = 800$ Hz. + Additional power estimated for digital.

Chapter 8

Design outlook and Conclusion

8.1 Design Outlook

The successful measurements of the fabricated chip validate the design concept, which enabled high linearity Nyquist SAR ADC. Further improvements shall focus on exploring the limits of the new concept to maximize speed and/or effective resolution. In the following, a brief discussion for the current limitations is included, with proposals for future changes in the design implementation.

8.1.1 Current limitations

The limitations of the current design are split into speed and resolution limitations. As seen in Fig. 6.8, almost 90% of the conversion time is consumed by the fine phase including the I-$\Sigma\Delta$ DAC and the fine comparator; the comparator decision is extensively delayed only for few decisions (2 or 3) during one conversion. Therefore, the dominant limitation on conversion speed is the I-$\Sigma\Delta$ DAC output settling to the required accuracy (considering redundancy) at each SAR step, which is determined by the slow output settling after the two passive RC stages in the reconstruction low-pass filter. On the other hand, the ADC effective resolution is currently determined by the noise level, which is much higher than the measured nonlinearity. As discussed in section 6.4.2.2, the colored noise (flicker or 1/f) dominates the ADC noise, with corner frequencies above 1 MHz, also transistor-level simulations show that the fine comparator is absolutely the dominant source for this colored noise.

8.1.2 Design proposals

Speed improvement: The ADC conversion time is fully dominated by I-ΣΔ DAC conversion time, due to the slow filter output settling. In the first implementation, a mostly passive filter implementation was favored for reduced power. However, a modified filter with multiple active stages, can provide faster output settling, which would lead to faster conversion, hence a reduced conversion power in the filter (static consumption). Another alternative would include a multi-bit or multi-stage ΣΔM, with sophisticated filter to workaround the linearity limitation. This can be especially effective due to the wide margin between ADC linearity and resolution, in the current design. Thereby, both speed and power consumption can be optimized. On the other hand, a very promising proposal for speed enhancement includes extending the CDAC to full resolution (e.g. by split-C), and limiting the I-ΣΔ DAC use only for calibration. Although, this would increase the CDAC complexity and layout overhead, the intrinsically linear calibration would recover CDAC linearity, while the ADC speed would be significantly boosted with reduced power consumption.

Resolution enhancement: The resolution is currently limited to the fine comparator low-frequency noise performance. It is not very efficient here to reduce the noise by increased sizing, as this would lead to increased kickback noise. Instead, system techniques for low-frequency noise reduction like CDS or chopping are preferred. However, a special attention is required to address the additional distortion accompanying these techniques[1]. Moreover, redesigning the comparator for different operating point (compared to the default used) can reduce the noise level. As seen in the measurements, improved performance is reported at increased CM, but this improvement was accompanied by degraded thermal noise attenuation. As a workaround, the PD, in the fine comparator, can be modified to adapt to the new VCO frequency (with wider dead-zone). On the other hand, recently published oscillator-collapse comparator has an attractive structure [40]. Although it performs similar power scaling to the eye-opening comparator, it excludes the PD, and relies only on a single VCO. This, besides simplifying the comparator structure, allows for an efficient control of the comparator operation by its CM.

[1]For example, effects on VCOs operation or cross-talk between the two VCOs.

8.2 Conclusion

In this interesting journey, a rich research has been conducted to develop new techniques for SAR ADCs, which allow them to enter the high-resolution high-linearity region. Only challenges make the PhD journey more interesting and more effective. My main challenge was to develop unprecedented high-linearity efficient solutions for the SAR ADC structure, the structure that occupied – in the last few years – the major research focus on Nyquist ADCs and has gradually extended into OS ADCs, which boosted the challenge further.

The novel proposals rely on breaking the dependency of ADC linearity on element matching and making use of NS concept in ΣΔMs to improve SAR linearity. Since direct integration of ΣΔ DAC in a Nyquist SAR is not possible, the first approach proposed a novel I-ΣΔ DAC to replace the conventional CDAC. This proposal was discussed in details on system level and implemented on transistor level. The design simulations proved the feasibility of the proposed high-linearity SAR ADC, however, at the cost of high power and area consumption. Therefore, the pros and cons of the first proposal were summarized, to introduce the more efficient second proposal.

The second approach kept the advantages of the first one and avoided its limitation. This was achieved by employing a hybrid DAC structure, which combined a power efficient CDAC with an intrinsically linear I-ΣΔ DAC. Assigning a coarse resolution to the CDAC reduced its implementation cost; simultaneously, it highly relaxed the I-ΣΔ DAC implementation, which provided only a coarse resolution. The SAR ADC architecture was completed with a hybrid/dual comparator to enable low-noise power-efficient conversion. Also, a hybrid supply was used for high input range and better power and area efficiency. Moreover, to enable the best functionality and efficiency of the proposed architecture, a special tool-set for error recovery was developed, by adapting the general concepts of redundancy and calibration to effectively handle this triple-hybrid structure.

After system design in Matlab, the complete ADC circuit was developed in 40 nm CMOS technology using Cadence software CAD-tools. Thereby, the complete evaluation by simulation (before manufacturing) was a major challenge, due to the targeted linearity, and also due to lake of available experi-

ence in the used technology. Thereafter, the ADC was manufactured through TSMC 40 nm fabrication process, and a dedicated test-setup was prepared to measure the ADC performance, which – once more – added another challenge, to ensure the capability of high-linearity measurement (unprecedented in the lab).

The measured performance reported a remarkable Nyquist-rate effective resolution and dynamic linearity with SFDR = 107 dB, at a very good power efficiency. Also, the chip presented good stability over temperature and voltage variations. Finally, the measured ADC advances the SoA with an attractive implementation, that employs digital-enhancement and simple design. The ADC provides a very high linearity at a minimum chip-area (determined by sampling C). Therefore, it presents a promising solution also for more recent CMOS technologies, especially, by considering the yet available margins to further improve resolution, power and conversion speed.

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List of Author Publications

During his work the author has done studies, theoretical analysis, simulations, implementations and measurements on systems and circuits. These are mainly in the field of SAR ADC, but also in analog circuit design and signal processing. A list of therefore resulting publications in leading international conferences and journals, as well as patents, is given below.

- **A. AlMarashli**, J. Anders, J. Becker and M. Ortmanns, "A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1493-1507, May 2018.

- **A. AlMarashli**, J. Anders and M. Ortmanns, "Signalumsetzer". German Patent Nr. DE 102016112516. German Patent and Trade Mark Office.

- **A. AlMarashli**, J. Anders, J. Becker and M. Ortmanns, "A 107 dB SFDR, 80 kS/s Nyquist-rate SAR ADC using a hybrid capacitive and incremental $\Sigma\Delta$ DAC," in *2017 Symp. on VLSI Circuits Dig. Tech. Papers*, Kyoto, 2017, pp. 240-241.

- **A. AlMarashli**, J. Anders, J. Becker, and M. Ortmanns, "A high linearity SAR ADC employing Sigma-Delta DAC," in *Kleinheubacher Tagung*, Miltenberg, Germany, September 2017

- C. Chu, J. Wagner, **A. AlMarashli**, J. Chi and M. Ortmanns, "A Study on Op-amp Nonlinearity in a Single-bit CT Modulator Employing GBW Compensation," in *Conference on PhD Research in Microelectronics and Electronics* (PRIME 2016), Lisbon, Portugal, Juni 2016.

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