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Scalable Integrated Radar Transceiver Front-Ends in SiGe BiCMOS Technology

DISSERTATION

zur Erlangung des akademischen Grades eines

DOKTOR-INGENIEUR

(Dr.-Ing.)

der Fakultät für Ingenieurwissenschaften
und Informatik der Universität Ulm

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Ulm, 18. Februar 2022

To my family.

Abstract

Rapid development and scaling of semiconductor technologies enabled implementation of high-performance radars on a single chip which led to an enormous increase in adoption of various radar systems in everyday life. Silicon-based technologies are well suited since they offer a cost-effective realization of integrated systems comprising a high-frequency front-ends and a digital part used for signal processing.

This work presents the design and implementation of scalable millimeter-wave radar transceiver (TRX) front-ends in silicon-germanium BiCMOS technology. Critical components, such as frequency multipliers and power amplifiers are analyzed and techniques are proposed to improve the performance of the circuits. Two efficient D-band frequency quadruplers are designed and implemented. Circuit techniques to enhance the conversion gain are explained. Two high-performance output stages using power combining techniques targeting E-band and G-band, respectively, are designed, fabricated and characterized. Furthermore, a transmitter-to-receiver (TX-to-RX) leakage problem in monostatic radar TRX is addressed and a compensation technique is proposed. Finally, complete monostatic and bistatic integrated radar TRXs for E-band and G-band are presented and evaluated using dedicated FMCW radar boards. Scalability of the system is demonstrated using a 2-channel E-band radar capable of two-dimensional area scanning achieving an excellent ranging precision. The range resolution is significantly enhanced by employing a G-band bistatic TRX version with on-chip antennas. Functionality of a TX-to-RX leakage compensation network is validated in both E-band and G-band monostatic TRXs effectively suppressing the crosstalk and improving detectability of near, weakly reflecting objects.

Zusammenfassung

Die fortschreitende Entwicklung und Skalierung von Halbleitertechnologien hat die Implementierung von hochperformanten Radaren auf einem einzelnen Chip ermöglicht. Dies hat zu einem enormen Anstieg der Anwendung verschiedenster Radarsysteme im Alltag geführt. Silizium-basierte Technologien sind hierfür hervorragend geeignet, denn sie erlauben eine kostengünstige Realisierung solch komplexer integrierter Systeme, die hochfrequente Front-Ends sowie digitale Signalverarbeitung monolithisch vereinen.

In dieser Arbeit wird der Entwurf und die Implementierung von skalierbaren Radar-Transceiver (TRX) Front-Ends in Silizium-Germanium BiCMOS Technologie präsentiert. Die kritischen Komponenten, wie Frequenzvervielfacher und Leistungsverstärker werden untersucht und Techniken, um die Leistung der Schaltkreise zu verbessern, werden vorgeschlagen. Zwei effiziente D-band Frequenzvervierfacher werden entworfen und implementiert. Dabei werden die Entwurfstechniken zur Erhöhung des Konversionsgewinns erläutert. Zwei hochperformante Ausgangsstufen mit Leistungskombinierung für das E-band und G-band werden entworfen, gefertigt und charakterisiert. Darüber hinaus wird das Problem der Signalkopplung vom Sender zum Empfänger (TX-to-RX Leakage) analysiert und eine Kompensationstechnik wird vorgeschlagen. Schließlich werden die vollständigen monostatischen und bistatischen integrierten Radar TRX für E-Band und G-Band dargestellt und mittels dedizierter FMCW Platinen evaluiert. Die Skalierbarkeit des Systems wird mit Hilfe einer 2-kanaligen E-band Radarplattform demonstriert, die den Ort in zwei Dimensionen scannen kann und eine exzellente Präzision erreicht. Die Entfernungsauflösung des Radars wird durch den Einsatz der bistatischen G-Band TRX Version mit integrierten Antennen deutlich verbessert. Die Funktionalität des TX-to-RX Leckkompensationsnetzwerkes im monostatischen TRX wird sowohl im E- als auch G-Band geprüft. Dieses Netzwerk unterdrückt effektiv das TX-to-RX Übersprechen und verbessert die Erkennung von nahen, schwach reflektierenden Objekten.

Acknowledgements

This thesis is the result of my research carried out at Leibniz-Institut für innovative Mikroelektronik (IHP) in Frankfurt (Oder), Germany.

First, I would like to thank my supervisor Prof. Dr.-Ing. habil. Dietmar Kissinger for offering me an opportunity to work on an interesting subject in an excellent environment at IHP and his invaluable guidance throughout my doctoral research. Also, I would like to thank Prof. Dr. techn. Linus Maurer for agreeing to serve as the second reviewer.

I would like to express my deep gratitude to Prof. Dr. Herman Jalli Ng for his constant support and many fruitful discussions that undoubtedly made me a better designer.

Special thanks are dedicated to all my colleagues at IHP for making the time spent there an unforgettable experience from which I will benefit in the future. In particular, sincere gratitude to Dr. Frank Herzel for introducing me to the world of integrated circuits and raising a new passion that dominated my professional life ever since.

Finally, I cannot forget to express my genuine love to my wife. This thesis would have not come to an end without her unimaginable support and understanding she had throughout the years. I dedicate this work to her and our lovely son and daughter. Also, I would like to thank my dear parents, my sister and the rest of my family for continuous support and encouragement.

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1 Introduction

Radars (**RA**dio **D**etection **A**nd **R**anging) have experienced a tremendous evolution since 1904 when Christian Hülsmeyer, German physicist and inventor, patented his *Telemobiloscope* (Fig. 1.1), an apparatus intended for a system preventing collisions between ships. For the next decades, including two World Wars, radars became extremely important in defense systems being the key components in many military applications. Along with rapid development of air- and spacecrafts radars helped not only safety and navigation but were found to be particularly functional in imaging systems using synthetic aperture (SAR). In recent years, the automotive sector played an important role in radar adoption for a variety of features improving safety and comfort. In healthcare, radar could be used for remote heartbeat measurement, which is also used to find humans in rubble since the electromagnetic wave can easily penetrate through certain solids. In industry, radar sensors are often used for accurate ranging in extreme environment, e.g. content level control in a blast furnace.

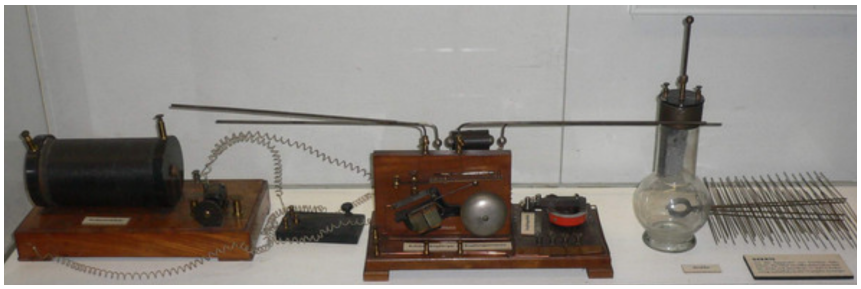
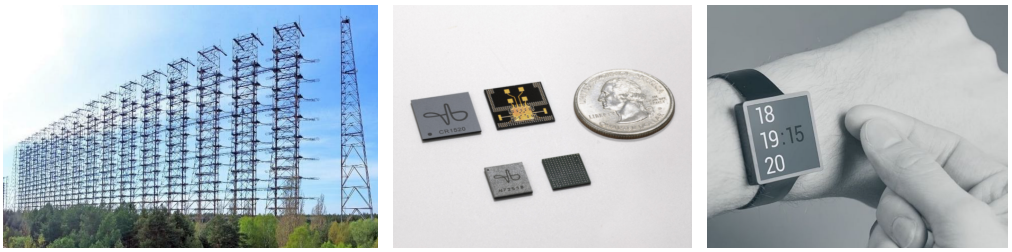


Figure 1.1: First radar constructed by Christian Hülsmeyer [1].

The development of semiconductor technologies enabled large scale circuit integration and constant size reduction of electronic devices, including radars (Fig. 1.2). Higher frequency spectrum could be exploited resulting in enhanced



(a) (b) (c)

Figure 1.2: From huge military radar facilities to miniature integrated sensors: (a) Duga over-the-horizon radar near Chernobyl (1972-1976) [2]. (b) Google's Soli integrated radar chip [3, 4] and (c) its potential use in touch-less gesture control [5]. Courtesy of Google, reused with permission from Google.

ranging precision and resolution. From bulky constructions, seen mostly in military facilities, radars underwent major miniaturization being nowadays present in almost everyone's life. Despite this fact, radars have still a great potential to at least approach the adoption level of other technological symbols of modern era like computers or smartphones.

1.1 Motivation of This Work

The motivation behind this work stems from the significant upside potential of radars to be adopted in modern electronics. Rapid development of technology enabled an enormous growth of highly automated systems supporting humans in their daily lives. Fully autonomous vehicles will fill the streets in the near future and the most critical parameter is the passenger's safety supported by dozens of various sensors scanning the surrounding area. Radars play a key role due to their natural ability to operate under severe atmospheric conditions and large scanned distances. As the integrated technologies continuously scale down, new frequency bands have become available creating new opportunities for application-dependent mm-wave radar systems. The current generation of automotive sensors targets 76-81 GHz band, with 76-77 GHz dedicated for long-range (LRR) and 77-81 GHz reserved for mid- (MRR) and short-range (SRR) radar [6]. Possible applications include adaptive cruise control (ACC), cross traffic alert

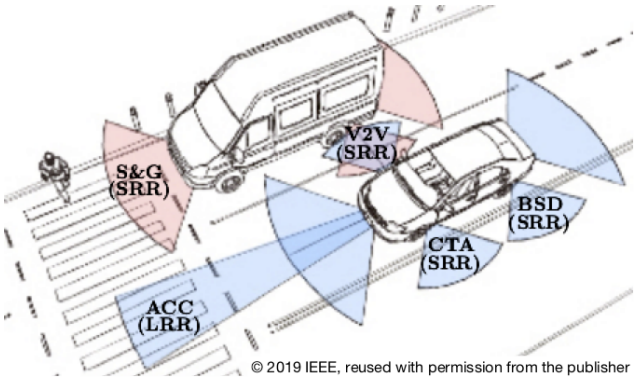


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Figure 1.3: Automotive radar applications [8].

(CTA), blind-spot detection (BSD), stop & go cruise control (S&G), park assist or even a simple vehicle-to-vehicle (V2V) communication for early warning, e.g., in case of an obstructed crossing pedestrian (Fig. 1.3). E-band utilization is not restricted to the automotive branch only. The 57-66 GHz band can also be used in applications such as gesture recognition, traffic monitoring, vital signs detection and others. As the global regulatory bodies, such as FCC, ETSI and ITU, plan to allow unlicensed use of frequency bands above 95 GHz, a next generation of sensors will emerge offering excellent resolution due to massively abundant spectrum [7].

In this work, a scalable radar system is proposed based on a single Q-band signal source and a theoretically unlimited number of single-channel transceivers (TRX) covering the E-band and G-band range. Since the local oscillator (LO) signal is multiplied in each TRX to the desired frequency, no additional generators are required. The system scales both in number of front-ends and the frequency, as long as the target band is a multiple of the LO frequency. Hence, it is possible to extend the operation to higher frequency bands once it becomes feasible from technological standpoint. This is advantageous in several aspects including more available bandwidth; thus, higher range resolution and more compact size due to direct integration of the antennas whose size decreases at higher frequencies.

Scalable single-channel TRX architectures offers several benefits over more complex multi-channel and multi-band chip solutions. Above all, they provide a high level of flexibility for the end-user in terms of system design. A multi-channel platform can be realized using any number of TRXs and a single signal source. If the

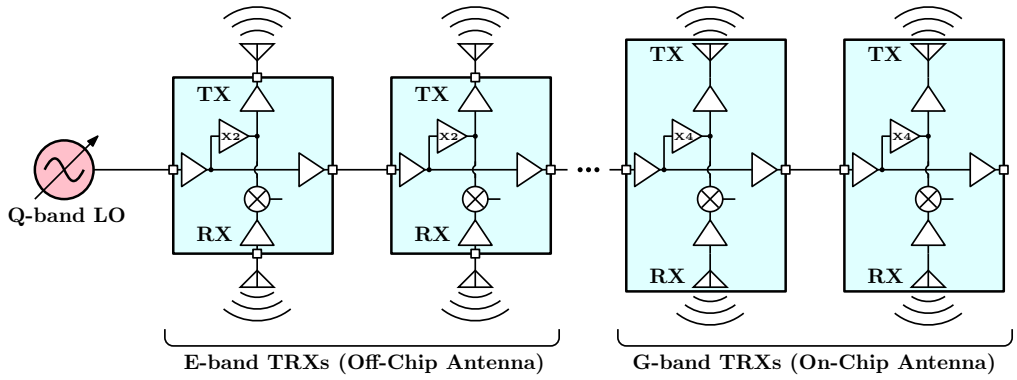


Figure 1.4: Conceptual block diagram of a scalable radar system.

number of channels changes afterwards, the system can be conveniently scaled on the PCB level. This can also be advantageous financially since no new chip design is needed in general. Owing to the separate signal generator IC, the source can also easily be replaced. Consequently, this scalable approach provides freedom in channel arrangement and LO distribution that can be used to increase reliability of the system [9]. However, system-on-chip (SoC) solutions might be more power-efficient and easier to handle since the complete high-frequency part is kept on-chip. This simplifies PCB implementation and reduces cost since low-priced laminates can be used. Finally, multi-chip solutions might require more sophisticated calibration than a single SoC.

1.2 Overview of This Work

This work consists of six chapters organized as follows: Chapter 2 gives a brief overview on semiconductor technologies and radar techniques. Principles of operation of two fundamental transistor types are described and the key parameters are compared. This is followed by a closer look at a hetero-junction bipolar transistor structure together with a short summary of the process used in this work. In the second part, basic radar sensing techniques are reviewed including pulse and frequency-modulated continuous-wave (FMCW) radars.

Chapter 3 covers the key building blocks of a mm-wave integrated radar front-end with an emphasis on efficient frequency multiplication and power amplifica-

tion. Two D-band frequency quadruplers (FQ) using different circuit techniques are analyzed and compared. A wide-band stacked Gilbert-cell (GC) FQ using a bootstrapping technique is presented, followed by a transformer-based injection-locked FQ with wide locking range. Subsequently, E-band and G-band power amplifiers (PA) are reported. Finally, the concept of TX-to-RX leakage cancellation is investigated with respect to possible solutions.

Realizations of E-band monostatic and bistatic radar platforms using single-channel scalable front-ends are presented in Chapter 4. For the monostatic version, a tunable TX-to-RX leakage canceller is proposed and implemented. The bistatic TRXs are employed in a two-channel FMCW radar equipped with a fully-integrated fractional-N phase-locked loop (PLL) to demonstrate scalability of the system.

G-band integrated radar transceivers with on-chip antennas are covered in Chapter 5. The introduced monostatic TRX incorporates tunable leakage cancellation for improved near object detectability whereas the bistatic version is optimized for high-performance regarding ranging precision and resolution. Finally, FMCW radar demonstrators using both transceivers are presented and the corresponding experimental results are shown and compared.

The thesis ends with a conclusion and an outlook discussing possible future work.

2 Fundamentals

In this chapter, semiconductor fundamentals are described with a focus on two basic transistor structures that became a cornerstone of modern microelectronics including integrated radar systems. This is followed by an overview of the basic radar techniques used in the state-of-the-art sensors.

2.1 Semiconductor Technologies

Modern semiconductor technologies are based on two types of transistors whose utilization evolved over the last decades as the integration level continuously increased, nowadays enabling fabrication of nanometer devices. First invented in 1947, bipolar junction transistors (BJT), played a key role in monolithic integrated circuits (IC) until complementary metal-oxide-semiconductor (CMOS) technology began to dominate the market, especially in digital ICs, constituting more than 90% of the total market share, today. Nevertheless, bipolar devices are still broadly used in RF applications that require high performance in the mm-wave frequency range. A bipolar complementary metal-oxide-semiconductor (BiCMOS) process proves to be particularly interesting since it combines advantages offered by BJT and CMOS devices. Thus, it enables the design of complex SoC comprising high-frequency front-ends and low-power digital logic blocks on a single die.

2.1.1 MOS Field-Effect and Bipolar Transistors

Fig. 2.1 presents a cross-section of a typical BiCMOS process with lateral BJTs. An *npn* BJT is a three-terminal device consisting of two pn-junctions between

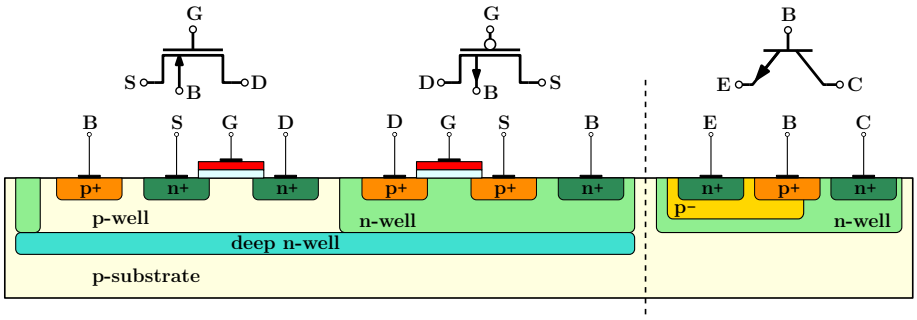


Figure 2.1: Cross-section of a typical BiCMOS process.

base (B) and emitter (E), as well as base and collector (C). Under typical operating conditions (forward-active region) the BE junction is forward-biased and BC is reverse-biased. The charge flow occurs through injection of majority carriers (electrons) from heavily doped emitter into the base, where they diffuse towards lightly doped collector. To reduce the amount of electrons being recombined with the injected holes the base region is very thin. As a consequence, small base current results in a larger collector current by a factor of β_F=$I_\mathrm{C}/I_\mathrm{B}$ (Fig. 2.2a). In forward-active region collector current is approximated by

$$I_\mathrm{C} = I_\mathrm{S}(1 + \frac{V_\mathrm{CE}}{V_\mathrm{A}})e^{\frac{V_\mathrm{BE}}{V_\mathrm{T}}}, \tag{2.1}$$

where I_S is reverse saturation current and V_T=$k_\mathrm{B}T/q$ denotes thermal voltage equal to approx. 26 mV at room temperature (300 K). V_A is the Early voltage and models base width modulation due to V_CE. Note that the collector current depends exponentially on the base-emitter voltage. Fig. 2.2b shows the BJT hybrid-

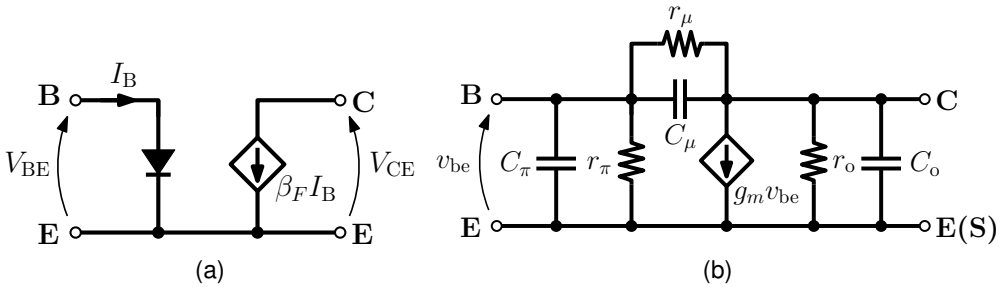


Figure 2.2: (a) Large-signal BJT model in forward-active region. (b) Hybrid-π small-signal BJT model.

π small-signal model which accounts for the main device parasitics and proves helpful at high frequencies as a first approximation. Capacitance C_π is composed of base-emitter depletion layer capacitance C_{je} and base-charging capacitance C_{b}. Collector-base resistance r_μ models the influence of V_{CE} on the base current I_{B}. C_π accounts for the base-collector depletion layer capacitance. Output resistance r_{o} results from Early effect and can be calculated from large-signal parameters as r_{o}=V_{A}/I_{C}. Finally, output capacitance C_{o} models collector-emitter and collector-substrate capacitances with the latter being typically much larger in a vertical BJT. For a given bias point, the small-signal transconductance can be found as

$$g_{\mathrm{m}} = \frac{\delta I_{\mathrm{C}}}{\delta V_{\mathrm{BE}}} = \frac{\delta}{\delta V_{\mathrm{BE}}} e^{\frac{V_{\mathrm{BE}}}{V_{\mathrm{T}}}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{T}}}, \tag{2.2}$$

provided that $v_{\mathrm{be}} \ll V_{\mathrm{T}}$. Transconductance g_{m} depends solely on the collector current and temperature regardless of device sizing and process. The BJT behaviour versus frequency can be examined by finding the transit frequency f_{T}, at which the magnitude of current gain of a short-circuit common-emitter stage is unity. Neglecting r_μ and the current flowing through C_μ leads to

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi(C_\pi + C_\mu)} = \frac{1}{2\pi(\tau_{\mathrm{F}} + (C_{\mathrm{je}} + C_\mu)/g_{\mathrm{m}})} \approx \frac{1}{2\pi\tau_{\mathrm{F}}} = \frac{\mu_{\mathrm{n}}}{\pi W_{\mathrm{B}}^2} V_{\mathrm{T}}, \tag{2.3}$$

where W_{B} denotes base width and τ_{F} is the base transit time.

The operation principle of a MOS transistor significantly differs from that of a BJT. During fabrication process a thin silicon-dioxide layer is grown on a p-type substrate with conducting polysilicon deposited on top of it to create gate (G) terminal. Such formed MOS planar capacitor can be used to change the distribution of charges near the oxide-semiconductor surface. Applying a positive voltage between the gate and the bulk (B) shifts holes in the bulk away from the surface, creating a depletion region at the semiconductor-insulator interface. As the applied voltage exceeds threshold voltage V_{th} an inversion layer is formed containing large electron concentrations that enable current flow between n-type source (S) and drain (D). For a pMOS device, the opposite doping is implemented and the current flows at negative gate-source voltage through the p-type channel. Contrary to the BJT, almost no current flows into the gate (Fig. 2.3a), and the drain

current is given by

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}}}{2} \frac{W}{L} (\underbrace{V_{\mathrm{GS}} - V_{\mathrm{th}}}_{V_{\mathrm{ov}}})^2 (1 + \lambda V_{\mathrm{DS}}), \tag{2.4}$$

where W and L represent the gate geometry, C_{ox} is the gate oxide capacitance per unit area and μ_{n} stands for electron mobility in the channel. λ is a reciprocal of the Early voltage and models effective channel modulation due to V_{DS}. The body (B) bias is assumed to be fixed at source potential, hence, its influence (*body effect*) is neglected for simplicity. The equivalent hybrid-π small-signal MOSFET

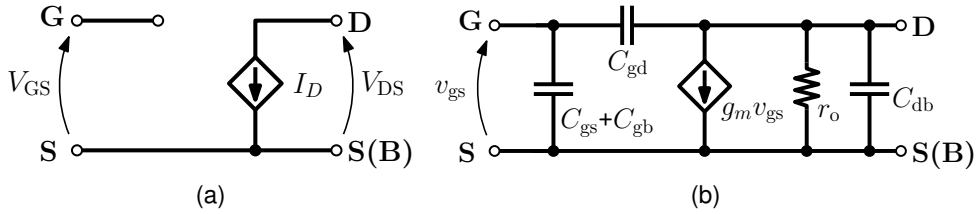


Figure 2.3: (a) Large-signal MOSFET model. (b) Hybrid-π small-signal MOSFET model.

model is shown in Fig. 2.3b, where C_{gs} and C_{gd} include overlap capacitance between the gate and the source and drain regions, respectively. Capacitance C_{db} results from depletion region in reversely biased drain-body pn-junction and C_{gb} accounts for gate-body parasitic capacitance outside the active area of the device. Since the body is at source potential, C_{db} appears at the output and C_{gb} at the input, respectively. The output resistance r_{o}=$1/\lambda I_{\mathrm{D}}$ corresponds to the Early voltage in a BJT. Small-signal transconductance in MOSFET device can be found by differentiating (2.4) with respect to the input voltage V_{GS}

$$g_{\mathrm{m}} = \frac{\delta I_{\mathrm{D}}}{\delta V_{\mathrm{GS}}} = \mu_{\mathrm{n}} C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{th}}) = \sqrt{2 \mu_{\mathrm{n}} C_{\mathrm{ox}} (W/L) I_{\mathrm{D}}}. \tag{2.5}$$

The above holds valid as long as $v_{\mathrm{gs}} \ll V_{\mathrm{ov}} = V_{\mathrm{GS}} - V_{\mathrm{th}}$. Unlike BJTs, the MOFETs transconductance depends strongly on device geometry. In general, BJTs provide significantly larger transconductance for the same current bias and geometry, in particular in a BiCMOS technology. MOSFET performance against the frequency can be found in similar way as for the BJT. Assuming no current

flows through C_{gd}, f_{T} reads

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gs}} + C_{\mathrm{gb}} + C_{\mathrm{gd}})} \approx \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{gs}}} = \frac{3\mu_{\mathrm{n}}}{4\pi L^2} V_{\mathrm{ov}}, \tag{2.6}$$

and can directly be compared to the results obtained for BJTs in (2.3). Interestingly, f_{T} of MOS devices can be enhanced using large V_{ov} whereas for BJTs V_{T} is fixed. However, in case of hetero-junction transistors (HBT) the base layer can be grown epitaxially with widths of few nm making it superior to MOSFETs with regards to high-frequency performance.

2.1.2 Hetero-Junction Bipolar Transistor

The constant trend toward higher level of transistor integration and speed became an incentive to search for potential improvements in semiconductor device architectures. Another key parameter next to cut-off frequency f_{T} given by (2.3) is the frequency at which the power gain becomes unity (f_{MAX}). For a BJT it reads

$$f_{\mathrm{MAX}} = \sqrt{\frac{f_{\mathrm{T}}}{8\pi C_{\mathrm{jc}} R_{\mathrm{B}}}}, \tag{2.7}$$

where C_{jc} is collector junction capacitance and R_{B} denotes base resistance. The product of both can be seen as a time constant τ_{d} determining f_{MAX} of the device. One could increase f_{MAX} and f_{T} by reducing base width W_{B}. This leads to several implications having negative impact on f_{MAX}. As W_{B} decreases, R_{B} increases since

$$R_{\mathrm{B}} \propto \frac{1}{qN_{\mathrm{A}}\mu_{\mathrm{p}} W_{\mathrm{B}}} \tag{2.8}$$

and no improvement in f_{MAX} is achieved. From (2.8) one could try to increase base doping density N_{A}. However, heavier base doping results in larger base-emitter junction capacitance due to narrower depletion layer; thus, increased charging time and lower f_{T}. More importantly, it makes forward current gain β_{F} lower due to

$$\beta_{\mathrm{F}}^{\mathrm{BJT}} = \frac{D_{\mathrm{n}} L_{\mathrm{p}} N_{\mathrm{D}}}{D_{\mathrm{p}} W_{\mathrm{B}} N_{\mathrm{A}}}, \tag{2.9}$$

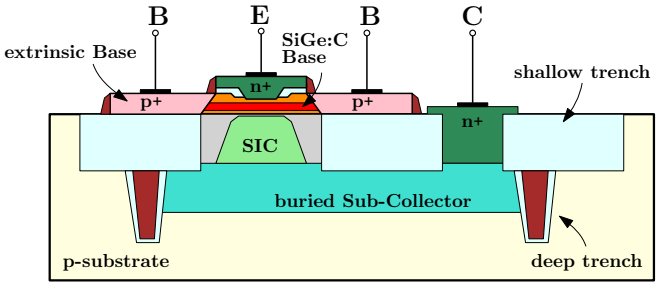


Figure 2.4: Cross-section of an HBT transistor.

where N_{D} is emitter doping density, D is the diffusion constant for holes and electrons, respectively, and L_{p} is the diffusion length for holes in the emitter. In (2.9) base current representing recombination of holes and electrons in the base region was neglected which is justified for small W_{B}. Having a hetero-junction of semiconductors with different bandgaps (2.9) modifies to

$$\beta_{\mathrm{F}}^{\mathrm{HBT}} = \frac{D_{\mathrm{n}} L_{\mathrm{p}} N_{\mathrm{D}}}{D_{\mathrm{p}} W_{\mathrm{B}} N_{\mathrm{A}}} \frac{n_{\mathrm{i_B}}^2}{n_{\mathrm{i_E}}^2} = \frac{D_{\mathrm{n}} L_{\mathrm{p}} N_{\mathrm{D}}}{D_{\mathrm{p}} W_{\mathrm{B}} N_{\mathrm{A}}} e^{\Delta E_{\mathrm{g}}/k_{\mathrm{B}}T}, \tag{2.10}$$

where $n_{\mathrm{i_{B,E}}}$ is the intrinsic carrier concentration specific to the used semiconductor materials and ΔE_{g} denotes the bandgap difference between them. Factor $e^{\Delta E_{\mathrm{g}}/k_{\mathrm{B}}T}$ potentially gives a significant boost in β_{F} relaxing doping level requirements and base width. This results in lower junction capacitances and base resistance enabling f_{T} and f_{MAX} of hundreds of GHz.

Fig. 2.4 presents cross-section of SiGe *npn* HBT [10, 11]. Here, SiGe material having lower bandgap with respect to Si is used in the base region. Addition of carbon (C) atoms relaxes the strain resulting from lattice mismatch. Carriers injected from the emitter into the base diffuses to a selectively-implanted collector (SIC) layer having an increased dopant concentration to reduce collector resistance. The base region is elevated to fit the emitter window and to reduce the base resistance. Finally, shallow and deep trenches are used to improve isolation of the transistor and to enhance its performance at high frequencies.

2.1.3 Technological Environment of This Work

This work was conducted completely at Leibniz-Institut für innovative Mikroelektronik (IHP GmbH) located in Frankfurt (Oder), Germany. The institute has developed its own in-house silicon-germanium (SiGe:C) BiCMOS process and offers manufacturing services for research and industrial projects for internal use as well as for external customers. Two strategic technology nodes are available 0.25 µm and 0.13 µm with a set of high-performance HBT transistors and special RF modules, such as through-silicon vias (TSV), localized backside etching (LBE) and photonic integrated circuits (PIC). Among two commercially available 0.13 µm process generations SG13S and SG13G2, the latter was used to implement circuits presented in this work [12, 13]. In 2012 a DOTSEVEN project started targeting $f_{\mathrm{T}}/f_{\mathrm{MAX}}$=500/700 GHz. Fig. 2.5 presents a cross-section of the

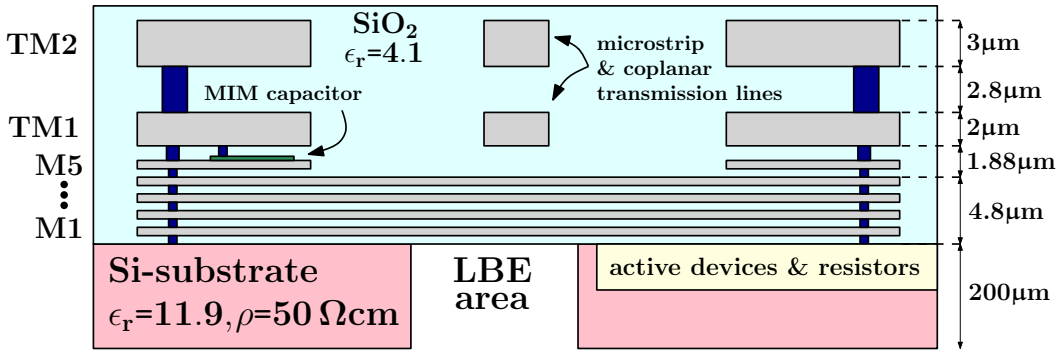


Figure 2.5: Metal layer stack in IHP BiCMOS SG13 process.

back end providing five thin and two thick metal layers deposited in silicon dioxide. In case of mm-wave designs, thick layers serve well as transmission lines (TL) due to low resistivity and distant placement over the lossy silicon substrate. For more robust modeling, the thin layers might be used as the ground plane for the TLs. The process offers metal-insulator-metal (MIM) capacitors situated between TM1 and M5 layers and three resistor types:

- silicided, n-doped gate polysilicon resistor (RSIL)
- unsilicided, p-doped gate polysilicon resistor (RPPD)
- unsilicided, partially compensated gate polysilicon resistor (RHIGH)

Table 2.1: Resistors and capacitors available in SG13 process [12] (updated).

Component	Parameter	Value
RSIL resistor	sheet resistance	7 Ω
	temp. coefficient	3100 ppm/K
RPPD resistor	sheet resistance	345 Ω
	temp. coefficient	-45 ppm/K
RHIGH resistor	sheet resistance	775 Ω
	temp. coefficient	-1800 ppm/K
MIM capacitor	capacitance/area	1.5 fF/µm^2
MOS varactor	capacitance/area	4.5 fF/µm^2

Table 2.1 summarizes key resistor and capacitor parameters. CMOS section includes thick-oxide high-voltage MOSFETs and low-voltage devices with 3.3 V and 1.2 V core supply, respectively. For RF purposes *npn*-HBT transistors with $f_{\mathrm{T}}/f_{\mathrm{MAX}}$=300/500 GHz can be used. In addition, the process allows LBE for inductors with enhanced Q-factor or efficient on-chip antennas.

2.2 Radar Techniques

This section provides a brief overview of basic techniques and signal processing used in the modern radar systems. Operation of a simple pulse radar is described followed by a short reminder of pulse compression and window functions used in detection of the targets. Finally, FMCW radar principles are presented.

2.2.1 Pulse Radar

Principal of operation of the first radars was based on short pulse transmission and reception of the reflected echo. A block diagram of a simple pulse-Doppler radar is shown in Fig. 2.6. In TX mode a short pulse is transmitted. Then it switches to RX mode receiving incoming echoes from the targets. The round trip delay time (τ_0) determines the range as follows

$$R = \frac{\tau_0 c_0}{2}, \tag{2.11}$$

where c_0 is speed of light in the air. Consecutive TX pulses are generated at the rate that determines maximum range of the system (PRI-pulse repetition

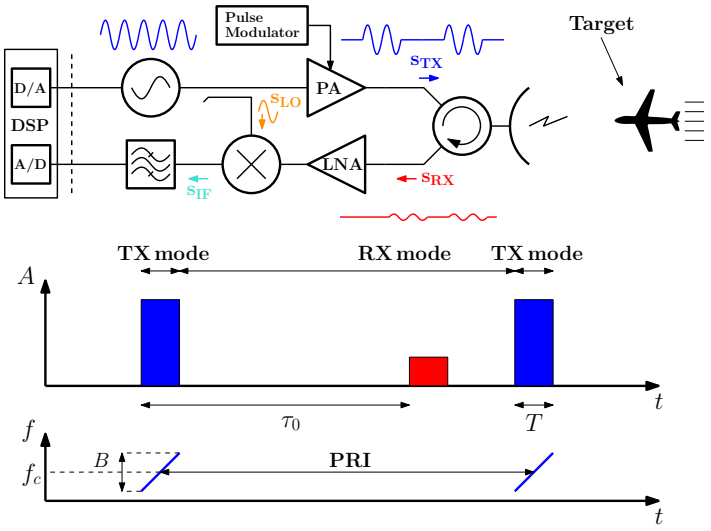


Figure 2.6: Block diagram of a coherent pulse-Doppler radar.

interval). The power at the receiver input reads

$$P_{\mathrm{RX}} = \frac{P_{\mathrm{TX}} \lambda^2 G_{\mathrm{ant}}^2 \sigma}{(4\pi)^3 R^4}, \tag{2.12}$$

where λ is the wavelength in the air, G_{ant} is antenna gain and σ denotes the radar cross-section (RCS) specific for a given target. RCS indicates how detectable an object is by a radar depending on several factors, e.g., object size and shape, orientation with respect to the radar or material the object is made of. The maximum detectable range is given by

$$R_{\mathrm{max}} = \sqrt[4]{\frac{P_{\mathrm{TX}} \lambda^2 G_{\mathrm{ant}}^2 \sigma}{(4\pi)^3 P_{\mathrm{N}}} \frac{1}{SNR_{\mathrm{min}}}}, \tag{2.13}$$

where P_{N}=$k_{\mathrm{B}} T B$ is noise power and SNR_{min} indicates the minimum signal-to-noise ratio required for target detection. In order to increase SNR and range resolution the RX signal is cross-correlated with the TX signal. Fig. 2.7a depicts this technique applied to a simple rectangular pulse. The complex envelope of an unmodulated rectangular signal reads

$$A(t) = \frac{1}{\sqrt{T}} \mathrm{rect}\left(\frac{t}{T}\right). \tag{2.14}$$

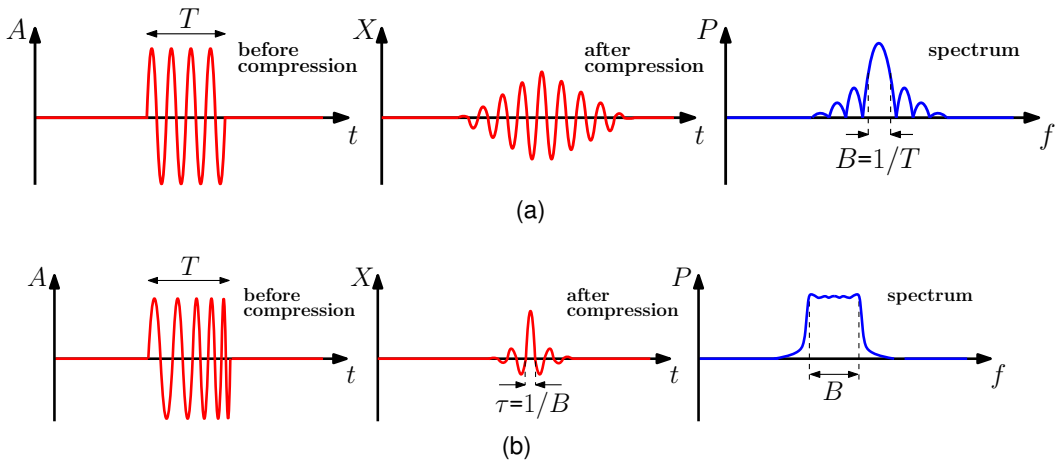


Figure 2.7: Radar signal before and after compression including its spectrum for (a) rectangular pulse (b) chirp.

Cross-correlation of that pulse results in a triangular function given by

$$X(t) = \begin{cases} 1 - \frac{|t|}{T} & |t| \leq T \\ 0 & , \text{otherwise} \end{cases} \tag{2.15}$$

with the energy concentrated around the peak at the time of pulse arrival [14]. To distinguish two triangular responses, the targets echoes must be separated by T. Thus, the range resolution is given by $\Delta R{=}c_0/2B$ and can be improved only by increasing the signal bandwidth, i.e., reducing the pulse width. However, a shorter pulse must have proportionally higher peak power to preserve the same SNR indicating a trade-off between ΔR and SNR. This can be resolved by applying pulse modulation, which removes the link between the pulse duration and the bandwidth enabling an independent optimization of SNR and ΔR.

Linear frequency modulation (LFM) is the most typically used technique to achieve pulse compression in radar systems. The complex envelope of an LFM signal (*chirp*) reads

$$A(t) = \frac{1}{\sqrt{T}} \text{rect}\left(\frac{t}{T}\right) \exp\left(j\pi k t^2\right), \tag{2.16}$$

where k=B/T denotes the ramp slope. Cross-correlation of (2.16) gives

$$X(t) = \begin{cases} \left| \left(1 - \frac{|t|}{T}\right) \frac{\sin\left[\pi B t (1-|t|/T)\right]}{\pi B t (1-|t|/T)} \right| & \text{for} \quad |t| \leq T \\ 0 & \text{, otherwise} \end{cases} \tag{2.17}$$

The compressed pulse width τ is approximately $1/B$ provided that the time-bandwidth product $BT \gg 4$. The compression ratio defined as T/τ equals approximately BT. This is depicted in Fig. 2.7b, where the signal bandwidth, ergo, range resolution is basically not constrained by the pulse duration. This permits using long pulses for good SNR whereas high range resolution is determined using LFM.

Although pulse compression using chirps improves range resolution and SNR at the receiver, the cross-correlation function of (2.16) produces significant sidelobes that would cover echoes from adjacent targets. Therefore, a commonly used technique is signal weighting before the pulse compression. The signal is multiplied by a weighting function (also known as window function) which shapes the pulse in a way that the sidelobes are attenuated at cost of worse SNR and wider mainlobe. Fig. 2.8a presents selected types of the weighting function in

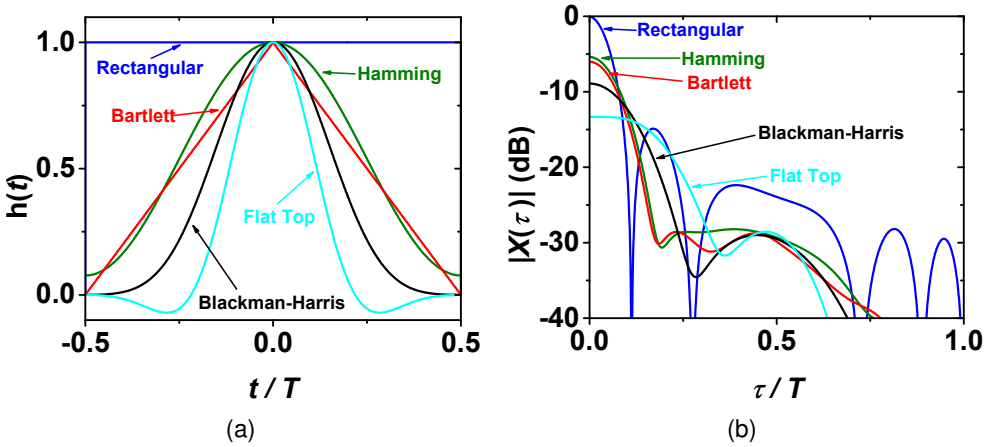


Figure 2.8: (a) Weighting (window) functions (b) Cross-correlation of the weighting function with the TX chirp.

time domain and its cross-correlation with the TX LFM pulse defined as

$$A(t) = \int_{-\infty}^{\infty} \overline{s_{\mathrm{TX}}(t-\tau)} h(t) \mathrm{d}t. \tag{2.18}$$

Each window type provides different characteristics of the compressed pulse. Unweighted pulse has the narrowest mainlobe but relatively strong sidelobes. Hamming, Hann or Bartlett windows attenuate the sidelobe level at cost of mainlobe broadening. Other window types (e.g. Blackman-Harris, flat top) provide even greater sidelobe suppression. Notably, signal power decreases after compression due to mismatch loss. Using weighting functions at the RX side only, results in an RX pulse not matched to the unweighted TX pulse. In practice, signal weighting is always applied to suppress the noise level and improve target detectability.

2.2.2 Frequency-Modulated Continuous-Wave Radar

FMCW radar is a type of sensor that utilizes a continuous-wave (CW) that is modulated in frequency domain. A simple CW radar is unable to measure the target range since it lacks timing information between the transmitted (TX) and received (RX) signals. However, it can still determine the object velocity due to the Doppler effect and difference in frequency between TX and RX signals given by

$$f_{\mathrm{d}} = f_{\mathrm{RX}} - f_{\mathrm{TX}} = 2 f_{\mathrm{TX}} \frac{v}{c_0 - v} \approx 2 f_{\mathrm{TX}} \frac{v}{c_0}, \tag{2.19}$$

where v and c_0 denote speed of the object and light in the air, respectively. f_{d} is known as Doppler frequency and is positive in case the object is approaching the sensor. By analogy, it turns negative if the object is moving away. Contrary to pulse radar, the SNR is dependent on the average transmitted power during target illumination, allowing for solid-state devices operating at low voltages to be implemented. Also, the target information is contained in a low-frequency signal (typically in MHz range) that can be easily processed using simple A/D converters (ADC). Thus, CW radars are cost-effective making them popular in many applications including sport accessories, police radars, motion detectors and heartbeat monitoring.

Applying frequency modulation on the CW signal enables target range measure-

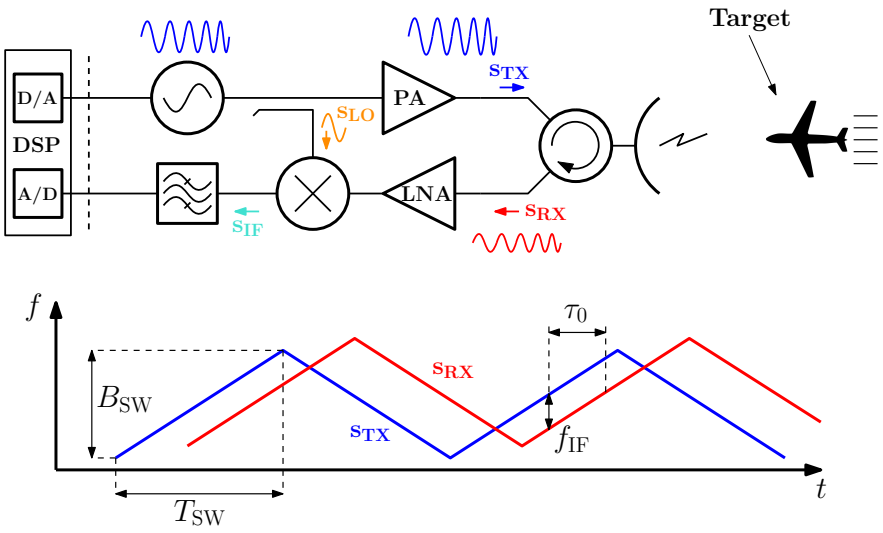


Figure 2.9: Block diagram of an FMCW radar.

ment. Fig. 2.9 depicts a simple FMCW radar sensing a moving object. A CW signal is linearly modulated in frequency such that a sweep bandwidth (B_{SW}) and duration (T_{SW}) are defined. Assuming perfect frequency ramp linearity, the round trip delay time (τ_0) can be calculated as follows

$$\tau_0 = \frac{T_{\mathrm{SW}}}{B_{\mathrm{SW}}} f_{\mathrm{IF}}, \tag{2.20}$$

where f_{IF}=f_{TX}-f_{RX}. Likewise as for pulse radar, the target range is given by (2.11). In time domain the transmitted signal reads

$$s_{\mathrm{TX}}(t) = A_{\mathrm{TX}} \cos\left(2\pi f_0 t + \pi k t^2 + \varphi_0\right), \tag{2.21}$$

where $k = B_{SW}/T_{SW}$. The received signal is an echo of the TX signal given by

$$s_{\mathrm{RX}}(t) = \alpha_\tau s_{\mathrm{TX}}(t - \tau_0), \tag{2.22}$$

where α_τ quantifies the attenuation. Typically, in an FMCW radar the TX signal is directly derived from an LO signal

$$s_{\mathrm{LO}}(t) = A_{\mathrm{LO}} \cos\left(2\pi f_0 t + \pi k t^2 + \varphi_0\right). \tag{2.23}$$

Assuming a simple mixer-based receiver architecture, the LO signal is multiplied with the RX signal, producing

$$s_{\mathrm{IF}}(t) = \underbrace{\frac{1}{2}\alpha_\tau A_{\mathrm{LO}} A_{\mathrm{TX}}}_{A_{\mathrm{IF}}} \Big(\overbrace{\cos\left(2\pi \underbrace{k\tau_0}_{f_{\mathrm{IF}}} t + 2\pi f_0 \tau_0 - \pi k \tau_0^2 - \varphi_R\right)}^{\text{difference}} + \overbrace{\cos\left((4\pi f_0 - 2\pi k\tau_0)t + 2\pi k t^2 - 2\pi f_0 \tau_0 + \pi k \tau_0^2 + 2\varphi_0 - \varphi_R\right)}^{\text{sum}} \Big) \quad . \tag{2.24}$$

The sum is removed by means of a low-pass filter and the difference containing a low-frequency component is being processed in the next steps. Performing Fourier transformation on (2.24) yields

$$S_{\mathrm{IF}}(f) = \int_{-\infty}^{\infty} s_{\mathrm{IF}}(t) e^{-j2\pi f t} dt = \frac{1}{2} A_{\mathrm{IF}} \Big(e^{j\Phi_{\mathrm{IF}}} \delta(f - f_{\mathrm{IF}}) + e^{-j\Phi_{\mathrm{IF}}} \delta(f + f_{\mathrm{IF}}) \Big)$$

In practice, the Fourier transformation occurs on a sampled IF waveform in the digital domain. A fast Fourier transform (FFT) algorithm is typically used for its enhanced speed with respect to discrete Fourier transformation (DFT). It is achieved through a significantly reduced computing complexity from $O(N^2)$ (DFT) to $O(N \log N)$ (FFT), where N is the data size. Similar to pulse radar, weighting functions are applied to the IF signal before FFT in order to suppress the noise and improve SNR at the cost of broadened peaks due to the target; thus, reduced range resolution.

3 Key Building Blocks in Integrated Radar Front-Ends

This chapter presents the most critical circuits used in modern radar RF front-ends. First, frequency multipliers providing an efficient signal conversion are presented, followed by massive E-band and G-band PAs reaching the output power levels close to the limits imposed by the used technology. Finally, a TX-to-RX leakage problem in radar TRX is discussed and a compensation circuitry is proposed. Most of the material presented in this chapter has already been published in [8],[15–17], and [18].

3.1 Efficient mm-Wave Frequency Multipliers

Most of the modern high-performance mm-wave transceivers contain an LO generation circuit that provides a stable signal for the transmitting and receiving modules (TX/RX). This is typically implemented with a phase-locked loop (PLL) that stabilizes a voltage-controlled oscillator (VCO). The signal generated by the VCO is chosen in the frequency range where a low phase noise and wide tuning range can be achieved. This is typically a compromise between the optimum resonant tank quality factor, transistor performance and a number of multiplying stages required to translate the signal to the frequency requested by the TX/RX modules. The use of frequency multipliers enables generation of stable high-frequency signals with a phase noise determined by the low frequency source. However, beyond $f_{\mathrm{T}}/f_{\mathrm{MAX}}$, free-running harmonic power sources might be the right solution for power generation [19].

Frequency multiplication can be realized using inherent non-linearity of a device, e.g., a diode or transistor. Recalling (2.1) the collector current (neglecting Early

voltage) reads

$$I_{\mathrm{C}} = I_{\mathrm{S}} e^{\frac{V_{\mathrm{BE}}}{V_{\mathrm{T}}}} = I_{\mathrm{S}} e^{\frac{V_{\mathrm{BE_Q}} + v_{\mathrm{be}}}{V_{\mathrm{T}}}} = I_{\mathrm{S}} e^{\frac{V_{\mathrm{BE_Q}}}{V_{\mathrm{T}}}} e^{\frac{v_{\mathrm{be}}}{V_{\mathrm{T}}}} = I_{\mathrm{C_Q}} e^{\frac{v_{\mathrm{be}}}{V_{\mathrm{T}}}}, \tag{3.1}$$

where $I_{\mathrm{C_Q}}$ and $V_{\mathrm{BE_Q}}$ denote the operating point of the transistor. Expanding (3.1) into Taylor series, collector current is given by

$$I_{\mathrm{C}}(v_{\mathrm{be}}) = \sum_{n=0}^{\infty} \frac{I_{\mathrm{C}}^{(n)}(0)}{n!} (v_{\mathrm{be}})^n = I_{\mathrm{C_Q}} (1 + \frac{1}{V_{\mathrm{T}}} v_{\mathrm{be}} + \frac{1}{2V_{\mathrm{T}}^2} v_{\mathrm{be}}^2 + \frac{1}{6V_{\mathrm{T}}^3} v_{\mathrm{be}}^3 + \ldots). \tag{3.2}$$

High-order harmonics are produced in collector current that can be extracted by using various techniques including bias optimization and matching. Another widely used technique, in particular for even multiplication factors, is based on current commutation by means of switching devices [20].

3.1.1 Stacked Bootstrapped Gilbert-Cell Frequency Quadrupler

The most convenient way to realize frequency quadrupling is to cascade or stack frequency doublers [18, 21–23]. There are basically two techniques used to double the frequency. The first employs a Gilbert-cell to mix the input frequency with itself thus producing a signal at the doubled frequency. Another technique is based on even harmonics superposition (so called push-push (PP) doublers). However, PP-doublers inherently have a single-ended output, which makes them unfavorable in fully-differential designs. Cascading two PP frequency doublers requires an interstage balun in order to generate differential signals to drive the second stage [24]. Another way is to drive two push-push doublers with quadrature signals in order to obtain a balanced signal that feeds the second stage [25]. This implies the use of additional circuitry for quadrature signals generation which inflicts more difficulties in the design process. On the other hand, push-push techniques, if combined with an injection-locked VCO, can be successfully used for frequency multiplication above $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ of the transistors [26]. Also it provides the possibility to tune the phase of the output signal which is a very attractive feature regarding phased-array applications.

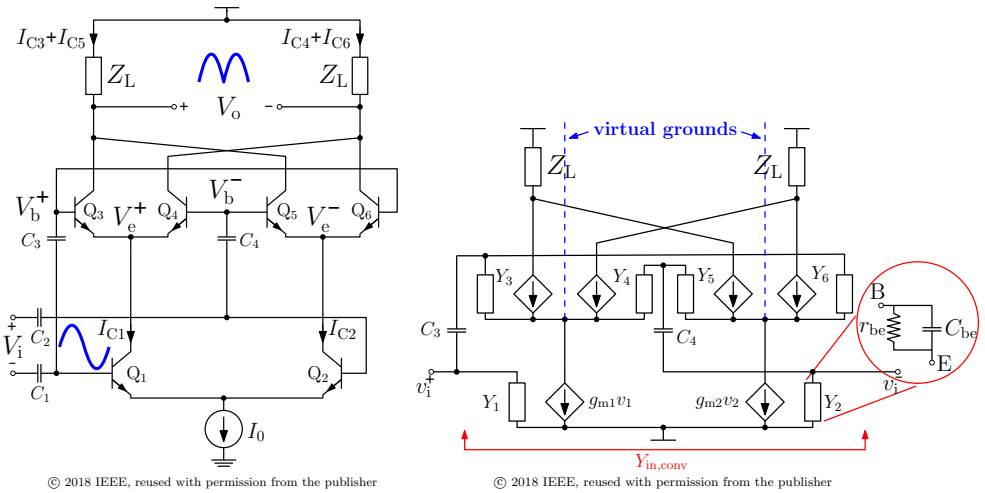


Figure 3.1: (a) Conventional Gilbert-cell frequency doubler topology. (b) Small-signal model used to determine the input admittance.[17]

Fig. 3.1a shows a conventional frequency doubler based on a Gilbert-cell. Q_{1-2} form a transconductance stage. The collector currents $I_{\mathrm{C1-C2}}$ become emitter currents of Q_{3-6} which perform the self-mixing operation since they are driven at the same rate as the input signal. Next, an analysis is performed to derive the conversion gain of that frequency doubler. Assuming that the saturation and base currents are negligible, the tail current source is ideal, and that the output resistances in the transistors are infinite [27], the output voltage reads

$$V_\mathrm{o} = I_0 Z_\mathrm{L} \tanh\left(\frac{V_\mathrm{i}}{2V_\mathrm{T}}\right) \tanh\left(\frac{V_\mathrm{b}}{2V_\mathrm{T}}\right). \tag{3.3}$$

Next, noticing that $\tanh(x) \approx x$ for $x \ll 1$, (3.3) can be rewritten as follows

$$V_\mathrm{o} = I_0 Z_\mathrm{L} \left(\frac{V_\mathrm{i}}{2V_\mathrm{T}}\right)\left(\frac{V_\mathrm{b}}{2V_\mathrm{T}}\right). \tag{3.4}$$

which holds true as long as $V_\mathrm{i}, V_\mathrm{b} \ll 2V_\mathrm{T}$. This assumption is justified since, unlike in case of a mixer, V_b greatly depends on V_i and can be considered small with respect to $2V_\mathrm{T}$. In the conventional frequency doubler $v_\mathrm{b} = v_\mathrm{i}$, assuming that

the capacitors C_{3-4} are perfect DC-blockers. Then (3.4) simplifies to

$$v_{\mathrm{o}} = \frac{I_0 Z_{\mathrm{L}}}{4V_{\mathrm{T}}^2} v_{\mathrm{i}}^2. \tag{3.5}$$

v_{i} is assumed to be a monotone excitation

$$v_{\mathrm{i}} = V_{\mathrm{i}} \cos\left(\omega_{\mathrm{i}} t + \varphi_0\right), \tag{3.6}$$

where V_{i} is the small-signal amplitude, ω_{i} is the input angular frequency and φ_0 denotes the initial phase, which for the moment can be considered to be zero. Then the small-signal output voltage reads

$$v_{\mathrm{o}} = \frac{g_{\mathrm{m}} Z_{\mathrm{L}} V_{\mathrm{i}}^2}{4V_{\mathrm{T}}} (1 + \cos 2\omega_{\mathrm{i}} t) \tag{3.7}$$

where the following relationship has been used $g_{\mathrm{m}} = I_{\mathrm{C1}}/V_{\mathrm{T}} = I_{\mathrm{C2}}/V_{\mathrm{T}} = I_0/2V_{\mathrm{T}}$. Since all transistors have the same sizes but differ in quiescent collector current, $g_{\mathrm{m1}} = g_{\mathrm{m2}} = g_{\mathrm{m}}$ and $g_{\mathrm{m3}} = g_{\mathrm{m4}} = g_{\mathrm{m5}} = g_{\mathrm{m6}} = g_{\mathrm{m}}/2$ due to halved I_{C1} and I_{C2} between Q_{3-4} and Q_{5-6}, respectively. From (3.7) it follows, that the output signal contains a component with doubled frequency and a DC part. Also, assuming the same input and output terminations, the output power depends quadratically with respect to the input power. Considering only the desired component at $2\omega_{\mathrm{i}}$, it follows

$$V_{\mathrm{o}} = \frac{g_{\mathrm{m}} Z_{\mathrm{L}} V_{\mathrm{i}}^2}{4V_{\mathrm{T}}} \tag{3.8}$$

and the small-signal voltage conversion gain reads

$$CG_v = V_{\mathrm{o}}/V_{\mathrm{i}} = V_{\mathrm{i}} \frac{g_{\mathrm{m}} Z_{\mathrm{L}}}{4V_{\mathrm{T}}} \tag{3.9}$$

Note, that the conversion gain is a function of the input voltage. This is expected since the output voltage is a function of the input voltage squared.

A small-signal equivalent circuit of the conventional frequency doubler is shown in Fig. 3.1b. Few assumptions are made to simplify the analysis. The collector-emitter output resistance r_{o} is considered to be infinite, as well as the parasitic capacitances C_{bc} and C_{ce} to be negligibly small. C_{be} is left as typically the largest in the transistor. Notice, that as C_{bc} increases, the input Miller capacitance may

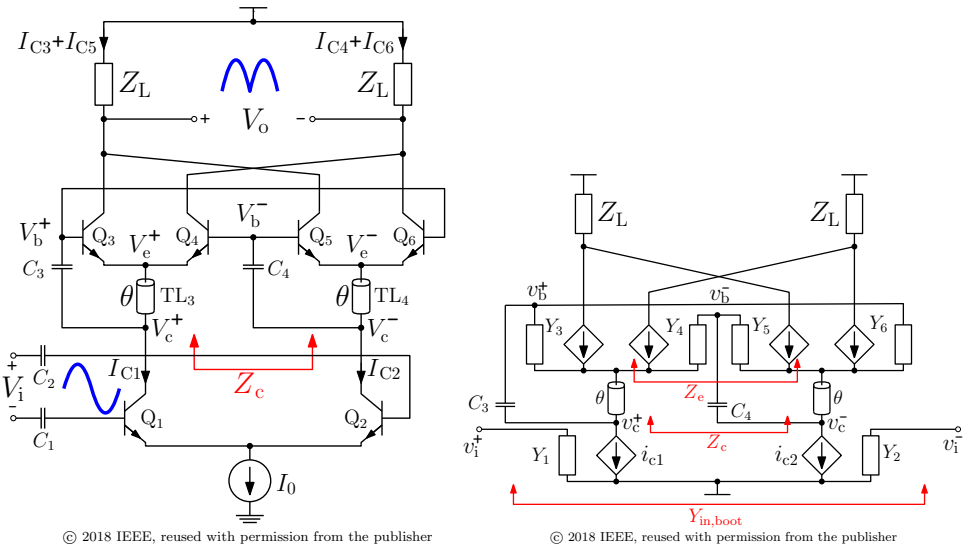


Figure 3.2: (a) Bootstrapped topology from [22]. The signal driving the switching quad is taken from Q_{1-2} collectors. (b) Small-signal model.[17]

become significant, which for high voltage gain will affect the input impedance. Next, the devices Q_{1-6} is assumed to have the same size (thus same r_{be} and C_{be}). Exploiting the virtual ground at the emitters of Q_{3-4} and Q_{5-6} the differential input admittance $Y_{\mathrm{in,conv}}$ reads

$$\left(\frac{Y_1}{1+Y_1/j\omega C_3}+Y_3+Y_6\right)||\left(\frac{Y_2}{1+Y_2/j\omega C_4}+Y_4+Y_5\right). \tag{3.10}$$

Treating C_{3-4} as perfect DC-blocks and assuming that admittances Y_{1-6} are equal, it follows

$$Y_{\mathrm{in,conv}}=\frac{3}{2}Y_1. \tag{3.11}$$

Next, the conversion gain and input admittance of a bootstrapped frequency doubler (Fig. 3.2a) is investigated. Since the base voltage is taken from Q_{1-2} collectors, $v_{\mathrm{b}}=v_{\mathrm{c}}$ assuming that C_{3-4} are infinite. In order to use (3.5) for obtaining the conversion gain, the following relationship can be applied

$$v_{\mathrm{b}}=v_{\mathrm{c}}=(i_{\mathrm{c1}}-i_{\mathrm{c2}})Z_{\mathrm{c}}=g_{\mathrm{m}}v_{\mathrm{i}}Z_{\mathrm{c}}. \tag{3.12}$$

Z_{c} is a transformed impedance Z_{e} presented by Q_{3-6} emitters

$$Z_{\mathrm{e}} \approx \frac{1}{g_{\mathrm{m}}}, \tag{3.13}$$

assuming that $Y_{3-6} \ll g_{\mathrm{m}}$ and noticing that g_{m} of Q_{3-6} is two times smaller than that of Q_{1-2} since I_{C1} is equally divided between Q_3 and Q_5. Z_{c} reads

$$Z_{\mathrm{c}} = Z_0 \frac{Z_{\mathrm{e}} + jZ_0 \tan(\theta)}{Z_0 + jZ_{\mathrm{e}} \tan(\theta)}, \tag{3.14}$$

where Z_0 is characteristic impedance and θ is the length of TL_{3-4}, respectively. Combining (3.14) and (3.12) gives

$$v_{\mathrm{b}} = g_{\mathrm{m}} v_{\mathrm{i}} Z_0 \frac{Z_{\mathrm{e}} + jZ_0 \tan(\theta)}{Z_0 + jZ_{\mathrm{e}} \tan(\theta)}. \tag{3.15}$$

Using (3.6) v_{b} is expressed with respect to v_{i} as follows

$$v_{\mathrm{b}} = V_{\mathrm{i}} g_{\mathrm{m}} Z_{\mathrm{c}} \cos(\omega_{\mathrm{i}} t + \varphi_0). \tag{3.16}$$

Using (3.5),(3.6) and (3.16) and assuming φ_0=0 the output voltage reads

$$v_{\mathrm{o}} = \frac{g_{\mathrm{m}} Z_{\mathrm{L}} V_{\mathrm{i}}^2}{4V_{\mathrm{T}}} g_{\mathrm{m}} Z_{\mathrm{c}} (\cos(2\omega_{\mathrm{i}} t)). \tag{3.17}$$

As previously, by extracting from (3.17) a component at $2\omega_{\mathrm{i}}$, a small-signal conversion gain is defined

$$CG_v = V_{\mathrm{o}}/V_{\mathrm{i}} = V_{\mathrm{i}} \frac{g_{\mathrm{m}} Z_{\mathrm{L}}}{4V_{\mathrm{T}}} g_{\mathrm{m}} Z_{\mathrm{c}}. \tag{3.18}$$

Comparing (3.9) and (3.18) gives

$$CG_{v,\mathrm{boot}} = CG_{v,\mathrm{conv}} g_{\mathrm{m}} Z_{\mathrm{c}}. \tag{3.19}$$

Two cases are particularly worth considering. If there is no TL_{3-4}, θ=0° and Z_{c}=Z_{e}=1/g_{m}. Then, using (3.18) results in

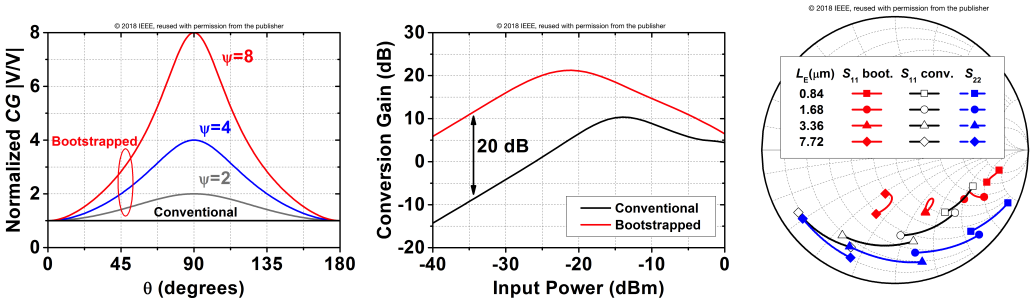
$$CG_{v,\mathrm{boot}} = CG_{v,\mathrm{conv}}. \tag{3.20}$$

The small-signal voltage conversion gain is equal for both configurations, if no delay between V_{b} and V_{e} is introduced. Next, θ=90° is assumed. From (3.18) and

(3.14) it follows

$$CG_{v,\mathrm{boot}} = CG_{v,\mathrm{conv}}(g_\mathrm{m}Z_0)^2. \tag{3.21}$$

The above considerations show, that $CG_{v,\mathrm{boot}}$ can be enhanced with respect to $CG_{v,\mathrm{conv}}$ provided that the factor $Z_0 > 1/g_\mathrm{m}$. Also, the inclusion of TL_{3-4} minimizes the DC component in the output signal, which for θ=90° is equal to zero. The influence of the DC component and a problem of imbalance at the output in general is discussed in [28]. Fig. 3.3a illustrates the derived conversion gain



(a) (b) (c)

Figure 3.3: (a) Normalized small-signal voltage conversion gain of a conventional and bootstrapped doubler versus θ for different $\Psi = (g_\mathrm{m}Z_0)^2$. (b) Example of simulated conversion gain of a conventional and bootstrapped frequency doubler with lossless matching networks. (c) Simulated input and output reflection coefficient of a conventional and bootstrapped FQ for a different transistor size.[17]

of the conventional and bootstrapped frequency doubler. Tuning the length of TL_{3-4} can enhance the gain of the bootstrapped doubler with respect to conventional one. Also, the DC component resulting from the self-mixing can be simultaneously minimized. Notice, that the above analysis does not account for the input impedance seen at the bases of the switching. This finite impedance limits the possible conversion gain improvement since it shunts Z_c. Fig. 3.3b shows a conversion gain example for a conventional and bootstrapped doubler. In this simulation the source and load terminations were matched to the input and output impedances of the circuit resulting in a lossless power transfer from the source to the device and from the output to the load. Both circuits have the same sized transistors with 4 fingers each (L_E=3.36 µm). The bootstrapped doubler has also $\mathrm{TL}_{3-4}$with optimized theta for the highest conversion gain. For low input power

($V_\mathrm{i}, V_\mathrm{b} \ll 2V_\mathrm{T}$) the conversion gain increases linearly with respect to the input power. Here, Z_0=40 Ω and g_m=100 mS resulting in Ψ=16, which corresponds to $CG \approx$24 dB. The simulated conversion gain for the bootstrapped doubler is around 20 dB higher than for the conventional one under the small signal conditions. The difference between the calculated and simulated values comes from neglecting many factors in the analysis. Nevertheless, the advantage of the bootstrapped topology over the conventional one is clearly visible. As the input power increases the conversion gain starts to compress and eventually it starts to decrease for high input power levels. Since the frequency doubler is typically operated with high input power, large-signal simulations were performed to obtain a fair comparison between the architectures (Fig. 3.3b).

The input admittance of the bootstrapped frequency doubler is determined only by the input transistors Q_{1-2} and is given by

$$Y_\mathrm{in,boot} = \frac{1}{2}Y_1 = \frac{1}{3}Y_\mathrm{in,conv}. \tag{3.22}$$

Notice, that the input admittance of a bootstrapped doubler is three times lower with respect to the conventional architecture which was confirmed in small-signal simulation of both structures. Fig. 3.3c presents input and output reflection coefficient in 25-55 GHz and 100-220 GHz range, respectively, for different emitter lengths L_E. In this simulation, the size of Q_{1-6} was kept equal so that all transistors have the same r_be and C_be. Due to less sensitive change of S_{11} over the frequency in case of a bootstrapped frequency doubler, this topology s expected to have larger bandwidth with respect to the conventional architecture. Notice, that the change of S_{22} over the frequency is more sensitive than the change of S_{11} (for a bootstrapped doubler) meaning that the circuit is bandwidth limited at the output.

Instead of cascading two frequency doublers, a stacked topology is proposed for wider bandwidth and less area consumption (Fig. 3.4). Although it requires higher supply voltage, it has an advantage in terms of bandwidth and compactness. Since a cascaded FQ consists of two branches, which must be DC-decoupled, it requires an interstage matching network, thus limiting the bandwidth, introducing more losses and having a negative impact on the circuit size. It also dictates using more complex biasing, since the stages must be DC-decoupled.

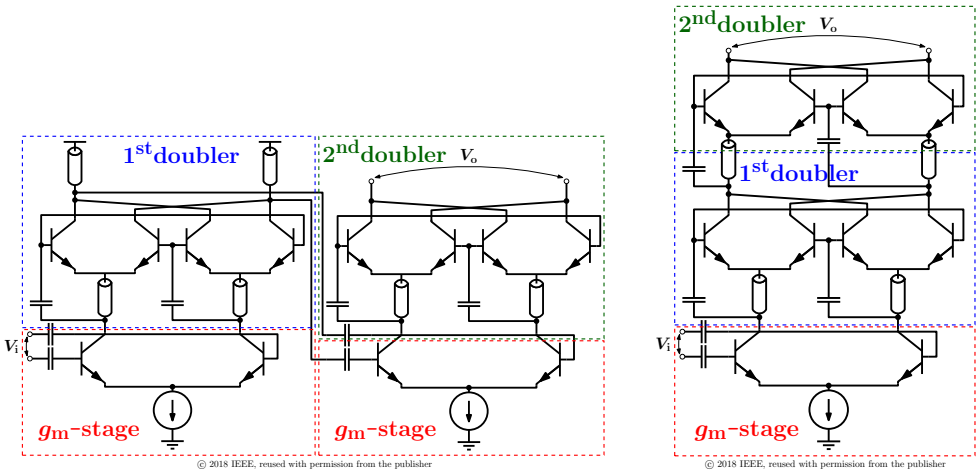


Figure 3.4: Frequency quadrupler formed with (a) two cascaded and (b) two stacked Gilbert-cell frequency doublers. Adapted from [17] with permission from the publisher.

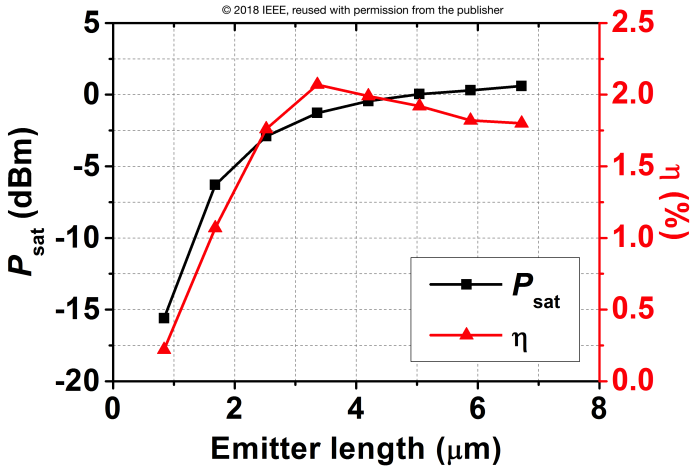


Figure 3.5: Simulated P_{sat} and DC-to-RF efficiency versus transistor size [17].

In order to optimize the FQ for bandwidth and output power, the transistor size has been varied at the constant optimum emitter current density $J_{\mathrm{E_{opt}}} \approx 1.2\,\mathrm{mA/\mu m}$ for the highest $f_{\mathrm{T}}/f_{\mathrm{MAX}}$. Power handling capabilities of a transistor can be improved by increasing its size. Fig. 3.5 shows simulated saturated output power and RF-to-DC efficiency of a stacked FQ for different emitter size of the available transistors. The IHP technology offers discretely scalable HBTs with maximum number

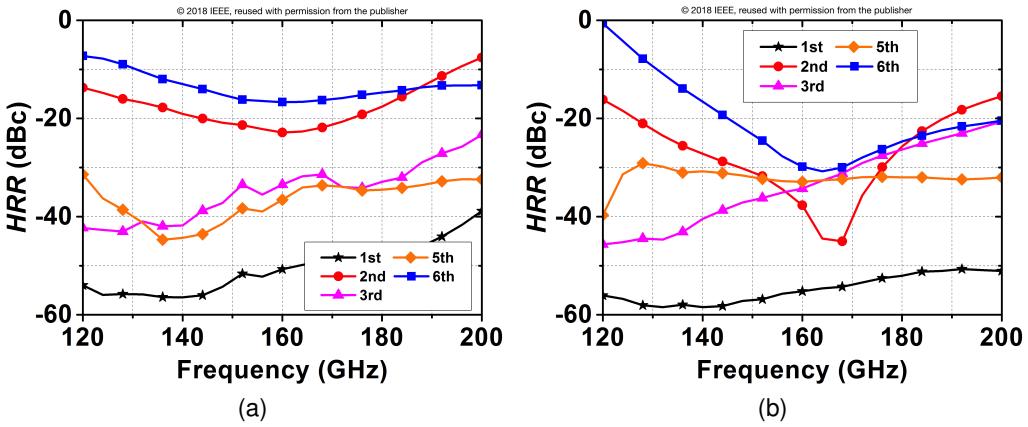


Figure 3.6: Simulated HRR (a) without tail resistor and (b) with tail resistor [17].

of eight fingers for a single device. A 5-finger transistor has been chosen as a compromise between maximum output power and RF - to-DC efficiency, which corresponds to 4.2 um emitter length. The analyses presented in 3.1.1 do not account for transistor parasitics and an EM simulation must be performed to obtain the optimum TL_{3-4} length. Also, DC-decoupling capacitors (C_{3-4} in Fig. 3.2a) change the optimum theta. The choice of C_{3-4} is dictated by their resonant frequency (determines the upper limit) and layout restrictions. In order to keep the layout compact, C_{3-4} should be small but still large enough to not impact the signal. Here, 200 fF was used. According to simulations, the phase of Vb is ahead of Ve by approx. 10 degrees (at 40 GHz) which makes the optimum theta less than 90°. After EM simulation, the optimum theta appeared to be approx. 60° which is beneficial from the layout point of view. The TL_{3-4} characteristic impedance Z_0 was chosen to be 70 Ω, g_{m}=170 mS and 85 mS for Q_1 and Q_{2-9}, respectively, which satisfies $Z_0 > 1/g_{\mathrm{m}}$ condition.

Fig. 3.6a shows simulated harmonic rejection ratios (HRR) of the stacked FQ without a tail resistor in the g_{m} - stage. The second and the sixth harmonics have visibly higher level than the other harmonics. The second harmonic current caused by the transistor nonlinearity not only leaks to the output, but it is also doubled and self-mixed in the switching quad. Adding a tail resistor in the g_{m} - stage improves second and sixth HRR by more than 10 dB at 150-180 GHz (Fig. 3.6b), since it introduces a degeneration for common-mode signals, especially the second harmonic.

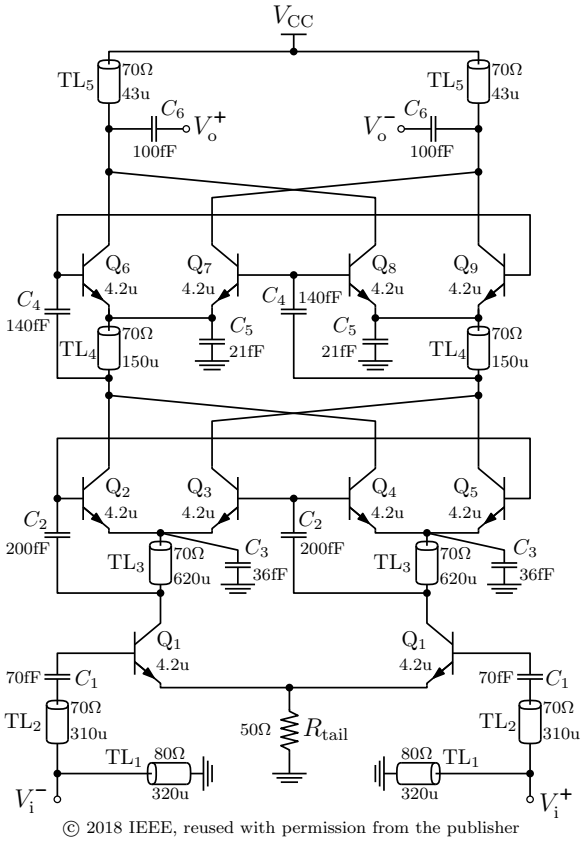


Figure 3.7: Schematic of the stacked bootstrapped Gilbert-cell FQ [17].

The schematic of the optimized stacked FQ is presented in Fig. 3.7. Current mirrors (not shown) were used to generate DC voltage bias for the core transistors. TL_3 and TL_4 introduce a delay for higher voltage swing at the switching quad and thus higher conversion gain. Small C_3 and C_5 help to increase HRR by shunting higher harmonics to ground while having a negligible effect on the fundamental signal and optimum theta. TL_1, TL_2, C_1 and TL_5, C_6 match the impedance to 100Ω at the input and output, respectively.

Fig. 3.8a presents simulated output power and conversion gain versus input power for V_{CC}=4.4 V. Due to high supply voltage, the device reliability was investigated. The simulated V_{CE} waveforms (Fig. 3.8b) show that that V_{CE} cyclically goes beyond BV_{CE0}=1.7 V. However, BV_{CE0} is defined in case of an open base terminal, which represents the worst possible conditions with respect to device reliability. Here, the DC impedance presented at the bases of Q_{6-9} is around 1 kΩ,

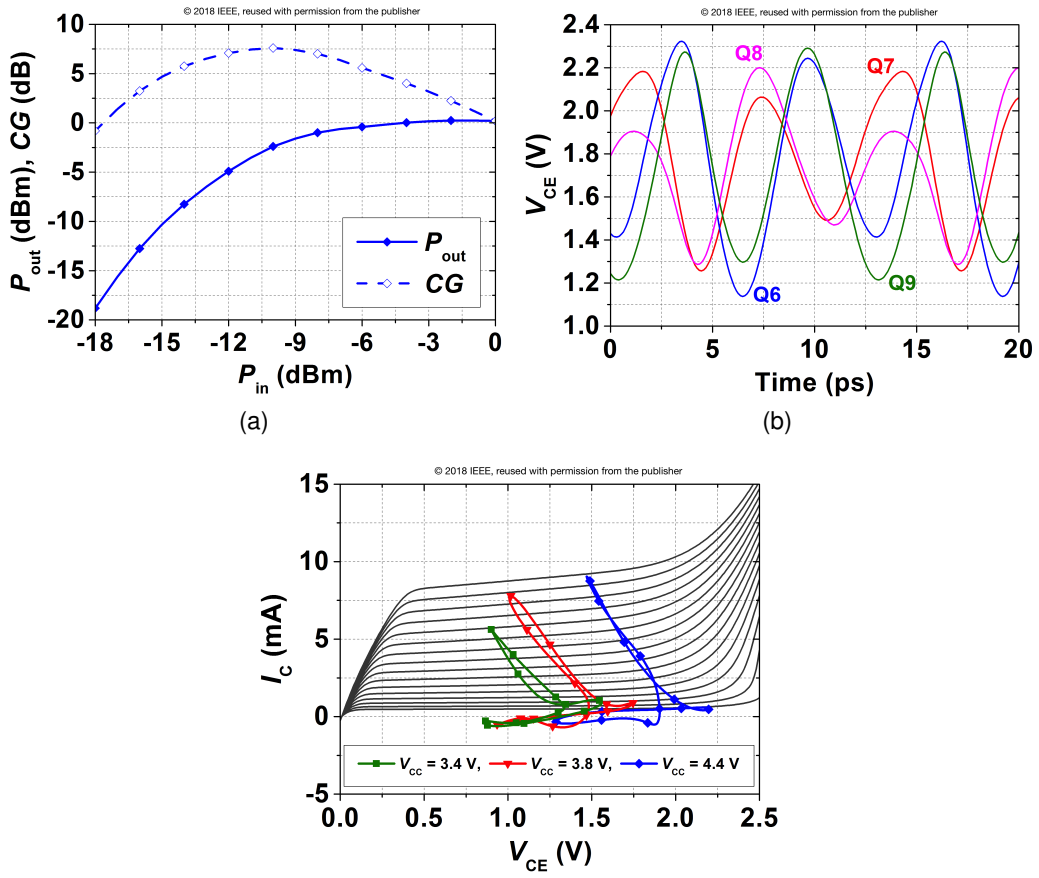


Figure 3.8: (a) Simulated output power and conversion gain for V_{CC}=4.4 V. (b) Simulated V_{CE} waveforms P_{sat} of Q_{6-9} for V_{CC}=4.4 V. (c) Dynamic loadline of Q_6 for different V_{CC}.[17]

which shifts BV_{CE} beyond 2.5 V. Also, as shown in Fig. 3.8c, large V_{CE} occurs at low collector currents meaning that the device is driven within the safe region.

A stacked Gilbert-cell frequency quadrupler was fabricated in a SiGe 130 nm BiCMOS technology using a SG13G2 process of IHP [13]. The transistors achieve $f_{\mathrm{T}}/f_{\mathrm{MAX}}$=300/500 GHz and have collector-emitter breakdown voltage BV_{CE0}=1.7 V. The die micrograph is presented in Fig. 3.9. The circuit occupies 0.61 mm^2 including bondpads and baluns. The size of the stand-alone FQ is only 0.08 mm^2. A back-to-back Q-band and D-band Marchand baluns have been designed and measured in order to convert differential signals to single-ended

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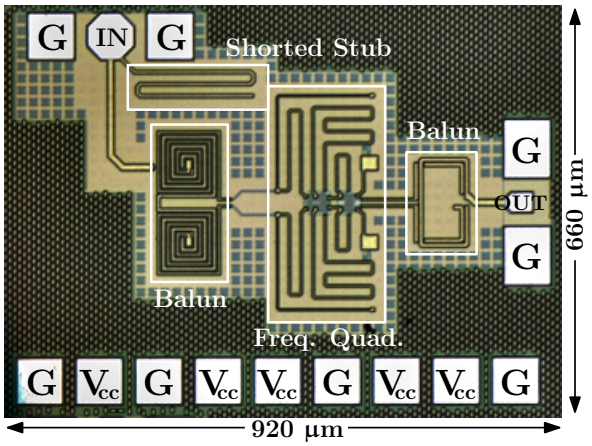

Figure 3.9: Chip micrograph [17].

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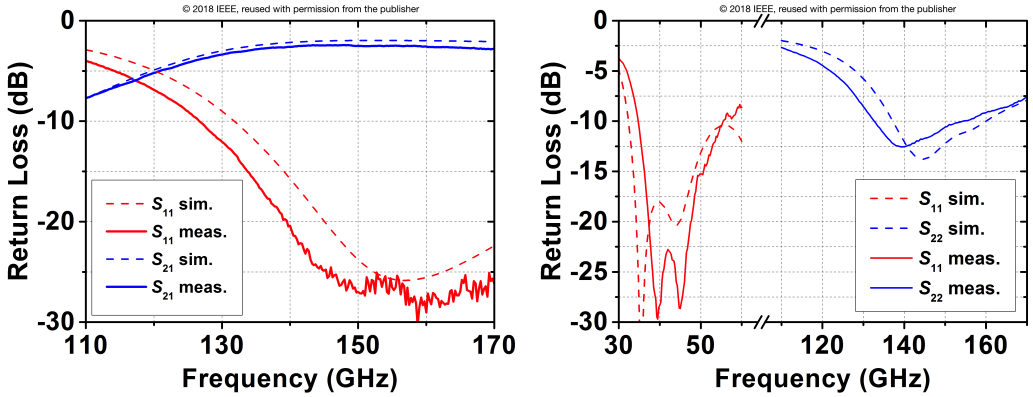


Figure 3.10: (a) Measured input return loss and transmission of the Marchand balun. (b) Measured input and output return loss of the FQ.[17]

format. Measured input return loss and transmission of the D-band balun is depicted in Fig. 3.10a. The input and output return loss of the frequency quadrupler is shown in Fig. 3.10b. Disregarding a slight shift towards lower frequencies there is a good agreement between simulated and measured values. Fig. 3.11 shows the measured saturated output power versus frequency. An external signal source was used to generate the 2.5 dBm driving signal in the 30-45 GHz range. The output power was measured for three different supply voltages using a VDI Erickson PM5 power meter. At 4.4 V the circuit achieves maximum output

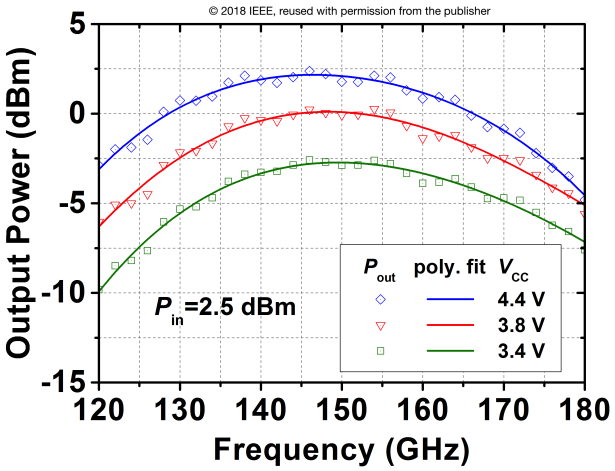


Figure 3.11: Measured output power versus frequency for different V_{CC} [17].

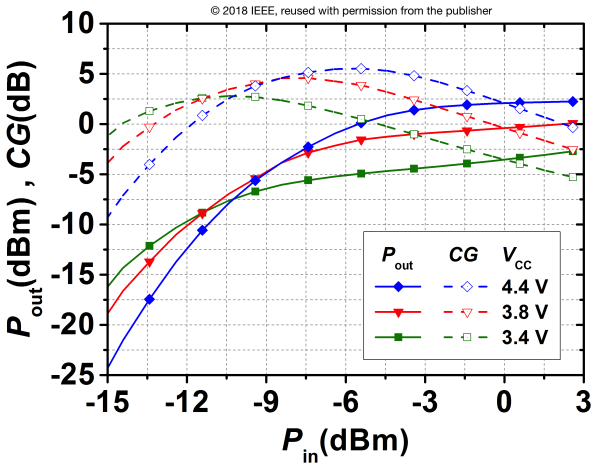


Figure 3.12: Measured output power and conversion gain at 155 GHz versus input power for different supply voltages [17].

power of 2.2 dBm and 3-dB bandwidth of 42 GHz. Fig. 3.12 presents the output power and conversion gain versus input power at 155 GHz for three different voltage supplies. At 4.4 V the circuit achieves 5 dB conversion gain and saturates at 2.2 dBm output power. At 3.4 V the quadrupler has still a positive conversion gain of 2.5 dB and saturates at -4 dBm output power. Fig. 3.13 shows the drain efficiency of the frequency quadrupler defined as the ratio of the RF output power to the DC power consumption (η) together with the power added efficiency accounting for the input power defined as $PAE = (P_{\mathrm{out}} - P_{\mathrm{in}})/P_{\mathrm{DC}}$. Also, the highest

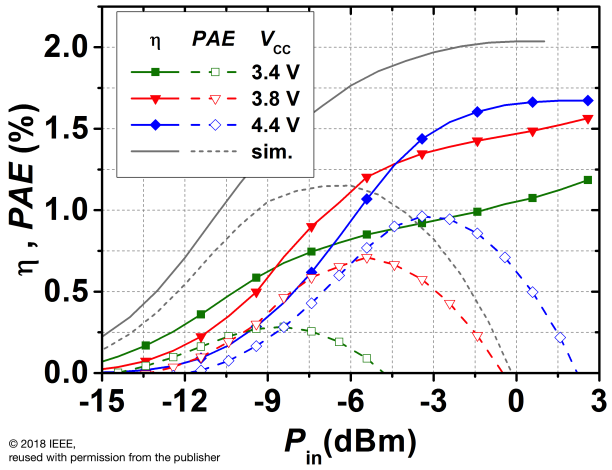


Figure 3.13: Measured efficiency at 155 GHz versus input power for different V_{CC} [17].

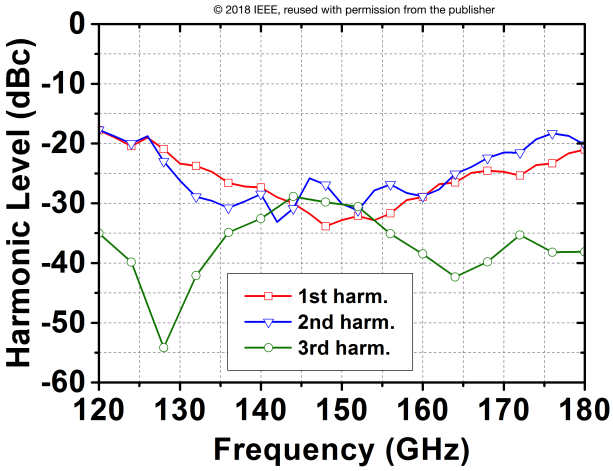


Figure 3.14: Measured HRR of the frequency quadrupler [17].

simulated η is plotted, which occurred for supply voltage of 3.4 V. Increasing the supply voltage in simulation did not necessarily led to better efficiency, which is probably due to inaccurate large-signal models of a transistor. Hypothetically, η could be further enhanced by removing the tail resistor but most likely it would not exceed 2.5%. At 4.4 V the presented circuit achieves 1.7 % DC-to-RF efficiency and 0.9 % PAE at 155 GHz. Fig. 3.14 presents the measured harmonic spur rejection defined as the power ratio of an unwanted harmonic signal to the desired fourth harmonic. In order to measure harmonic signals, different measurement

setups were used. The leaked fundamental signal was measured directly using a 50 GHz E4448A spectrum analyzer from Agilent. For the 2th and 3rd harmonic, E-band and F-band setups were used including waveguide sections and subharmonic mixers. In the 129-171 GHz range, the unwanted harmonic leakage is well below -20 dBc with respect to the fourth harmonic. Differences between simulated and measured values of HRR can be due to fact, that in simulation it is not possible to capture coupling occurring through the substrate. Due to lack of measurement equipment, higher harmonics could not be measured.

3.1.2 Transformer-Based Injection-Locked Frequency Quadrupler

Another group of frequency multipliers are based on injection-locking phenomenon, which has been studied since 1946 [29]. Injection-locked oscillators (ILO) drew attention in recent years due to high-efficiency and low-power potential in clock recovery systems [30,31]. An ILO can serve as a frequency multiplier, if it is locked by a harmonic of an injected signal. Since the oscillator is a self-regenerating circuit it is expected to provide constant output power at very low input power levels. In locked state, the oscillator tracks the phase of the injected signal providing a clean and stable output signal [30]. Also, injection-locked VCOs enable phase tuning, which is very attractive for phased-array applications. Until now, mostly injection-locked frequency triplers (ILFT) [32,33] have been reported whereas only few frequency doublers or quadruplers can be found in the literature [26,34].

Generation of higher harmonics usually requires nonlinear amplifiers biased in weak inversion or even cut-off regions [32, 33]. This results in narrow locking range, since a strong driving signal is needed to generate the harmonic at the desired power level. Therefore, a push-push VCO topology was chosen in order to implement the second frequency doubling and relax the requirements on the harmonic generator. The harmonic generator has to generate a second harmonic of the input signal (40 GHz to 80 GHz) in order to lock the VCO. The signal strength of this generated second harmonic is much larger than the fourth harmonic which would be required if the VCO ran at fundamental 160 GHz. The VCO is implemented as a common-collector Colpitts oscillator for the following reasons. The

tank circuit is inherently buffered from the output by a small base-collector capacitance. A Colpitts topology allows for simple biasing of the bipolar transistors with respect to a cross-coupled configuration and it can be conveniently combined with accumulation-mode MOS varactors available in the IHP technology.

Placement of the harmonic generator, also called an injector, is critical in terms of ILFQ locking range. From [29] the maximum locking range of the VCO can be found to be

$$\Delta\omega_{\max} = \frac{I_{\mathrm{inj}}}{I_{\mathrm{osc}}}\frac{\omega_0}{2Q} \tag{3.23}$$

where I_{inj} and I_{osc} are the injected and free-running VCO currents, ω_0 is the free-running VCO frequency and Q is the LC-tank circuit quality factor. In order to maximize the locking range, the injected signal should be strong with respect to the VCO signal whereas Q should be as low as possible to maintain the oscillation. Fig. 3.15 shows two possible configuration, where a signal V_{inj} is injected into the VCO. In Fig. 3.15a (dashed) the signal is injected through devices that are placed in parallel with the core transistors [26,35]. Since V_{inj} pulls the current from the collectors, only a small portion of the injected signal leaks to the tank circuit resulting in poor locking range. Another solution is to place injecting transistors directly at the tank circuit (Fig. 3.15a (dotted)) but this would have a heavy impact on the tuning range (TR) due to parasitic capacitances associated with the injecting devices. Here, a solution is proposed, which implements the injection of the locking signal through a transformer created from the emitter inductors (Fig. 3.15b). Fig. 3.15c shows a VCO half-circuit used to determine impedance transformation from harmonic generator output. The oscillation frequency of the Colpitts VCO is

$$\omega_0 = \frac{1}{\sqrt{L_{\mathrm{b}}C_{\mathrm{eq}}}} = \frac{1}{\sqrt{L_{\mathrm{b}}\frac{C_1 C_{\mathrm{eff}}}{C_1} + C_{\mathrm{eff}}}} \tag{3.24}$$

where L_{b} is the base inductor, C_1 is the capacitor shunting the intrinsic nonlinear base-emitter capacitance and C_{eff} is the effective capacitance given by

$$C_{\mathrm{eff}} = \mathrm{Im}(Y_{\mathrm{E}})/\omega \tag{3.25}$$

where Y_{E} denotes an equivalent admittance of the circuit comprising the transformer. Notice, that Y_{E} must be capacitive to provide positive loop gain in the VCO. Typically L_{e} is large enough so that the resonant frequency f_0 of the C_{var}-

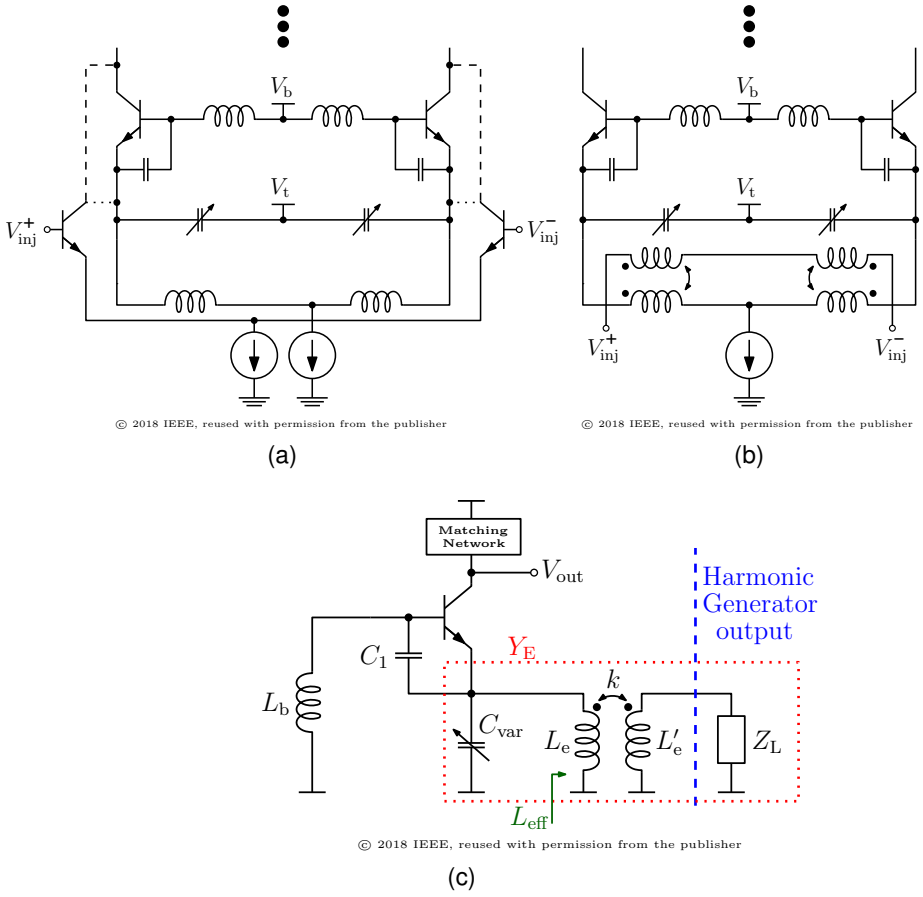


Figure 3.15: (a) Conventional direct injection with parallel transistors. (b) Proposed indirect injection using coupled inductors. (c) Half IL-VCO circuit. The load presented by the harmonic generator (Z_L) is transformed changing Y_E and L_{eff}. [17]

L_e network lies well below ω_0. According to [36], L_e also improves the VCO tuning range, since the parasitic capacitance of the current source is no longer shunted to C_{var}. Taking the transformer into account (Fig. 3.15c), the effective impedance Z_{eff} seen at the input of L_e can be expressed as

$$Z_{eff} = j\omega \underbrace{\left(L_e - \frac{k^2 X_e X'_e L'_e}{Z_L^2 + X_e'^2}\right)}_{L_{eff}} + \underbrace{\frac{k^2 X_e X'_e}{Z_L + \frac{X_e'^2}{Z_L}}}_{R_{eff}} \tag{3.26}$$

where k is coupling factor, X_e and X'_e are reactances of L_e and L'_e, respectively,

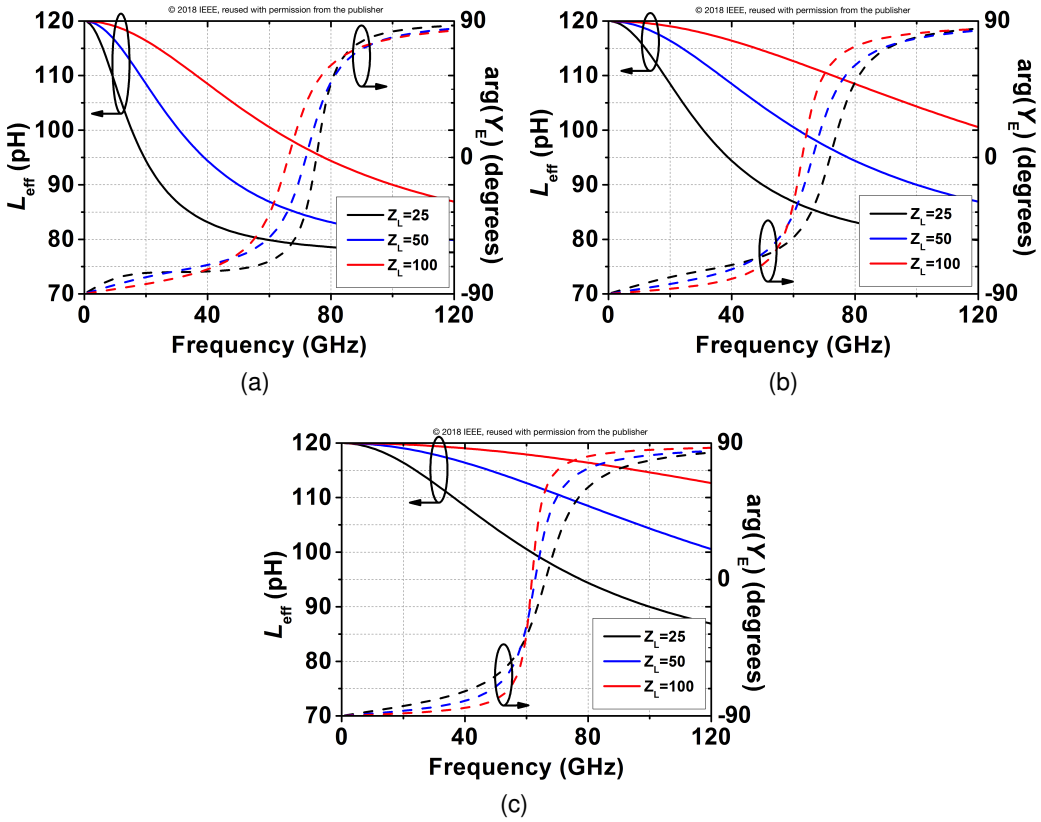


Figure 3.16: L_{eff} and Y_{E} phase for different Z_{L}. (a) L_{e}=120 pH, L'_{e}=240 pH. (b) L_{e}=120 pH, L'_{e}=120 pH. (c) L_{e}=120 pH, L'_{e}=60 pH. Phase zero-crossing indicates f_0 of the C_{var}-L_{e} network (C_{var}=50 fF). [17]

and Z_{L} denotes the load impedance presented by the harmonic generator circuit. In general, Z_{L} is a complex value, but in order to simplify the analysis Z_{L} is assumed to be real, which is a realistic scenario if the imaginary component is compensated by a matching network. According to (3.26), Z_{L} can effectively decrease the inductance and change the resonant frequency of the C_{var}-L_{eff} network so it is instructive to investigate the influence of Z_{L} on L_{eff}. Next, the coupling factor k is assumed to be 0.6, which is high and still achievable in the used technology. High coupling is desired to maximize the signal injected into the VCO tank circuit. Fig. 3.16 presents effective inductance and Y_{E} phase for different real load impedances Z_{L}. The zero-crossing of the Y_{E} phase indicates the resonant frequency of the C_{var}-L_{eff} network. L_{e} and L'_{e} values are arbitrary and serve to depict Z_{L} influence for different $L_{\mathrm{e}}/L'_{\mathrm{e}}$ ratio. The following observations result from

the analysis:

- The lower Z_{L}, the lower L_{eff}. In the extreme case, L_{eff}=(1-k^2)L_{e} for $Z_{\mathrm{L}} \rightarrow 0$.
- L_{eff} deviation from L_{e} is smaller for higher $L_{\mathrm{e}}/L'_{\mathrm{e}}$ ratios.
- High L_{eff} from L_{e} deviation shifts f_0 of the C_{var}-L_{eff} network towards f_{osc}. As a result, Y_{E} may not be purely capacitive at f_{osc} and the VCO will fail to oscillate [36].
- If the transformer is properly designed, i.e., f_0 of the C_{var}-L_{eff} network lies well below VCO frequency range, then the VCO tuning range is only slightly affected, since there are no parasitic components associated with it.

The transformer used to couple the harmonic generator with the PP-VCO was implemented using the topmost thick metal layer TM2 for minimum losses. A $L_{\mathrm{e}}/L'_{\mathrm{e}}$ ratio of around 2 was chosen in order to minimize Z_{L} influence on L_{eff}. Such ratio (case shown in Fig. 3.16c) ensures ,that the deviation of L_{eff} from L_{e} is smaller. This is important since if L_{eff} decreases to much, then the resonant circuit C_{var}-L_{eff} might become inductive. This will cause a Colpitts oscillator not working since it needs a capacitive divider created by C_1 and C_{eff}. Here, the primary (L_{e}) and the secondary coil (L'_{e}) are chosen to have 90 pH and 41 pH, respectively. The simulated loss of the transformer is only 1.3-1.4 dB in 70-90 GHz range. A 250 μm long transmission line $\mathrm{TL_e}$ further increases L_{eff} and shifts the resonant frequency of the C_{var}-L_{eff} network down to around 40 GHz. Having a long transmission line is also desired to ease layout implementation of the ILFQ. Minimum spacing (2 μm) between the inductors is applied resulting in a coupling factor of 0.6 (Fig. 3.17).

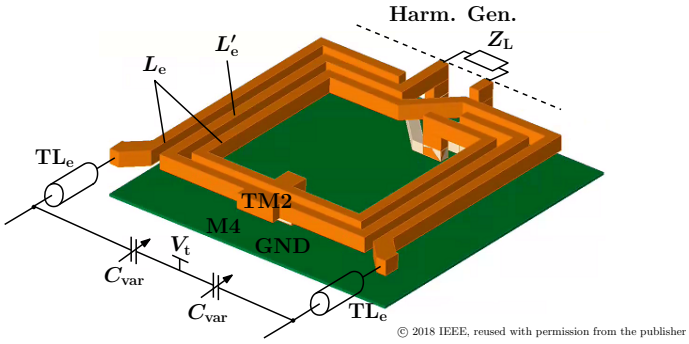


Figure 3.17: Layout of the transformer (1.4 dB loss in the 70-90 GHz range) [17].

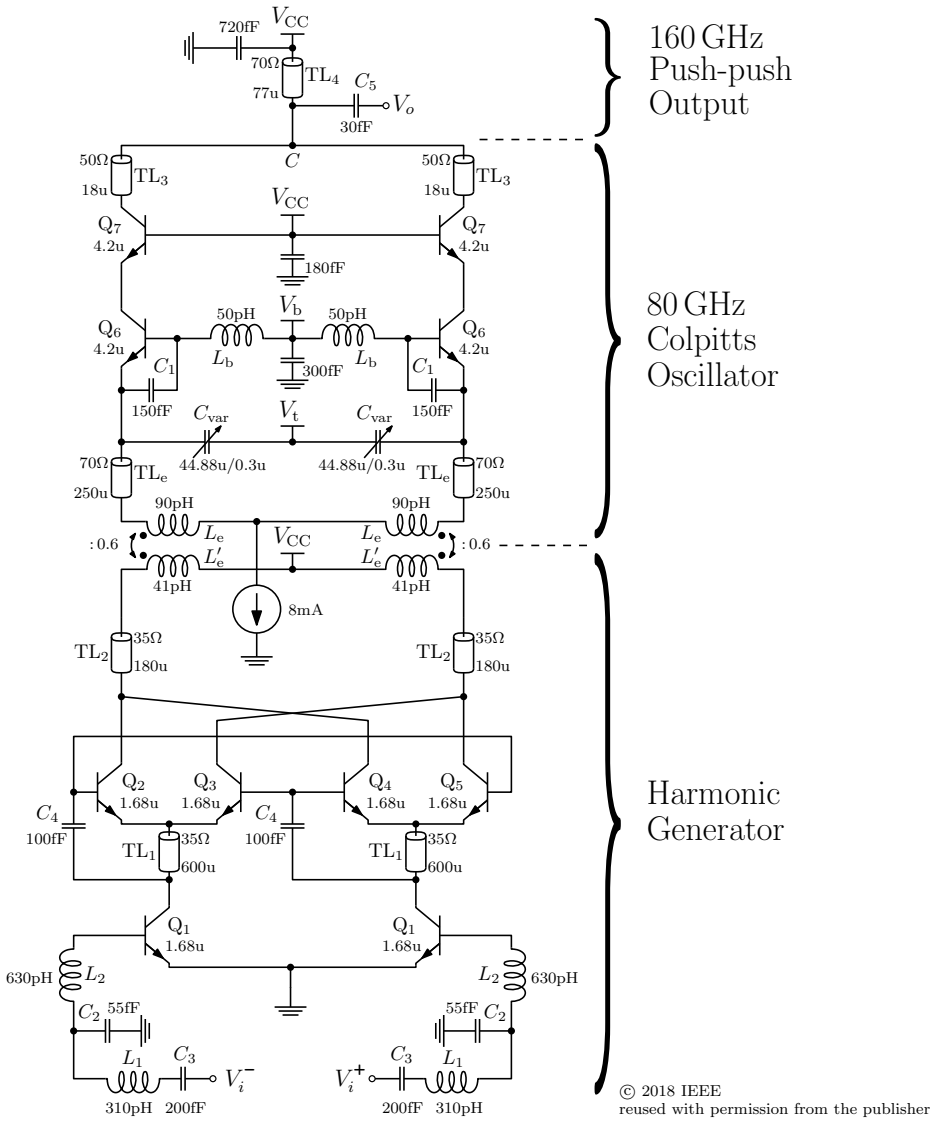
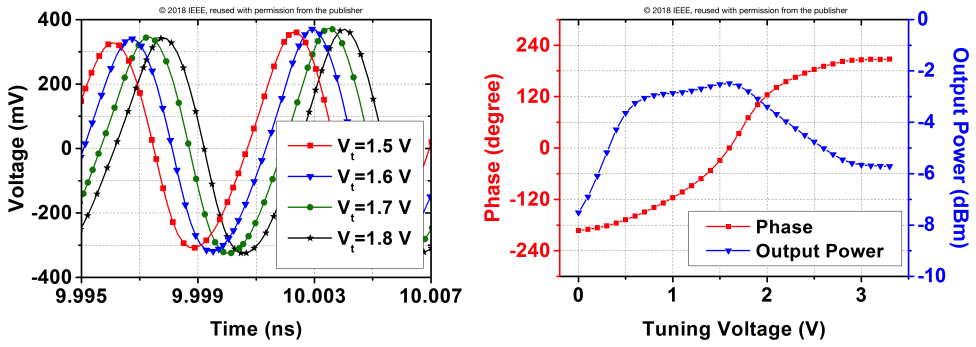


Figure 3.18: Schematic of the IL push-push frequency quadrupler [17].

Choice of the injector topology is dictated by the efficiency of harmonic signal generation. Since the PP-VCO realizes the second frequency doubling, only the second harmonic of the input signal must be generated by the injector. A bootstrapped Gilbert-cell frequency doubler topology was chosen for its superior conversion gain and differential nature. High CG ensures high input sensitivity and injection efficiency, since low power input signals can lock the VCO. It also helps to increase ILFQ locking range as for a certain input power level more energy is

injected into the VCO. The injected signal strength is limited only by power driving capabilities of the harmonic generator. 2-finger HBTs should provide enough maximum power (Fig. 3.5) to lock the VCO.

The design flow of the transformer-based ILFQ (T-ILFQ) begins by implementing a PP-VCO, which should be tunable in the desired frequency range. The process of designing a Colpitts VCO is well described in [36]. Then, the emitter inductors must be replaced by a transformer in such way, that the conditions presented in 3.1.2 are satisfied. This requires a proper transformation ratio $L_\mathrm{e}/L'_\mathrm{e}$ and load Z_L presented by the harmonic generator. At the end, the harmonic generator is implemented to provide an efficient second harmonic injection to the VCO. The schematic of the proposed T-ILFQ is presented in Fig. 3.18. The 80 GHz VCO is implemented as a common-collector Colpitts circuit. Transistors Q_7 serve as a common-base (CB) buffer to increase the output power and improve isolation between the load and the VCO [36]. The even harmonic signals from both half-circuits add in phase at the common node C while the odd harmonics are canceled. TL_4 and C_5 match the load to the optimum impedance for the highest output power at 160 GHz. The transformer used to couple the VCO tank circuit with the injector is composed of L_e and L'_e. A bootstrapped frequency doubler serves as the harmonic generator. Transmission lines TL_2 compensate the capacitance of Q_{2-5}. A matching network comprising L_1, L_2, C_2 and C_3 match the input to 100 Ω at 40 GHz. The simulated maximum locking range for -10 dBm and 0 dBm input power is 149-172 GHz and 144-186 GHz, respectively, where the



(a) (b)

Figure 3.19: (a) Simulated ILFQ output voltage waveforms at 160 GHz for different V_t. (b) Simulated P_out and phase versus V_t at 160 GHz. [17]

whole VCO tuning range was exploited by adjusting V_{t}. Fig. 3.19 shows simulated waveforms of a locked ILFQ at 160 GHz. By changing the control voltage the signal phase can be tuned in 0°-360° range showing potential, e.g., for phased-array systems [37]. However, as the natural VCO frequency is de-tuned from the V_{inj} frequency (160 GHz), the output power decreases due to lower voltage swing at the VCO core.

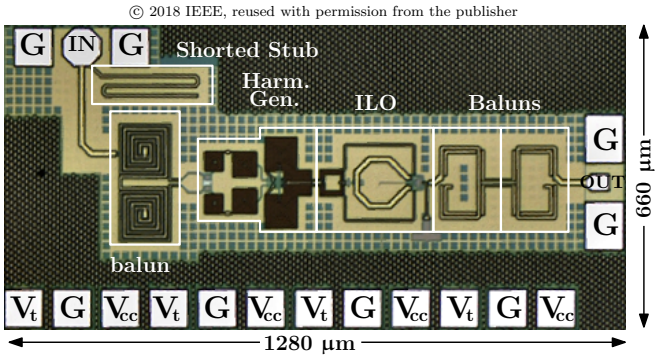


Figure 3.20: Chip micrograph of the ILFQ [17].

A T-ILFQ was manufactured in a SiGe 130 nm BiCMOS technology using a SG13G2 proccess of IHP [13]. The die micrograph is shown in Fig. 3.20. The circuit occupies 0.84 mm^2 including bondpads and baluns. The size of the ILFQ core is only 0.09 mm^2. First, a free-running 160 GHz PP-VCO was measured in the absence of an injected signal. The tuning range as well as the phase noise

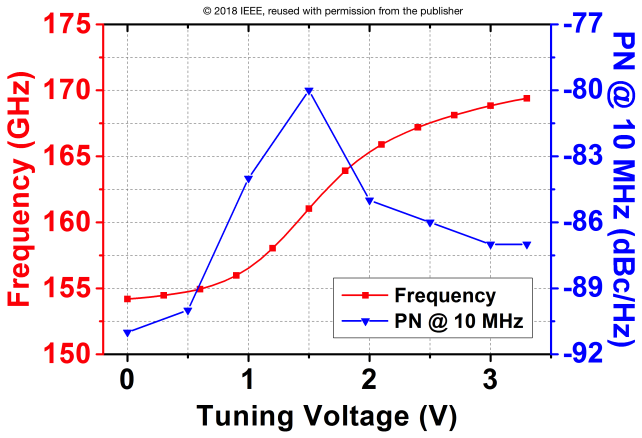


Figure 3.21: Measured TR and PN of the free-running 160 GHz PP-VCO [17].

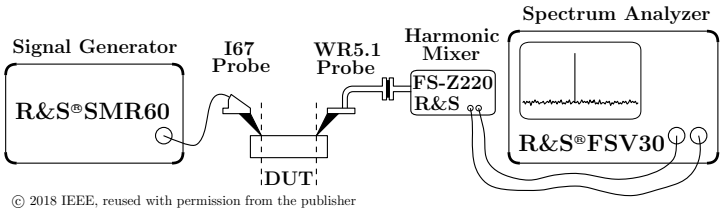


Figure 3.22: Setup for the output power and phase noise measurement [17].

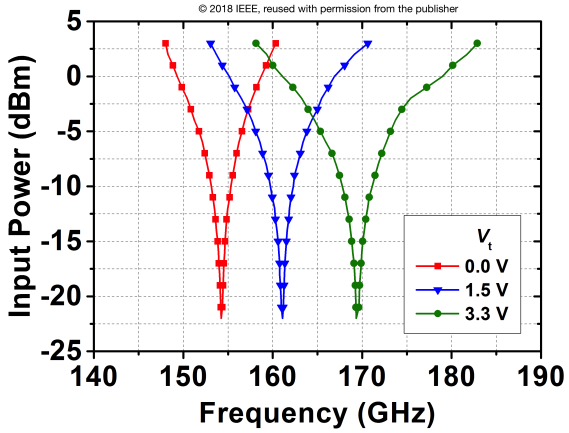


Figure 3.23: Measured locking range of the ILFQ [17].

at 10 MHz frequency offset from the carrier is presented in Fig. 3.21. The setup used to measure the phase noise and output power is presented in Fig. 3.22. The phase noise was calculated using the following formula

$$PN(f_{\mathrm{m}})[\mathrm{dBc/Hz}] = P_{\mathrm{N}}[\mathrm{dBm}] - P_{\mathrm{C}}[\mathrm{dBm}] - 10\log(\mathrm{RBW}[\mathrm{Hz}]), \tag{3.27}$$

where f_{m} is the frequency offset, P_{N} is the noise power at f_{m}, P_{C} is the carrier power and RBW is the bandwidth of RBW filter in the spectrum analyzer. The VCO can be tuned in the 154-169 GHz range which corresponds to 9.3% tuning range. This is around 25% less than simulated mostly due to not properly modeled varactor capacitance at higher frequencies. The phase noise of a free-running VCO varies in -91 to -80 dBc/Hz range. The worst phase noise is observed in the middle of the tuning range where the VCO gain reaches the highest value. Next, a 40 GHz signal was applied in order to lock the VCO. Fig. 3.23 presents measured T-ILFQ locking range for different tuning voltages. As expected, if the quadrupled frequency of the V_{inj} is very close to the natural fre-

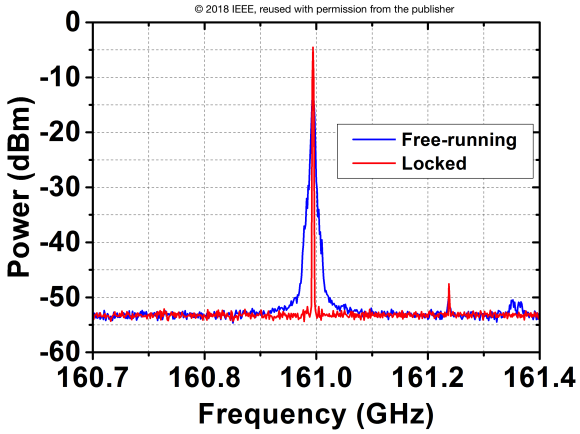


Figure 3.24: Spectrum of the free-running and injection-locked VCO [17].

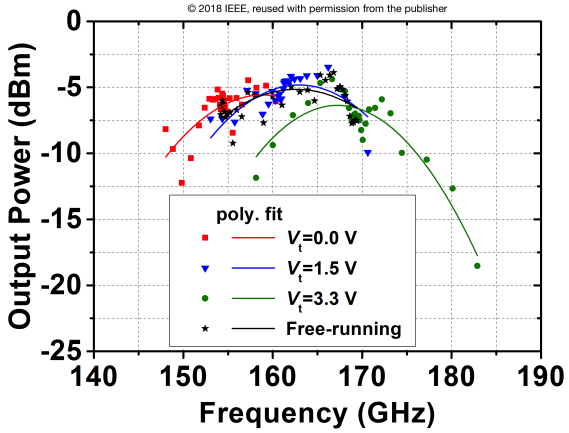


Figure 3.25: Measured output power of the ILFQ [17].

quency of a free-running VCO, only -22 dBm input signal is needed to lock the VCO. As the input frequency changes, more input power is required in order to lock the VCO. By adjusting V_t the locking range of the T-ILFQ can be extended and it reaches 35 GHz around 165.5 GHz for +3 dBm input power. The ILFQ consumes 14.8 mA from 3.3 V supply. A spectrum of a free-running and locked VCO is shown in Fig. 3.24 indicating a stable 161 GHz output signal locked to the 40.25 GHz signal coming from the signal generator. Fig. 3.25 presents measured locked T-ILFQ output power for different tuning voltages and also when the VCO is free-running. For this measurement, a setup presented in Fig. 3.22 was used. Unfortunately, due to aging and extensive use of the subharmonic mixer the cali-

Table 3.1: Summary of stacked FQ performance and comparison with the state of the art [17].

Ref.	Process	$f_{\mathrm{T}}/f_{\mathrm{MAX}}$	Type	Frequency [GHz]	BW_{f}^{a} [%]	P_{sat} [dBm]	CG_{max} [dB]	η_{max}^{b} [%]	PAE_{max}^{c} [%]	P_{DC}^{d} [mW]	Area [mm^2]
[38]	32 nm CMOS	300/350	$\times 4$	124-158	24.1	2.3	-21	5.3	<0	32	0.06[e]
[39]	250 nm InP	350/650	$\times 4$	110-130	16.6	7	2	10	3.9	47	0.13[e]
[40]	130 nm SiGe	NR	$\times 4$	121-137	12.4	-2.4	0.6	1.6	0.2	35	0.03[e]
[41]	130 nm SiGe	NR	$\times 4$	124-132.5	6.6	4.4	3	2.4	1.2	115	0.12[e]
[42]	55 nm SiGe	320/370	$\times 4$	130-154	16.9	10	5	1.6	1.1	610	0.71[e]
[43]	130 nm SiGe	250/370	$\times 4$	128-156	19.7	4	26	1.9	1.9	132	0.11[e]
[44]	90 nm SiGe	300/350	$\times 4$	214-245	13.5	2	-10	0.8	<0	200	1.44
[45]	130 nm SiGe	300/500	$\times 2$	138-170	20.7	5.6	4.9	10.9	7.6	36	0.48
[46]	250 nm InP	350/600	$\times 2$	120-158	27.3	4.2	-2	11.9	<0	19.2	0.18
[46]	250 nm InP	350/600	$\times 3$	162-189	15.3	3.8	-1	7.7	<0	26	0.36
This Work	**130 nm SiGe**	**300/500**	$\times 4$	**129-171**	**28.0**	**2.2**	**5**	**1.7**	**0.9**	**100**	**0.08**

[a] $BW_{\mathrm{f}} = (f_{\mathrm{max}} - f_{\mathrm{min}})/f_{\mathrm{center}}$, [b] $\eta = P_{\mathrm{sat}}/P_{\mathrm{DC}}$, [c] $PAE = (P_{\mathrm{out}} - P_{\mathrm{in}})/P_{\mathrm{DC}}$, [d] at P_{sat},
[e] estimated from the chip photo

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bration table no longer fits to reality causing a heavy ripple seen in the measured output power. The T-ILFQ achieves - 4 dBm output power at 163 GHz and more than - 7 dBm in 153-172 GHz range.

The performance of the stacked and injection-locked frequency quadruplers is summarized in Tab. 3.1 and Tab. 3.2, respectively. Due to bootstrapping technique, the stacked FQ achieves the widest bandwidth among other reported circuits providing moderate conversion gain and output power. Since it is a single-branch circuit, the silicon area can be greatly reduced. It is possible to save even more area by replacing long transmission lines with compact inductors. Combination of a Colpitts PP-VCO and bootstrapped frequency doubler enabled the ILFQ to achieve the widest locking range among other IL frequency multipliers while providing moderate efficiency and output power.

The stacked FQ is superior in terms of several parameters with respect to injection-locked FQ. It provides wider bandwidth and more output power at the

Table 3.2: Summary of ILFQ performance and comparison with other IL frequency multipliers [17].

Ref.	Process	$f_{\mathrm{T}}/f_{\mathrm{MAX}}$	Type	Frequency [GHz]	Locking Range[a] [%]	P_{out} [dBm]	PAE^{b}_{max} [%]	P_{DC} [mW]	Area [mm^2]
[32]	65 nm CMOS	NR	$\times 3$	85-95.2	5.7	-3.8	8.0	5.2	0.09
[47]	90 nm CMOS	155/250	$\times 3$	56-65	14.9	-24.7	<0.1	23.8	0.09
[48]	90 nm CMOS	NR	$\times 3$	88.1-108.5	20.7	-15	<0.1	55.2	0.35
[33]	90 nm CMOS	NR	$\times 3$	91.2-97.1	6.3	-20	1.0	1	0.49
[49]	65 nm CMOS	185/255	$\times 9$	88-99.5	12.3	8.5	1.6	438	0.45
This Work	**130 nm SiGe**	**300/500**	$\times 4$	**148-183**	**21.1**	**-4**	**0.8**	**49**	**0.09**

[a] $(f_{\mathrm{max}} - f_{\mathrm{min}})/f_{\mathrm{c}}$, [b] $PAE = (P_{\mathrm{out}} - P_{\mathrm{in}})/P_{\mathrm{DC}}$

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similar DC-to-RF efficiency. However, in a narrower frequency range, the ILFQ can be locked at very low input power levels resulting in high conversion gain. In addition, due to phase shifting potential, it can be used in efficient high frequency phased-array systems. To provide such functionality, the stacked FQ would need to implement additional circuitry resulting in more area and power hungry design. Both frequency quadruplers show similar performance in terms of power consumption and silicon area.

3.2 Solid-State mm-Wave Power Amplifiers

Following the frequency conversion up to the desired band, the TX signal is amplified to the level that ensures a high probability of target detection. At mm-wave frequencies the radiated signal experiences an enormous attenuation due to the propagation loss and backscattering from the targets. This requires a proper PA stage to be used in order to compensate that loss and relax the requirements for the RX gain and antenna directivity.

3.2.1 Two-way E-band Power Amplifier

The design of a PA begins with optimization of the output stage (OS) for maximum output power without compromising on bandwidth and long-term reliability [8]. Recently, an extensive research has been conducted on stacked amplifiers, which provide several benefits over conventional cascode topologies [50], [51]. The main restriction limiting the maximum output power is the breakdown voltage (BV), which for SiGe technology is in the 1.5-6 V range depending on the base termination [52]. The problem becomes more severe for very large-scale integration (VLSI) technologies, where BV drops below 1 V. For a given output power a limited output voltage swing dictates a large current amplitude, which results in a very low output impedance and narrow bandwidth. Transistor stacking permits using a higher supply voltage, since the output swing is equally distributed between the stacked elements, provided that each transistor has an isolated bulk (a feature that is generally not available for HBTs). A slight modification to a bipolar cascode amplifier is introduced allowing for an increased voltage swing at the base of the stacked stage which is beneficial in terms of bandwidth and reliability. Fig. 3.26a shows the schematic of a PA output stage unit consisting of

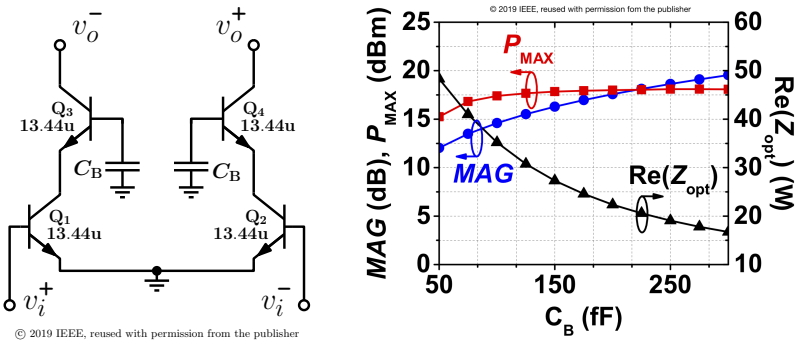


Figure 3.26: (a) Schematic of the capacitively degenerated cascode output stage. (b) MAG, $P_{\max}$ and Re(Z_{opt}) for $P_{\max}$ versus C_{B}. [8]

4 large hetero-junction transistors (HBTs) forming a stacked amplifier. Lack of a "tail" resistor worsens $CMRR$ but ensures higher efficiency since no DC power is dissipated in that component. Also, more voltage headroom is available for the transistors which leads to higher maximum output power. Instead of exploit-

ing the virtual ground to provide a low-loss RF ground at the bases of the CB stage, a series capacitor (C_{B}) is used in order to increase the real part of the optimum load impedance for the maximum output power (Fig. 3.26b). This results in smaller impedance transformation required to match a differential 100 Ω antenna, thereby, higher bandwidth and less losses associated with the combining network. However, a capacitive degeneration in the CB stage decreases the maximum available gain (MAG) and, for small C_{B} values, the maximum output power. From Fig. 3.26b it appears that for C_{B}≈120 fF the $P_{\max}$ maintains high while $\mathrm{Re}(Z_{\mathrm{opt}})$ increases to 32 Ω. The MAG drops by 3 dB but is still large enough to provide desired amplification.

Layout of the large devices dictates using long connections changing the impedance as well as introducing losses. Fig. 3.27a depicts a single OS footprint

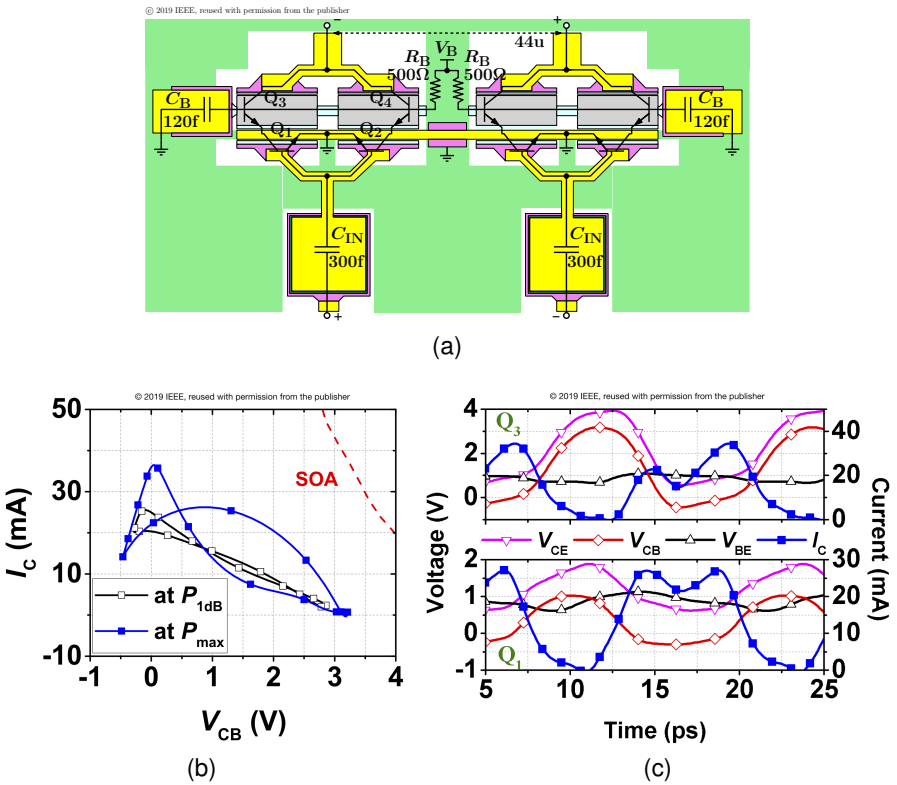


Figure 3.27: (a) Layout of the differential output stage consisting of four 8-finger HBTs. (b) Dynamic loadline of the Q_3 collector current versus collector-base voltage at 1 dB ($P_{1\mathrm{dB}}$) and 5 dB ($P_{\max}$) gain compression point. (c) Waveforms of Q_1 (CE) and Q_3 (CB). [8]

comprising optimized shunt C_{B} and input decoupling C_{IN}. Owing to significant HBT size, the separation between the output pins is 44 µm. Ground plane for the TLs and DC current return path is implemented using two thin metal layers (M2 and M4). Dense metal areas are placed close to the HBTs to avoid problems caused by electromigration. Another limitation concerning high-power designs is the breakdown voltage, which is determined by the process. Here, BV_{CE0}=1.7 V and BV_{CB0}=4.8 V, where the former is given at open base terminal condition. Interestingly, decrease of base impedance results in a higher BV_{CE0}, which eventually reaches BV_{CB0}. Extensive research on transistor's reliability has shown that the maximum allowed voltage constraints are too conservative in case of RF applications [52]. Fig. 3.27b presents the dynamic loadline of a single 8-finger device Q_3 in the CB stage. Notice, that Q_3 operates in safe operation area (SOA) during the whole cycle and does not enter breakdown region. Voltage and current waveforms of Q_1 and Q_3 are shown in Fig. 3.27c. Notably, V_{CE} of the CE stage does not swing beyond its BV (2.4 V) due to typically low impedance seen at the emitter of the CB stage.

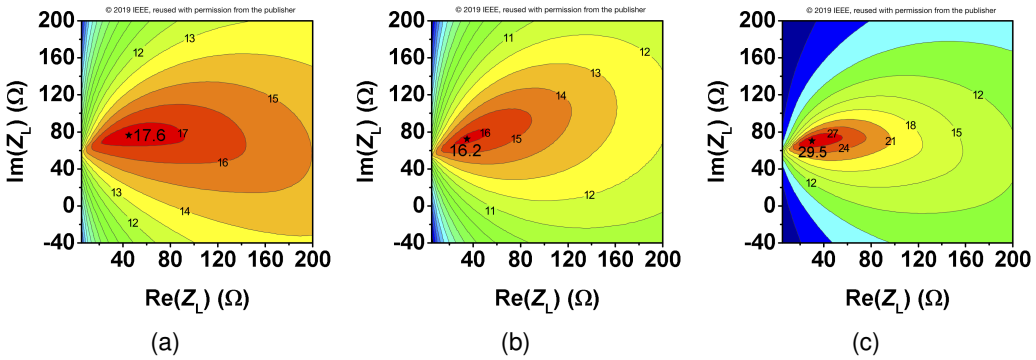


Figure 3.28: Load-pull contours for (a) saturated output power (b) output power at 1 dB CP (c) power-added efficiency. [8]

An OS load-pull simulation was performed to obtain the optimum load impedance, at which the PA achieves the highest output power (P_{max}), linearity (P_{1dB}) and efficiency (PAE_{max}). The simulated contours of constant P_{max}, P_{1dB} and PAE_{max} at 79 GHz are presented in Fig. 3.28. The optimum load impedance for maximum output power of 17.6 dBm is 45+76j Ω and changes to 35+72j Ω, at which the highest P_{1dB}=16.2 dBm is achieved. The best PAE is obtained for Z_{L}=30+70j Ω.

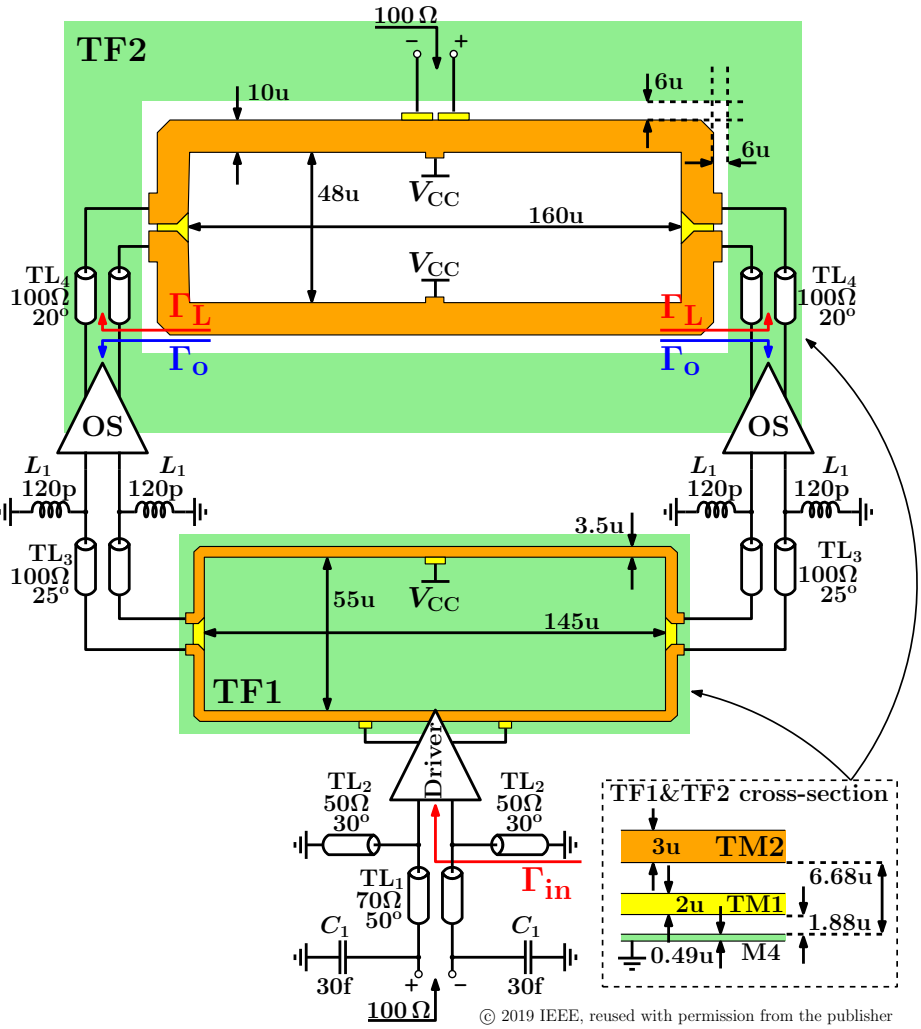
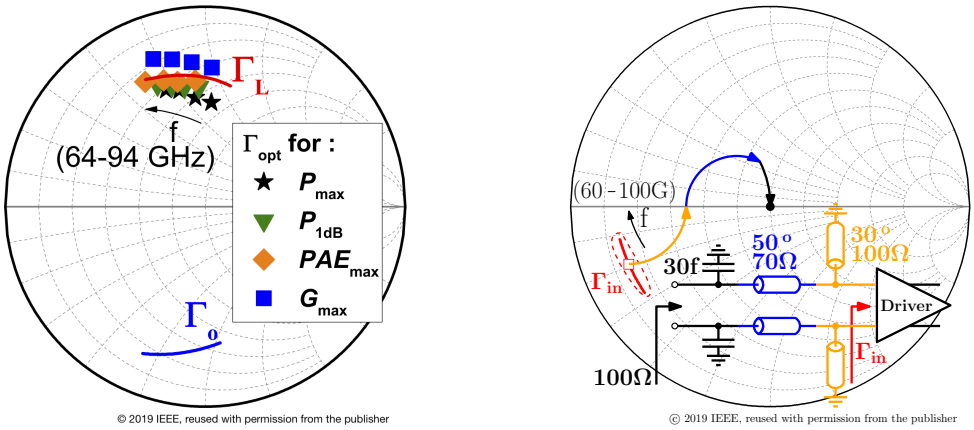


Figure 3.29: Schematic of the 2-way PA. The power is split (TF1) and combined (TF2) by means of a DAT-series combiner using TM1 and TM2 [8].

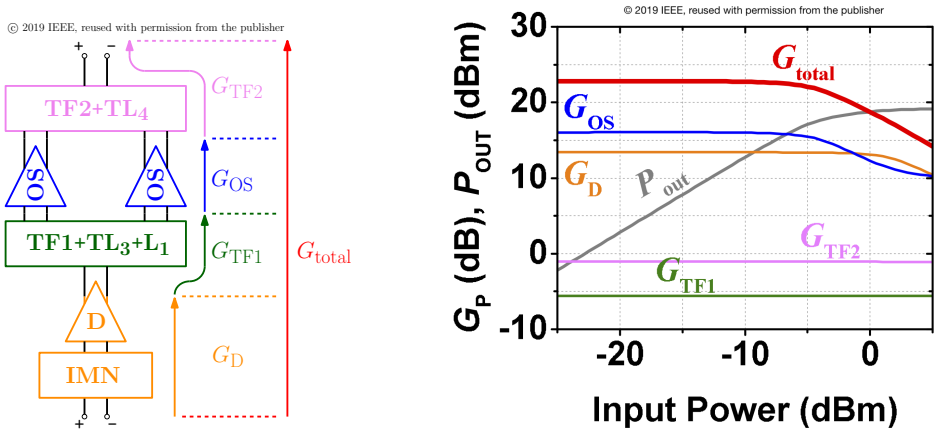
A critical component is the output combining network which transforms the 100 Ω antenna impedance to the desired Z_L at minimum insertion loss. Fig. 3.29 presents the schematic of a two-way PA with visualized output (TF2) and input (TF1) transformers for power combining and splitting, respectively. A single driver stage is sufficient for the large gain available from the cascode circuit (Fig. 3.26b). A distributed-active-transformer-series (DAT-series) structure was chosen to sum the output power from two adjacent OSs [53]. This type of combiner proved to be compact and efficient in the mm-wave frequency range [54, 55]. It consists of



(a) (b)

Figure 3.30: (a) Optimum impedance for $P_{\max}$, $P_{1\mathrm{dB}}$, $PAE_{\max}$ and $G_{\max}$ in the 64-94 GHz range. Γ_{o} indicates the OS output impedance and Γ_{L} is the impedance presented by TF2 and TL_4. (b) Input matching network and impedance transformation from Γ_{in} to 100 Ω. [8]

two closely coupled TL sections implemented in top thick metal layers (TM1 and TM2). Since the TM2 TLs from the adjacent PAs meet at the center of TF2, it is a convenient point to supply the power there. Secondary, TM1 TL is placed directly under the primary ensuring full coupling and small loss. Additionally, the solid ground metal plane under TF2 is removed to reduce parasitic shunt capacitance. The size of TF2 and TL_4 was optimized to transform the 100 Ω load to the desired impedance that is seen by each OS. Here, Z_{L}= 33+79jΩ is between the optimum impedance for P_{max} and G_{max} and close to the best value with respect to PAE_{max} (Fig. 3.30a). Power splitting and interstage matching is realized by means of a DAT-series transformer TF1, TL_3 and shunt L_1. The driver stage employs the same cascode configuration as the OS with Q_{1-4} having 13.44 µm emitter length each. Fig. 3.30b depicts impedance transformation of the driver input (Γ_{in}) to differential 100 Ω. For broadband matching, a shorted stub TL_2 is used to resonate the input capacitance and TL_1 with C_1 serve as a reduced-size quarter-wave transformer to finally match 100 Ω. Fig. 3.31a and Fig. 3.31b show the gain contribution of each segment and compression with respect to the input power. Notably, the OS starts to saturate at around 6 dB lower input power with respect to the driver stage, which results in a high $P_{1\mathrm{dB}}$ and P_{max}.



(a) (b)

Figure 3.31: (a) Gain distribution and (b) gain versus input power. The OS compresses first, indicating a proper driving from the preceding stage. [8]

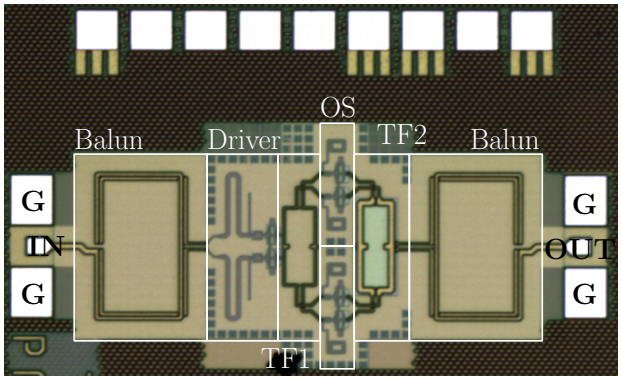


Figure 3.32: Die photograph of the E-band 2-way PA. The circuit occupies 0.15mm excluding bondpads and baluns [8].

The two-way PA was fabricated using the SG13G2 process from IHP [13]. A chip micrograph is shown in Fig. 3.32. Fig. 3.33 presents the large-signal measurement setup for characterization of the PA. A WR-12 signal source from OML is used to drive the PA. A manual attenuator serves to control the input power level, which is verified using a 20 dB directional coupler and harmonic mixer connected to a R&S spectrum analyzer. The loss of the mixer and the coupler is calibrated by measuring the power level at the end of the coupler with an ELVA power detector. The same device is then used to measure the PA output power. The loss of the waveguide probes is de-embedded from the results. Since the

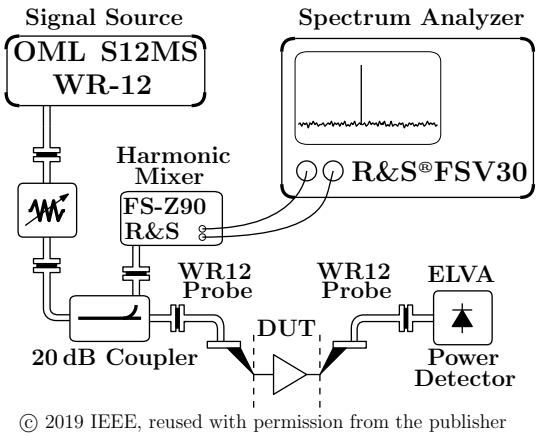
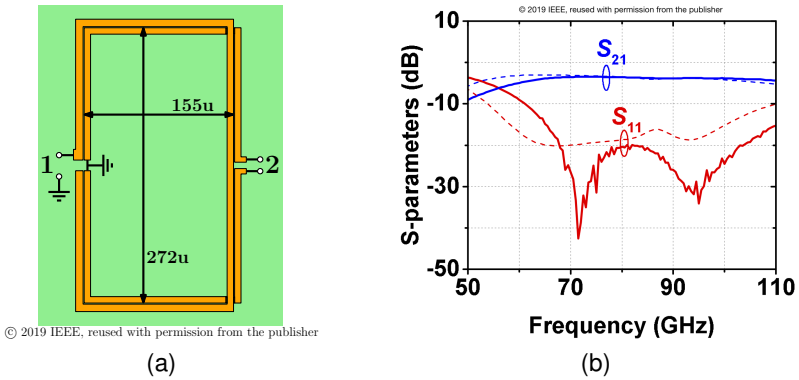


Figure 3.33: Large-signal measurement setup for PA characterization [8].

PA needs a differential input drive, an on-chip planar Marchand balun was implemented to balance the single-ended input signal (Fig. 3.34a). A back-to-back



(a) (b)

Figure 3.34: (a) Layout of a planar Marchand balun. The TLs are 6 µm wide with minimum spacing of 2 µm. (b) Simulated (dashed) and measured (solid) S-parameters of a back-to-back structure. Insertion loss of a single balun is around 1.7 dB. [8]

structure of th same was measured and the loss of the balun was subtracted from the PA measurement results (Fig. 3.34b). Furthermore, a 110 GHz S-parameter setup was used to measure S-parameters of the PA. The circuit achieves 23.4 dB linear gain with broadband matching around 79 GHz. A very good fit to the simulated results is observed owing to thorough EM characterization of the complete structure. Fig. 3.35b shows large-signal measurement results. The PA delivers

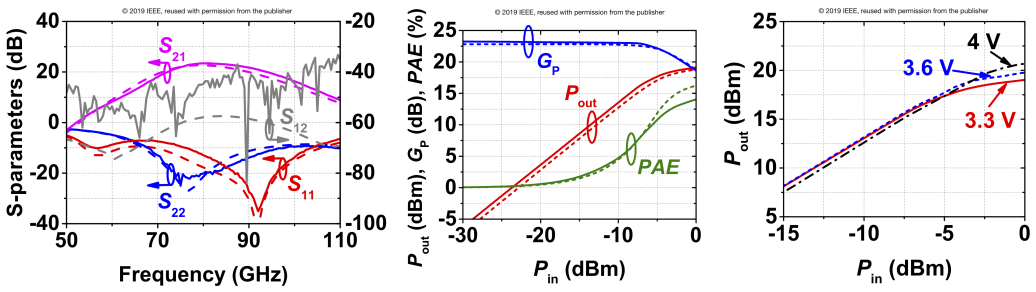


Figure 3.35: (a) Simulated (dashed) and measured (solid) S-parameters of the two-way PA. (b) Simulated (dashed) and measured (solid) large-signal parameters. (c) Measured P_{out} versus P_{in} for different V_{CC}. [8]

Table 3.3: Comparison table of recently reported silicon-based E-band and W-band power amplifiers [8].

Ref.	**This Work**	TMTT'19 [56]	JSSC'17 [50]	ISSCC'17 [57]	TMTT'16 [58]	TMTT'15 [55]	JSSC'14 [51]
Process	**SiGe 130nm**	SiGe 120nm	SiGe 90nm	SiGe 55nm	SiGe 90nm	CMOS 40nm	CMOS 45nm
Supply [V]	**3.3**	2.0	6.5	2.3	1.8	1.8	3.4
Frequency [GHz]	**79**	70	83	80	76	73	91
$\lvert S_{21}\rvert BW_{\text{-3dB}}$ [GHz]	**20**	13	-	20	12	7.6	15
P_{max} [dBm]	**19.3**	19.5	23.3	19	27.3	22.6	19.2
G_{max} [dB]	**17.9**	18.5	21[b]	21	19.3	25.3	12.4
P_{1dB} [dBm]	**17.3**	14.5	-	18	22.3	18.9	15[b]
PAE_{max} [%]	**14**	11	17.1	23	12.4	19.3	14
Power Combining	**2-way Diff.**	4-way Diff.	No Single	No Single	16-way Single	4-way Diff.	No Single
Core Area [mm^2]	**0.15**	1.46[a]	1.95[a]	0.24	6.48[a]	0.25	0.23

[a] w/ bondpads, [b] graphically estimated

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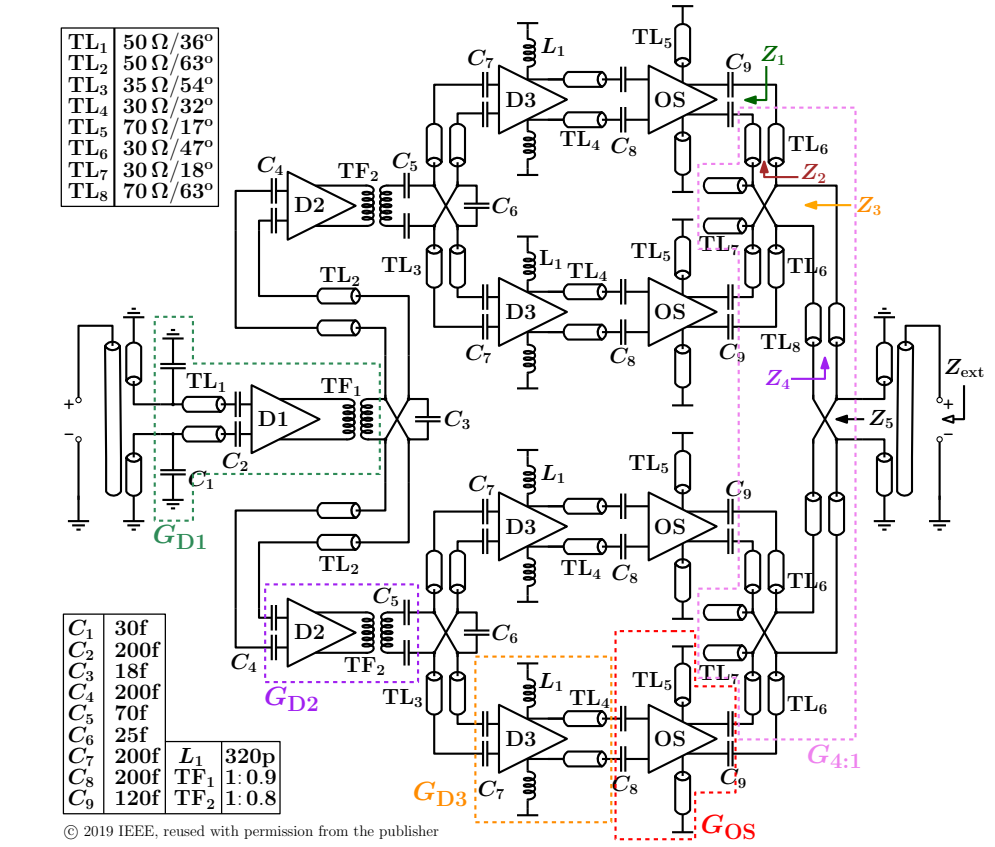
19.3 dBm output power at 5.5 dB gain compression. It achieves PAE_{max}=14% and P_{1dB}=17.3 dBm at 79 GHz. As discussed in Section 3.2.1, a higher voltage can be applied to cascode circuits without great risk of breakdown. As expected, a higher voltage supply results in higher output power and better linearity at slightly decreased power gain (Fig. 3.35c). For V_{CC}=4V, the PA achieves 20.9 dBm output power at P_{in}=0 dBm. The PA performance is summarized in Table 3.3. It achieves more than 25% fractional bandwidth while occupying compact chip area due to optimized matching networks. The maximum output power, gain, efficiency and linearity are comparable with the state-of-the-art despite the largest technology node among other circuits.

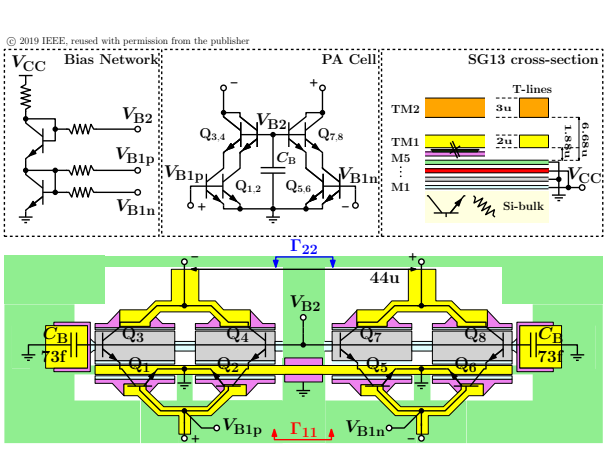
3.2.2 Four-way G-band Power Combiner

As in the previous section, the design of the PA begins with optimizing the OS for maximum output power at reasonable output impedance [15]. Increasing the OS size results in large biasing currents and parasitic capacitance inducing low bandwidth due to high transformation ratio needed for 50 Ω load matching. Once the OS is designed a combining network is synthesized based on an optimum impedance (Z_{opt}) that needs to load the OS for maximum output power. The number of combined elements is subject to available die size, power consumption and efficiency. Large arrays require a complex, area-consuming combining network exhibiting significant loss which directly affects the efficiency.

Here, the size of the OS was dictated by minimum P_{out} requirements and layout implications. Supposing a four-element combining in order to achieve P_{out}=17 dBm, a single OS should deliver P_{max}=13 dBm assuming a 2 dB loss of the combiner. The foundry provides HBT transistors with discretely scalable size up to eight fingers. Larger dimensions can be implemented by connecting multiple devices in parallel implying more losses due to complicated layout. Preliminary simulations showed P_{max}=14.5 dBm for a cascode stage consisting of eight-finger HBTs and P_{max}=17.2 dBm for 16-finger devices (two eight-finger HBTs in parallel). For having safe margins, a 16-finger HBT was chosen for the OS. The schematic of the four-way PA is shown in Fig. 3.36a. It comprises four stages for sufficient power drive and gain. An active power splitter consisting of transformer-loaded stages (D1 and D2) and T-junctions garantees efficient power transfer to the D3 drivers. All driver stages are implemented using an 8-finger HBT cascode topology. Input and output Marchand baluns are realized for measurement purposes. Fig. 3.36b presents the schematic of the OS power cell and the corresponding layout with depicted back end of line (BEOL) cross-section. The lack of "tail" resistor enhances efficiency traded for worse common-mode rejection ratio ($CMRR$). This is compensated by using transformers $\mathrm{TF}_{1,2}$ and differential lines in the matching structures. The bases of $\mathrm{Q}_{3,4,7,8}$ are shorted, thus exploiting the virtual ground for maximum gain. Additional C_{B} ensures low impedance in case of process and mismatch variations. Each device is biased at 2 mA/finger, which corresponds to J_{E}=20 mA/µm^2 providing optimum conditions in terms of maximum output power and $f_{\mathrm{T}}/f_{\mathrm{MAX}}$. Owing to the large OS size, the input and



(a)



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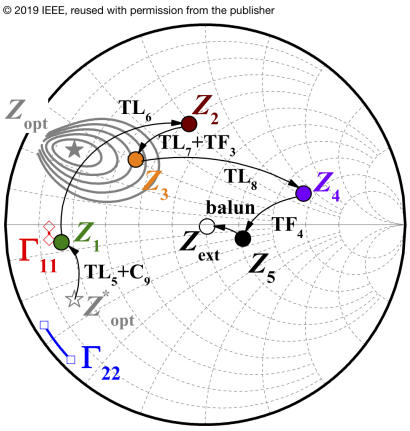
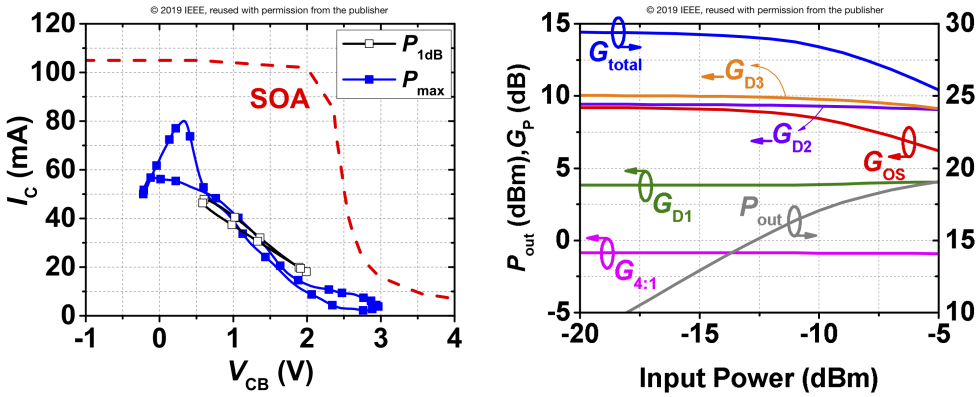


(c)

Figure 3.36: (a) Schematic of the four-way PA. (b) Schematic and layout of the output power cell and BEOL cross-section of SG13 process. (c) Impedance transformation from 50 Ω to Z_{opt} presented to the OS for maximum output power. Constant output power contours are plotted in -0.5 dB to -2.5 dB range with respect to P_{max} with 0.5 dB steps.[15]

output impedances are Z_{in}=12.2-2.5j Ω and Z_{out}=3-35j Ω, respectively. A load pull simulation results in Z_{opt}=15+26j Ω for maximum output power. Input and output reflection coefficients (Γ) in the 140-180 GHz range, load pull power contours and impedance transformation from Z^*_{opt} to Z_{ext}=50 Ω are depicted in Fig. 3.36c. The output matching begins with a shorted stub TL_5 for compensating the imaginary part of Z^*_{opt}. It is also a convenient point for applying voltage bias. Adding a DC-decoupling capacitor C_9 moves the impedance to Z_1. Combination of TL_5 and C_9 including interconnections in the transistor core decreased the maximum achievable OS output power from 17.2 dBm to 15.7 dBm. TL_6 transforms Z_1 to Z_2 from where it is halved and partially compensated by an open stub (TL_7) implemented in TM1. TL_8 moves the impedance from Z_3 to Z_4 where it is again halved to Z_5. At this point the PA is already well matched to differential 100 Ω. Minor influence



(a) (b)

Figure 3.37: (a) Simulated $\mathrm{Q}_{3,4}$ loadline at P_{1dB} and P_{max}. Red dashed line indicates SOA. (b) Simulated total G_{P} breakdown versus input power. The OS starts to saturate first confirming proper power drive.[15]

of the Marchand balun results in almost perfect matching to external the 50 Ω load ($Z_5 \rightarrow Z_{\mathrm{ext}}$). Since the OS output impedance Z_{out} is basically different from Z^*_{opt} the synthesized combining network provides the optimum matching in terms of P_{max} rather than Γ_{ext}. The simulated performance of the four-way PA after careful electromagnetic extraction predicts P_{max}=19.2 dBm and PAE_{max}=6 % at 160 GHz. Since a relatively high output power is generated by a single OS, a dynamic loadline of the CB stage was investigated to prevent hazardous transistor operation. As depicted in Fig. 3.37a the loadline curve at P_{max} is entirely within

SOA. Fig. 3.37b presents the gain distribution of each amplifying stage including losses of matching networks except for T-junction splitters/combiners. The OS starts to saturate first before D3, D2 and D1 drivers indicating proper power drive of each stage for maximum P_{out} and P_{1dB}.

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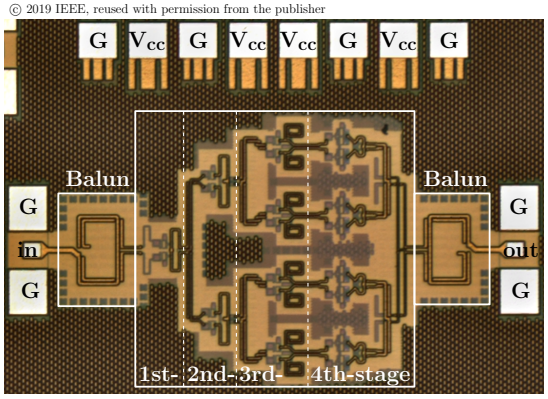


Figure 3.38: Die photograph of the PA[15].

The PA was manufactured using the SG13G2 process from IHP [13]. The die microphotograph is presented in Fig. 3.38. The PA occupies 0.31 mm^2 of silicon area. Inclusion of bondpads and baluns for characterization purposes results in a total die size of 0.85 mm^2. The losses of the bondpad and balun were extracted from a back-to-back structure. Due to the lack of WR5 converters (140-220 GHz), two independent S-parameter setups using R&S ZC170 (WR6) and ZC260 (WR4) extenders in conjunction with an R&S ZVA67 VNA were used to characterize small-signal parameters of the PA. For large-signal measurements, the ZC260 was used to generate the input signal. The power delivered to the PA was first calibrated using a PM5 power detector whereas the loss of the WR4 input probe was extracted from the datasheet. Then, the PM5 was mounted for output power measurement using a WR5 probe from GGB. The loss of the probes and on-chip baluns was de-embedded from the results. Fig. 3.39a presents S-parameters of the PA. The visible discontinuity comes from using two different setups. The PA achieves 30.2 dB peak linear gain and more than 27.2 dB gain in the 155-180 GHz range. Fig. 3.39b presents the large-signal PA parameters over frequency. The PA achieves 18 dBm saturated output power at 22.5 dB power gain and 4.5 % maximum PAE. The PA stability was investigated by calculating μ-factors based on measured S-parameter data (Fig. 3.40). The amplifier is uncon-

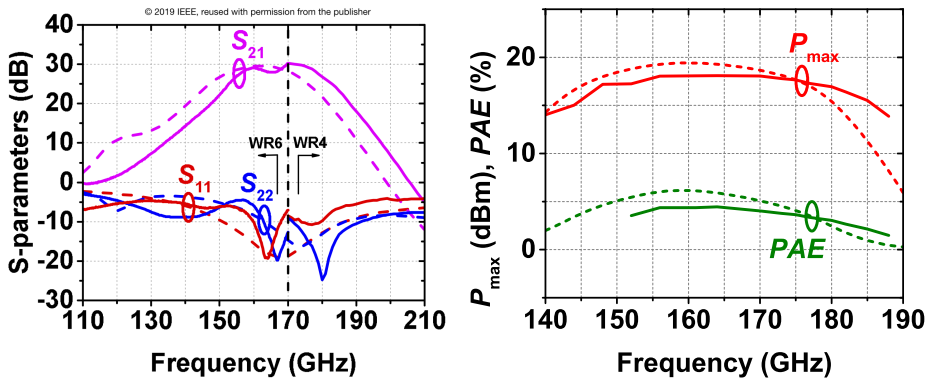


Figure 3.39: (a) Simulated (dashed) and measured (solid) S-parameters of the PA[15]. (b) Simulated (dashed) and measured (solid) large-signal parameters of the PA versus frequency (for constant P_{in}=-4.5 dBm).

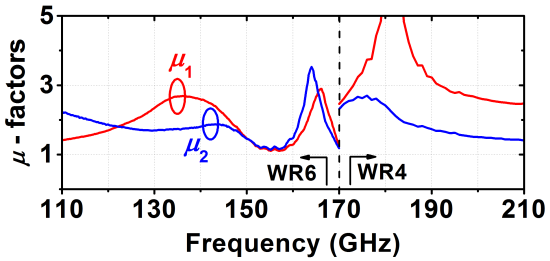
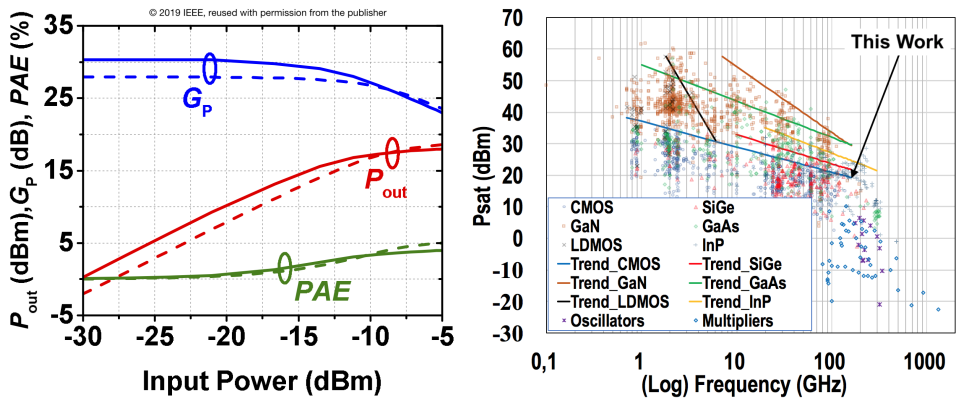


Figure 3.40: Measured stability factors of the PA.

ditionally stable ($\mu_1, \mu_2 > 1$), however, small margin is observed around 160 GHz. Fig. 3.41a shows the PA behaviour with respect to the input power level. The gain compresses by 1 dB at 15.6 dBm output power. Table 3.4 summarizes the PA performance with other prior works. Fig. 3.41b depicts the PA performance in terms of P_{max} with other circuits based on various semiconductor technologies. The PA achieves an outstanding output power reaching the limit of SiGe technology. The PA efficiency and linearity is exceptional compared to other SiGe PAs and approaches the performance of InP circuits benefiting from a higher $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ and supply voltage that can be applied.



(a) (b)

Figure 3.41: (a) Simulated (dashed) and measured (solid) large-signal parameters of the PA at 170 GHz[15]. (b) State-of-the-art power amplifiers based on various semiconductor processes [59].

Table 3.4: Summary of other reported D-band and G-band power amplifiers[15].

Ref.	**This Work**	ISSCC'19 [60]	EuMIC'18 [61]	MWCL'17 [62]	MWCL'17 [63]	EuMIC'16 [64]	BCTM'16 [65]	ESSCIRC'16 [66]
Process	**SiGe 130nm**	SiGe 130nm	InP 130nm	InP 250nm	SiGe 130nm	SiGe 130nm	SiGe 130nm	SiGe 130nm
Supply [V]	**3.3**	3.3	5.9	2.5	4.0	2.7	5.2	-
Freq. [GHz]	**155-180**	200-255	220-245	181-207	131-180	100-180	153-159[b]	200-225
$BW_{\text{-3dB}}$ [GHz]	**25**	55	25	26	49	80	6	25
$P_{\max}$ [dBm]	**18.0**	13.5	18.0	11.0	15.5	11.0	14.0	9.6
$G_{\max}$ [dB]	**30.2**	15.5	22.7	22.4	27.0	24.8	35.4	25
$P_{1\text{dB}}$ [dBm]	**15.6**	10.5	16.0[b]	3.0	13.5[b]	9.5	10.3	4.0
$PAE_{\max}$ [%]	**4.5**	3.0	4.8	9.6	7.2	5.0	4.8	0.5
Power Combining	**4-way Diff.**	4-way Diff.	2-way Single	No Single	No Diff.	No Diff.	No Diff.	4-way Diff.
Area [mm^2]	**0.85**	0.83	0.91	0.45	0.48	0.42	0.06[a]	1.44

[a] w/o bondpads, [b] graphically estimated © 2019 IEEE, reused with permission from the publisher

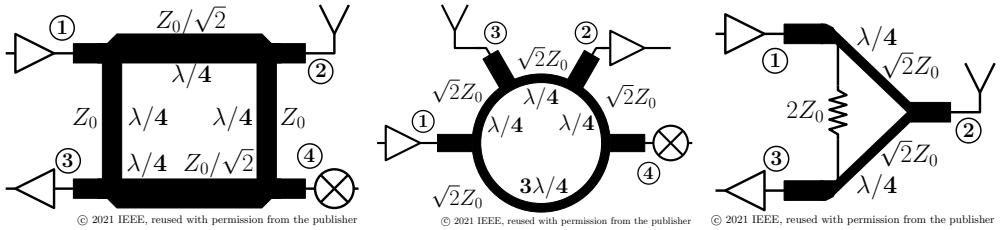
3.3 TX-to-RX Leakage Cancellation in Monostatic Radar Transceivers

Two general radar architectures are commonly used, either employing a single antenna (monostatic) or two separate radiators (bistatic)[16]. For a monostatic radar, a circulator is required to facilitate CW operation. Due to lack of ferrite materials in standard silicon technologies, the circulator is often implemented by

means of passive couplers [67–71]. They usually provide sufficient TX to RX isolation at the cost of additional losses in TX/RX paths resulting in a degraded output power (P_{TX}) and noise figure (NF). A quasi-circulator using active devices was proposed in [72–74] that contributes less losses against a standard coupler at the cost of degraded linearity. An addition of an impedance tuner can further improve the TX-to-RX isolation down to -30 dB [75].

Fundamentally, the problem of TX-to-RX leakage is more emphasized in monostatic radar architectures. Due to the finite isolation between TX output and RX input ports a small portion of the transmitted signal leaks to the RX input and drives a low-noise amplifier (LNA). The higher TX output power (P_{TX}) the higher the required LNA linearity becomes to avoid RX compression. Nonetheless, strong leakage results in a peak in the origin and additional noise since it impacts the optimum LNA bias point. TX to RX coupling also makes TX chain noise an issue since it might increase the noise floor at the LNA input degrading the NF. The elevated noise is broadband and cannot simply be high-pass filtered after down-conversion. Although signal filtering eliminates the DC component resulting from the leakage, it also attenuates responses from close objects and consequently cannot be applied in some cases. This implies the need for a leakage cancellation to be performed in front of the LNA [76, 77].

Typically, in a monostatic TRX, the TX and RX are separated by a circulator that provides possibly low losses in one direction, i.e. TX-to-ANT and ANT-to-RX and high isolation in the reverse direction, e.g. TX-to-RX. Since circulators are non-reciprocal circuits they can be implemented either using ferrites or active devices. The former is typically not available in IC technology whereas the latter raises other issues, e.g. limited linearity or higher noise figure. Recently, a topology based on clocked switched capacitors has been proposed to mimic non-reciprocity of ferrite circulators [78] . Unfortunately, applying this method in the mm-wave range would require a stable high-frequency signal source increasing complexity to a large extent. A convenient way to implement circulator functionality (at least partially) is to use a coupler. It provides high isolation traded for at least 3-dB extra loss in the TX/RX paths resulting in decreased P_{TX} and degraded NF. An interesting approach avoiding this 3-dB loss was presented in [79], where orthogonal signals drive an antenna supporting circular polarization. In this case the TX-to-RX isolation is limited to -22 dB but still could be improved if combined



(a) (b) (c)

Figure 3.42: Possible monostatic TRX configurations using (a) branchline coupler (b) ratrace coupler and (c) Wilkinson combiner. TX and RX are connected to inherently isolated ports 1 and 3. In 4-port networks half of P_{TX} can be reused as a LO drive for the down-conversion mixer.[16]

with leakage cancellation.

Different types of couplers might be used to mimic behaviour of a circulator. Structures relying on EM coupling, such as a directional coupler or Lange coupler provide a broadband isolation but are not easily implementable due to limited minimum spacing between the lines. The coupling might be improved by introducing more coupled sections (tandem coupler) but the structure becomes bulky and not practical in certain cases. For that reason a conventional TL-based coupler was considered, despite narrower bandwidth, that is mostly limited by other active circuits. Fig. 3.42 presents possible configurations based on a rat-race coupler (used in [80]), branchline coupler and Wilkinson combiner. Four-port structures offer an opportunity to drive the down-conversion mixer with halved TX output power (P_{TX}), whereas for a Wilkinson combiner half of the TX signal is dissipated in the resistive load. On the other hand, it only needs two $\lambda/4$ sections making it more compact compared to the other couplers.

A critical parameter from the system point of view is the isolation between TX and RX ports which is infinite provided perfect matching and line dimensions. Even under such conditions the perfect signal cancellation occurs only at the center frequency and worsens when deviating from the carrier since the isolation depends on the wavelength. Fig. 3.43a shows the TX and RX port isolation for branchline, rat-race and Wilkinson couplers over frequency. The Wilkinson coupler clearly has an advantage over the other structures regarding the frequency response as it provides more than 15 dB isolation at 60% fractional bandwidth. Intuitively, us-

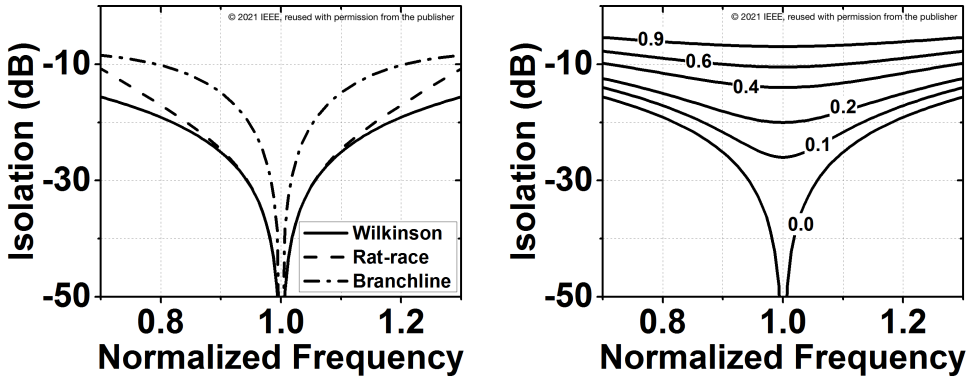


Figure 3.43: (a) Isolation in various coupler structures. (b) Isolation in a Wilkinson coupler for different $|\Gamma_{\mathrm{ANT}}|$ versus frequency.[16]

ing less dispersive transmission lines (TL) should be beneficial in terms of bandwidth. Another critical factor influencing the isolation is the antenna port. Any mismatch at the antenna interface results in signal reflection back to the source but also towards the LNA. Fig. 3.43b presents simulated TX-to-RX isolation using a Wilkinson coupler for different reflection coefficient at the antenna port. In the worst case the isolation degrades down to 6 dB which can be intuitively derived: First, half of the TX signal is terminated in the resistor (-3 dB). Assuming full reflection at the antenna port, the signal is subsequently equally split towards RX and TX (-3 dB).

So far, it was shown that inherent coupler isolation might not be sufficient to provide desired TX-to-RX signal attenuation and extra canceling should be applied to secure low-noise operation and decrease DC offset at the mixer output. Fig. 3.44 depicts the concept of leakage cancellation followed in this section. Assuming a simple FMCW radar front-end the transmitted signal s_{TX} is radiated towards the targets after experiencing losses in the coupler. A portion of s_{TX} is back-scattered from reflecting objects and received by the antenna and directed to the LNA input through the coupler. Depending on the target cross-section and range the strength of s_{RX} is substantially lower than s_{TX}. Due to finite TX-to-RX isolation a part of s_{TX} leaks directly to the RX. Since the leaked signal s_{leak} does not experience off-chip propagation loss it is typically much larger than s_{RX} (Fig. 3.44a). Consequently, performing an FFT on the down-converted signal s_{IF} in a limited

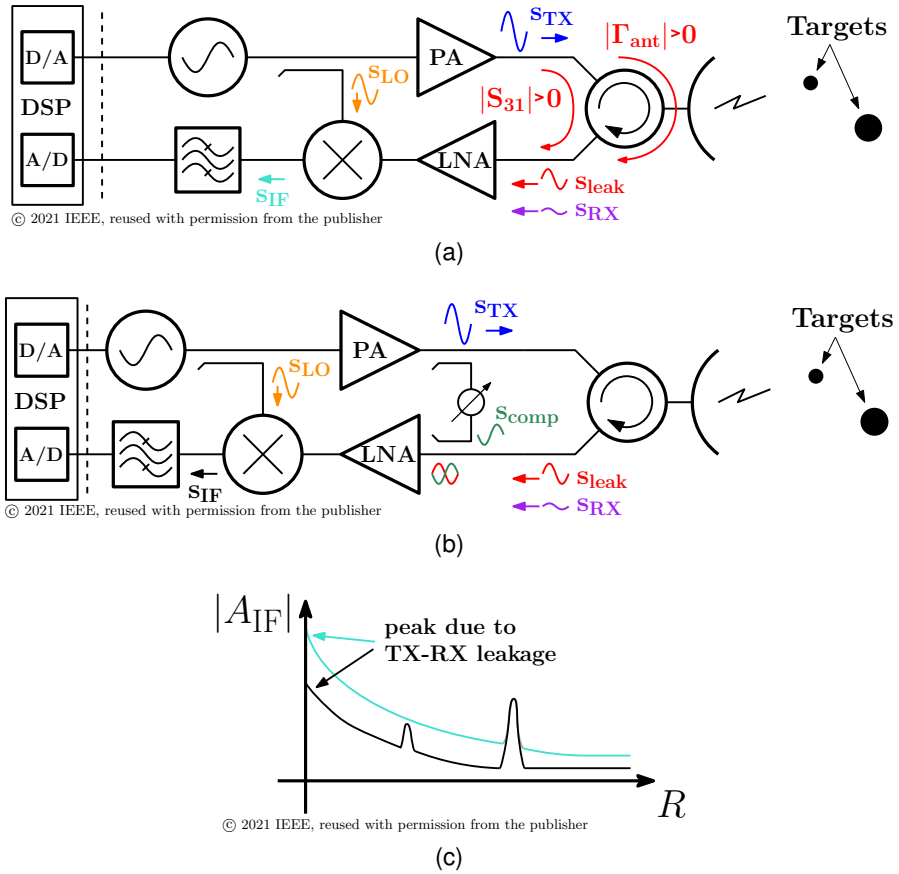


Figure 3.44: (a) Block diagram of a simple FMCW radar system. Finite TX-RX isolation and mismatch at antenna port results in leaking signal s_{leak} (b) FMCW radar with a compensation circuitry for leakage attenuation. (c) Effect of TX-to-RX leakage compensation on FMCW range measurement. Weakly reflecting objects become detectable.[16]

time window results in a strong peak close to zero and weak responses from the targets. In order to attenuate the leakage a compensation network composed of directional couplers and a vector modulator is placed between TX and RX (Fig. 3.44b). A part of s_{TX} is sensed using a low-loss coupler. Its phase and amplitude is tuned in such a way that $s_{\text{comp}} = -s_{\text{leak}}$. Tunability of the compensation network seems indispensable since several factors can affect the real TX-to-RX isolation including antenna matching, characteristic impedance mismatches and isolation resistor precision. Additional leakage suppression effectively reduces DC offset, low-frequency noise and improves detectability of near objects.

This is depicted in Fig. 3.44c where leakage cancellation uncovers weak response from the small target located closer to the sensor. The leakage cancellation is described as follows

$$C_{\mathrm{LC}} = 10\log_{10}(\frac{P_{\Delta}}{P_{\mathrm{leak}}}), \tag{3.28}$$

where P_{leak} is the leaked TX signal power and P_{Δ} denotes power residue due to not perfect leakage compensation and is given by

$$P_{\Delta} = \frac{1}{Z_{\mathrm{L}}}\frac{1}{T}\int_{t_0}^{t_0+T}[s_{\mathrm{leak}}(t) - s_{\mathrm{comp}}(t)]^2\mathrm{d}t, \tag{3.29}$$

where Z_{L} is the load at the LNA input. Having

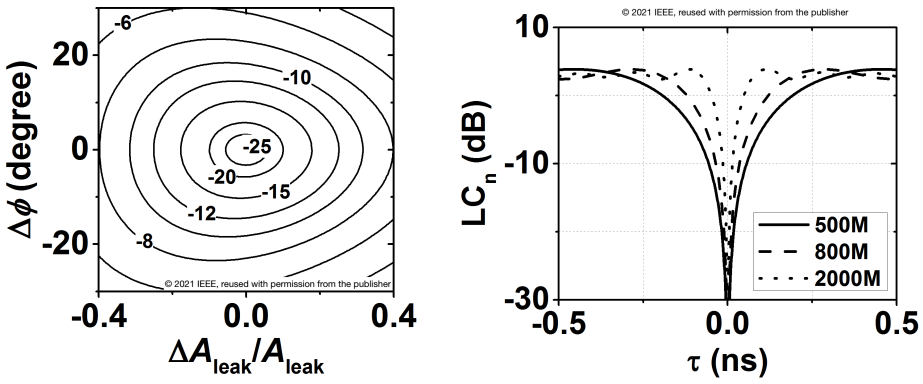
$$\begin{aligned} s_{\mathrm{leak}}(t) &= A_{\mathrm{leak}}\cos(2\pi f_0), \\ s_{\mathrm{comp}}(t) &= (A_{\mathrm{leak}} + \Delta A_{\mathrm{leak}})\cos(2\pi f_0 + \Delta\phi), \end{aligned} \tag{3.30}$$

and using (3.29), the analytic expression for leakage cancellation reads

$$\begin{aligned} C_{\mathrm{LC}} = 10\log_{10}\Big(1 - 2(1 + \frac{\Delta A_{\mathrm{leak}}}{A_{\mathrm{leak}}})\cos(\Delta\phi) \\ + (1 + \frac{\Delta A_{\mathrm{leak}}}{A_{\mathrm{leak}}})^2\Big), \end{aligned} \tag{3.31}$$

where ΔA_{leak} and $\Delta\phi$ is amplitude and phase mismatch of the compensation signal, respectively. Equation (3.31) is consistent with the expression presented in [81]. If (3.30) represents an FMCW signal, then (3.29) cannot be analytically solved since antiderivative of $\int \cos x^2\mathrm{d}x$ does not exist. However, numerical solution of particular integrals yields the same result as given in (3.30). The contours of constant leakage cancellation ratio C_{LC} calculated in (3.31) are plotted in Fig. 3.45a. Small phase and amplitude deviations from the center of the plot result in significantly worse cancellation. For example, C_{LC} better than 20 dB is obtained, if $|\Delta A_{\mathrm{leak}}/A_{\mathrm{leak}}|$<0.1 and $|\Delta\phi|$<5 degrees. Note that it is an excess cancellation which improves the isolation provided by the TX-RX coupler. Assuming the leakage noise is a stationary band-limited process with constant power spectral density, its auto-correlation function reads

$$R_{\mathrm{n}}(\tau) = E[n(t)n(t+\tau)], \tag{3.32}$$



(a) (b)

Figure 3.45: (a) Cancellation ratio in decibels versus amplitude and phase mismatch of the compensation signal. (b) Noise cancellation ratio in decibels versus noise time mismatch (τ).[16]

where τ denotes the time-lag that represents the delay of the compensation noise with respect to the leaked noise. The ratio of the noise residue and leakage noise is given by

$$\begin{aligned} C_{\mathrm{LC_n}}(\tau) &= \frac{VAR[\Delta n(t)]}{VAR[n(t)]} = \frac{VAR[n(t) - n(t+\tau)]}{VAR[n(t)]} \\ &= 2(1 - \frac{R_n(\tau)}{\sigma_n^2}), \end{aligned} \tag{3.33}$$

where σ is the noise standard deviation. Fig. 3.45b presents noise cancellation in decibels for different noise bandwidths plotted versus time-lag. Reasonably, as τ deviates from zero, the correlation weakens and so does the cancellation. Actually, for large time-lags $C_{\mathrm{LC_n}}$ becomes positive converging to 3 dB which means that the noise power at the LNA input doubles. Indeed, adding or subtracting two uncorrelated noise sources would result in increased noise power which is the case for large delays between the compensation and the leakage noise.

4 E-Band Integrated Radar Transceivers

This chapter is dedicated to integrated radar transceivers operating in 76-81 GHz band, which is the basic frequency range for modern automotive mm-wave sensing systems. Two TRX versions (monostatic and bistatic) are presented and evaluated using a customized FMCW radar platforms. Most of the material presented in this chapter has already been published in [70] and [8, 9].

4.1 Monostatic Radar Sensor with TX-RX Leakage Cancellation

In this section, a design of an integrated monostatic E-band radar transceiver is presented that implements a tunable leakage canceller to compensate the TX-to-RX crosstalk[70]. The TRX was used to build a simple FMCW radar demonstrator to show the influence of leakage cancellation on the range measurements.

4.1.1 TRX Architecture

To remedy the issues mentioned in Section 3.3, a TRX architecture including a leakage cancellation is proposed (Fig. 4.1). The radar front-end requires a 39.5 GHz LO signal, which is amplified and up-converted to E-band by a Gilbert-cell based frequency multiplier. The LO signal can also be fed to the other transceivers in multi-TRX scenarios supporting e.g. MIMO applications. After frequency doubling the signal goes to the Gilbert-cell based BPSK modulator

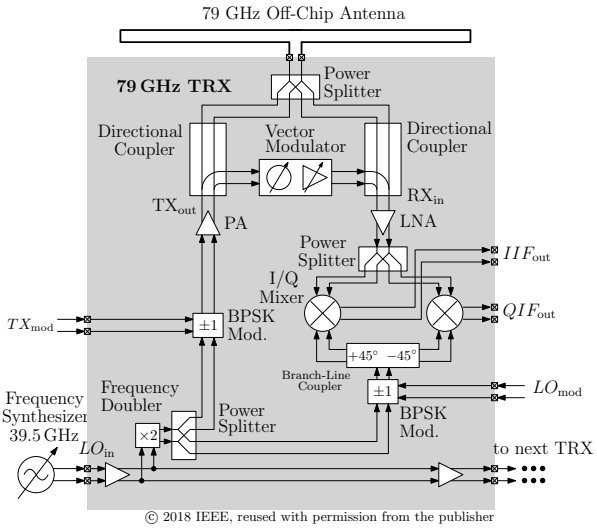


Figure 4.1: Schematic of the scalable 79 GHz monostatic radar transceiver. Several TRXs can be cascaded to form a daisy chain [82][70].

where it is amplified and fed to the power amplifier. The BPSK modulators in the TX and RX path can also support other radar types where the carrier is modulated by pseudo-random noise sequences [83]. The PA output signal goes to the antenna port via a coupler, which in this case is implemented as a Wilkinson power divider. It provides a wide-band isolation between the TX and RX paths with respect to other types of couplers, e.g. branchline or rat-race. However, as for the other reciprocal circuits, it introduces losses in the TX and RX leading to less TX output power and higher RX noise figure. The received signal is amplified by an LNA and fed to an I/Q mixer, which is realized by means of a 90°-branchline coupler and Gilbert-cell based converters. All blocks are differential circuits for their superior immunity to common-mode noise originating from the supply and the ground network.

4.1.2 Tunable Leakage Canceller

The inherent TX-RX isolation provided by a Wilkinson power divider depends significantly on the antenna port termination. Since a typical E-band antenna is relatively large with respect to the chip size, it is most often implemented as an off-chip component. The bondwire transitions and other compensation networks, if

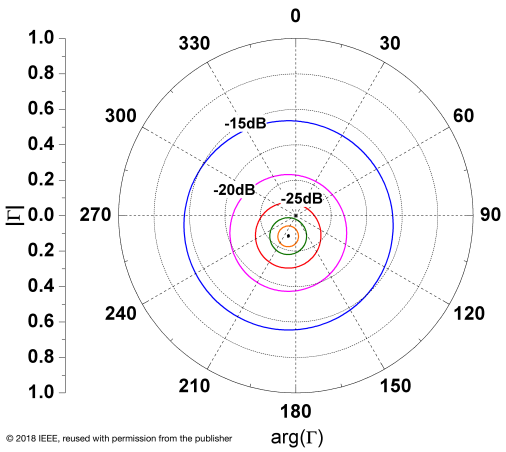


Figure 4.2: TX-RX isolation contours depending on antenna reflection coefficient[70].

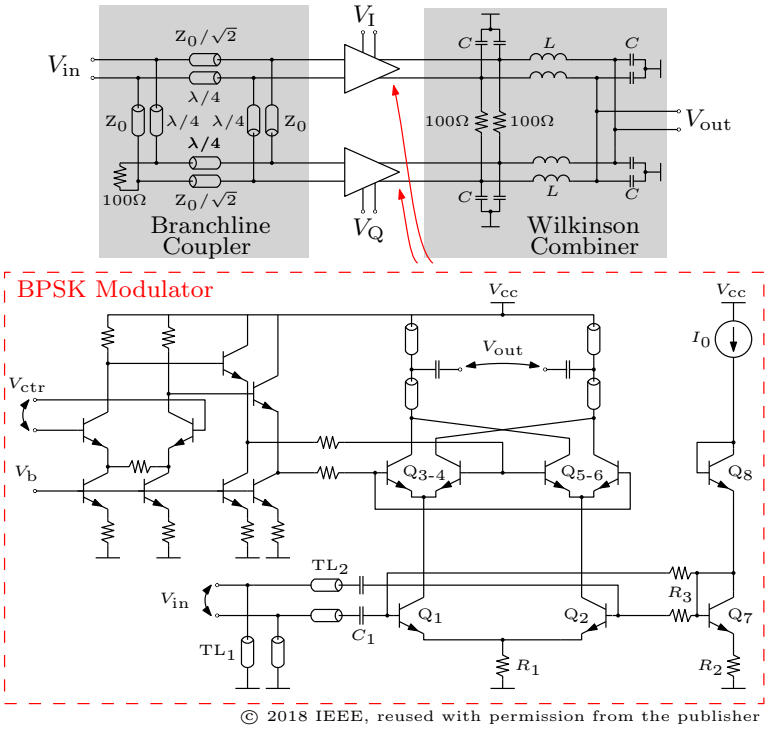


Figure 4.3: Schematic of the vector modulator[70].

not precisely defined, can introduce impedance mismatches resulting in a higher return loss at the antenna port. This leads to a poorer TX-RX isolation, since a part of the signal after being reflected from the antenna port goes directly to

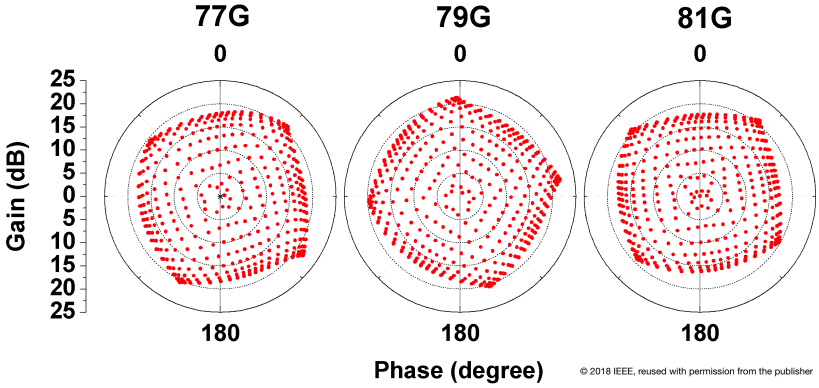


Figure 4.4: Simulated gain and phase of the vector modulator [70].

the RX. Fig. 4.2 presents simulated TX-RX contours on the antenna reflection coefficient plane. It is obvious, that the highest isolation is obtained only for one antenna impedance and it drops as we move away from this optimum point. It appears, that for -6 dB antenna matching, presenting a real scenario, the TX-RX isolation can be only around -15 dB. Thus, an additional leakage cancellation might be required to suppress the unwanted signal going to the RX.

Here, a vector modulator based solution is proposed, known from full-duplex communication systems, where almost 100 dB of overall TX signal suppression is required to obtain the desired dynamic range. The leakage canceler consists of two -10 dB directional couplers placed after the PA and before the LNA. A part of the TX output signal is coupled to the vector modulator, which tunes the amplitude and the phase in such a way that the signal coupled back to the input of the LNA is the inverted replica of the leaked TX signal. Both signals, the leaked and the coupled, cancel each other before driving the LNA. Fig. 4.3 and Fig.4.4 show the schematic of the proposed vector modulator and its simulated tunability for three different frequencies. The circuit comprises two BPSK modulators, a branchline coupler and a reduced-size Wilkinson power combiner. It is capable of tuning the gain up to 15 dB and the phase to any arbitrary value in a 0°- 360° range.

Fig. 4.5 presents the operation of the proposed leakage canceler for two scenarios. In the first case, there is no reflection from the antenna port resulting in a good inherent TX-RX isolation reaching -30 dB at 81 GHz. Activation of the leakage canceler significantly improves the isolation to -40 dB in 78-83 GHz range.

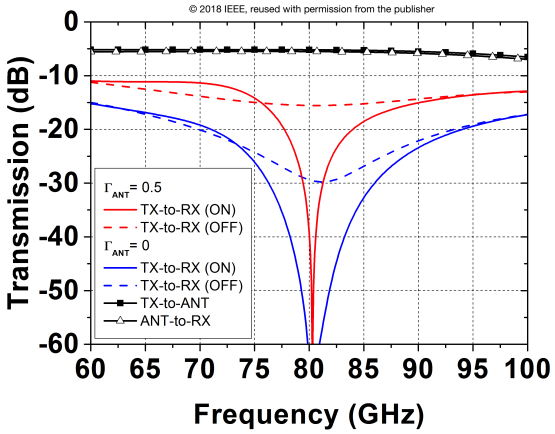


Figure 4.5: Simulated S-parameters of the coupler including enabled (ON) and disabled (OFF) leakage cancellation [70].

In the case of a poorly matched antenna (around -6 dB return loss) the TX-RX isolation can still be improved, but within a rather limited bandwidth. Also, due to losses of the Wilkinson coupler and the losses of the directional couplers, the degradation of the TX output power and RX noise figure is around 5 dB.

4.1.3 Experimental Results

The E-band monostatic radar transceiver featuring a leakage canceler was fabricated using the SG13G2 process from IHP [13]. The chip photograph with marked components is presented in Fig. 4.6. The TRX was measured on wafer using a single-ended waveguide E-band probe from GGB Industries. Since the TRX antenna port is differential, one pad was left open while the other one was used for measurements. The calibrated TX output power and RX gain over the frequency is shown in Fig. 4.7a. The TRX achieves 4 dBm output power with a 1-dB bandwidth of 70-87 GHz. The RX reaches 18 dB voltage gain and is larger than 15 dB in the 75-89 GHz range. The RX gain versus RF input power at 79 GHz is presented in Fig. 4.7b. The gain compresses by 1 dB at -5 dBm RF input power. The RX gain difference between the I/Q IF outputs does not exceed 0.3 dB.

Since the TRX works in full-duplex, the leaked TX and the LO signals have the same angular frequency ω_{L}. Due to the mixing process, the IF signals can be

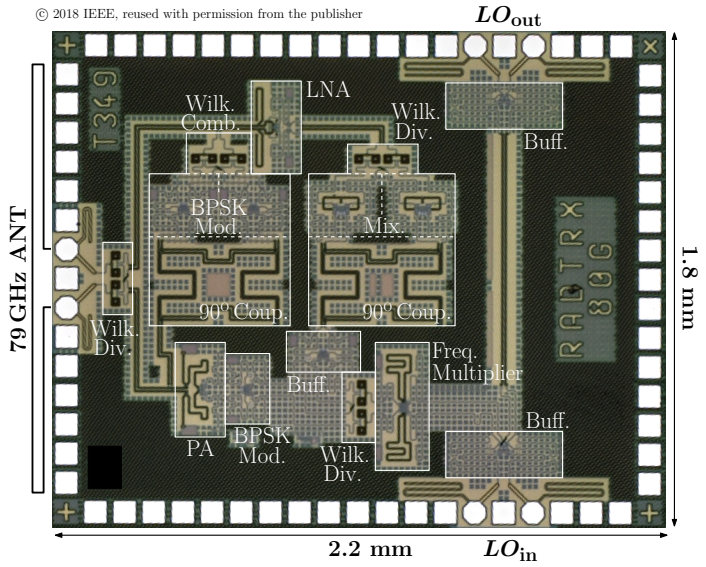


Figure 4.6: Micrograph of the 130 nm BiCMOS chip [70].

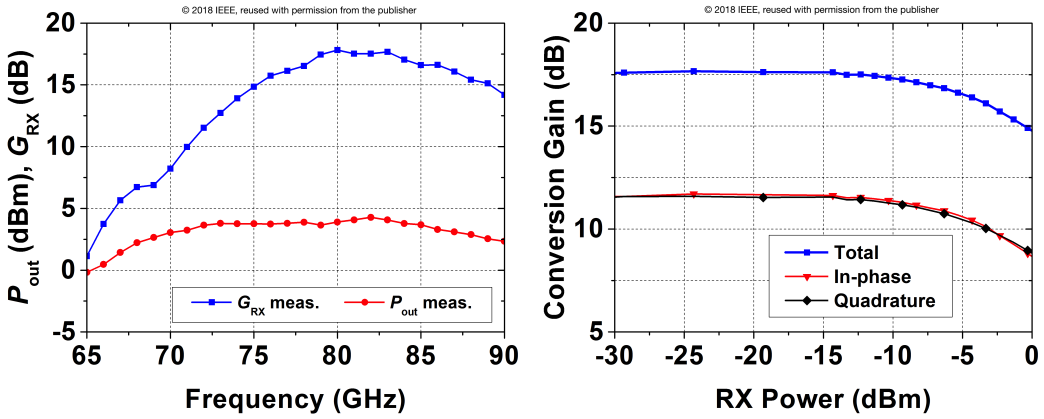


Figure 4.7: (a) Measured TX output power and RX gain over the frequency. (b) Measured RX gain versus RF input power at 79 GHz.[70]

obtained as follows

$$s_{\mathrm{IF}} = A_{\mathrm{TX_l}} \sin(\omega_{\mathrm{L}} t + \varphi_{\mathrm{A}}) * A_{\mathrm{LO}} \sin(\omega_{\mathrm{L}} t + \varphi_{\mathrm{B}}) \tag{4.1}$$

where $A_{\mathrm{TX_l}}$,A_{LO} are the amplitudes and φ_{A},φ_{B} are the phases of the TX leaked

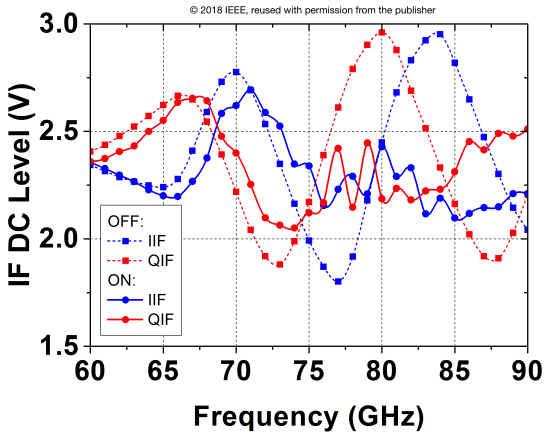


Figure 4.8: Measured I/Q IF output DC levels in ON and OFF states of the LC [70].

Table 4.1: Summary of the state-of-the-art monostatic radar transceivers [70].

Ref.	**This Work**	[84]	[75]	[85]	[86]	[80]
Process	**SiGe 130nm**	SiGe 130nm	SiGe 130nm	SiGe 350nm	SiGe 130nm	SiGe 180nm
Freq. [GHz]	**75-89**	58.3-63.9	75-80	55-70	91-97	74.1-81.1
BW [GHz]	**14**	5.6	5	15	6	7
P_{out} [dBm]	**4**	6.4	NR[b]	6.3	6.5	7
G_{RX} [dB]	**18**	20.6	22	28	7	14
IP_{1dB} [dBm]	**-5**	-24	-12	-24	2.5	0
P_{DC} [mW]	**396**	520[a]	223	924[a]	248	3300[c]
Area [mm^2]	**3.96**	1.03[a]	1.56	6.72[a]	1.1	6.82[c]

[a] w/ VCO, [b] ext. LO fed to passive TX, [c] 2TX+4RX+VCO

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and LO signals, respectively. The resulting s_{IF} reads

$$0.5A_{\mathrm{TX_1}}A_{\mathrm{LO}}[\cos(\varphi_{\mathrm{A}}-\varphi_{\mathrm{B}})-\cos(2\omega_{\mathrm{L}}t+\varphi_{\mathrm{A}}+\varphi_{\mathrm{B}})] \tag{4.2}$$

revealing a DC and $2\omega_{\mathrm{L}}$ components. The latter is filtered out while the DC part causes the problems described in Section 4.1.1. As indicated in 4.2, the DC level of the IF output depends on the phases φ_{A} and φ_{B} and therefore it varies over the frequency. This is depicted in Fig. 4.8, where the IF outputs were measured in order to investigate the leakage cancellation feature. Two measurements were performed with enabled and disabled vector modulator, indicating ON and OFF

state, respectively. In OFF state, a large DC level variation at the mixer output is observed due to TX-to-RX leakage. Perfect TX-RX isolation would result in a flat DC characteristic over the frequency at around 2.3 V. A large DC level variation and thus poor TX-RX isolation is due to an unbalanced antenna port termination resulting in around -15 dB TX-to-RX leakage (see Fig. 4.5). This can still be compensated, as shown in Fig. 4.8, where the DC level variation is significantly smaller in the 76-85 GHz range with activated leakage cancellation. The results of the presented monostatic TRX are summarized in Table 4.1.

4.1.4 Single-Channel Monostatic E-Band Radar Demonstrator

The TRX was used to demonstrate its functionality in a radar. A bare die was mounted on a dedicated PCB, fabricated using Rogers RO3003 microwave laminate (see Fig. 5.1). A four-element series-fed patch antenna was used for its simple implementation and assembly with the silicon die through bondwires. An external LO signal is fed to the TRX via a V-band connector and planar wideband balun.

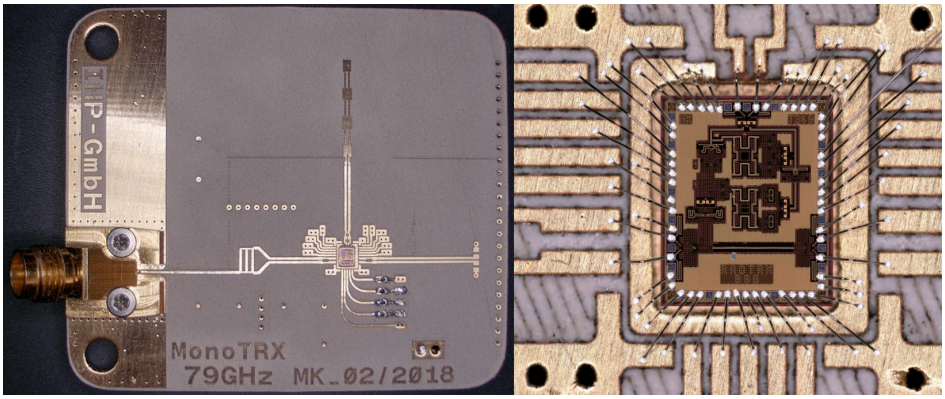


Figure 4.9: Photo of the PCB containing the TRX and the 79 GHz patch antenna.

The antenna was designed based on a structure proposed in [87]. In such an array the signal is easily distributed between the elements separated by $\lambda/2$. However, each consecutive patch is driven with a signal slightly delayed in phase, which results in a frequency-dependent antenna radiation pattern, known as ”beam squinting”. Fig. 4.10 presents simulated radiation patterns in elevation and

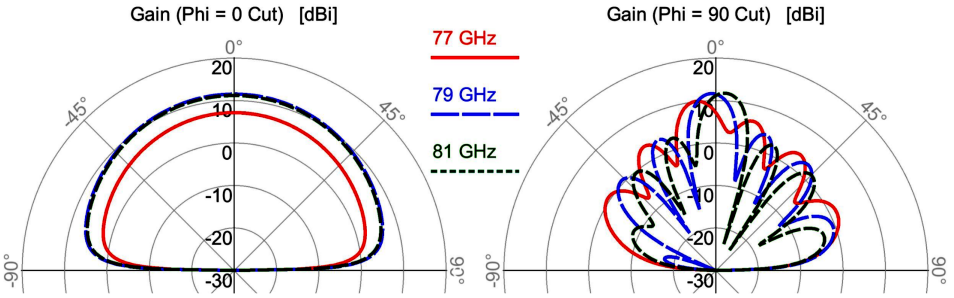
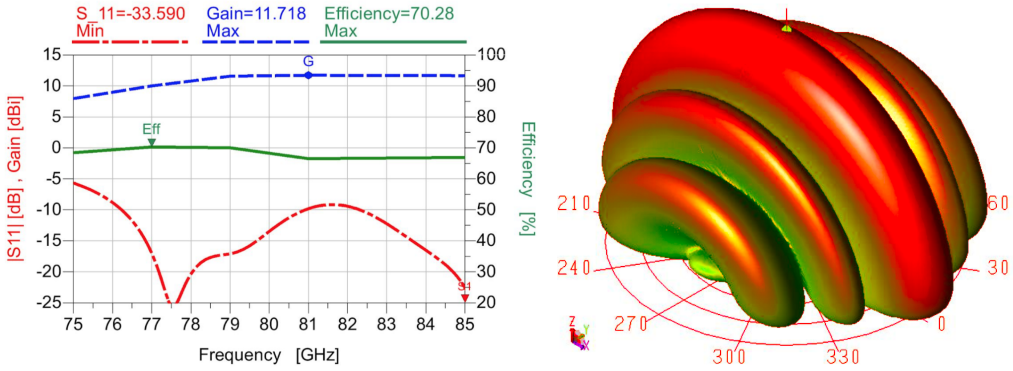


Figure 4.10: Antenna radiation pattern in azimuth and elevation.



(a) (b)

Figure 4.11: (a) Simulated S_{11}, G_{ant} and η_{ant} of the antenna. (b) 3-D radiation pattern.

azimuth. Notably, antenna gain in elevation is flat whereas in azimuth one could distinguish a main lobe having the maximum at slightly different angle due to beam squinting. The gain reaches 11 dB at 79 and 81 GHz. Visible sidelobes are around 10 dB lower than the peak of the mainlobe. At 77 GHz the maximum gain slightly decreases and the sidelobe level increases. The input return loss, gain and efficiency of the antenna is presented in Fig 4.11a. 3-D visualization of the antenna radiation pattern is shown in Fig. 4.11b. The TX-to-RX leakage cancellation implemented in the monostatic TRX was evaluated using an FMCW radar demonstrator. A range measurement setup was arranged in an anechoic chamber to bring environmental influence to a minimum level (Fig. 4.12). A separate LO board containing a 39.5 GHz PLL (described in more detail in Sec. 4.2.2) was used to provide an FMCW signal to drive the TRX. The IF output signal was

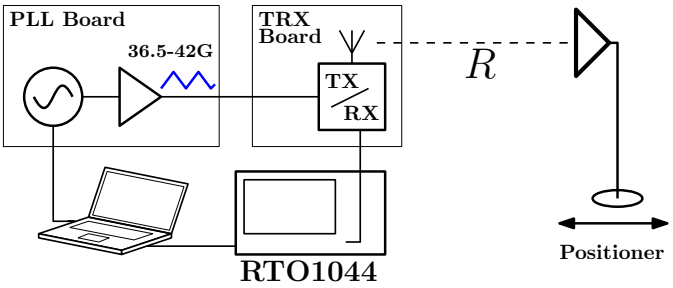


Figure 4.12: Range measurement setup in anechoic chamber. A separate PLL board is used to generate FMCW signal driving the TRX.

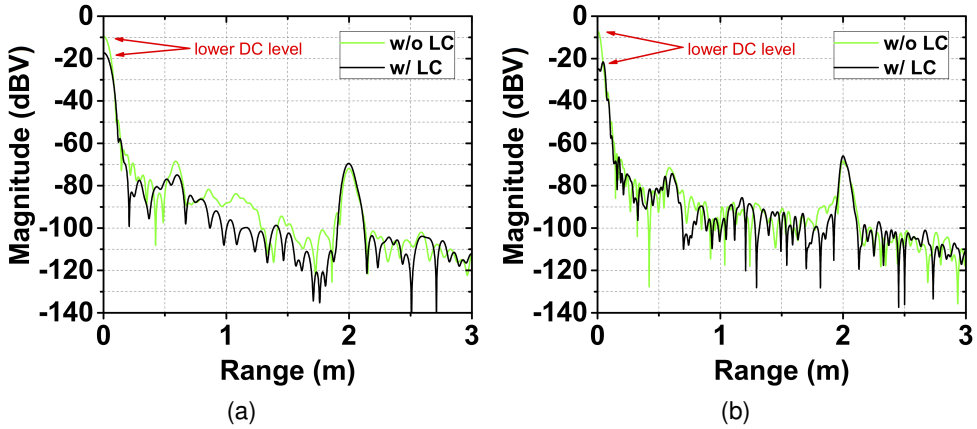


Figure 4.13: Range measurement with the LC in OFF (green) and ON (black) state with T_{SW}=1 ms and (a) B_{SW}=4 GHz and (b) B_{SW}=8 GHz.

recorded using a RTO1044 digital oscilloscope and processed by a simple MATLAB script. A corner cube (CC) with RCS of around 150 m^2 was placed on a positioner to serve as a target. Fig. 4.13 presents two range measurements. The ramp duration (T_{SW}) was set to 1 ms. The sweep bandwidth (B_{SW}) varied from 4 GHz to 8 GHz. A low-pass filter at the input of the oscilloscope with 5 MHz cut-off frequency was enabled. Each measurement was performed with the leakage canceller in both states. LC activation resulted in a lower DC level in the IF output and also slightly lower noise level. A set of 1000 measurements was recorded in the 1 m to 5 m range for both LC modes. Fig. 4.14 shows ranging precision (σ_{R}) calculated as standard deviation from the mean value of each measurement set. LC activation results in 50% improvement in ranging precision. Notably, σ_{R} degrades with distance due to lower SNR ratio.

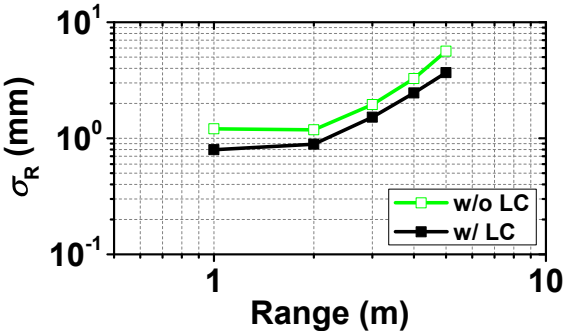


Figure 4.14: Ranging precision of the monostatic TRX in both LC modes.

4.2 Radar Platform Based on Bistatic Single-Channel TRXs

In the following, a scalable-system concept is shown based on a single-channel cascadable radar TRXs and single LO enabling an arbitrary number of channels to be realized depending on the target application [8, 9, 82, 88, 89]. The architecture supports FMCW signals as well as phase modulation of the transmitted signal that can potentially be used, e.g., in beamforming applications or communication.

The block diagram of the proposed radar transceiver is presented in Fig. 4.15. The architecture supports a scalable system concept based on single-channel transceiver chips [82, 89–91]. A multi-channel platform can be realized using either parallel- or series-fed TRXs providing a certain degree of flexibility depending on the target application. All the building blocks are realized as differential circuits for their superior immunity to common-mode noise, which can heavily affect single-ended structures. The input and output impedance of each block is 100 Ω differentially in order to be conveniently reused in other systems. The matching is realized using transmission lines (TL) and capacitors. An external 39.5 GHz signal is fed to the LO input (LO_{in}). It is then amplified and distributed to the frequency multiplier and to the output (LO_{out}). After frequency multiplication the signal is split between the transmitter and receiver. In the TX the signal is amplified in the PA and terminated by an off-chip antenna. A vector modulator (VM) can be used to modulate the carrier for communication or beam-forming

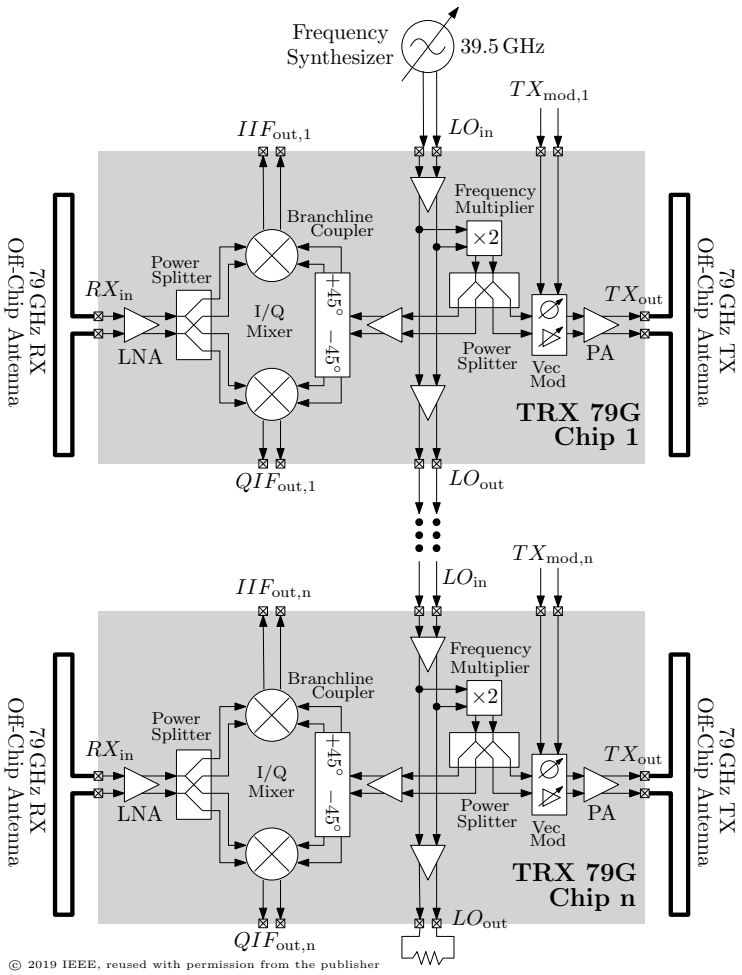


Figure 4.15: Block diagram of a scalable 79 GHz radar platform based on single-channel transceivers. An external 39.5 GHz LO signal is regenerated on-chip before feeding the subsequent TRX [8].

purposes. The received signal is amplified by means of an LNA and fed to the down-converters. An I/Q mixer is implemented for higher signal-to-noise (SNR) ratio at the receiver and complex signal demodulation, since the TRX can also be applicable for simple communication between the vehicles as described in [9].

4.2.1 TRX Architecture

All buffers and the LNA are realized as single-stage cascode circuits [82]. Each buffer consumes 11 mA including biasing network and comprises a tail resistor, which increases $CMRR$ and stabilizes the quiescent current with respect to process, voltage and temperature (PVT) variations. Degeneration TLs at the emitters of the input stage are introduced for simultaneous gain and noise matching in case of the LNA. Each transistor is a 5-finger HBT device biased at optimum current density for the highest $f_{\mathrm{T}}/f_{\mathrm{MAX}}$.

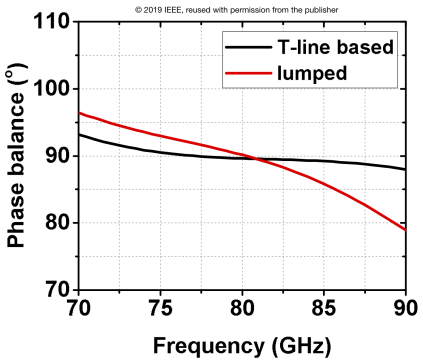


Figure 4.16: Phase balance at quadrature outputs after electromagnetic simulation using ADS Momentum Microwave [8].

An I/Q mixer requires quadrature LO signal generation, which typically is realized using a branchline coupler. It consists of four quarter-wave sections with characteristic impedance of Z_0 and $Z_0/\sqrt{2}$. The phase difference between the output ports is 90° at the center frequency. Despite the simplicity and relatively broadband behavior a TL-based branchline coupler is a relatively large structure owing to long transmission lines in E-band ($\lambda \approx$1.9 mm). Instead, a lumped version using series inductors and shunt capacitors is implemented for size reduction. However, this comes at the cost of narrower bandwidth and ultimately worse phase balance characteristic (see Fig. 4.16), but which is still satisfactory in the targeted 77-81 GHz range ($90^{\mathrm{o}} \pm 2^{\mathrm{o}}$). The inductors are realized as spiral structures, where the inductance is extracted after careful electromagnetic (EM) simulations using ADS 2.5D Momentum solver. The capacitors are metal-insulator-metal (MIM) components placed between second top metal layer (TM1) and top most thin layer (M5) with tolerance of $\pm 10\%$. Among three different types

available in the process, unsalicided p-doped gate polysilicon (RPPD) resistors are chosen for their superior tolerance ($\pm 10\%$) and low temperature coefficient (170 ppm/K). The down-conversion mixer is based on a Gilbert-cell topology with inductive degeneration at the emitters of the input stage for linearization [9]. Frequency doubling is conveniently achieved by applying a slight modification of a Gilbert-cell [23].

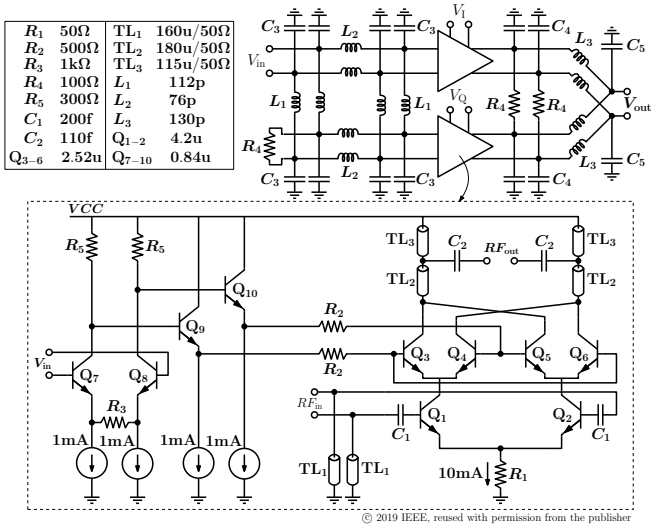


Figure 4.17: Schematic of the vector modulator [8].

Implementation of the VM is based on two BPSK modulators driven with quadrature signals. The schematic of the VM is presented in Fig. 4.17. A lumped branch-line coupler is used to generate I/Q signals. Each BPSK modulator provides $0^o/180^o$ phase shift and variable gain depending on the differential control voltage inputs V_{I} and V_{Q}. Summation of these I/Q components is realized by a lumped Wilkinson power combiner for size reduction. Such structure provides isolation between the combined ports and low insertion loss of 4 dB. It is also used for LO signal splitting between the TX and RX sections. The presented VM can provide a continuous phase shift in the 0° - 360° range and variable gain up to 2 dB.

The minimum required output power of a radar sensor depends on the maximum detectable range. Assuming an implementation for SRR, R_{MAX} is 30 m. Rewriting (2.12), it follows

$$P_{\mathrm{TX_{MIN}}} = \frac{(4\pi)^3 R_{\mathrm{MAX}}^4 P_{\mathrm{RX_{MIN}}}}{G_{\mathrm{ant}}^2 \lambda^2 \sigma}. \tag{4.3}$$

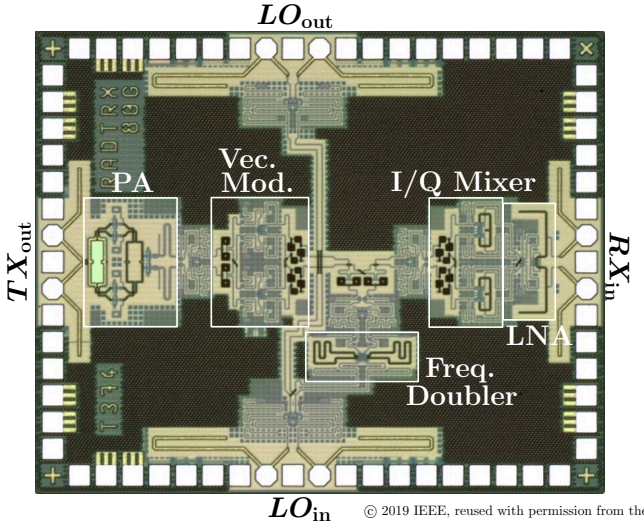


Figure 4.18: Photograph of the E-band TRX (1.74mm×2.14mm) [8].

Assuming that the bandwidth of the receiver is 1 MHz, the equivalent noise power at the receiver input is

$$P_{\mathrm{N}} = k_{\mathrm{B}}TB = -114\,\mathrm{dBm}. \tag{4.4}$$

Further assuming a noise figure (NF) and minimum SNR of 10 dB, respectively, the minimum power of the reflected signal needs to be -94 dBm. Using (4.3), P_{TX}=16.6 dBm in order to detect a target with RCS=10 m^2 at 30 m from the sensor. Here, G=10 dBi is considered which is easily achieved using low-cost planar antennas. The calculated P_{TX} is a rather challenging value for silicon technologies that often imposes using power combining techniques. The PA described in Section 3.2.1 fulfills the above requirements; therefore, it is used for the output stage in the TRX.

Radar TRX as well as standalone vector modulator were fabricated using the SG13G2 process from IHP [13]. A chip micrograph with marked main blocks is depicted in Fig. 4.18. Fig. 4.19 shows measured gain and phase of the vector modulator for multiple V_{I} and V_{Q} combinations at 77, 79 and 81 GHz. The VM achieves a maximum gain of 2 dB for full 360° phase shift at each frequency.

An SMR60 signal source from R&S was used to generate the LO_{IN} signal for the TRX. The TX output power is presented and compared with the earlier generation in Fig. 4.20a. The first version is able to deliver around 10 dBm in wide frequency

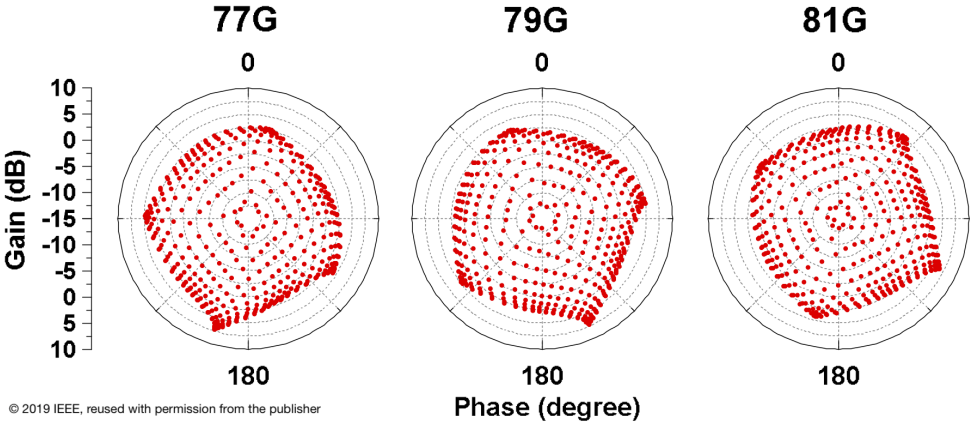
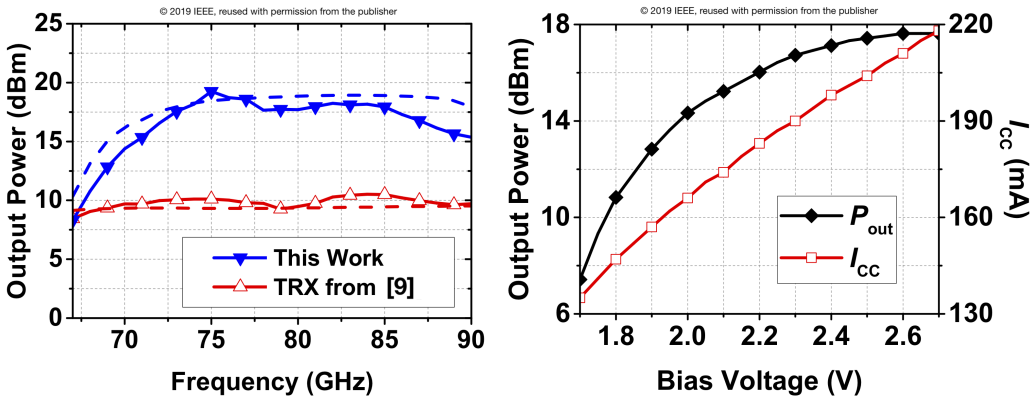


Figure 4.19: Measured gain and phase of the VM at different frequencies[8].



(a) (b)

Figure 4.20: (a) Simulated (dashed) and measured (solid) output power of the TRX. (b) Measured TX output power and TRX current consumption versus PA control voltage at 79 GHz. [8]

range, whereas the next generation TRX achieves 19.2 dBm at 75 GHz and more than 16.2 dBm in the 72-88 GHz range. Fig. 4.20b shows the TRX output power and DC current consumption against PA control voltage. The RX was measured using a similar setup as presented in Fig. 3.33. The E-band RF input signal is generated using an OML S12MS source, tunable attenuator, directional coupler, harmonic mixer, and spectrum analyzer from R&S. A 30-45 GHz LO_{IN} signal is fed from an R&S SMR60 generator and IF outputs are measured with a Teledyne Lecroy oscilloscope. Each of the I/Q channels provides 21.5 dB peak voltage con-

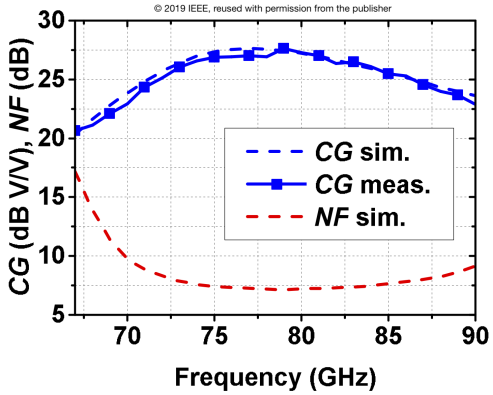


Figure 4.21: Simulated (dashed) NF, CG and measured (solid) CG of the RX [8].

version gain. The total I/Q voltage conversion gain against frequency is presented in Fig. 4.21. The RX achieves 27.5 dB gain at 79 GHz and more than 24.5 dB in 71-88 GHz range. Due to the lack of an E-band noise source, only simulated NF is shown which is 7.2 dB at 79 GHz. The total RX gain compresses by 1 dB at -10 dBm input power which is highly advantageous in the presence of strong TX-to-RX leaking signals. Table 4.2 summarizes the TRX current consumption break-down.

Table 4.2: TRX current consumption breakdown [8].

Buff.	Freq. Doub.	Mix.	LNA	PA	Vec. Mod.	$\mathbf{Total}^*$
41	11	21	10	96	42	**200(220) mA**

* meas. value in brackets

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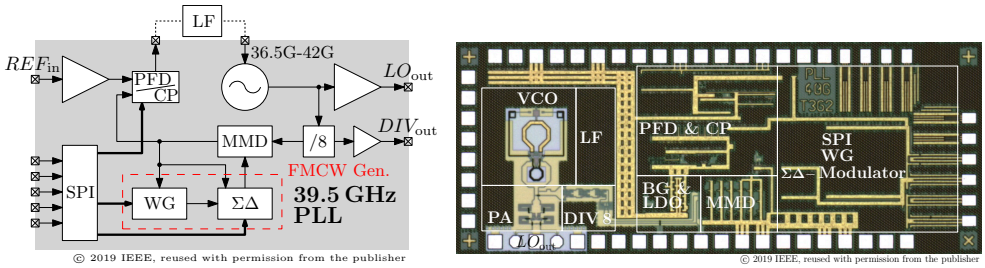
4.2.2 Fully-Integrated 39.5 GHz Fractional-N PLL

Accounting for frequency deviation due to PVT variations, the signal source should be controlled in the 37-41.5 GHz range which corresponds to an 11.5% tuning range. Addition of small margin requires the VCO to achieve 5 GHz TR around 39.5 GHz. Owing to the system architecture based on a separate signal source and TRX chips the generator must deliver a certain level of output power in order to overcome possible losses due to bondwire transitions, mismatches



(a) (b)

Figure 4.22: (a) 39.5 GHz PLL block diagram. (b) Die photograph.[8]

and long PCB traces. The minimum VCO output power is set to be above -3 dBm differentially in order to drive the divider chain and the output stage. The last design goal is to provide isolation of the VCO core with respect to the load. Poor isolation may lead to a heavily disrupted tuning characteristic or even oscillation failure. Based on the above considerations, VCO phase noise optimization is performed. Unlike in communication standards, there are no strict rules regarding the minimum phase noise level in the radar system. Interestingly, the influence of VCO/PLL phase noise on the ranging precision seems to be of less importance comparing to the RX noise provided that PLL noise level is within state-of-the-art values [92]. Due to PLL noise correlation the ranging precision is less sensitive to the TX noise, in particular for distant targets. As the round trip delay time decreases, the SNR improves and the influence of the PLL noise becomes more significant. The PLL phase noise was optimized for minimum jitter using a MATLAB script based on the PLL model presented in [93]. The charge pump (CP) current required for sufficient CP noise attenuation is 2 mA and the optimum PLL bandwidth is around 1 MHz.

A fractional-N PLL architecture was chosen to realize a signal source intended for frequency ramp generation. The block diagram of the synthesizer, as well as die photograph are depicted in Fig. 4.22a and Fig. 4.22b, respectively. The chip was fabricated using the IHP SiGe BiCMOS technology SG13S process with $f_{\mathrm{T}}/f_{\mathrm{MAX}}$=250/300 GHz. The PLL is composed of a phase and frequency detector (PFD), charge pump (CP), loop filter (LF), VCO, divide-by-8 prescaler, multi-modulus divider (MMD), $\Sigma\Delta$-modulator (SDM) with 27 bit fractional resolution, waveform generator (WG) and serial peripheral interface (SPI). RF and divider (DIV) buffers are included for driving external loads.

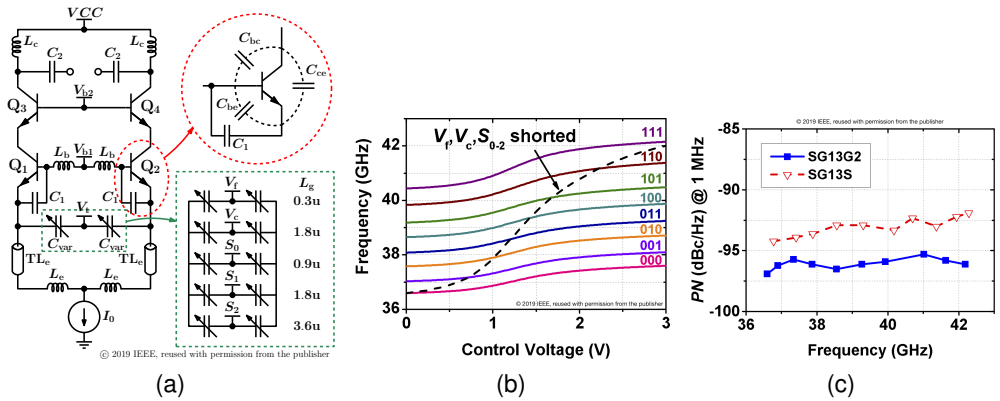


Figure 4.23: (a) Schematic of the Colpitts VCO. (b) Measured tuning curves of the VCO. (c) Measured phase noise at 1 MHz offset from the carrier.[8]

A limiting reference buffer (REF) amplifies the signal coming from the external crystal oscillator, so that its jitter is reduced due to decreased rise/fall times of the signal. The WG modulates the VCO frequency by re-programming the SDM division ratio at every reference clock cycle. The chirp bandwidth and duration are not pre-defined and hardwired. The WG also offers full flexibility in defining the chirp characteristics. The SPI is necessary for setting the control inputs with minimum number of I/O pads. The CP current is also programmable via SPI between 160 µA and 2.4 mA. This helps to compensate for VCO gain variations in single-carrier generation mode. Also, with programmable CP currents, the loop bandwidth can be adjusted according to the desired chirp slope [94]. The synthesizer includes two CP blocks for two different PLL configurations; dual- and single-loop. The dual-loop configuration can be preferred over single-loop for the case that the PLL synthesizes a single target frequency in fractional-N operation [95, 96]. All components, except for the major part of the LF, are integrated on-chip. The synthesizer occupies 2.75 mm^2 silicon area. An off-chip LF eases the loop bandwidth and phase noise optimization.

The VCO is a differential common-collector Colpitts oscillator with a capacitive voltage divider created by C_1 and C_{var} (Fig.4.23a). This configuration provides immunity to the nonlinear base-emitter parasitic capacitance, which is bypassed by a large capacitor C_1. It should be mentioned that C_{be} is the largest among the other parasitic capacitors in the transistor. Eliminating its influence on the circuit results in better reproducibility with respect to PVT variations. The oscillation

Table 4.3: List of the VCO components and their values [8].

$\boldsymbol{L_b}$	110 pH	$\boldsymbol{C_1}$	660 fF	$\mathbf{Q^*_{1-2}}$	2.88 µm
$\boldsymbol{L_e}$	450 pH	$\boldsymbol{C_2}$	80 fF	$\mathbf{Q^*_{3-4}}$	1.92 µm
$\boldsymbol{L_c}$	500 pH	$\mathbf{TL_e}$	270 µm @ 80Ω	$\boldsymbol{I_0}$	4 mA
$\boldsymbol{C_{var}}$	660 fF				

* emitter length (the width is always 0.12 um)

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frequency can be approximated by

$$f_0 = \frac{1}{2\pi\sqrt{L_\mathrm{b}C_\mathrm{tot}}} \tag{4.5}$$

where L_b is the base inductance and C_tot is the total capacitance resulting from capacitors C_var, C_1 and transistor parasitic capacitances C_be, C_bc and C_ce and can be calculated as follows

$$C_\mathrm{tot} = (C_1 + C_\mathrm{be})||(C_\mathrm{var} + C_\mathrm{ce}) + C_\mathrm{bc}. \tag{4.6}$$

It is assumed here that the inductance introduced by L_e and $\mathrm{TL_e}$ is large enough and does not impact C_var [36]. Also, no effects coming from the resistors, as well as transistor nonlinearities are considered. Nevertheless, (4.5) and (4.6) serve as a good starting point in the design process. Since all the parasitic capacitors are typically much smaller than C_1 and C_var, their influence on the oscillation frequency is negligible. The common-collector topology also provides intrinsic isolation between the tank circuit and the load. An additional common-base buffer ($\mathrm{Q_3}$,$\mathrm{Q_4}$) improves the isolation and output power. Unfortunately, the loading effect of the this buffer may impact the Q-factor of the tank circuit (through C_bc) causing worse phase noise performance [36]. A binary weighted varactor bank was implemented to provide flexibility in terms of VCO gain. By digital control of S_0, S_1 and S_2 a family of 8 tuning curves with low VCO gain can be realized (Fig. 4.23b). It is favorable in terms of phase noise due to weaker AM-PM conversion at the control input. However, all tuning pins can be shorted if a single large tuning range is desired. All components and their values are presented in Table 4.3.

A breakout circuit including the VCO was manufactured and measured. The VCO

can be tuned in the 36.5-42.0 GHz range. The measured phase noise at 1 MHz frequency offset from the carrier with all control inputs shorted is presented in Fig. 4.23c. The phase noise increases with frequency from -94 to -92 dBc/Hz. The same VCO test circuit was fabricated using the SG13G2 process for comparison. The phase noise performance is around 2-4 dB better than the SG13S VCO due to the higher f_{T} of the SG13G2 compared to SG13S. Table 4.4 summarizes the VCO performance against other Ka-band circuits published in the past. Regarding significant tuning range the VCO achieves moderate phase noise, which can be potentially improved by removing the CB stage at collectors of the core transistors or by increasing the bias current of the VCO.

Table 4.4: Summary of VCO performance and comparison with the state-of-the-art [8].

Ref.	Proc.	Freq. [GHz]	TR [%]	P_{DC} [mW]	PN^{*} [dBc/Hz]	FOM_{T}^{**} [dBc/Hz]
[97]	180 nm CMOS	38.2	19.6	28	-96.0	-179
[36]	350 nm SiGe	41.5	26.3	280	-107.0	-183
[36]	350 nm SiGe	46.3	10.8	490	-99.5	-167
[98]	130 nm CMOS	40.0	27.0	12	-95.0	-185
[99]	130 nm CMOS	35.0	26.0	11	-100.1	-189
[100]	250 nm SiGe	36.3	10.4	105	-104.6	-176
[101]	130 nm SiGe	32.5	18.1	20	-97.0	-180
[102]	65 nm CMOS	35.0	5.1	-	-95.0	-
This Work	**130 nm SiGe**	**39.5**	**13.9**	**13**	**-92.0**	**-176**

* worst case at 1 MHz offset

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** $FOM_{\mathrm{T}} = PN - 20\log(f_{\mathrm{c}}TR) + 10\log(P_{\mathrm{DC}}) - 40$

Three stages of divide-by-two circuits (DTC) were implemented in order to scale down the frequency before driving the MMD. Since the maximum operating frequency at the input of the MMD is around 6 GHz, a prescaler ratio of 8 satisfies this requirement. The divided signal DIV_{out} is in the 4.56-5.25 GHz range and is also suitable for phase noise measurement using an SSA E505B. Choosing a higher prescaler ratio is in general not desired due to larger variation of the division ratio at the PFD input (in fractional mode) and thus elevated in-band phase

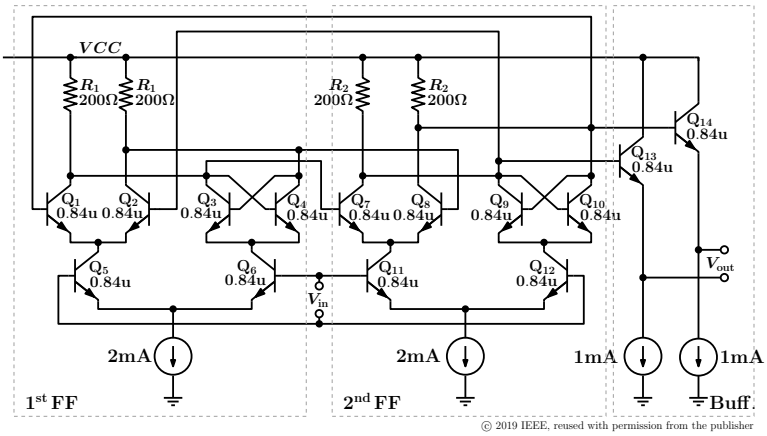

Figure 4.24: Schematic of a single DTC consisting of two cascaded D-type flip-flops with negative feedback [8].

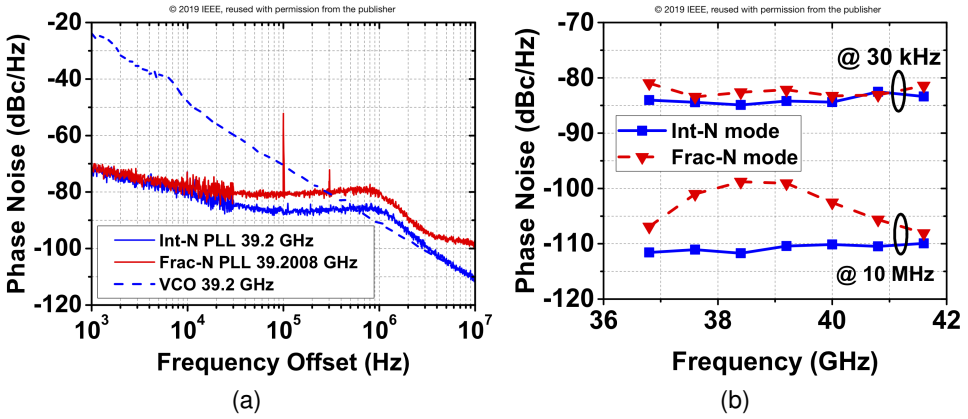

Figure 4.25: (a) Measured (solid) PLL and VCO phase noise. (b) In-band and out-of-band PLL phase noise. [8]

noise floor [103]. A single DTC is presented in Fig. 4.24. It consists of two cascaded D-type flip-flops with feedback. Each flip-flop includes emitter followers for driving the next stage, thus improving the speed at the cost of higher power consumption. Each transistor is biased at the optimum current density for the highest $f_{\mathrm{T}}/f_{\mathrm{MAX}}$. The highest simulated frequency, at which the DTC still operates properly is around 55 GHz after parasitic extraction. A common-emitter buffer after the frequency divider chain is included to drive a 50 Ω external load. A 39.5 GHz PA after the VCO increases the output power and improves the isolation between the oscillator and external loads.

Details concerning the low-frequency part of the PLL, i.e., PFD/CP, SDM, WG, SPI, as well as MMD can be found in [104]. A fourth-order LF was implemented using SMD components. A loop bandwidth of 1 MHz was chosen as a compromise between phase noise performance and settling time. A narrower loop bandwidth would lead to lower out-of-band phase noise resulting from SDM quantization noise. However, due to inevitably longer settling times, the PLL performance might become worse in case of fast frequency ramps, where the instantaneous frequency error has a strong impact on the ranging precision.

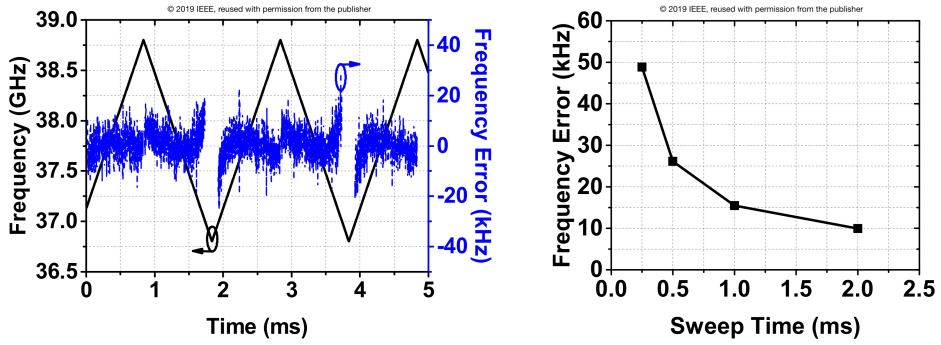

Figure 4.26: (a) Measured triangle frequency ramp (solid) with $\mathrm{T_{SW}}$=1 ms, $\mathrm{B_{SW}}$=2 GHz and instantaneous f_{err} (dashed). (b) Measured RMS frequency error versus sweep time (constant $\mathrm{B_{SW}}$=2 GHz).[8]

A dedicated synthesizer PCB was manufactured for PLL characterization. An R&S FSW67 signal and spectrum analyzer was used for measurements. The PLL can be locked in the 36.4-41.84 GHz frequency range, which corresponds to a 13.9 % locking range. A small shift in the frequency between the VCO breakout circuit and PLL chip can be accounted to PVT variations. Fig. 4.25a presents the phase noise spectrum measured at 4.9 GHz and scaled up to 39.2 GHz by adding $20\log_{10}8$=18 dB, where 8 is the prescaler ratio. Notice an elevated in-band phase noise plateau in fractional mode as well as influence of SDM quantization noise around 10 MHz offset. Also, significant spurious tones exist in the spectrum, especially pronounced when the fractional part of the division ratio is within the loop bandwidth and cannot be attenuated by the LF. Fig. 4.25b presents the measured phase noise level at 30 kHz and 10 MHz offset in integer and fractional mode. At 30 kHz, the phase noise performance in fractional mode is, in worst case, 4 dB

larger with respect to integer mode. At 10 MHz the difference rises up to 12 dB at the center of the frequency range. This is caused by the widest loop bandwidth in this region. At the limits of the tuning range the VCO gain decreases which results in a narrower loop bandwidth and better attenuation of the out-band SDM quantization noise.

By exploiting the demodulation feature available in the source analyzer, the PLL was tested in FMCW mode. Several chirps were measured and evaluated in terms of frequency error. A demodulated signal with T_{SW}=1 ms, B_{SW}=2 GHz and corresponding frequency error is presented in Fig. 4.26a. The frequency error is defined as a difference between the instantaneous frequency and ideal value resulting from a linear fit of the ramp. The standard deviation of the frequency error for different chirp lengths (constant B_{SW}=2 GHz) is shown in Fig. 4.26b. Faster sweeps are less accurate resulting in a larger frequency error in the range of tens of kHz.

4.2.3 Two-Channel FMCW Radar Demonstrator

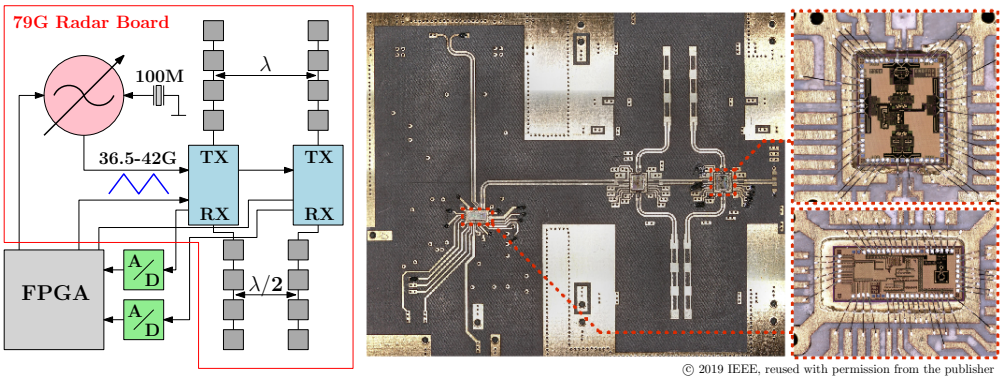

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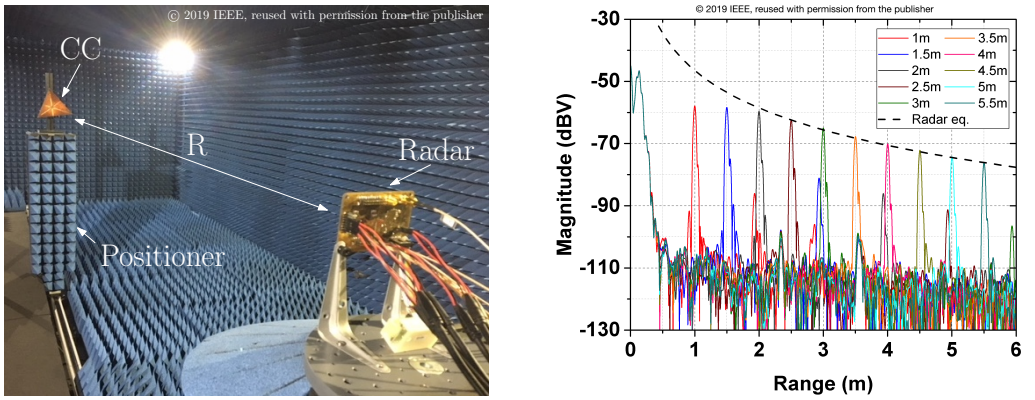
Figure 4.27: 2-channel radar demonstrator with a 39.5 GHz FMCW generator [8].

In order to investigate applicability of the PLL and TRX circuits in a radar system, a 2-channel FMCW radar demonstrator was fabricated using a Nippon Pillar H260AS microwave substrate with 127 µm thickness and relative dielectric constant of 2.7. The substrate was laminated on FR4 material to provide mechanical stability of the entire radar board. The block diagram of the 2-channel radar PCB



(a) (b)

Figure 4.28: (a) Setup for range measurement in an anechoic chamber. (b) Range measurement with averaging of 1000 samples.[8]

and its front side is presented in Fig. 4.27. The left side of the board is occupied by the 39.5 GHz PLL. All connectors and SMD components including an off-chip LF and the 100 MHz crystal are placed at the backside to reduce the backscattering effect as much as possible. The differential 39.5 GHz signal is fed to two cascaded 79 GHz TRX front-ends located at the right side of the PCB. A four-element series-fed patch antenna is connected at the TX and RX side of each transceiver [87]. The distance between the TX and RX antenna arrays is λ and $\lambda/2$, respectively, for better angular resolution and unambiguity [105]. The differential I/Q outputs are digitized using a dedicated analog-to-digital converter (ADC) and processed in an FPGA. Both ADCs and FPGA are implemented on another PCB that can be easily connected to the radar board.

Fig. 4.28a shows the range measurement setup in an anechoic chamber to reduce the clutter as much as possible. A corner cube (CC) with RCS of around 150 m^2 is used to imitate reflection from an automobile. Fig. 4.28b presents a range measurement of a CC placed at various distances from the sensor using one active TRX. 1000 measurements were performed at each distance, averaged and processed. The data is sampled with f_s=2 MHz and stored using an R&S oscilloscope RTO1044. A MATLAB script was written for FFT and visualization. A strong IF amplitude is visible at the right position of the CC. In addition, significantly weaker peaks can be found at longer distances due to multi-path effects of the signal being reflected from the board and again from the CC (so-called ping-

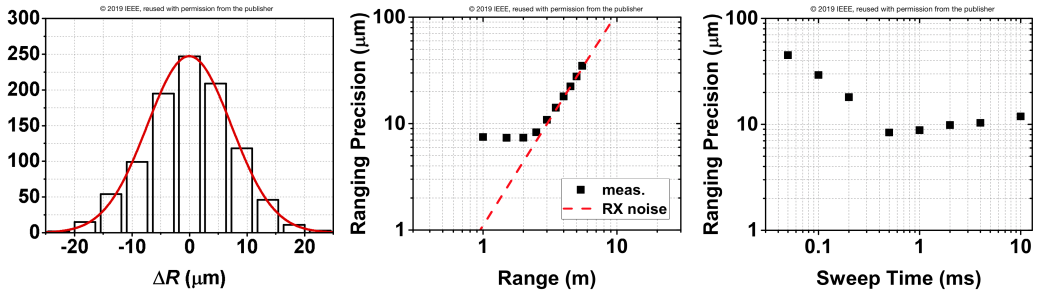
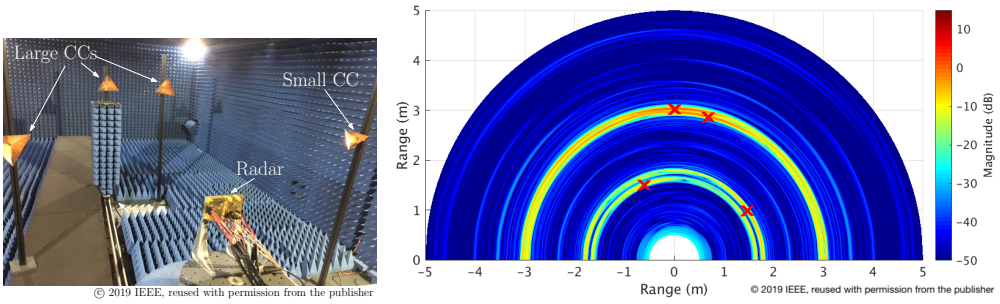


Figure 4.29: (a) Histogram for the ranging error at 2m. Sweep time T_{SW}=1 ms and sweep bandwidth B_{SW}=8 GHz. (b) Ranging precision. Receiver noise contribution (dashed) with $\sigma_R \propto R^2$ [92]. (b) Ranging precision versus sweep time at 2 m.[8]

pong effect). The range measurement was performed using a linear chirp in the 73.6-81.6 GHz range (B_{SW}=8 GHz) with a sweep duration T_{SW}=1 ms. Notice that above 2 m the received power follows the radar equation. For smaller distances the RX power level is less than expected probably due to imperfect alignment of the CC with respect to the sensor and near-field effects.

Fig. 4.29a presents a histogram of 1000 measurements performed using a target placed 2 m from the sensor. Here, an FFT length of 2^{26} was used in order to provide a sufficiently fine range step to characterize the ranging precision. A Gaussian function is drawn upon the results to obtain a standard deviation (σ_R) of the range measurement, thus, ranging precision. At 2 m σ_R=7.5 µm and is limited due to the finite SNR. A set of 1000 measurements was performed for a target located from 1 m to 5.5 with 0.5 m step. Range standard deviation was calculated for each target position and is shown in Fig. 4.29b. As expected the ranging precision decreases with distance due to worse SNR. For distances below 2 m the precision does not improve due to quasi-constant SNR in this region (see Fig. 4.28b) and more exacerbated influence of the PLL noise. The relationship between σ_R and R is in general a subject to various noise sources in the system including the white noise at the receiver, PLL noise or quantization noise due to the limited ADC resolution [92, 106]. According to [92], the measured σ_R points fit to a curve $\propto R^2$ indicating that the ranging error results mostly from the noise at the receiver. A dependency of σ_R with respect to $\mathrm{T_{SW}}$ was investigated for a tar-



(a) (b)

Figure 4.30: (a) Setup for 2-dimensional range measurement with four reflectors in an anechoic chamber. (b) 2-D range measurement of four targets. Crosses indicate the peaks.[8]

get placed at 2 m from the sensor (Fig. 4.29c). The same modulation bandwidth of 8 GHz was kept constant. For faster ramps (below 0.5 ms) σ_R increases significantly and for $\mathrm{T_{SW}}$=50 µs it reaches 45 µm. For shorter sweep times the PLL fails to lock due to relatively narrow loop bandwidth and the chirp is not generated. The worse σ_R probably results from a larger frequency error associated with fast ramps (see Fig. 4.26b).

Owing to the 2-channel implementation of the radar board the targets can be resolved not only in range but also in the angle they are located with respect to the sensor. Due to the utilized scalable radar architecture, a calibration is required to correct the phase mismatches in the measured IF signals. It is done by measuring a reference object placed at 0 degree angle from the radar. A digital beam-forming method was used to process four data sets from two TRXs (each TRX generates I/Q output signals) and calculate a 2-dimensional position of each target [105, 107]. Fig. 4.30 presents four targets in a Cartesian coordinate plane with the sensor located at the origin (0,0). Note that the angular resolution is essentially low owing to a small number of antennas. The performance of the TRX and the PLL is summarized in Table 4.5.

Table 4.5: Summary of the state-of-the-art Si-based E-band radar TRXs [8].

Ref.	**This Work**	ISSCC'18 [108]	JSSC'17 [109]	JSSC'17 [110]	JSSC'16 [111]	TCAS'14 [83]	IMS'14 [112]	TCAS'13 [113]	TMTT'12 [114]	TMTT'12 [115]	JSSC'10 [116]	JSSC'10 [117]
Process	**SiGe 130nm**	CMOS 45nm	CMOS 28nm	SiGe 130nm	CMOS 65nm	SiGe 180nm	SiGe 180nm	CMOS 65nm	SiGe 180nm	SiGe 180nm	CMOS 65nm	CMOS 90nm
Radar technique	**FMCW + PLL**	FMCW + PLL	PMCW + PLL	FMCW + PLL[e]	FMCW + PLL	PMCW + PLL	FMCW + PLL[e]	FMCW + PLL	FMCW + PLL[e]	FMCW + PLL[e]	FMCW + PLL	FMCW + DDS
# TX / # RX	**1/1**	3/4	2/2	2/6	1/2	1/1	1/4	1/1	1/4	1/1	1/1	1/1
Integration level	**2 Chips**	1 Chip	1 Chip	1 Chip	1 Chip	1 Chip	2 Chips	1 Chip	2 Chips	3 Chips	1 Chip	1 Chip
Frequency (GHz)	**79**	79	79	79	77	77	79	76	79	80	76	77
PN (dBc/Hz) at 1 MHz	**-80**	-91	-85	-99	-81	-105	-97	-85	-95	-85	-85	-85
σ freq. error (kHz)/mod. rate (GHz/ms)	**10/2 15/4 26/8 49/16**	0.06^b % /100	-	-	674/1.93	-	-	73/-	-	-/6.6	64/1	93/2.46
P_{TX} (dBm)	**19.2**	10.8	8.5^c	18	13.2	6.2	17	6.4	13	-1	5.1	-2.8
G_{RX} (dB)	**27.5**	-	45	15	48-101	24	16	23	19	11	38.7	23.1
NF (dB)	**7.2**[h]	18	12^c	11	5	13	12	14.8	12	12	7.4	15.6
RX $IP_{1\mathrm{dB}}$ (dBm)	**-10**	-7	2^d	1	-	-14	-2	-	-5	-1.2	-	-
B_{SW} (GHz)	**8**	4	2	-	1.93	4.25	-	0.7	-	26.5	0.5	0.614
Range res. (cm)	**1.8**	3.75	7.5	-	7.8	3.5	-	21.43	-	0.7	30	24.4
Range precision (µm)	**7.5**	-	-	-	-	1020	-	-	-	0.36	-	1000-8000
P_{DC} (W)	**1.02**[a]	3.5	1	1.8^f	0.34	1.2	1.95	0.27	2.5	0.49^g	0.24	0.52
Chip area (mm^2)	**6.68**[a]	22	7.9	12.7	4.64	5.9	12.6	0.97	18.5	3^g	1.04	6.8
Antenna type	**Series-fed 1x4 patch**	-	-	-	-	Horn	-	-	-	Horn	Corp.-fed 8x8 patch	Horn
G_{ant} (dBi)	**11**	-	-	-	-	20	-	-	-	20	20	20

[a] TRX+PLL, [b] ramp nonlinearity, [c] after packaging, [d] output referred, [e] on-chip VCO w/ ext. PLL, [f] 1 TX/6 RX, [g] TRX only, [h] sim. value

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5 G-Band Integrated Radar Transceivers with On-Chip Antennas

Continuous technology node scaling and device structure optimization has shifted transistor's $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ above 300/500 GHz and made several frequency bands (D, G, J, Y) applicable due to decent performance of the active devices [118]. Therefore, numerous radar transceivers working beyond 100 GHz have been reported over the last decade. The F-band (90-140 GHz) centered around 122 GHz became interesting as an unregulated ISM band [68, 119, 120]. However, heavy propagation loss due to peak oxygen and water absorption at 120 GHz and 183 GHz, respectively, limits maximum detectable range in long distance scenarios, making higher frequency bands attractive [121–124],[125–128]. Nonetheless, atmospheric attenuation is still significant and limits radar usage to short range applications, e.g., high-precision ranging for vibration detection, imaging or gesture recognition.

Most of the reported TRXs comprise integrated antennas due to acceptable size with respect to other building blocks [79, 89, 129, 130]. Typically, such on-chip radiators suffer from poor gain and efficiency which can be improved by using localized backside etching (LBE) of the substrate [119] and placing additional focusing lenses [127, 130]. Another technique includes wire bonding a separate antenna chip to the transceiver die and placing them in a package (Antenna-in-Package (AiP)) or using embedded wafer-level ball-grid array (eWLB) package for direct antenna and TRX co-integration [125, 131]. The latter method exhibits much less parasitics easing antenna matching and reducing resistive losses when compared to conventional solutions based on wire bonding [69, 121].

5.1 Monostatic Radar TRX with TX-to-RX Leakage Cancellation

In the following, a monostatic FMCW radar TRX is presented, in which the leakage cancellation technique described in Section 3.3 has been adopted. An on-chip antenna using the LBE feature offered by the foundry was designed and incorporated in the TRX. Most of the material presented in this section has already been published in [16].

5.1.1 TRX Architecture

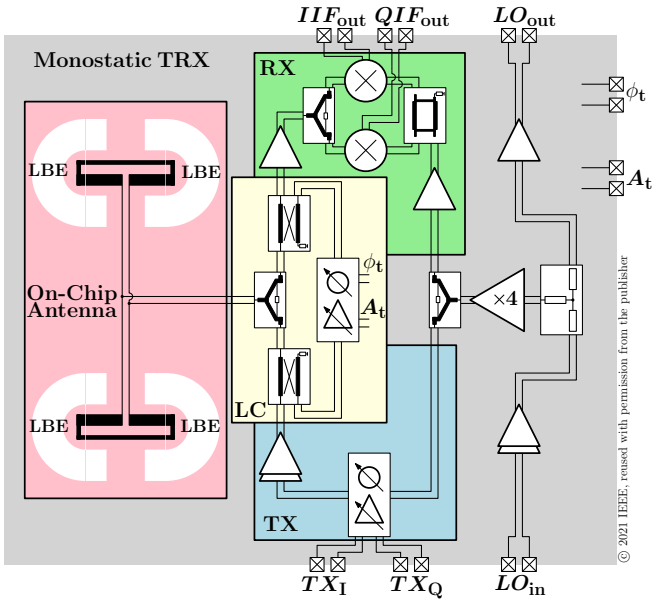
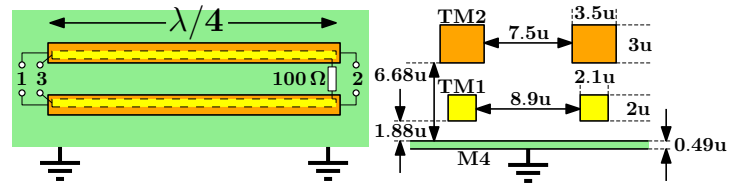


Figure 5.1: Block diagram of the monostatic TRX [16].

The block diagram of the circuit is presented in Fig. 5.1. The TRX configuration follows a scalable system concept presented in Section 1.1. Here, a Q-band LO signal is used to drive an on-chip frequency quadrupler that converts the frequency up to G-band. Frequency multiplication is realized using the stacked bootstrapped Gilbert-cell described Section 3.1.1[17]. The LO signal is amplified and by-passed to the output for optional driving the other TRXs in the chain.



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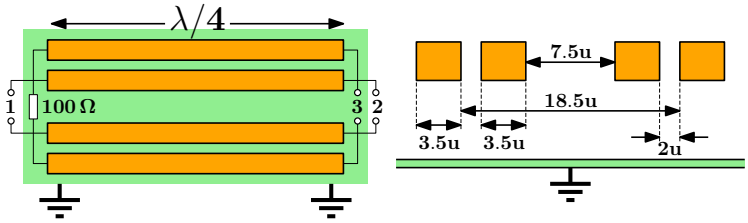
(a)



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(b)

Figure 5.2: Top view layout of the directional coupler in (a) TX and (b) RX path. [16]

The up-converted LO signal is split between the TX and RX blocks by means of a Wilkinson power splitter. The TX signal is fed to the VM for phase-tuning in beam forming applications. The VM can also be used for complex carrier modulation. After the VM, the signal is amplified by a two-stage cascode PA. On the RX side the signal is amplified using a two-stage cascode low-noise amplifier and split between two Gilbert-cell mixers for I/Q down-conversion. A branchline coupler is implemented for quadrature LO signals generation.

5.1.2 TX-to-RX Leakage Cancellation

The leakage canceller (LC) section comprises a TX-RX coupler, two directional couplers for signal extraction/injection and a VM for adjustment of the leakage replica. A part of the TX signal is coupled to the VM, delayed and amplified accordingly to the leakage and fed back to the input of the LNA. A Wilkinson power splitter is used as TX-RX coupler for reasons described in Section 3.3. The directional coupler consists of two quarter-wave TLs deposited in close proximity to obtain the desired coupling factor. The physical implementation of the TX and RX directional couplers is presented in Fig. 5.2a and Fig. 5.2b, respectively.

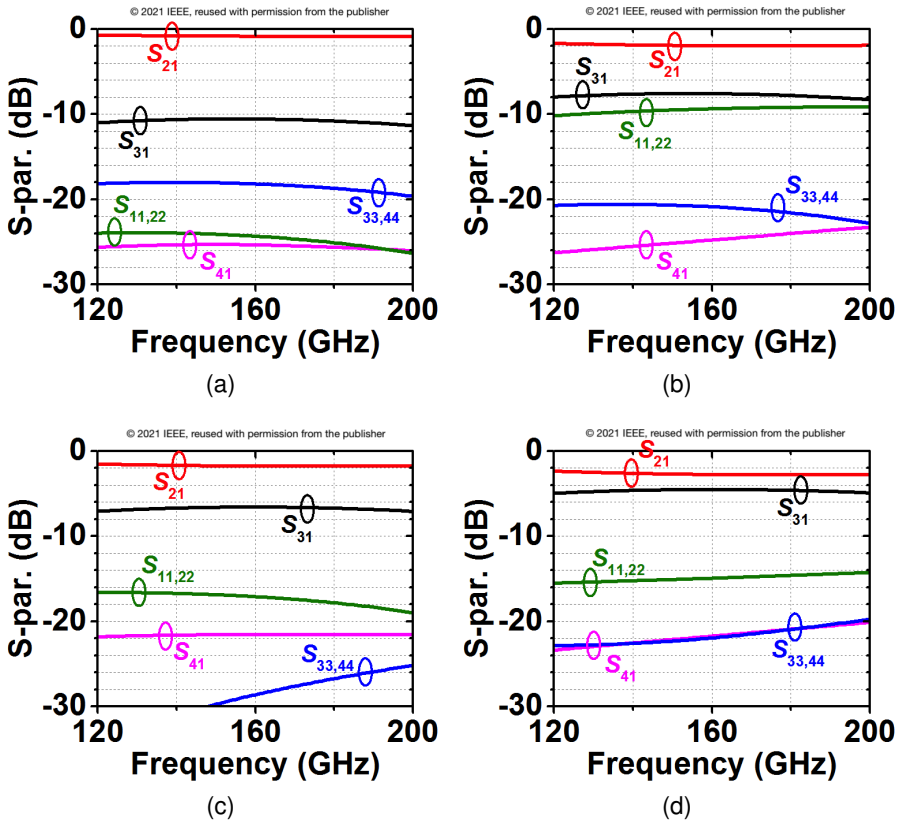

Figure 5.3: Simulated S-parameters of the directional coupler in the (a) TX (differential mode) (b) TX (common mode) (c) RX (differential mode) (d) TX (common mode).[16]

The simulated S-parameters of each structure for differential and common-mode is presented in Fig. 5.3. The primary $\lambda/4$-TL is realized as a 100 Ω differential microstrip line in the top most metal layer (TM2). At the TX, the coupled TL section is implemented in the second top most metal layer (TM1). The ground shield for the microwave structures is at fourth metal layer (M4) which leaves the M1-M3 layers for other purposes, e.g., supply and bias connections. The arrangement presented in Fig. 5.2a results in 11 dB coupling factor and 1 dB insertion loss. On the RX side, the coupled TL section is placed closer to the primary and is implemented in TM2 which ensures a higher coupling factor of 7 dB traded for a higher insertion loss of 2 dB. Common-mode (CM) signals experience stronger attenuation at the through port. More CM signal power couples to the LC but is then suppressed by the VM. A stronger coupling in RX case results from a higher mar-

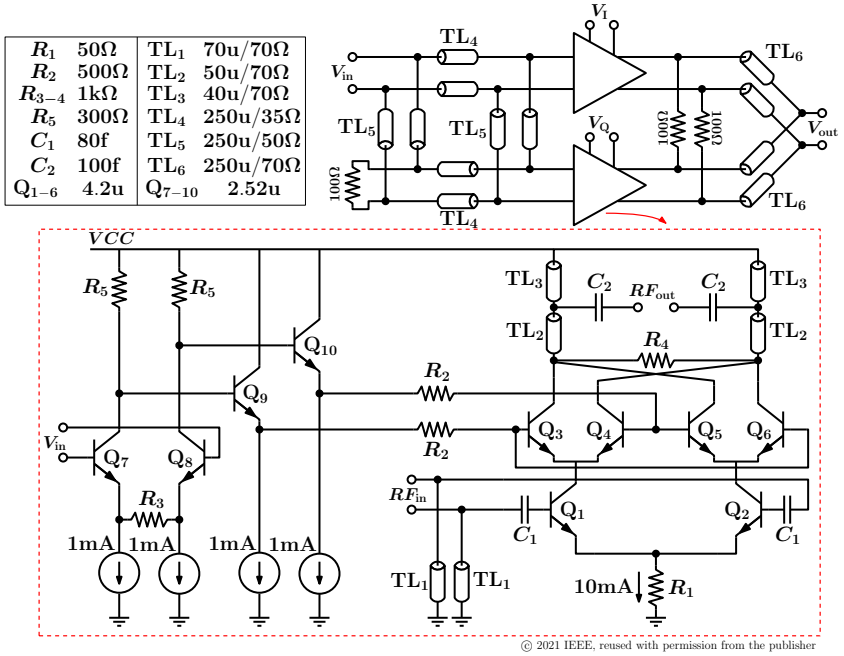

Figure 5.4: Schematic of the vector modulator comprised of two BPSK modulators, branchline coupler and Wilkinson combiner [16].

gin put on the compensation signal power. To arrive at full leakage compensation the following must be satisfied

$$L_{\mathrm{TX}} + I_{\mathrm{TX-RX}} + L_{\mathrm{RX}} = C_{\mathrm{TX}} - G_{\mathrm{VM}} + C_{\mathrm{RX}}, \tag{5.1}$$

where $L_{\mathrm{TX,RX}}$ is the insertion loss of the directional coupler, $C_{\mathrm{TX,RX}}$ is its coupling factor, $I_{\mathrm{TX-RX}}$ is the isolation provided by the Wilkinson splitter and G_{VM} denotes the gain of the vector modulator. Solving (5.1) for $I_{\mathrm{TX-RX}}$ results in a minimum TX-RX isolation of 10 dB that still can be compensated. Fig. 5.4 presents the detailed schematic of the vector modulator. It includes two binary phase-shift keying (BPSK) modulators driven by quadrature signals with combined outputs for full amplitude and phase tuning range. Each BPSK modulator is based on a Gilbert-cell topology and includes G_m-stage and switching quad consuming 10 mA from a 3.3 V supply. Simulated S-parameters for two different $V_{\mathrm{I,Q}}$ settings are presented in Fig. 5.5a. Note, that the VM provides CMRR above 20 dB thus sufficiently suppressing CM signals. This is mostly due to tail resistors in the BPSK modulators and the branchline coupler. The latter is composed of closely coupled TLs result-

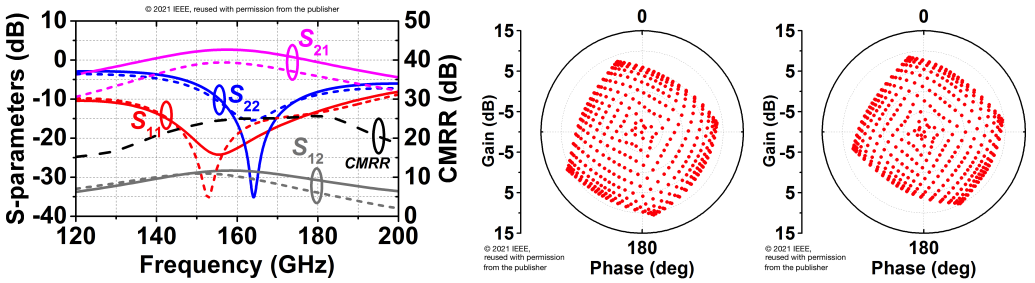

Figure 5.5: (a) Simulated VM S-parameters for two different settings. VM constellation plot at (b) 160 GHz and (c) 170 GHz.[16]

ing in improved CM rejection owing to a high even-mode impedance. Constellation plots of the VM followed by a buffer at 160 GHz and 170 GHz are shown in Fig. 5.5. The complete compensation network was designed and electromagnetically simulated. For LC evaluation, the antenna port was terminated with a 100 Ω resistor. Fig. 5.6 presents simulated TX-RX isolation for two states of the

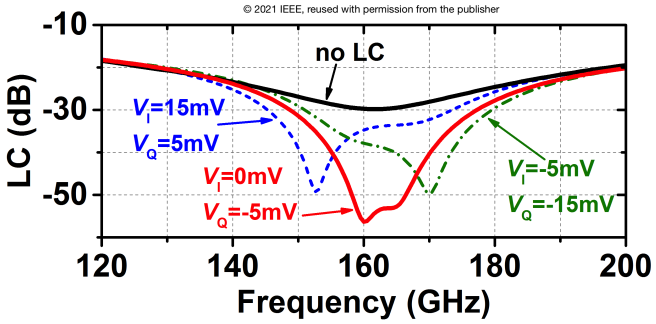

Figure 5.6: TX-to-RX leakage using the EM-characterized Wilkinson coupler (black). Enabling leakage cancellation improves TX-RX isolation above 40 dB in a 15 GHz bandwidth (red). The maximum isolation can be shifted by changing the VM settings (blue and green) [16].

LC. In OFF mode the compensation network is disabled and inherent isolation of the Wilkinson TX-RX coupler reaches -30 dB leakage attenuation at 161 GHz. Activation of the LC network and optimization of the compensation signal improves the total TX-RX isolation significantly down to -40 dB in the 155-170 GHz range. Sweeping the VM settings can change the frequency at which the maximum isolation is obtained. Temperature variation has significant influence on the

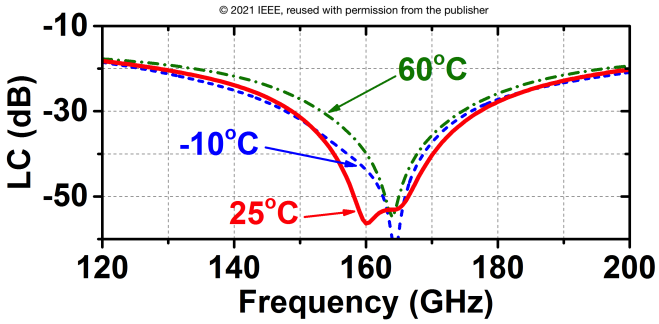

Figure 5.7: TX-to-RX leakage for three temperatures after adjustment [16].

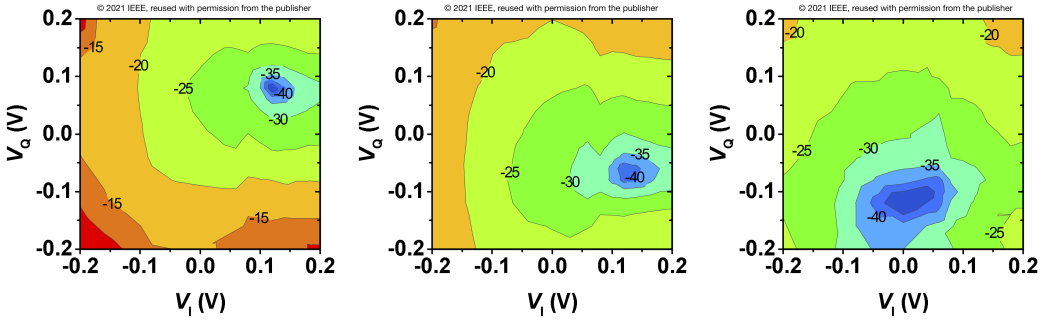

Figure 5.8: Measured TX-to-RX isolation for different vector modulator settings at (a) 150 GHz, (b) 160 GHz and (c) 170 GHz.[16]

cancellation accuracy, therefore the LC settings should be automatically adjusted to optimized the compensation. Fig. 5.7 presents TX-to-RX leakage for three temperatures after adjustment. The side effect is more narrowband behaviour mostly due to active devices in the LC network. A breakout circuit containing the LC has been manufactured for independent characterization. The antenna port was terminated with a 100 Ω resistor as in simulation. A D-band (110-170 GHz) S-parameter setup including a R&S VNA and frequency extenders was used to measure the TX-RX isolation.

Fig. 5.8 presents measured constant isolation contours with respect to VM settings at 150, 160 and 170 GHz. The LC enables effective leakage attenuation that can be tuned depending on the frequency of operation. The measured cancellation can be better than -40 dB, which extends the inherent Wilkinson TX-RX coupler isolation. In this work VM settings are adjusted manually. However, an

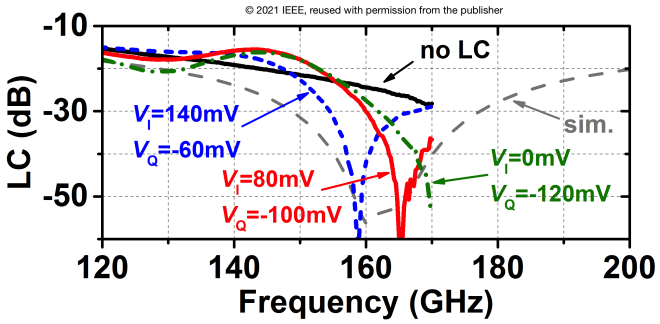

Figure 5.9: Measured leakage cancellation for different VM settings over the frequency [16].

automated calibration would be feasible by using predefined VM settings based on FMCW radar parameters. Using such a look-up table (LUT) might work assuming that the leakage is stationary. Another calibration scheme could employ a feedback loop, where V_I, V_Q would be swept until the DC offset is minimized. Such dynamic method would be appropriate if different ramp bandwidth/speed is applied that might change leakage properties. Fig. 5.9 presents the measured leakage cancellation for three different VM settings over the frequency. Enabling of LC results in an isolation improvement with respect to the disabled LC case, however, in a limited bandwidth compared to simulation. The measurements were performed on a LC breakout circuit incorporating baluns and a 100 Ω termination at the antenna port.

The main constraint of the proposed approach is the limited bandwidth in which the canceller effectively compensates the leakage. This might be a serious problem for applications using wideband modulated signals where the LC would only partially cancel the leakage. However, for FMCW radar this can be alleviated since the instantaneous phase/frequency is well defined and the LC could hypothetically track the signal by automatic gain and phase adjustment based either on a LUT or feedback loop.

5.1.3 On-Chip Antenna

The TRX is equipped with an integrated antenna for its relative compactness with respect to other building bocks. Full integration eliminates typical interconnection

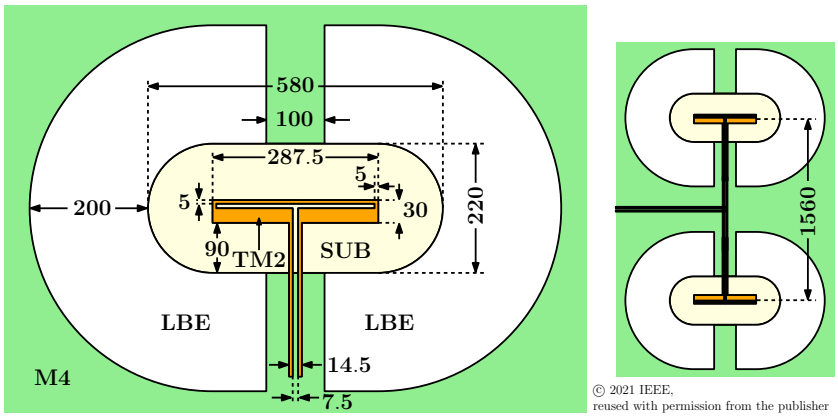

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Figure 5.10: Folded-dipole antenna layout (dimensions in micrometers) [16].

issues and is reasonable at sufficiently high frequencies. A double-folded dipole element was optimized for the 160-170 GHz range. It benefits from a localized backside etching (LBE) feature which improves gain and radiation efficiency remarkably [132, 133]. The arrangement of LBE areas around the radiating element effectively attenuates substrate surface waves while ensuring mechanical stability and reliability. Fig. 5.10 presents the sizing of a single folded-dipole element optimized for matching and gain. Two radiators are placed at around $\lambda/2$ for gain enhancement. Cavities around the antenna improve radiation efficiency and make the design less susceptible to the overall width and length of the silicon die. However, the chip thickness still plays a key role and determines the antenna performance and must be accounted for during the EM simulations. A 200 µm thinned substrate (SUB) was chosen to maintain mechanical stability. The remaining SUB island under the antenna does not affect the performance significantly, but makes the structure more resilient to mechanical stress. Fig. 5.11 shows the simulated

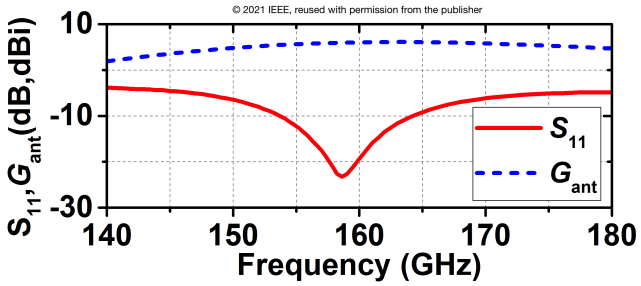
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Figure 5.11: Simulated antenna matching and gain [16].

input return loss and gain over frequency. The antenna achieves 6 dBi gain at 162 GHz and more than 3 dBi in the 144-180 GHz range reaching 60% peak radiation efficiency. The complete structure was modeled using 3-D FEM solver from Ansoft HFSS.

5.2 Bistatic Radar TRX

A monostatic architecture for integrated radar TRXs leads to several restrictions compared to a bistatic topology, where TX and RX are physically separated and feature dedicated antennas. The TX-to-RX leakage is an issue limiting the TX output power and RX noise figure but a single antenna saves die area which might be crucial if chip compactness is of priority. However, for high-performance applications, a bistatic radar architecture would be the right choice for unrestricted P_{TX} and NF_{RX} optimization. This section describes such a wideband bistatic radar TRX for G-band applications. Most of the material has already been published in [16].

5.2.1 TRX Architecture

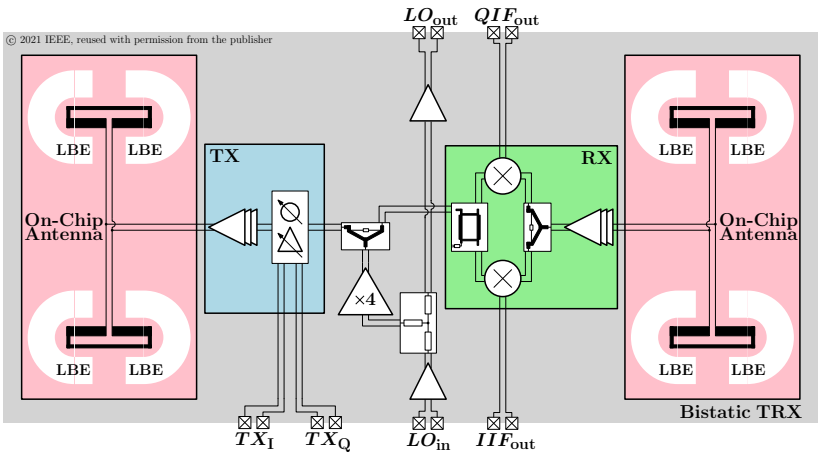


Figure 5.12: Block diagram of the bistatic TRX [16].

Fig. 5.12 presents a block diagram of the bistatic TRX comprising separate TX and RX on-chip antennas. The simulated cross-talk between the antennas is

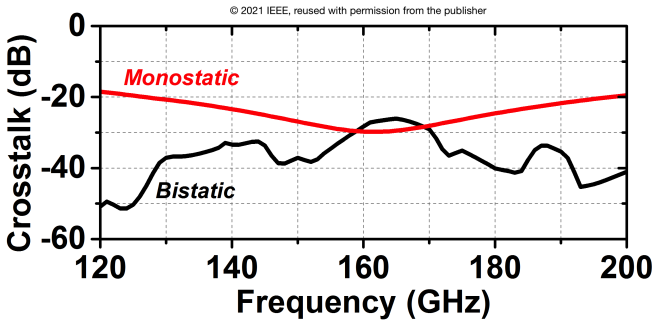


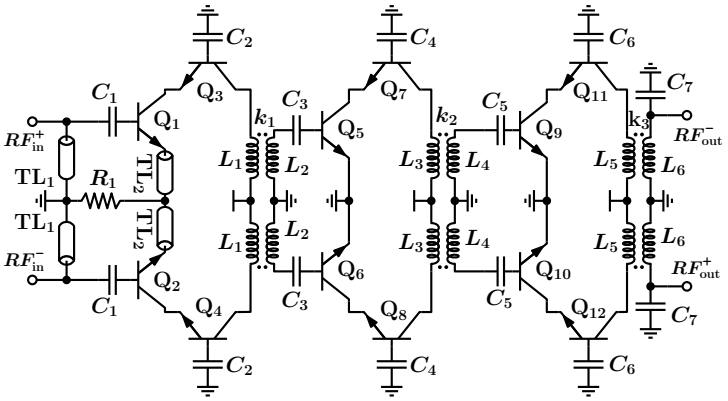
Figure 5.13: Simulated TX-RX crosstalk for both TRXs. In monostatic case a perfect 100 Ω termination at antenna port is assumed [16].

depicted in Fig. 5.13. In the simulation the possible cross-talk paths include the free space between the antennas and the silicon substrate. The cross-talk reaches surprisingly high values at the center frequency and diminishes outside the band becoming comparable with monostatic case around 160 GHz, where a direct cross-talk path through the coupler was considered. Higher cross-talk in the middle of the band for the bistatic TRX is due to better antenna matching and gain as more power is sensed by the RX antenna. A limited radiation efficiency also means that part of the TX signal couples to the RX port in form of substrate waves. However, the cross-talk in the monostatic TRX is expected to be worse due to not perfect antenna matching and isolation provided by the Wilkinson coupler. Similar to the monostatic version the bistatic architecture follows a scalable system concept with LO signal bypassed to the output for driving the next in-chain units.

Several circuits including the frequency quadrupler, down-conversion mixers and VM were reused. Major effort has been dedicated to the PA and LNA design for high-performance wideband operation.

5.2.2 Wide-Band Low-Noise Amplifier

Fig. 5.14 presents a schematic of the three-stage wideband LNA. Each stage implements a differential cascode topology for high gain and isolation with respect to the conventional common-emitter (CE) architecture. The balanced structure makes the circuit less susceptible to common-mode noise coming from supply



Q_{1-4}	4.2µ	Q_{5-12}	6.72µ	L_3	67p	L_6	90p	C_3	42f	C_6	146f	k_1	0.4
TL_1	65Ω/38°	L_1	90p	L_4	60p	C_1	80f	C_4	146f	C_7	30f	k_2	0.3
TL_2	50Ω/14°	L_2	80p	L_5	90p	C_2	95f	C_5	70f	R_1	50Ω	k_3	0.5

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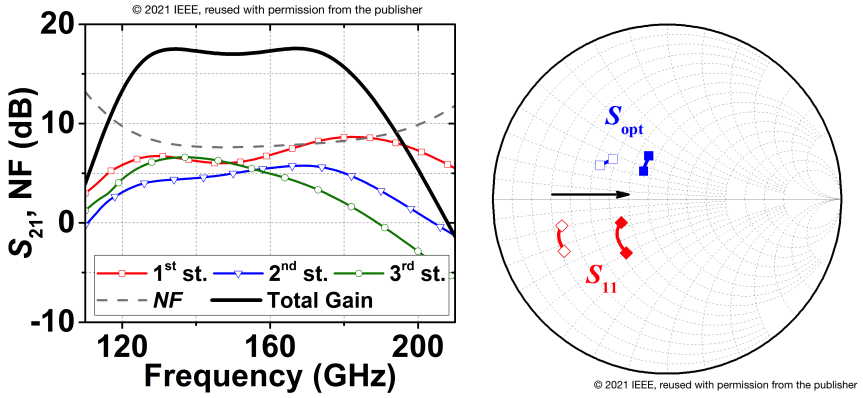
Figure 5.14: Three-stage LNA schematic [16].



(a) (b)

Figure 5.15: (a) Simulated LNA NF and gain distribution. (b) Influence of TL_2 on the optimum source impedance with respect to NF.[16]

and ground planes. Each of the input HBT devices comprises five fingers resulting in 4.2 µm total emitter length. The transistor size is a product of the desired linearity and minimum noise figure. In an FMCW radar the RX must handle relatively strong TX leakage, thus, LNA linearity becomes an important design aspect. The target LNA gain was set to above 15 dB in order to suppress the mixer noise to negligible levels. Assuming $OP_{1\mathrm{dB}}$=0 dBm and equal gain distribution among the stages, the calculation for cascaded $P_{1\mathrm{dB}}$ estimates $OP_{1\mathrm{dB}}$ of the first cas-

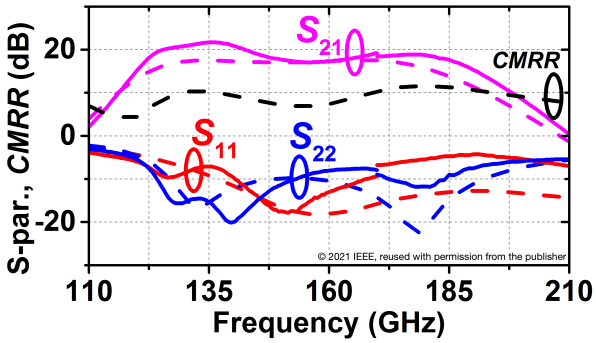
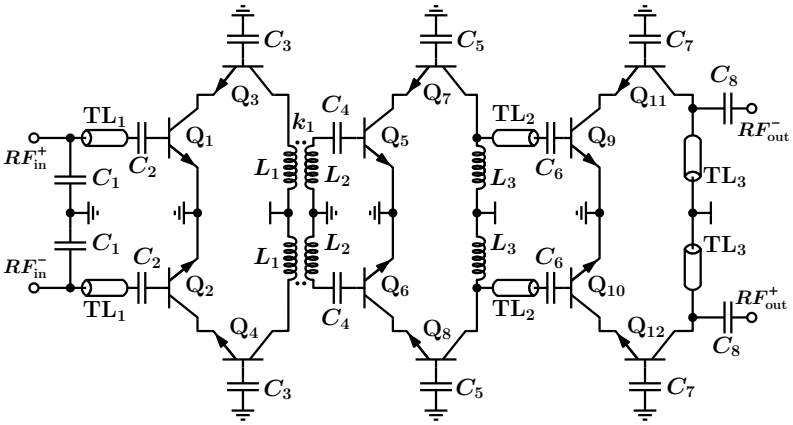


Figure 5.16: Simulated (dashed) and measured (solid) S-par. of the LNA [16].

code to -5 dBm. This resulted in 7 mA bias current and emitter current density J_{E}=6.9 mA/µm^2. Two two following stages are biased at 9 mA and 17 mA, respectively, resulting in 33 mA total current consumption from a 3.3 V supply. Fig. 5.15a depicts the simulated small-signal gain and noise figure. The total gain is decomposed into contributions from each stage in order to visualize the bandwidth extension. The first stage peaks at 140 GHz, whereas the gain maxima of the middle and the last cascodes are located at 165 GHz and 180 GHz, respectively. This was realized by introducing a mismatch between the stages. Fig. 5.15b the shows S_{11} and S_{opt} change due to degeneration TL_2. This step brings the real part of both coefficients closer to each other and facilitates simultaneous matching for gain and noise at the cost of lower maximum available gain (MAG). The minimum simulated NF is 8.5 dB at 150 GHz. Fig. 5.16 presents simulated and measured S-parameters of the LNA in the 110-210 GHz range using WR-6 (110-170 GHz) and WR-4 (170-250 GHz) setups. The circuit yields slightly higher gain and bandwidth than expected with stronger in-band ripple.

5.2.3 Wide-Band Power Amplifier

Fig. 5.17 presents the schematic of the three-stage PA. The circuit resembles the LNA except for device sizing and matching networks. The OS comprises four HBTs, each composed of two 8-finger transistors connected in parallel. The bias current is set to a maximum level at which peak f_{T} is obtained, i.e., 1.8 mA per finger. The single device size as well as bias current in the middle stage (D2) is reduced with respect to the OS. A large inductor L_3 with self-resonance frequency



Q_{1-8}	6.72µ	TL_1	50Ω/36°	L_1	57p	C_1	30f	C_4	200f	C_7	73f
Q_{9-12}	13.44µ	TL_2	30Ω/32°	L_2	83p	C_2	200f	C_5	85f	C_8	120f
k_1	0.9	TL_3	70Ω/17°	L_3	320p	C_3	85f	C_6	200f		

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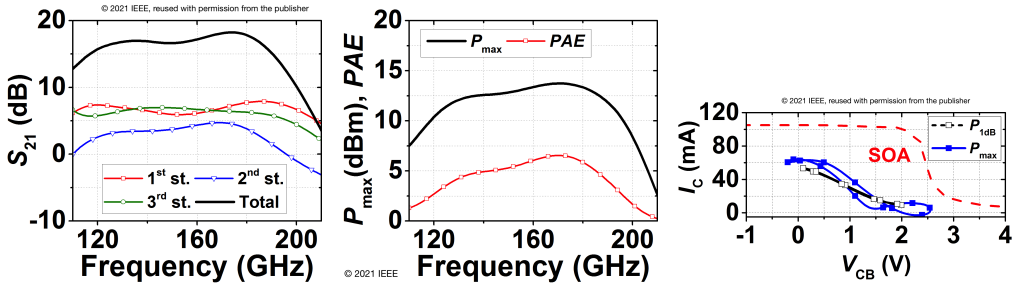
Figure 5.17: Three-stage PA schematic [16].



(a) (b) (c)

Figure 5.18: (a) PA gain distribution. (b) Maximum output power and PAE for P_{in}=0 dBm. (c) Simulated loadline of Q_{11} for P_{1dB} and P_{max}.[16]

(SRF) slightly above the range of operation was chosen to act as an RF choke. The input stage (D1) consists of HBTs sized as in the previous case except for current bias, which was set to 1 mA per finger. A mismatch between the stages provides wideband operation as depicted in Fig. 5.18a. The gain at the boundaries is boosted by the input stage, whereas in the middle it is compensated by D2 and OS. Simulated output power for 0 dBm input power as well as PAE is plotted in Fig. 5.18b. The peak P_{out} is 13.8 dBm with 6.5% PAE at 170 GHz. Even though BV_{CE0}=1.7 V and BV_{CB0}=4.8 V, the SOA is extended in case of cascode amplifiers provided that the base terminal is kept at low impedance [52].

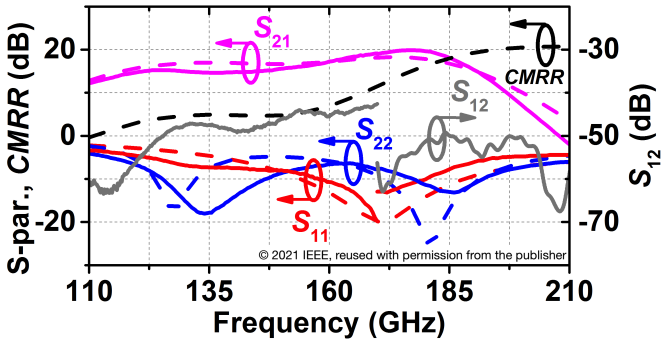
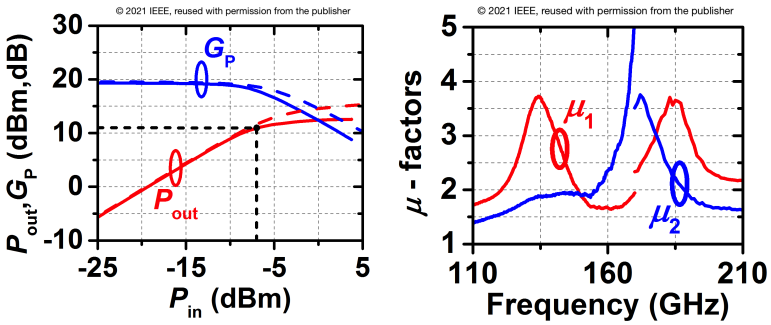


Figure 5.19: Simulated (dashed) and measured (solid) S-par. of the PA [16].

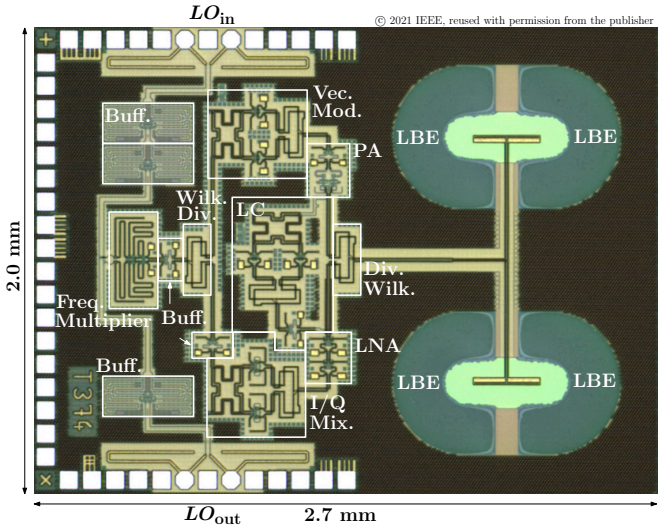


(a) (b)

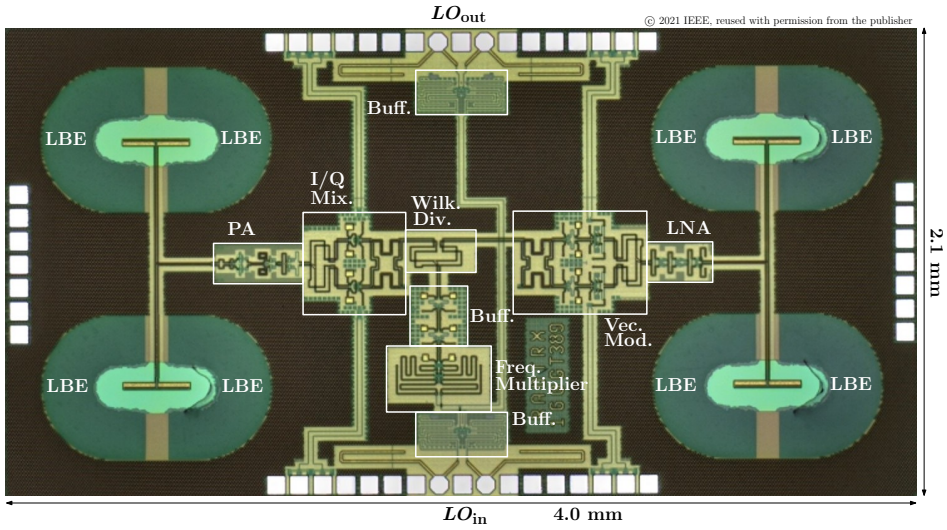
Figure 5.20: (a) Measured PA output power and power gain versus input power at 170 GHz. (b) Measured stability factors of the PA [16].

A dynamic loadline of the output stage transistors was investigated to ensure safe HBT operation (Fig. 5.18c).

Fig. 5.19 shows simulated and measured S-parameters of the PA. Good agreement can be observed with slightly increased gain deviation in the band of operation. Furthermore, Fig. 5.20a presents measured P_{out} and G_{P} versus input power at 170 GHz. Stability factors calculated from measured s-parameters are depicted in Fig. 5.20b showing unconditional PA stability in the band of interest. The PA and the LNA were characterized as standalone circuits using Marchand baluns [17] in order to enable single-ended measurements. The loss of the baluns was de-embedded from the gain and output power.



(a)



(b)

Figure 5.21: Die photograph of the (a) monostatic and (b) bistatic radar TRX.[16]

5.3 Experimental Results

Both monostatic and bistatic TRX have been manufactured using the SG13G2 process from IHP [13]. Photographs of the fabricated chips are presented in Fig. 5.21. The area of the TRX is 5.7 mm^2 and 8.4 mm^2 for monostatic and bistatic version, respectively. The area occupied by the double folded-dipole antennas

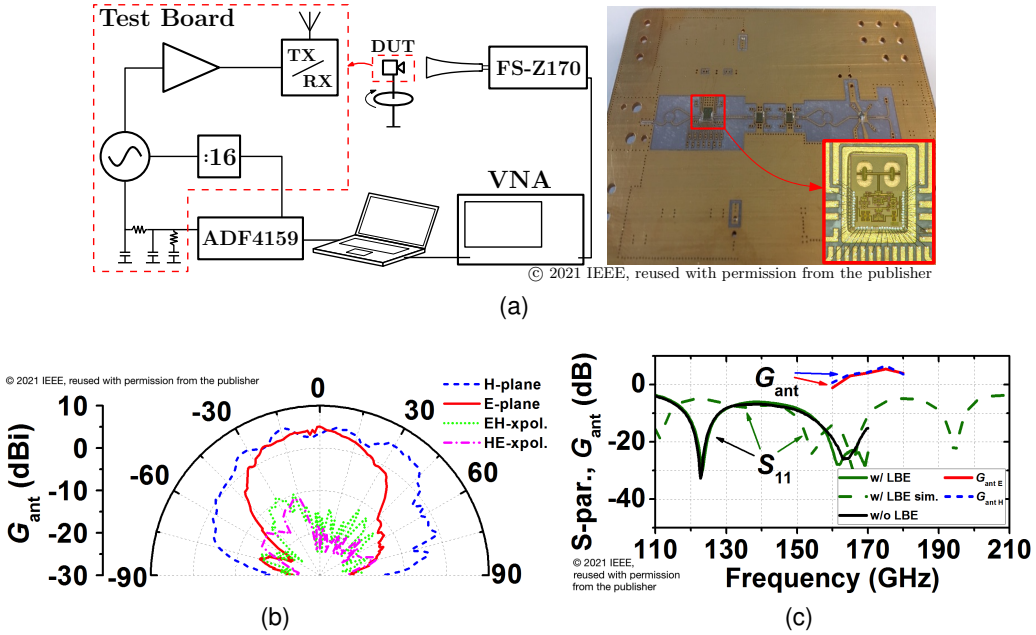


Figure 5.22: (a) Far-field measurement setup. (b) Radiation patterns of the double-folded dipole antenna. (c) Measured S_{11} and G_{ant}.[16]

constitutes 40% (monostatic) and 60% (bistatic) of the silicon die. This means around 33% area reduction for the benefit of the former topology.

A breakout structure containing a double-folded dipole antenna has been fabricated for characterization. Since the structure is differential, an on-chip Marchand balun published in [17] was used to facilitate single-ended measurement. Fig. 5.22a depicts a setup used to measure the antenna far-field pattern. The test board contains the TRX with on-chip antenna under test, an LO buffer, 36.5-42 GHz VCO integrated with a frequency divider (/16) and a low-pass loop filter (LF) used to synchronize with an external ADF4159 PLL. More details about the VCO can be found in [8]. The test board is placed on a rotary table whose angular position is programmed from a Matlab script. A reference D-band horn antenna with R&S FS-Z170 harmonic mixer connected to the VNA is used to receive the radiated TRX output power. Fig. 5.22b presents measured double-folded dipole radiation patterns for E-plane, H-plane and corresponding cross-polarization planes. It achieves 5 dBi and 4 dBi at an angle of 0 degrees in E-plane (horizontal) and H-plane (vertical), respectively. The 3-dB beamwidth for E-plane is around 45°, whereas for H-plane it increases to 90°. The cross-polarization

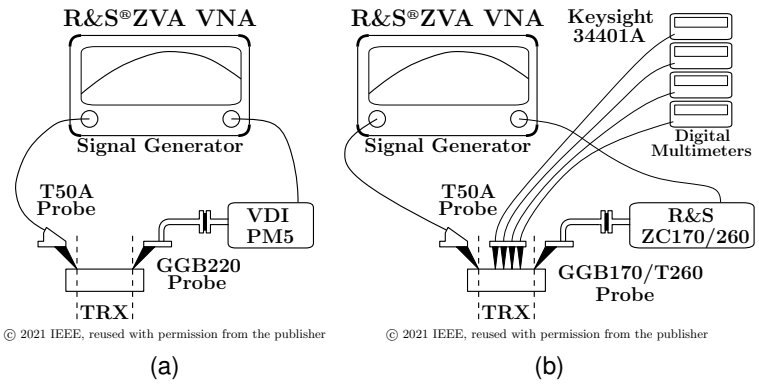


Figure 5.23: Large-signal measurement setup for (a) the TX and (b) the RX.[16]

gain does not exceed -10 dBi for both EH and HE combinations. A break-out circuit comprising antenna and a Marchand balun was fabricated for characterization. Fig. 5.22c presents measured input return loss and antenna gain for E- and H-planes versus frequency. S_{11} is below -10 dB in the 150-170 GHz range. Addition of LBE area under the radiator slightly improves the matching. The resonance at 120 GHz is due to balun and is visible in the simulation at 110 GHz. The antenna reaches 5 dBi peak gain at 175 GHz.

The transceivers have been measured using the setups depicted in Fig. 5.23. Dedicated TRX versions without antenna were fabricated to make TX/RX characterization feasible on wafer level. A PM5 power detector from VDI and R&S VNA as a Q-band LO signal source were employed to measure P_{TX} in the 140-200 GHz range (Fig. 5.23a). The same LO source was adopted for RX conversion gain (G_{RX}) measurements. Another VNA port was used to drive R&S ZC170/260 extension modules covering the 110-170 GHz and 170-260 GHz bands. The LO and RF signals were swept simultaneously with a constant frequency difference of 1 MHz (IF signal). Quadrature differential IF waveforms were measured for RMS voltage using digital multimeters. Finally, Fig. 5.24 presents P_{TX} measured at the probe-tip level and equivalent isotropic radiated power ($EIRP$) characterized using the complete radar board with on-chip antennas. The values are plotted versus frequency for both TRXs with marked 3-dB bandwidth. The monostatic variant generates 4 dBm output power at 169 GHz and more than 1 dBm in the 160-178 GHz range. The bistatic TRX outperforms this, reaching a maximum of 13 dBm and more than 10 dBm in the 150-182 GHz band owing to its wideband

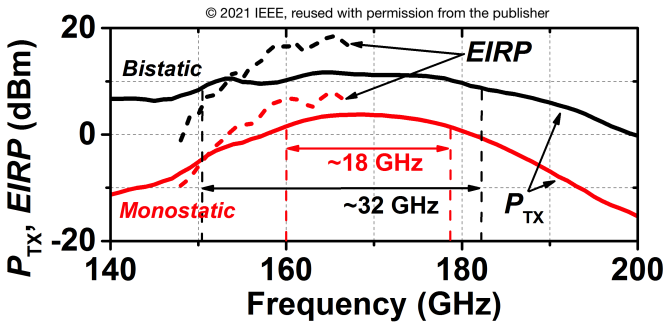


Figure 5.24: TX output power of the monostatic and bistatic TRXs measured on the probe-tip level and $EIRP$ inluding on-chip anntennas [16].

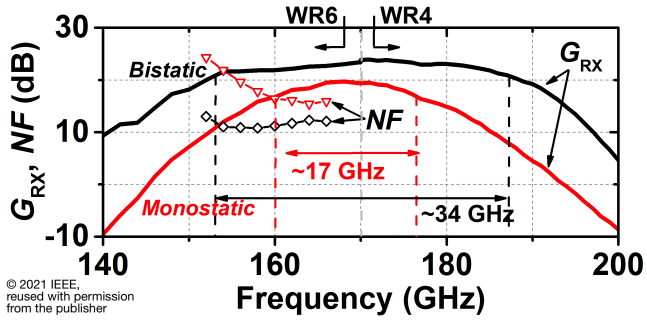


Figure 5.25: RX conversion gain of the monostatic and bistatic transceivers (solid) and RX noise figure (symbols) [16].

PA. Significantly larger P_{TX} for the bistatic TRX results from direct connection to the antenna and lack of lossy LC circuitry. Also, a larger output stage was also implemented with respect to the monostatic version. Maximum measured $EIRP$ is 8 dBm and 18 dBm at 0° angle which is larger than P_{TX} due to on-chip antenna gain at the cost of limited bandwidth. $EIRP$ characterization above 170 GHz was not possible due to a limited frequency range of the VCO implemented in the radar boards. The measured G_{RX} is shown in Fig. 5.25. The peak gain is 19 dB and 24 dB for monostatic and bistatic TRX, respectively. The 3-dB bandwidth of the bistatic TRX is effectively doubled (34 GHz) with respect to the monostatic TRX (17 GHz). A small discontinuity at 170 GHz occurs due to two slightly different setups used to cover frequencies below (WR6) and above 170 GHz (WR4). The noise figure (NF) was estimated using the radar boards. Due to lack of dedicated RF noise sources the gain method was applied. The minimum NF is 15.5 dB for the monostatic and 11 dB for the bistatic TRX. Fig. 5.26 presents G_{RX} versus P_{RF}

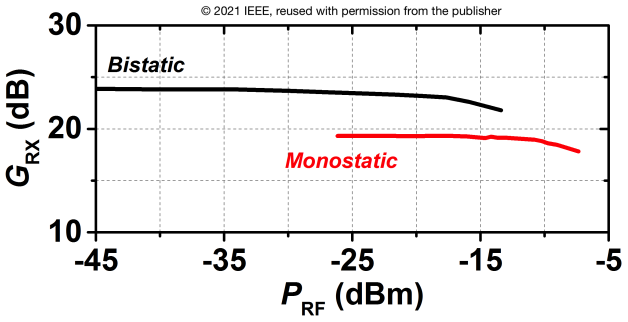


Figure 5.26: RX conversion gain of the monostatic and bistatic transceivers versus RF input power at 170 GHz [16].

at 170 GHz measured on-wafer. The RX compresses by 1 dB at -10 dBm and -18 dBm input power for the monostatic and bistatic case, respectively.

5.3.1 FMCW Radar Demonstrators

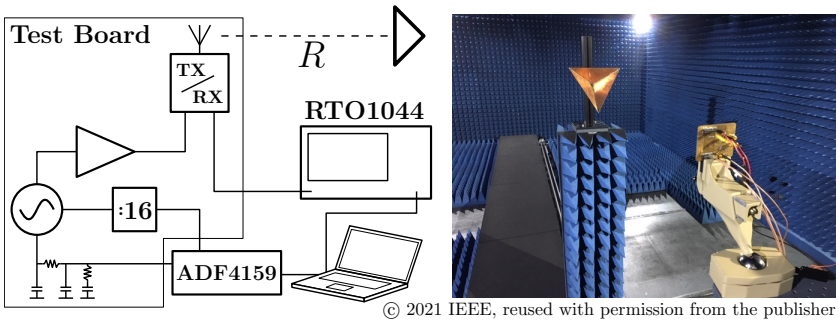


Figure 5.27: Range measurement setup using both TRXs with B_{SW}=20 GHz [16].

To evaluate the aforementioned radar transceivers, in particular the monostatic version with tunable leakage cancellation, an FMCW radar demonstrator was built. The same test board from the antenna charaterization setup was reused. Four quadrature differential IF outputs are connected to an RTO1044 digital oscilloscope used to store and transfer the data to the PC. A Matlab script was created to control each unit and calculate real-time FFT of the received signals. The setup was arranged in an anechoic chamber to reduce influence of clutter (Fig. 5.27). A corner reflector was placed at a programmable positioner for precise range measurements. The FMCW signal was generated using on-board

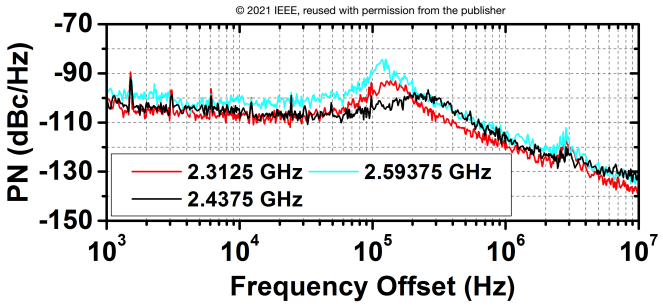


Figure 5.28: PLL phase noise measurement at the divider output for 37 GHz, 39 GHz and 41.5 GHz VCO frequency [16].

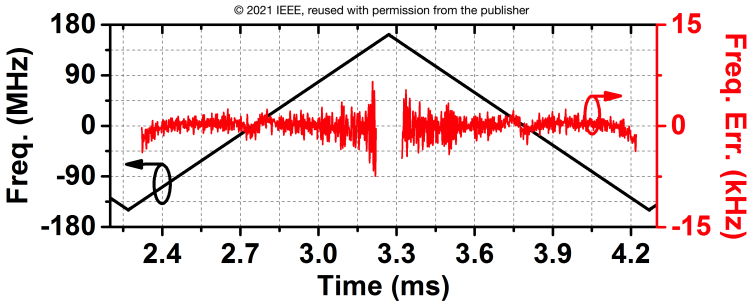


Figure 5.29: Measured frequency ramp at the divider output and corresponding instantaneous frequency error f_{err}. $\sigma_{f_{\mathrm{err}}}$ is 1.22 kHz which scales up to 19.52 kHz at 39.5 GHz and 78.08 kHz at 158 GHz, respectively. The FMCW output signal bandwidth is 20 GHz. [16]

components (VCO with frequency divider, LF) and an EVAL-ADF4159 evaluation board comprising a PLL. The VCO signal is scaled down to the 2.3-2.6 GHz band using four divide-by-two circuits (DTC). It is used to drive the PLL and also serves for phase noise (PN) and frequency ramp measurements. Fig. 5.28 presents the PLL PN results in integer-N mode. The plots were recorded at three frequencies located at the center and both boundaries of the VCO tuning range. The loop bandwidth changes due to a varying VCO gain (K_{VCO}) reaching its maximum at the center frequency of 39.5 GHz. The in-band PN at the divider output varies from -108 dBc to -102 dBc. The worst case out-of-band PN at 1 MHz frequency offset is -115 dBc. Fig. 5.29 shows a measured triangular frequency ramp at the divider output and the corresponding instantaneous frequency error. The sweep bandwidth (B_{SW}) is 312.5 MHz which scales up to 20 GHz at the radar TRX output. Standard deviation of the frequency error calculated for the middle 90% of

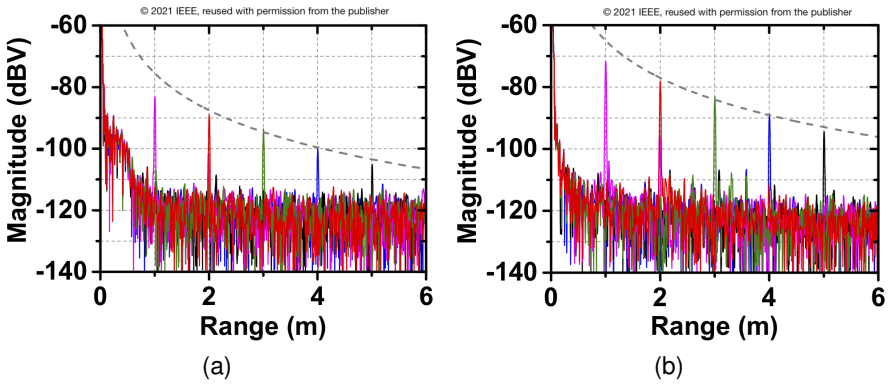


Figure 5.30: Range measurement using (a) monostatic and (b) bistatic TRX.[16]

the ramp duration is 1.22 kHz at the divider output and 78.08 kHz at the TRX output, respectively. Fig. 5.30 presents range measurements for both transceivers performed for the target placed 1 m to 5 m from the sensor using an automatically adjusted positioner. Radar measurement is performed using a simple MATLAB script. Once the ramp is generated, the ADF4159 outputs a signal that triggers the oscilloscope. Knowing the ramp duration, the settings of the oscilloscope are adjusted to capture IF signals from one UP sweep. The saved time window is trimmed by excluding 5% at the beginning and at the end of the sweep, respectively, to eliminate the effect of settling and thus increased ramp nonlinearity. The time data is then converted to frequency via an FFT and scaled to distance using (2.20) and (2.11). The following FMCW parameters were applied: $B_{\mathrm{SW}} = 20$ GHz, $T_{\mathrm{SW}} = 1$ ms. Strong and narrow IF peaks are visible at the correct positions of the target with amplitude following the radar equation (dashed line) given by (2.12). As expected, the received signals are stronger in case of a bistatic TRX. Also, the low-frequency noise as well as the peak at zero occurring due to TX-to-RX leakage is more severe for monostatic TRX. Fig. 5.31 compares both transceivers with respect to ranging precision. A set of 1000 measurements was performed and a ranging standard deviation (σ_{R}) was calculated at each target distance. As expected, σ_{R} increases with distance due to reduced SNR. For that reason the monostatic TRX exhibits around 10 times worse ranging precision compared to the bistatic version which reaches 13 µm at 2 m. Fig. 5.32 presents the radar response for a target at 1 m distance using bistatic and monostatic TRX with enabled/disabled LC. The DC offset occuring due to TX-RX leakage is the smallest

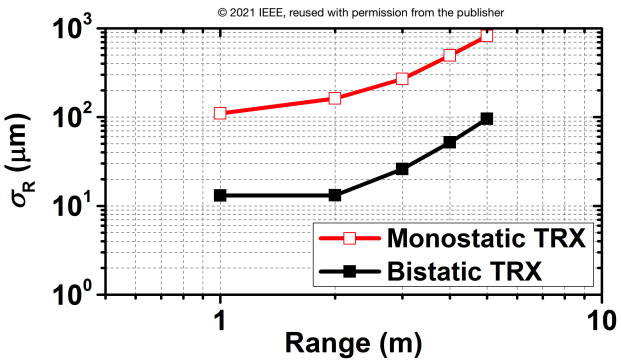


Figure 5.31: Ranging precision of the monostatic and bistatic TRX [16].

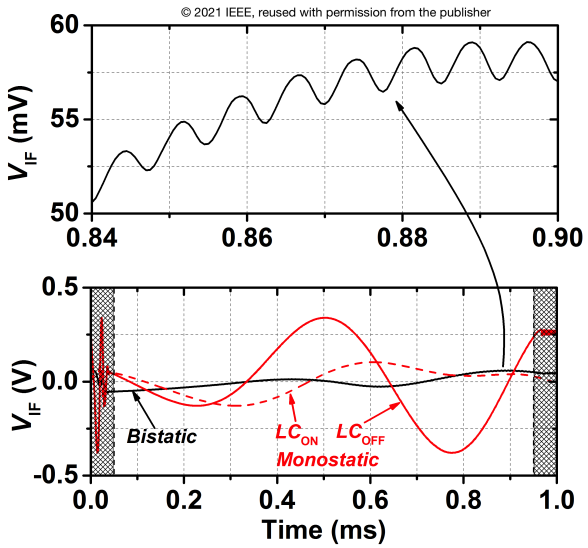


Figure 5.32: Radar response for a target at 1 m distance using bistatic and monostatic TRX with enabled/disabled LC. The bistatic TRX response is shown in detail. Shaded regions are not post-processed [16].

for the bistatic case. Also, LC activation reduces the DC offset in the monostatic TRX. Shaded areas show settling of the ramp and are not post-processed since they would significantly deteriorate the spectrum.

In order to evaluate the leakage cancellation feature implemented in the monostatic TRX a setup with three CC reflectors was prepared. Two big CCs were placed at 1.9 and 2 m from the sensor while a small CC was positioned at 0.7 m to act as a weakly reflective nearby object. Fig. 5.33a presents two consecutive radar measurements depicting leakage cancellation. The first plot (green) was

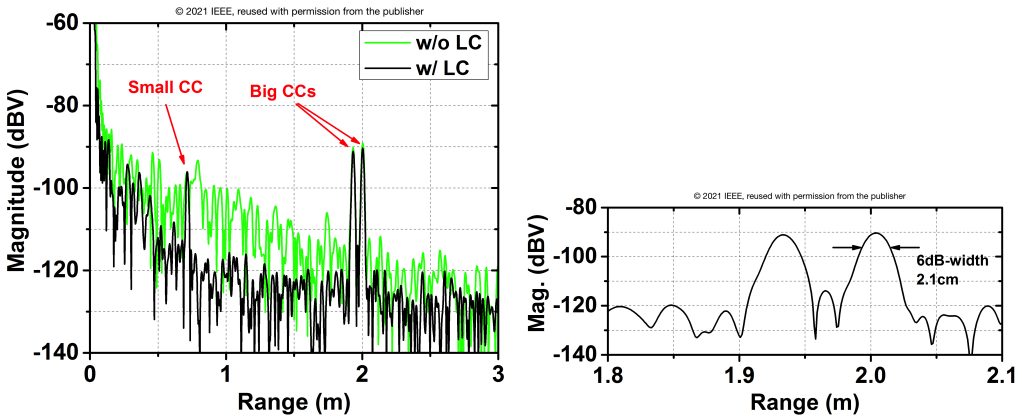


Figure 5.33: (a) Range measurement using the monostatic TRX operating in LC OFF (green) and LC OFF (black) mode ($B_{\mathrm{SW}} = 20\,\mathrm{GHz}$, $T_{\mathrm{SW}} = 1\,\mathrm{ms}$). (b) Detailed spectrum showing the effective ΔR of 2.1 cm.[16]

recorded with disactivated LC network. Once the canceller was enabled, the gain and the phase was manually adjusted in order to reduce DC offset visible on the oscilloscope. Note that noise level is significantly elevated compared to the case with enabled LC (black). Furthermore, it is impossible to detect the closely located target since it is completely hidden in the noise. LC activation effectively attenuates the leakage and shifts the noise floor lower uncovering the response from the small CC. The strong peaks resulting from two big CCs are clearly visible and separable due to high resolution guaranteed by large sweep bandwidth. Notably, noise reduction is negligible at distances above 3 m, which corresponds to an IF of 400 kHz. This is expected since the noise cancellation weakens for larger frequency offsets. Fig. 5.33b presents the spectrum in detail with marked 6-dB width of the main lobe which corresponds to 2.1 cm range resolution. This is 2.8x larger than expected from the ideal sweep bandwidth (0.75 cm) due to non-flat output power over the bandwidth and a Hann window function applied in post-processing. The latter factor reduces the range resolution by 65 %. Also, no additional calibration for other parasitic effects was performed which could possibly improve the resolution.

The performance of monostatic and bistatic TRX characterized on probe-tip level as well as using the complete radar board is summarized in Table 5.1. The monostatic version achieves state-of-the-art performance offering enhanced leakage

attenuation which improves detectability of weakly reflecting near objects. It provides 3 dBm peak radiated P_{out} and 19 dB peak G_{RX} with -10 dBm input referred 1-dB compression point. The bistatic TRX reaches remarkable bandwidth of more than 30 GHz and outstanding peak output power of 11 dBm compared to the state-of-the-art. It provides 24 dB peak G_{RX} and excellent NF of 11 dB. Incorporation of the bistatic TRX in a FMCW radar demonstrated an exceptional ranging precision of 13 µm without focusing lenses. Choosing the compact monostatic version featuring leakage cancellation imposes trade-offs that lead to performance degradation with respect to the bistatic TRX. However, this might be acceptable if the chip compactness is of priority.

Table 5.1: Summary of state-of-the-art Si D-band and G-band radar TRXs [16].

Ref.	Proc.	Rad. type	# TX/ # RX	Freq. (GHz)	PN^a (dBc/Hz) @ 10 M	P_{TX} (dBm)	G_{RX} (dB)	NF (dB)	RX $IP_{1\mathrm{dB}}$ (dBm)	Mod. BW (GHz)	ΔR (cm)	σ_{R} (µm)	P_{DC} (W)	Chip area (mm^2)	Ant. type	G_{ant} (dBi)
[68]	SiGe 130nm	M	1/1	122	-120	3.6^{l}	13	11.5	-20	-	-	-	0.90	5.72	on-chip	6
[121]	SiGe 130nm	B	1/1	140	-100	5	19.5	13.5	-23	-	-	-	0.72	1.16	off-chip	-
[122]	SiGe 130nm	M	1/1	148	-	-12	15.5	10.5	1	-	-	-	0.8	5.98	off-chip	-
[125]	SiGe 180nm	B*	1/1^{b}	160	-	1	-	17^{e}	-4^{e}	3	5	-	0.75	7.48	AiP	-
[123]	SiGe 130nm	B*	1/1^{b}	130	-	5^{l}	5^{e}	11^{e}	-	20	-	-	0.38	1.32	on-chip	0.7
[126]	CMOS 65nm	B	4/4	160	-101	4^{l,m}	29.3	22.5	-14	7	-	-	2.2	20	AiP	8.8
[69]	SiGe 180nm	M	1/1	146	-104	-1^{l}	8.3^{e}	19.3^{e}	-2.9^{e}	48	0.59	0.29^{j}	0.65	3.86	off-chip	20
[129]	SiGe 130nm	B*	1/1	125	-	3.2^{l}	15.5^{e}	9.5^{e}	-	30	0.71	-	0.77	3.11	on-chip	4
[134]	SiGe 130nm	B*	1/1	122	-	2.7^{l}	15^{l}	-	-	6	-	-	0.54	3.6	AiP	11
[79]	SiGe 130nm	M*	1/1	240	-106	5	12.1	21.1	-9	60	0.26	-	1.6	3.19	on-chip	26.6
[120]	SiGe 130nm	B*	1/1	131	-	11	15	8^{e}	-7.5	-	-	-	0.82	3.86	off-chip	-
[119]	SiGe 130nm	B*	1/1	122	-98	5^{l}	21^{l}	12.7^{e}	-11^{l}	10	3	52.5^{i}	0.63	10.14	on-chip	6
[127]	SiGe 130nm	B	1/1	156	-112	5^{l}	-1	12	-	16	0.97	4.2^{i}	0.36	2	on-chip	6+36^{c}
[71]	SiGe 130nm	M	1/1	154	-95	3	2	20	-	7	-	-	-	1.9	on-chip	-
[130]	SiGe 55nm	B	1/1	221	-78	-4.6^{d}	-	-	-	62	0.27	-	0.08	0.51	on-chip	-
[135]	CMOS 28nm	B*	1/1	145	-	11.5	80	8	-	-	1.1	-	0.5	6.56	on-chip	2.5
[136]	SiGe 130nm	B	1/1	224	-100	1.8	16.8^{e}	13.9^{e}	-3.9^{e}	52	0.3	3.3^{g,k}	3.5^{h}	5.33^{f}	on-chip	2+35^{c}
This work	**SiGe 130nm**	**M***	**1/1**	**169**	**-100**	**3**^{d}	**19**^{l}	**15.5**	**-10**^{l}	**20**	**2.1**	**105**^{i}	**0.86 (0.76)**	**5.40**	**on-chip**	**5**
This work	**SiGe 130nm**	**B***	**1/1**	**168**	**-100**	**13**^{d}	**24**^{l}	**11**	**-18**^{l}	**20**	**2.1**	**13**^{i}	**1.05**	**8.40**	**on-chip**	**5**

* ext. LO, ^{a} worst case, ^{b} sep. TX/RX chips, ^{c} w/ lens, ^{d} radiated P_{out}, ^{e} sim., ^{f} graphically est., ^{g} accuracy, ^{h} complete sensor, ^{i} at 1 m, ^{j} at 0.5 m, ^{k} at 0.2 m, ^{l} at probe-tip level, ^{m} single TX

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6 Conclusion and Future Work

In this thesis, fundamentals related to semiconductor technology and radar techniques used in this work were presented. Careful study was dedicated to the key components of a radar front-end, namely efficient frequency multipliers and power amplifiers as well as leakage cancellation circuitry. Two frequency quadrupling techniques were proposed and implemented. The one based on stacked bootstrapped Gilbert-cells was successfully used in G-band transceivers. It operates in an exceptionally wide bandwidth providing a high output power and conversion gain. The FQ based on an IL oscillator presents an alternative approach enabling phase shifting and very low input power operation unreachable using the conventional techniques. Two state-of-the-art power combiners for E-band and G-band, respectively, were designed. The E-band power amplifier was directly applied in the bistatic E-band transceiver. Both PAs provide an outstanding output power reaching the limit of the SiGe technology at high efficiency. Finally, TX-to-RX leakage was studied and a cancellation technique was proposed and embedded in both E-band and G-band monostatic transceivers. Consequently, monostatic and bistatic E-band and G-band radar front-ends able to support scalable radar systems were designed and fabricated. The functionality of the TRXs was validated in FMCW radar demonstrators. A leakage cancellation technique was used in the monostatic versions improving the performance in terms of ranging precision. The suppression of the TX-to-RX leakage efficiently reduced the noise improving the SNR for weakly reflecting close-in targets. The bistatic TRX versions provide high-performance in terms of output power and bandwidth resulting in remarkable dynamic range and range resolution without the use of high-gain radiators. In case of the E-band bistatic TRX, a two-channel radar platform using a custom fractional-N PLL was built showing its utilization in a two-dimensional sensing system.

Overall, this work was dedicated to the research of mm-wave radar front-ends to be used in a scalable system that provides a significant flexibility and optimization level with respect to the intended application. It was shown that scalability both in number of TRX units as well as in operating frequency is beneficial in terms of the key sensor parameters. Operating in lower frequency bands results in a higher SNR ratio and, thus, in an increased maximum range and sensitivity. Using higher frequency ranges, in turn, provides an enhanced range resolution. A proper choice of TRX number seems particularly interesting as various features can be implemented, such as digital beamforming with high angular resolution, polarization-sensitive detection or three-dimensional radar scanning.

In the future, the presented circuits will be the key components used in a complete scalable radar system operating in multiple frequency bands and entailing several TRX units to enable multi-dimensional sensing. In case of the monostatic TRX, further improvements shall be pursued including automatic calibration and adaptive TX-to-RX leakage cancellation. The latter feature seems particularly prospective in an FMCW radar. A synchronous TX-to-RX leakage canceller tracking the instantaneous frequency of the transmitted FMCW signal could theoretically provide a perfect leakage compensation.

List of Acronyms and Symbols

ACC	adaptive cruise control
ADC	analog-to-digital converter
ADS	Advanced Design System
AiP	antenna-in-package
AM	amplitude modulation
ANT	antenna
ASIC	application-specific integrated circuit
AWGN	additive white Gaussian noise
BC	base-collector
BEOL	back-end-of-line
BE	base-emitter
BiCMOS	bipolar complementary metal-oxide-semiconductor
BJT	bipolar junction transistor
BPF	bandpass filter
BPSK	binary phase-shift keying
BSD	blind-spot detection
B	base/bulk
CB	common-base
CC	corner cube
CE	collector-emitter/common-emitter
CMOS	complementary metal-oxide-semiconductor
CMRR	common-mode rejection ratio
CP	charge pump/compression point

CS	collector-substrate
CTA	cross traffic alert
CW	continuous-wave
C	collector
DAC	digital-to-analog converter
DAT	distributed active transformer
DC	direct current
DFT	discrete Fourier transform
DIV	divider
DSP	digital signal processor
DS	drain-source
DTC	divide-by-two circuit
DUT	device under test
D	drain/driver
EM	electromagnetic
ETSI	European Telecommunication Standards Institute
E	emitter
FCC	Federal Communications Commission
FFT	fast Fourier transform
FMCW	frequency-modulated continuous-wave
FM	frequency modulation
FPGA	field programmable gate array
FQ	frequency quadrupler
GaAs	gallium-arsenide
GaN	gallium-nitride
GB	gate-bulk
GC	Gilbert-cell
GD	gate-drain
GSG	ground-signal-ground
GS	gate-source
G	gate
HBT	hetero-junction bipolar transistor

HPF	high-pass filter
I/Q	in-phase/quadrature
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
ILFQ	injection-locked frequency quadrupler
ILFT	injection-locked frequency tripler
ILO	injection-locked oscillator
IMN	input matching network
InP	indium-phosphide
ISM	industrial scientific medical
ITU	International Telecommunications Union
LBE	localized backside etching
LC	leakage cancellation
LDMOS	double-diffused MOSFET
LFM	linear frequency modulation
LF	loop filter
LNA	low-noise amplifier
LO	local oscillator
LPF	low-pass filter
LRR	long-range radar
LUT	look-up table
MIMO	multiple input multiple output
MIM	metal-insulator-metal
MMD	multi-modulus divider
mm	millimetre
MOSFET	metal-oxide-semiconductor field-effect transistor
MOS	metal-oxide-semiconductor
MRR	mid-range radar
nMOS	n-type metal-oxide semiconductor
OMN	output matching network
OS	output stage

PA	power amplifier
PCB	printed circuit board
PFD	phase/frequency detector
PIC	photonic integrated circuit
PLL	phase-locked loop
pMOS	p-type metal-oxide semiconductor
PM	phase modulation
PP	push-push
PRBS	pseudo-random binary sequence
PVT	process,voltage and temperature
RBW	resolution bandwidth
RF	radio frequency
RHIGH	unsilicided, partially compensated gate polysilicon resistor
RMS	root mean square
RPPD	unsilicided, p-doped gate polysilicon resistor
RSIL	silicided, n-doped gate polysilicon resistor
RX	receiver
S&G	stop and go
SA	spectrum analyzer
SDM	$\Sigma\Delta$-modulator
SIC	selectively-implanted collector
SiGe:C	silicon-germanium carbon
SiGe	silicon-germanium
SiO_2	silicon dioxide
SiP	system-in-package
Si	silicon
SMD	surface-mount device
SOA	safe operation area
SoC	system-on-chip
SPI	serial peripheral interface
SRR	short-range radar
SSA	signal source analyzer

S	source
T-ILFQ	transformer-based injection-locked frequency quadrupler
TF	transformer
TL	transmission line
TRX	transceiver
TSV	through-silicon via
TX	transmitter
USB	universal serial bus
V2V	vehicle-to-vehicle
VCO	voltage-controlled oscillator
VDI	Virginia Diodes Inc.
VLSI	very large-scale integration
VM	vector modulator
VNA	vector network analyzer
WG	waveform generator

Symbols

α_τ	damping factor
β_F	common-emitter current gain
ΔE_g	band gap
ΔR	range resolution
ϵ_r	relative permittivity
η	drain/collector efficiency
Γ	reflection coefficient
λ	signal wavelength/channel-length modulation parameter in MOSFET
μ_1, μ_2	stability factors
μ_n	electron mobility
μ_p	hole mobility
ω	angular frequency
Ψ	CG boosting factor defined as $(g_\mathrm{m} Z_0)^2$ in bootstrapped frequency doubler
ρ	resistivity

σ	standard deviation/radar cross section
σ_{R}	ranging precision
τ_0	round trip delay time
τ_{F}	base transit time
θ	phase shift
φ, ϕ	signal phase
A	amplitude
B, BW	bandwidth
B_{SW}	sweep bandwidth
BV	breakdown voltage
BV_{CB0}	collector-base breakdown voltage
BV_{CE0}	collector-emitter breakdown voltage
C	capacitance value
c_0	speed of light in vacuum
C_{LC}	leakage cancellation
C_{RX}	coupling factor of the directional coupler in the RX
C_{TX}	coupling factor of the directional coupler in the TX
CG	conversion gain
D_{n}	diffusion constant for electrones
D_{p}	diffusion constant for holes
$EIRP$	equivalent isotropic radiated power
f_0	start frequency
f_{c}	center frequency
f_{d}	Doppler frequency
f_{IF}	intermediate frequency
f_{MAX}	maximum frequency
f_{m}	frequency offset
f_{RX}	received signal frequency
f_{TX}	transmitted signal frequency
f_{T}	transit frequency
FOM_{T}	figure of merit including VCO tuning range
G	gain

G_{ant}	antenna gain
g_{m}	small-signal transconductance
G_{VM}	vector modulator gain
HRR	harmonic rejection ratio
I	current
i	small-signal current
I_{S}	saturation current
$I_{\mathrm{TX-RX}}$	Wilkinson splitter isolation between TX and RX ports
IP_{1dB}	input-referred compression point
J	current density
j	imaginary unit
k	frequency ramp slope
k_{B}	Boltzmann constant
L	inductance value/channel length of MOSFET
L_{E}	emitter length
L_{p}	diffusion length for holes
L_{RX}	insertion loss of the directional coupler in the RX
L_{TX}	insertion loss of the directional coupler in the TX
MAG	maximum available gain
N	division ratio/data size
N_{A}	acceptor concentration
N_{D}	donor concentration
n_{i}	intrinsic carrier concentration
NF	noise figure
O	computing complexity
P	power
P_{1dB}	output power at 1 dB gain compression
P_{C}	carrier power
P_{max}	maximum output power
P_{N}	noise power level
P_{sat}	saturated output power
PAE	power-added efficiency

PN	phase noise
PRI	pulse repetition interval
Q	quality factor
q	elementary charge
R	resistance value/range
R_{B}	base resistance
R_{n}	noise auto-correlation function
RCS	radar cross section
s_{comp}	compansation signal
s_{leak}	leakage signal
s_{LO}	LO signal
s_{RX}	received signal
s_{TX}	transmitted signal
SNR	signal-to-noise ratio
SRF	self-resonance frequency
T_{SW}	sweep time
TR	tuning range
V	voltage
v	object velocity/small-signal voltage
V_{A}	Early voltage
V_{ov}	overdrive voltage in MOSFET
V_{th}	threshold voltage
V_{T}	thermal voltage
V_{t}	tuning voltage
W	channel width of MOSFET
W_{B}	base width
X	reactance/cross-correlation
Y	admittance
Z	impedance
Z_0	characteristic impedance
Z_{ext}	external impedance
Z_{opt}	optimum impedance

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Teile dieser Dissertation wurden bereits in folgenden Fachartikeln veröffentlicht:

- M. Kucharski, A. Malignaggi, D. Kissinger, and H. J. Ng, “A wideband 129–171 GHz frequency quadrupler using a stacked bootstrapped Gilbert cell in 0.13 µm SiGe BiCMOS,” in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 158–161.
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Der Lebenslauf wurde aus Gründen des Datenschutzes entfernt.

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