

ulm university universität
uulm

High-Linearity Receivers for Mobile Communication Applications using SiGe Technology

DISSERTATION

Zur Erlangung des akademischen Grades eines

DOKTOR-INGENIEURS (DR.-ING.)

der Fakultät für Ingenieurwissenschaften
und Informatik der Universität Ulm

von

Frank Gruson
aus Heidenheim

1. Gutachter:	Prof. Dr.-Ing. Hermann Schumacher
2. Gutachter:	Prof. Dr.-Ing. Joachim Burghartz
Amtierender Dekan:	Prof. Dr.-Ing. Michael Weber

Ulm, 10.06.2010

Applying the calculus concept of limits,
the specialist gets to know more and more
about less and less until, in the limit,
he retires, knowing everything about nothing.
The generalist learns less and less
about more and more until, in the limit,
he retires, knowing nothing about everything.
Neither is quite the ideal life.

Lawrence J. Kamm

Contents

1 Introduction **1**

2 Introduction to mobile communication systems **2**

2.1 Digital modulation and the need for linear receive front-ends 2

2.2 Mobile phone standards 5

2.2.1 The evolution of mobile communications 5

2.2.2 CDMA 5

2.2.3 Narrow-band CDMA 6

2.2.4 Wide band CDMA (UMTS) 7

2.3 Professional mobile radio systems 10

2.4 Wireless Local Area Networks 11

2.5 Global Positioning Systems 14

3 System considerations and level planning **16**

3.1 Intermodulation distortion 18

3.1.1 Derivation of LNA IIP_3 requirements 22

3.1.2 Derivation of receiver NF requirements 24

4 Device technology **26**

4.1 Technology selection criteria 26

4.2 SiGe1 and SiGe2 bipolar processes 26

4.3 SiGe1 model verification 27

4.4 at46000 SiGe BiCMOS process 31

4.5 Atmel's at46000 0.35μm CMOS technology 32

4.6 Packaging 34

5 Modelling of passive components **36**

5.1 Passive components on Silicon substrates 36

5.2 Lumped element circuit design 36

5.3 Loss mechanisms of passive components on silicon 37

5.4 Spiral inductors in the Atmel SiGe1 and SiGe2 processes 38

5.5 Equivalent circuit extraction 41

5.6 Definition of the 'quality factor' . . . 44
5.7 The choice of the metal layers . . . 46
5.8 Influence of the via geometry . . . 47
5.9 Inductors on high resistivity substrates . . . 48
5.10 The channel stopper . . . 49
5.11 Influence of the substrate . . . 50
5.12 Improving Q factor and reducing crosstalk by patterned ground shields . . . 52
5.13 Electromagnetic field simulation . . . 55
5.13.1 2.5D simulators based on the method of moments . . . 55
5.13.2 Why a planar inductor is not a two-dimensional structure . . . 56
5.13.3 Sensitivity of the EM simulation . . . 60
5.13.4 Comparison of 2.5D and 3D EM simulators . . . 61
5.14 Analysis of process spreads . . . 62
5.15 Modelling . . . 64
5.16 Multilevel spiral inductors . . . 70
5.17 Symmetrical, centre-tapped inductors . . . 70

6 The low noise amplifier 75
6.1 Harold Black and the negative feedback amplifier . . . 75
6.2 Broadband LNA designs . . . 75
6.2.1 Transimpedance amplifier . . . 75
6.2.2 Darlington circuits . . . 79
6.2.3 Transformer based LNAs . . . 81
6.3 Simultaneous noise and power match in narrowband LNAs . . . 82
6.3.1 Application to CMOS LNAs . . . 88
6.4 Bias considerations . . . 88
6.5 The influence of bias conditions on linearity . . . 93
6.6 Effect of series and parallel feedback on noise figure and linearity . . . 95
6.7 Linearity considerations for bipolar transistors . . . 96
6.7.1 Analytical considerations . . . 96
6.7.2 Linearisation by series feedback . . . 98
6.8 LNA circuit implementations . . . 102
6.8.1 Influence of bias resistor . . . 102

6.8.2 Broadband source termination . . . 102
6.8.3 Low frequency termination using LC trap networks . . . 103
6.8.4 Low frequency termination using bias inductors and a diode . . . 105
6.8.5 Low frequency termination using active bias networks . . . 112
6.8.6 CMOS LNA implementations . . . 116
6.8.7 Cancellation by capacitive feedback in narrow band amplifiers . . . 118
6.8.8 Matching networks with notch filters . . . 121
6.8.9 Comparison of the circuit design techniques for linearization enhancement . . . 125

7 The downconverter 131
7.1 Super-hetero and direct-conversion receivers . . . 131
7.2 Mixing operation . . . 132
7.3 Mixers utilising device nonlinearities . . . 133
7.4 Switching mixers . . . 133
7.5 Commutating mixers . . . 136
7.5.1 Passive commutating mixer using Schottky Diodes . . . 137
7.5.2 Passive commutating mixer using FET (NMOS) transistors . . . 139
7.6 The Gilbert mixer: An active, commutating mixer . . . 140
7.7 Image rejection mixers . . . 142
7.8 Mixer summary and conclusions . . . 147

8 Conclusion 149

A Noise figure measurements 152
A.1 General considerations . . . 152
A.2 The Gain Method . . . 152
A.3 The Y Factor Method . . . 153
A.4 Improving measurement accuracy by a low-noise preamplifier . . . 157
A.5 Example . . . 160

B Measuring intermodulation distortion products 162
B.1 Combining the sources . . . 162
B.2 Setting up the spectrum analyser . . . 163
B.3 Using a frequency translating vector network analyser . . . 163

C On-wafer characterisation of inductors - the measurement challenge **165**

C.1 Getting the right contact 165

C.2 Influence of the coaxial calibration technique 165

C.3 Pad removal techniques (de-embedding) 167

C.4 Wafer level calibration as an alternative to de-embedding 170

C.5 Choosing the right technique 173

C.6 On-wafer characterisation of 3-ports 173

D Details about the SiGe processes **175**

E Detailed schematics and benchmarks **176**

F Dimensioning spiral inductors **186**

G Glossary of terms **189**

H List of symbols **193**

References **195**

1 Introduction

Modern mobile communication systems shaped the semiconductor industry during the last decade: The demand for lower cost and higher speed at reduced power consumption and increased functionality has been a key driver for CMOS technology scaling and even at today's gate geometries of 45 nm Moore's law continues to go on. Alternative technologies like Silicon-Germanium Heterobipolar (SiGe HBT) technology displaced established receiver architectures based on discrete semiconductors and III-V electronics into the niche of power-amplifiers and antenna switch modules – before SiGe HBT finally will be displaced by RF CMOS to higher-frequency applications like automotive radar.
This thesis applied a wide range of available circuit design techniques to realize very linear receivers with low noise figure to satisfy the system needs of applications like UMTS, CDMA, GPS, TETRA and WLAN. Circuits have been realized that show comparable or better linearity and noise performance than implementations using discrete or III-V technology. As the author of this thesis escorted SiGe technology from early infancy in the clean rooms of the Daimler research labs via the production transfer to Temic (later renamed Atmel, now TELEFUNKEN Semiconductors [1]) – where he was part of the team that developed the first commercially available SiGe frontend circuit – a big part of this work is dedicated to device modelling. This is essential, as only accurate models enable the trend to first-time right designs with optimum performance. At Ulm University he joined forces with a team that innovated MMIC design at frequencies up to 24 GHz using commercially available SiGe HBT production lines from Atmel [2].
A good circuit needs to fulfil the requirements of the system, rather than the system coping with the limitations of the circuit. Therefore chapter 2 shortly explains the mobile communications systems used in this thesis and derives the system requirements for the receivers to be realized in chapter 3. The common demand of all these systems is: (i) High linearity (ii) Low power consumption and (iii) Low noise figure. While SiGe HBT technology allows for the realisation of low-noise, low-power RF circuits, high linearity typically is achieved by high operating currents. Therefore circuit design techniques were necessary to satisfy the linearity needs without the use of excessive current. Chapter 4 briefly compares the different technologies used, including an experimental verification of the active device models in the design kit. This is then followed in chapter 5 by an extensive measurement and modelling campaign to remove the deficiency of the passive device models in the design kit: After improving both the accuracy of the on-wafer measurements (see appendix C) and the quality of the electro-magnetic field simulations, both techniques have been merged to derive a set of scaleable inductor models, greatly facilitating RF circuit design at RF frequencies. Chapter 6 is dedicated to the low-noise amplifier (LNA) and uses circuit design techniques to optimise linearity at a minimum of noise and current consumption, followed by extensive benchmarking. Mixer designs are evaluated in chapter 7, identifying *different* mixer types to optimally serve the requirements of *different* systems. The thesis ends up with a conclusion and gives an outlook where further studies might be directed to.

2 Introduction to mobile communication systems

2.1 Digital modulation and the need for linear receive front-ends

The move from analog phone systems like NMT (Nordic Mobile Telephone) and AMPS (Advanced Mobile Phone System) with AM or FM modulation to digital standards like GSM and UMTS using digital modulation techniques provides more information capacity, compatibility with digital data services, higher data security and better quality communications. The RF spectrum must be shared, yet every day there are more users for the available spectrum as the demand for communications services increases. Digital modulation schemes have greater capacity than analog modulation schemes to convey large amounts of information. There is a fundamental trade off in communications systems: Simple hardware can be used in transmitter and receivers to communicate information. However, this uses a large amount of spectrum which limits the number of users or the available data rates. Pagers, for example, use simple digital modulation algorithms like 2-level FSK or BPSK (see Fig. 1) which can be demodulated even deep inside modern steel/concrete buildings. Alternatively, more complex transmitters and receivers can be used to transmit the same information over less bandwidth. This transition to more and more spectrally efficient transmission techniques requires more and more complex hardware. Complex hardware is difficult to design, test, and build due to more demanding specifications. [3]. They key specifications which need to be met in a complex receiver are noise figure, linearity and power consumption.

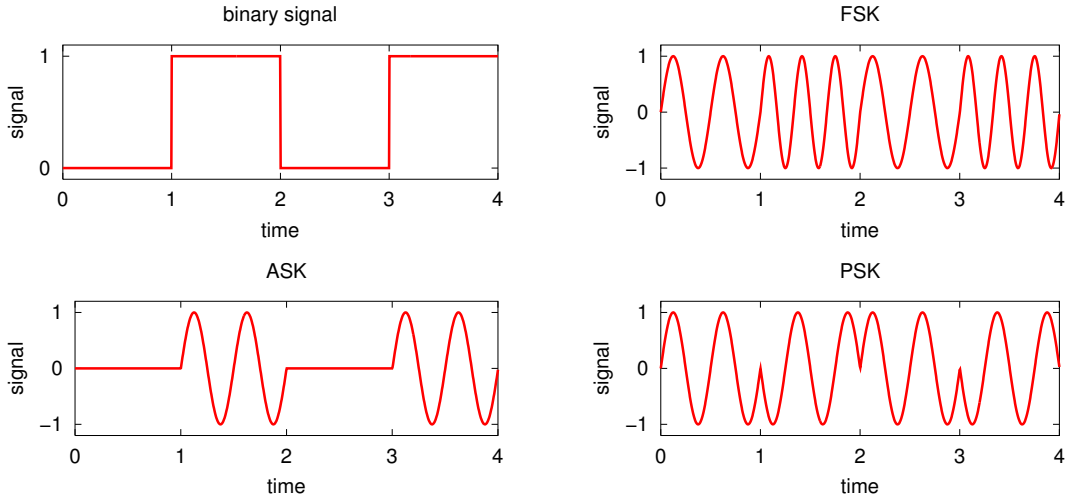


Figure 1: Digital bit stream (top left) encoded with simple modulation formats like Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK) and Phase Shift Keying (PSK).

A symbol is defined as a state in the polar IQ plane at a given time (see Fig. 2). The signal bandwidth for the communications channel depends on this symbol rate. BPSK (Bi-Phase Shift Keying) has got 2 states (0 or 180°) corresponding to just one bit of information ('0' or '1'). Here the bit rate just equals the symbol rate, but the states can be distinguished ('demodulated') easily. This is important for spread-spectrum satellite-based systems like GPS due to the high attenuation between the transmitter in the satellite and the terrestrial receiver and the fact that the signal level is below the thermal noise floor. Due to the low bit rate of BPSK, it takes around 35 seconds even with a good sky view until the GPS receiver has all the necessary information to calculate a valid position[1]. A low receiver noise figure is important to acquire the weak GPS signals, while linearity is not important for stand-alone GPS receivers. However, as most GPS receivers need to work close to mobile phones that transmit with power levels that are up to 10^{17} times stronger than the weak GPS signals at an offset of just 200 MHz, linearity becomes important for GPS receivers, too. The GPS system is sketched in section 2.5 and the low-noise preamplifier developed in this thesis in chapter 6.8.8.

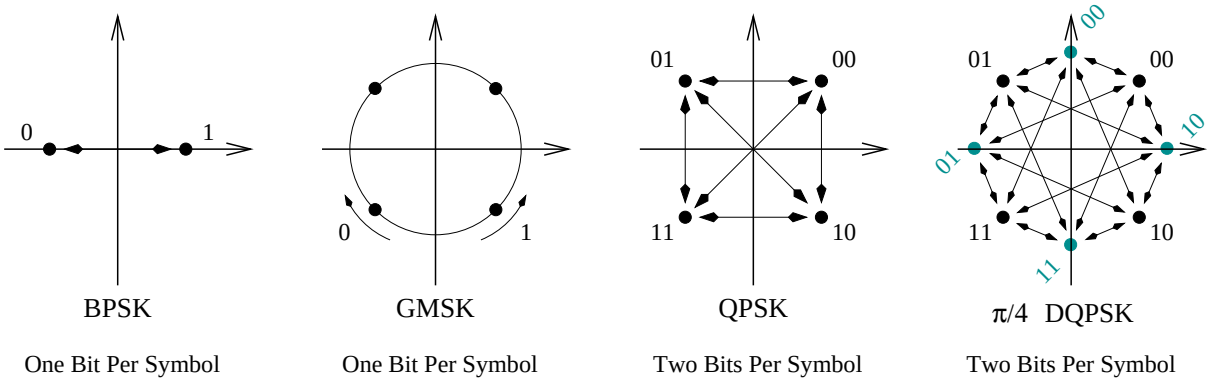


Figure 2: Digital modulation formats of the systems covered in this thesis shown in a constellation diagram.

In FSK, the frequency of the carrier is changed between two values as a function of the modulating signal (data) being transmitted. For Minimum (frequency) Shift Keying, MSK, the difference between these two frequencies is chosen to be half the data rate, with the result that the modulated carrier contains no phase discontinuities and frequency changes occur at the carrier zero crossings (see Fig. 1, top right) [4]. Thus, a static frequency shift translates into a linearly varying phase shift. This leads to a vector rotating either clockwise or counterclockwise, the absolute states in the constellation diagram being irrelevant. A long series of binary ones would result in a series of positive, counter-clockwise transitions, a long series of binary zeros in a series negative, clockwise transitions (see Fig. 2). As MSK is not spectrally efficient, the data stream is filtered

[1] To speed that up, satellite information can be transmitted via a cellular network with a higher data rate, so that only code and timing synchronisation need to be aligned via the slow satellite link (assisted GPS, A-GPS).

using a Gaussian filter, a pre-modulation lowpass filter with a sharp cutoff frequency and very little overshoot in its impulse response [4]. When demodulating a GMSK signal in the receiver section, care needs to be taken to preserve low phase distortion. This is a major concern when the receiver is demodulating the signal down to baseband, and care must be taken in the design of the IF filtering to protect this characteristic [4]. GMSK receivers require high carrier frequency accuracy between receiver and transmitter, imposing tough requirements on the VCO / synthesizer section (which is beyond the scope of this thesis). The strong point of GMSK is in the transmitter section: As the amplitude of the modulated signal remains constant and there are no zero-crossings, this constant-envelope schemes allow for the use of very power-efficient class-C power amplifiers, generating mainly harmonics, which can be filtered out easily. Therefore more efficient amplifiers (which tend to be less linear) can be used with constant-envelope signals, reducing power consumption. Again, for GMSK simpler hardware with lower power consumption comes at the expense of a smaller bit rate (1 bit per symbol).
Moving to more sophisticated modulation techniques that carry several bits per symbol (QPSK, QAM, OFDM), amplitude variations are inevitable. They exercise nonlinearities in an amplifier's amplitude transfer function, generating undesired spectral regrowth leading to power leakage into adjacent channels. Power amplifiers in class A or AB operation are necessary which have high power consumption. For QPSK (or 4QAM), 4 states carry 2 bits of information. This modulation scheme is more spectrally efficient than BPSK as the bit rate is twice the symbol rate. This comes at the expense of a more difficult demodulation: In general, schemes that rely on more than two levels (e.g. QAM, QPSK) require better signal to noise ratios (SNR) than two-level schemes for similar bit-error-rate (BER) performance [4]. Higher orders of quadrature amplitude modulation like 16QAM or 64QAM are used for satellite communications where the chance of perturbations due to interferers is low. M-QAM with M up to 64 is the modulation format of the Orthogonal Frequency-Division Multiplexing (OFDM) technique used in 802.11a/g Wireless Local Area Networks (WLAN, see table 4). OFDM is a frequency-division multiplexing (FDM) scheme utilised as a digital multi-carrier modulation method: A large number of closely-spaced orthogonal sub-carriers are used to carry data simultaneously. The data is divided into several parallel data streams or channels, one for each sub-carrier. Each sub-carrier is modulated with M-QAM (m=2...64, e.g. BPSK, QPSK, 16QAM, 64QAM) at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth [5]. OFDM systems are used in applications with frequency-selective fading due to multipath, such as DAB, DVB and WLAN [5]. As WLAN terminals typically operate at distances within 50m of a base-station, the link budget is not so tight compared to systems like GPS and the low noise figure for the front-end is mainly needed to overcome the high noise figure in the receive chain of the low-cost CMOS-based transceiver chip sets nowadays used in this application. $\pi/4$-DQPSK is a so-called differential modulation scheme, alternating between two QPSK constellation diagrams that are rotated by 45°: Starting from a 'black' state in Fig. 2, transitions must occur to a 'grey' state from where, again, transitions are only allowed back to a 'black' state. This avoids zero-crossings and guarantees that there is always a phase change,

making clock recovery easier. Note that the transitions between the states in practice are not straight as this would consume infinite bandwidth. Filtering is applied instead, leading to sophisticated transitions. At the decision points, however, the location is at (or close) to the corresponding state. For an excellent introduction into digital modulation in communications systems see [3].
Another layer of complexity in today's systems is multiplexing. Three principal types of multiplexing (or 'multiple access') are TDMA (Time Division Multiple Access)[2], FDMA (Frequency Division Multiple Access) and CDMA (Code Division Multiple Access). This means that different users are assigned to different time slots (TDMA), different carrier frequencies (FDMA) or different spreading codes (CDMA). From these modulation schemes it can be derived that new, spectrally more efficient systems require cleaner data at the baseband input in order to demodulate them properly with a low bit-error rate. As will be explained in section 3.1, this is especially true if a small receive signal is masked by strong interferers close to the desired frequency channel. Linear receive front-ends with low noise figure are the answer to the increased complexity of modern mobile communication systems.

2.2 Mobile phone standards

2.2.1 The evolution of mobile communications

Analog systems of the 1st generation (1G) like NMT or AMPS have been followed by digital 2G systems like GSM or IS-95. 2G systems were designed for voice transmission and offer only low data rates. This capability was enhanced in 3rd generation systems like EDGE (a GSM modification with 8-PSK modulation instead of GMSK), CDMA2000 (an evolution of IS-95) and the Universal Mobile Telephone System (UMTS) based on wideband CDMA. 4G will use a variable spreading factor, orthogonal frequency code-division multiplexing (VSF-OFCDM) for down-link data rates of up to 100 Mbit/s and variable spreading factor CDMA (VSF-CDMA) for 20 Mbit uplink data rates [6]. In this thesis, among others, circuits for IS-95 and UMTS have been designed. Therefore the key technical properties are sketched in the following sections.

2.2.2 CDMA

CDMA (Code Division Multiple Access) is an access method where multiple users are permitted to transmit simultaneously on the same frequency (full duplex system) and most often even timeshare the same channel. Frequency division multiplexing is still performed, but using just a few, very wide channels (e.g. 4 channels, each 5 MHz wide for UMTS) which are assigned to different operators, not different users. The users can be distinguished by a unique higher-rate digital sequence which is overlaid on their transmission. As these codes are orthogonal, distinction can be achieved by correlating

[2] introduced by Emile Baudot in 1874.

the received spectrum with a users overlaid sequence, which causes the signals of the other users to vanish if the signals have been transmitted without distortion via the transmit chain of the sender to the receive chain of the addressee. Therefore linearity is a key requirement of CDMA systems. The correct signal is amplified by the coding gain which is given by the code length. For a 128 bit code, the coding gain is $10 \cdot \log(128) = 21\,dB$. With decreasing data rate, the code length is increased, and thus the base station can improve signal reception from a mobile phone which is far from the base station simply by reducing the data rate [7]. The overlay sequence is based on codes which are shared between the base and the mobile stations [3]. The overlaid signals, just distinguished by different Walsh codes, together with the fact that CDMA phones receive and transmit at the same time (full duplex mode), make CDMA receivers the most demanding RF parts in terms of linearity which are treated in this thesis.

2.2.3 Narrow-band CDMA

Frequency bands [MHz]	824 - 849 (up-link) 1750 - 1780 (up-link) 1850 - 1910 (up-link)	869 - 894 (down-link) 1840-1870 (down-link) 1930-1990 (down-link)	cellular (USA)* Korean PCS American PCS
Data structure	CDMA / FDMA		
Duplex method	FDD		
Orthogonal codes	Walsh		
Channel per frequency	32-64 (Dyn. adapt)		
Number of channels	19-20		
Modulation	QPSK (mobile) OQPSK (base-station)		
Mobile output power	10 nW to 1 W		
Symbol rate	1.2288 Mbit/s (spreading)		
Channel spacing	1.25 MHz		
Filtering	Chebyshev low pass (FIR)		
Peak data rate	115 kbit/s (IS-95B)		

* same as AMPS frequency range

Table 1: IS-95 key parameters [3, 8].

Wireless CDMA mobile communication networks based upon the narrow-band IS-95 and IS-98 standards are widely used as a 2nd generation cellular standard throughout the US, South America and Asia (especially Korea) with different frequency allocations (see table 1). An IS-95/98 receiver needs to coexist in an harsh environment with other multi-standard mobile phones, imposing tough system conditions on the radio. As will be explained in section 3, the strongest interferer is the mobile phone's own power amplifier leaking through the antenna diplexer (see Fig. 15) to the receiver. In order to cover the various frequencies shown in table 1, four different IS-95 CDMA / GPS multi-band LNA/mixer combos have been developed by Atmel and TriQuint semiconductors [9, 10,

Frequency bands	1920 - 1980 MHz (up-link)	2110 - 2170 MHz (down-link)
Data structure	CDMA / FDMA	
Duplex method	FDD	
Orthogonal codes	OVSF (orthogonal variable spreading factor)	
Channels per frequency	4 ... 512	
Users per channel	15 ... 50	
Modulation	HPSK (mobile)	QPSK (base-station)
Symbol rate	3.96 Mbit/s (spreading)	
Channel spacing	5 MHz	

Table 2: W-CDMA key parameters.

11, 12, 13, 14], where this thesis contributed to the design of the 1900 MHz LNA and Mixer (see Fig. 3).

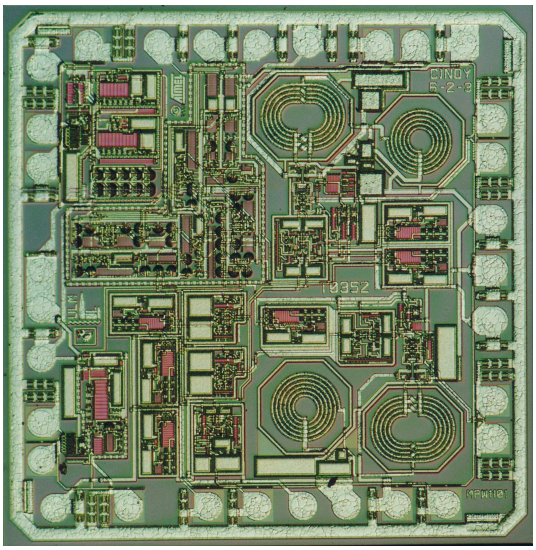


Figure 3: Chip photograph of the CDMA/GPS LNA/mixer combination [9, 10, 11, 12, 13, 14]: Top left: PCS LNA, top right: PCS mixer, bottom left: GPS LNA, bottom right: GPS mixer

2.2.4 Wide band CDMA (UMTS)

Compared to narrowband CDMA, the wideband CDMA (WCDMA) modulation used in UMTS uses a wider bandwidth (3.84 MHz as opposed to 1.23 MHz for IS-95) and the signals are spread using orthogonal variable spreading factor (OVSF) rather than Walsh codes. In the UMTS frequency-division duplex (FDD) mode, the 1920-1980 MHz band is allocated for the up-link (mobile → base-station) and the 2110-2170 MHz band to the

down-link (base-station → mobile), where individual operators acquired 5 or 10 MHz of paired spectrum, respectively. The full-duplex FDD mode is appropriate for a mix of voice and data services and is favoured by most operators. The TDD service is more suited for data transmission and uses just 5 MHz of unpaired 3G spectrum, which is interesting as many European 3G licenses include bandwidth of this unpaired spectra. This TD-CDMA interface performs up-link and down-link in a single band and separated by time.

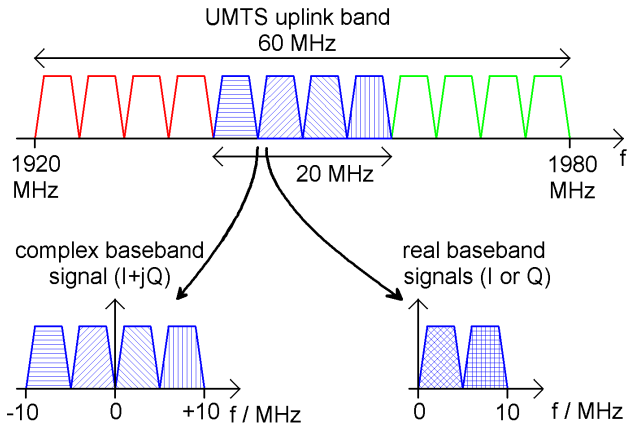


Figure 4: The SCUBA receiver down-converts 4 channels simultaneously [15, 16].

Commercial products are available for UMTS mobile receivers which are able to receive a single W-CDMA channel (e.g. [17, 18]). However, current base station receivers, which are designed to process four neighbouring channels simultaneously, are built-up using discrete components. Since a high pressure for cost reduction of the equipment exists on the telecommunication market, an integration of the analog receiver functionality even for the base stations is desirable. Due to stronger requirements in terms of bandwidth and linearity compared to mobiles, the development of such a base station receiver IC is challenging. In a joint effort between Atmel, Ulm University, and Alcatel SEL research, Stuttgart, a UMTS base station chip set has been developed within the MEDEA+ project SCUBA (**S**ystem-on-**C**hip solutions for advanced **U**MTS **BA**sestations). The direct down conversion receiver (DCR) down-converts 4 adjacent WDMA frequency channels of 3.84 MHz bandwidth and 5 MHz spacing simultaneously to the base band [19] (see Fig. 4): Important design parameters of the fully ESD-protected device are a noise figure NF $\leq$ 2 dB and a voltage gain of 48-54 dB into a 1000 Ω differential load (AD converter). The system architecture of the receiver is described in detail in [15, 16] and uses an IQ down-converter based on two Gilbert cell mixers, where the LO quadrature signals are derived from a 3.84-3.96 GHz VCO using a divider constructed from master-slave flip-flops in ECL technology, which leads to a low phase error [20] (see Fig. 5). A balanced preamplifier with 6 dB of variable gain in front of the mixers accommodates for gain variations due to fabrication tolerances and temperature of the whole receiver chain (antenna, diplexer and the receive ASIC itself). The mixers are followed by an active baseband low pass filter

with very high linearity and a sharp roll-of outside the 10 MHz pass band (see Fig. 4, bottom). The complete receive IC was realized in Atmel's SiGe1 bipolar technology [1], which is briefly sketched in section 4.2.

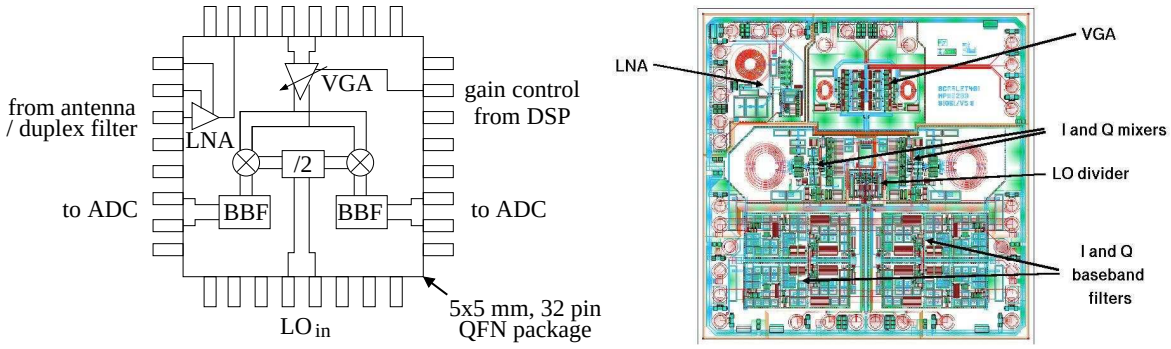


Figure 5: The SCUBA UMTS receiver in the version with integrated LNA.

Known problems of DCRs are relaxed using this architecture, as

- DC offsets after the mixer can be filtered by coupling capacitors, as there is no spectral content at zero IF frequency (see Fig. 4, bottom).
- and LO feed through from the VCO back through the mixer and the LNA to the antenna is reduced due to the VCO running at twice the input frequency.

Originally it was intended to realize the LNA onto the same SiGe die as the preamplifier, mixers and IQ baseband filter (see Fig. 5). Beside tough specifications like a gain of more than 17 dB and a sub-1.5 dB noise figure, a reverse isolation of 40 dB was required in order to fulfil the limits for radiated LO power from the antenna (see table 17). A first LNA design integrated into a 32 pin QFN package showed a reverse isolation $|S_{12}|$ of just 33 dB [15, 16], despite the exposed die attach having an almost ideal, inductance-free connection to ground. Even worse, the large inductor of the LNA's output match picked up LO signals which were coupled into the substrate via MIM capacitors driven by the 800 mV_{pp} outputs of the LO divider. As cost was not a prime concern, no additional efforts to improve the reverse isolation have been spent (e.g. using inductors with a patterned ground shield to avoid substrate coupling (see section 5.12), but the safe way was chosen to realize the LNA as a separate IC in a TSSOP8 package (Fig. 6).

This thesis contributed to the SCUBA project in two ways:

1. Design of the UMTS LNA according to the specifications in table 17, with emphasis on an extremely low noise figure and a high reverse isolation. Compared to the narrow-band CDMA LNA, a different linearization approach has been used, as for the UMTS receiver the linearity was tested with an interferer spaced 5 MHz apart, while it was 0.9 MHz for the narrow-band IS-95 LNA. This item is discussed in detail in section 6.8.4.

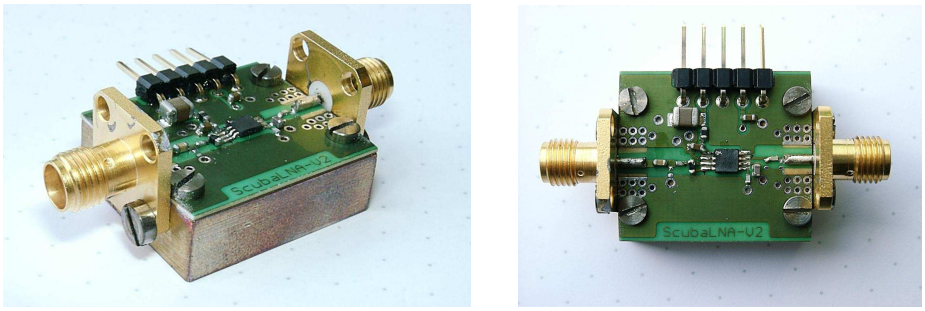


Figure 6: The SCUBA LNA optimised for lowest noise figure and high reverse isolation will be discussed in detail in section 6.8.4.

2. A second work package of the SCUBA project concentrated on the realisation of accurate, scaleable models for all kind of passive inductors on silicon using electromagnetic field simulation, verified by on-wafer measurements. This topic is covered in chapter 5.

2.3 Professional mobile radio systems

Professional Mobile Radio (PMR) terminals based on analog technology are widely used to fulfil the communication needs of professional organisations including all emergency response services as there are police, fire brigade, rescue teams as well as customs, private security companies, airports and transportation companies. Advantages of PMR technology over cellular systems like GSM or UMTS are

- the ability to operate between mobile terminals without the need for a base station (direct mode operation)
- guaranteed access to the network even under heavy load (e.g. in an emergency [21])
- group calls and broadcasting (point to multi point communication)
- reconfigurable networks
- a wider operating range which is achieved by using the UHF range (400 or 800 MHz) in Europe and the UHF (403. . .512 MHz, 806. . .870 MHz) and VHF (136. . .174 MHz) range in the United States.

Analog technology will be replaced by digital PMR technology within the next years. In Europe there are presently two competing standards: TETRA (TErrestrial Trunked Radio Access), as proposed by ETSI, combines FD/TDMA (4 time slots) with $\pi/4$-DQPSK modulation. TETRAPOL initially was developed as a proprietary standard and large networks are already operational in more than 30 countries [22]. TETRAPOL uses FDMA

	TETRA	TETRAPOL	P25
source	ETSI standard *www.tetramou.com*	TETRAPOL forum *www.tetrapol.com*	TIA (U.S.A)
multiple access	FD / TDMA	FDMA	FDMA
modulation scheme	$\frac{\pi}{4}$DQPSK	GMSK	C4FM (phase 1) CQPSK (phase 2)
channel spacing [kHz]	25	10 or 12.5	12.5 (phase 1) 6.25 (phase 2)
frequency range	UHF	UHF	VHF and UHF

Table 3: Overview of different standards for PMR terminals [23, 24, 25]

multiplexing and a robust GMSK modulation. Depending on the country, several bands are allocated to PMR systems. They can be grouped into the 400 MHz bands (380-430 MHz, 440-490 MHz and 470-520 MHz) and a 800 MHz band (750-870 MHz). Within the MEDEA+ project *SUPERSTAR* (**S**ilicon **U**niversal **P**latform for **S**ecured **T**elecom **A**pplications), TETRA/TETRAPOL multi-mode terminals are developed which target the European market as well as the American market and therefore need to fulfil the American APCO 25 standard as well. For APCO, analog *Mutual Aid Channels (MACh)* are required to allow inter-system communication with analog handhelds according to standard TIA-603-B. However, none of the RF parameters is determined by these MACh's. Inherent to all three standards is a low channel spacing of 6.25 ... 25 kHz (see table 3). This requires both LNA and mixer to be robust against 3rd order intermodulation from two very closely spaced tones due to co-location interference in rugged environments. As interferers appear in the receive band they cannot be reduced in amplitude by a SAW filter between LNA and mixer as it is the case in the IS-95, UMTS and GPS receiver developed during this thesis. Therefore, special design techniques have been used to make (i) the LNA robust against interferers at small offset frequencies and (ii) to design a mixer with very high linearity (see section 7.5.2) which considerably differs from the mixers designed for CDMA and WLAN. The main differences between TETRA, TETRAPOL and APCO are summarised in table 3. The two receive ICs – one for the 400 MHz band and one for the 750-870 MHz band – are shown Fig. 7 and will be discussed in detail in section 6 and 7. Fig. 8 shows a fully equipped LNA/Mixer board using the IC shown in Fig. 7.

2.4 Wireless Local Area Networks

Wireless Local Area Networks (WLANs) are a low-cost alternative to cellular networks in providing data services at retailers, hotel chains, property owners, airports and train stations to offer business travellers high-speed connectivity to their corporate networks as well as broadband internet access including voice-over-IP (VoIP) phone calls, without having to invest into UMTS license fees [26]. Compared to cellular networks, WLAN

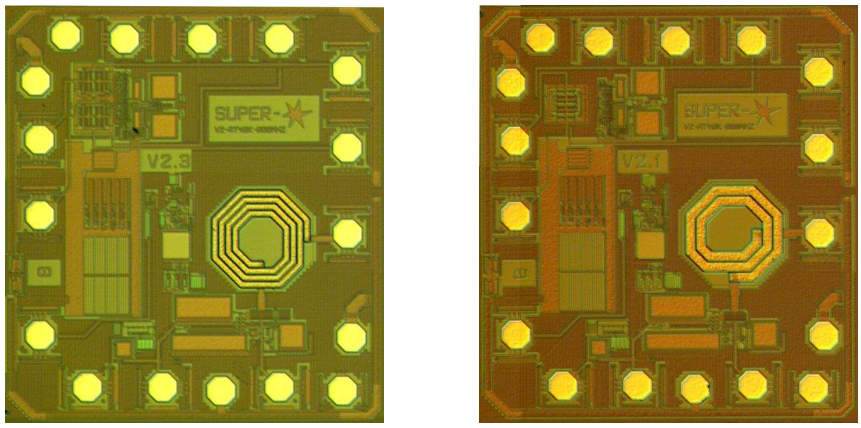


Figure 7: 400 MHz version (left) and 800 MHz (right) version of the LNA / mixer IC developed for TETRA/TETRAPOL handhelds using Atmel's at46k SiGe BiCMOS technology.

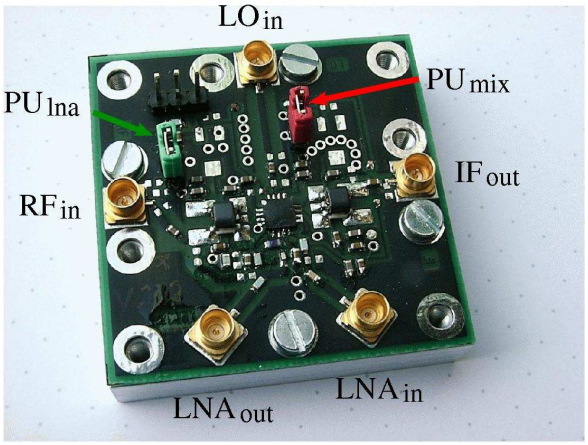


Figure 8: Fully equipped test board for the TETRA/TETRAPOL/APCO-P25 receiver.

offers a higher data rate (up to 54 Mbit/s per cell versus 3 Mbit/s for TD-UMTS, see section 2.2.4). Spectral allocations for WLAN are in the 2.4 GHz and in the 5-6 GHz band. The latter offers 200-455 MHz of unlicensed spectrum in many regions, with the potential to realize both fixed and portable wireless multimedia applications [27]. The different frequency bands which are allocated by the FCC in the US and by European and Asian authorities are shown in table 4. The European HiperLAN and Japanese HiSWAN standards are history, the market meanwhile is completely dominated by the 802.11a/b/g standards.

In order to meet the high demand associated with these applications, low-cost silicon-based radio transceiver front-ends capable of performing at 2.4-5.85 GHz are essential.

standard	country of origin	frequency range [GHz]	maximum data rate	air access	channel spacing
802.11b	US	2.4 - 2.4835	11 Mbps	FHSS DSSS using CCK	1 MHz 25 MHz
802.11g	US	2.4 - 2.4835	54 Mbps	OFDM using CCK	20 MHz
802.11a	US (U-NII)	5.15 - 5.25 5.25 - 5.35 5.725- 5.825	54 Mbps	OFDM	20 MHz
ISM bands		*2.40 - 2.4835* *5.725 - 5.85*		*Spread spectrum*	

Table 4: Current WLAN standards [28, 29, 30]. Data for the ISM bands are for comparison only.

Using Atmel's SiGe-1 technology, a broadband image-reject (IR) mixer has been developed within this thesis which achieves an image-rejection of more than 40 dB without the need for any post-tuning (section 7.7). However, due to the low integration level, this receiver did not make it into a product. Pure 5 GHz CMOS transceivers have been reported with impressive RF performance [31, 32, 33, 34], albeit this comes at the expense of a high power consumption [31]. While CMOS offers an advantage with respect to the integration level, the noise behaviour, current driveability and device matching is inferior compared to bipolar devices. In 2004, both BiCMOS and CMOS radios coexisted,

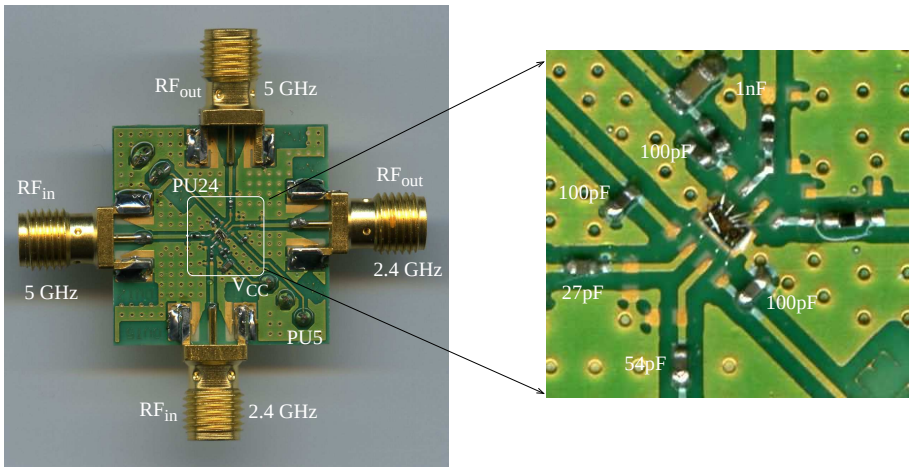


Figure 9: Test board of the 2.4 GHz / 4.9-5.9 GHz dualband WLAN LNA. The IC is mounted chip-on-board (COB) onto a 2-layer PCB made from RO4003, 200μm (8 mil) thick, with 17.5μm Cu cladding [35]. A support layer is glued below for mechanical rigidity. Losses in LNA input and output are just 0.1 dB @ 2.4 GHz, each, including connectors. SMD capacitors: Taiyo Yuden, 0201 size (except 1nF which is 0402).

where SiGe BiCMOS offers 5 dB higher sensitivity compared to CMOS [36]. Due to the enormous price pressure and the trend towards very high integration levels, CMOS radios using direct conversion architectures (DCR) will inevitably win the race. Opportunities for SiGe remain, but only in the front-end section (power amplifier or low noise amplifier). To date most CMOS radios offer reasonable noise performance at 2.4 GHz, but 5 GHz performance is still poor with receiver (RX) noise figures around 5-6 dB [32, 34]. Therefore, at the end of this thesis, a 4.9-5.9 GHz LNA has been developed according to the specifications of a European manufacturer of front-end modules [37]. These modules are fabricated using low-temperature co-fired ceramic (LTCC) and integrate a T/R switch (usually GaAs pHEMT), band pass filters for receiver (RX) and transmitter (TX), and sometimes a power amplifier [38]. This PA is usually built with InGaP HBTs [39, 40] or GaAs pHEMTs [41], as SiGe HBTs optimised for large breakdown voltages lack sufficient gain at high frequencies (see table 26). Interfaces to the radio are either single-ended or balanced, the latter being electrically superior but requiring additional signal lines. While some of the front-end modules on the market do not contain active parts in the RX path and show a transmission loss of ≈3 dB [42], the 802.11a standard benefits from a low noise preamplifier within the module. Modules with integrated LNA are on the market and use GaAs pHEMT technology for both switch and LNA [43, 38]. The LTCC process allows passive components such as resistors, inductors and capacitors with high quality factors[3] to be embedded in a multilayer, integrated module with high density and low cost [44, 38]. It turned out, however, that larger values of capacitors (>500 fF) and inductors consume large area on the LTCC and require the use of SMD components placed on the top of the module, which is unwanted. Finally, to keep prices low, all passives of the LNA were realised on silicon, except the input blocking capacitor, which - when integrated on Si - would increase the noise figure by more than 0.5 dB at 2.4 GHz (ADS simulation). The LNA results are presented in section 6.8.9. A balanced architecture, as it was published by our group earlier [45], is easier to package due to a virtual ground at the symmetry point and offers a better signal integrity. However, as the antenna interface is always single-ended, a single ended LNA design was chosen here. The output can then be converted to a balanced signal by a balun on the module. In addition, the use of SiGe2-Power for the single-ended design offers much better noise performance than the balanced LNA using SiGe1. Later on, a 2.4 GHz LNA for 802.11b/g systems was added to the 5 GHz LNA (see Fig. 9).

2.5 Global Positioning Systems

The *G*lobal *P*ositioning *S*ystem [46] has been launched by the US for military navigation purposes. It is a satellite-based location/time finding system with 24 satellites (plus reserve satellites) orbiting the earth. They are located in 6 orbital planes in an altitude of 20180 km with an inclination of 55°. The satellites, which have a period of revolution of 11h58m00s, transmit signals in both the L_1 band (1575.42 MHz) and the L_2 band

[3]The quality factor is defined in detail in section 5.6.

at $60/77 \times f_{L1}$ (1227.6 MHz) which can be distinguished by different Gold codes used to spread the signal. The L_2 band transmits the P (precision) code, a military code of $2.35 \cdot 10^{14}$ bit length which has not been disclosed to the public so far. Therefore, for commercial applications, just the L_1 band is of interest. In the L_1 band, each satellite transmits a specific 1023 bit Gold code with a chip rate of 1.023 Mcps using BPSK modulation. These C/A (coarse acquisition) codes therefore repeat every 1 ms. In contrast, the military P-code repeats every 265 days. Using the location and time information sent by the satellites and time-of-arrival (TOA) from at least 4 visible satellites, four equations can be solved for altitude, latitude, longitude, and time [47, 48]. Within this thesis a 1575 MHz GPS LNA was designed as part of Atmel's ANTARIS™chipset [48]. The LNA is sold under the name ATR0610 [49, 50, 51] and its design is explained in detail in section 6.8.8. The latest generation of the ANTARIS™chipset, which is a system-in-package consisting of a BiCMOS die for the RF part, a CMOS die for the baseband part as well as 6 passive components, along with a complete description of how to build a high-performance GPS receiver from antenna selection to the software interface has been published by the author recently in [48] (see Fig. 10). The partitioning is such that the SiGe LNA (developed in

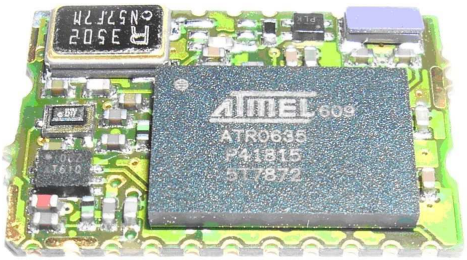


Figure 10: GPS receiver module containing the Antaris chipset [48]. Top left: 23.104 MHz TCXO, top right: 32.768 kHz crystal resonator for the real time clock, left: LNA and SAW filter, right: ATR0635 GPS receiver (system-in-package).

this thesis) is directly connected to the antenna with no filtering. After amplification by the SiGe LNA, a SAW band pass filter with balanced outputs feeds the signal to the mixer of the bipolar receiver IC. The differential architecture of the SAW filter can easier deal with the parasitic capacitance effects of the SAW package, achieves higher attenuation in the stop band and replaces a bulky transformer on the board [52]. As the SAW filter is located *behind* the LNA, a low LNA noise figure directly translates in good GPS signal strength C/N_0 (measured in dB/Hz). In a GPS system, GPS signal strength directly relates to the key system parameters "acquisition sensitivity" and "tracking sensitivity". On the other hand, this architectures forces the LNA to tolerate all out-of-band jammers, as no filtering is used in front of the LNA, except the usually used, narrow-band ceramic patch antenna [48]. Therefore the key specifications of the GPS LNA have been (i) low noise figure (ii) high linearity to tolerate jammers e.g. in the 1750 MHz GSM transmit band along with (iii) low power consumption. The GPS LNA developed in Atmel's SiGe1-technology is housed in a PLLP6-package that measures just 1.6×2.0 mm^2 and is merely

	GPS	Galileo
# of satellites (reserve)	24 (6)	27 (3)
altitude	20180 km	23616 km (MEO)
equatorial inclination	55°	56°
frequency bands	1575.42 MHz (L1) 1227.60 MHz (L2)	1561-1590 MHz (L1) 1176-1207 MHz (E5a, E5b) 1269-1289 MHz (E6)
modulation	BPSK	Binary Offset Carrier (BOC)
chip rate	1.023 Mcps (CA code)	1.023 Mcps
speed	50 bit/s (CA code)	250 symbols/s
pilot channel	no	yes (BPSK modulated)
code	Gold (1023)	Gold (8184-10230)
power		5-6 dB above GPS level

Table 5: Key parameters of the American GPS and the European Galileo system [46, 55, 56].

bigger than the size of a discrete transistor (see section 6.8.8). This small size and its full ESD protection make it an ideal candidate for active GPS antennas.
When the European Galileo system will go into operation somewhere in 2013 [53], the combined correlation of GPS and Galileo satellites shall give an availability of position information in 95% of all cases together with an improved location accuracy. Galileo is a Global Navigation Satellite System (GNSS) initiated by the European Commission and the European Space Agency (ESA) and compatible with but independent from the American Global Positioning System (GPS). The main differences between GPS and Galileo are sketched in table 5. Compared to a GPS receiver, for optimum performance a Galileo receiver will need a broadband front-end with a flexible frequency plan to cover all 4 bands. The standard consumer receiver, however, will just receive the free Galileo service in the L_1 band [54]. Due to its broadband nature, the GPS SiGe LNA developed in this thesis can be used to receive the important Galileo L_1-band as well.

3 System considerations and level planning

A typical setup of a CDMA phone is shown in Fig. 11[4]: Connected to the antenna is a band pass filter which blocks signals below the TX-band and above the RX-band. Due to the full duplex mode of a CDMA phone, the diplexer (see Fig. 15), the equivalent of the antenna switch of a TDMA phone, is a very important part: It needs to have a low attenuation from the PA to the antenna in order to guarantee a good PA efficiency and

[4]The isolator following the PA is often omitted in modern phones in order to improve power added efficiency (PAE) of the transmitter and save cost as well as PCB real estate. This, however, requires the PA to withstand VSWR-ratios of higher than 10:1 without damage.

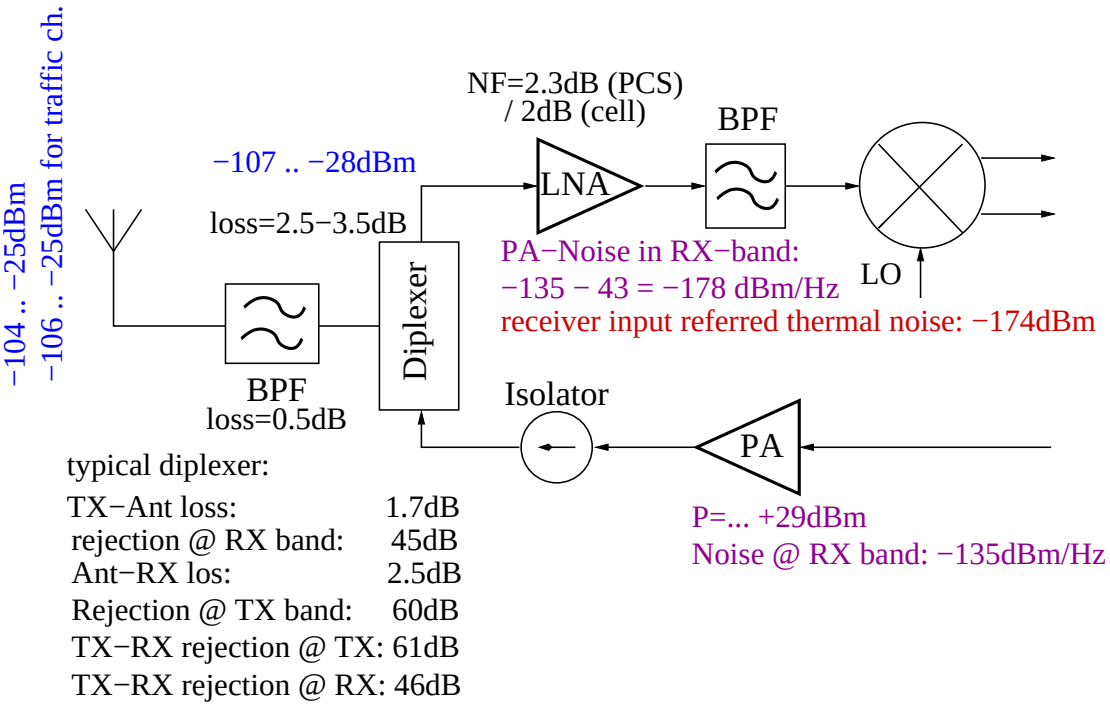


Figure 11: Typical setup of the RF front-end for a CDMA mobile phone [57].

a low attenuation from the antenna port to the LNA to maintain a high signal-to-noise ratio. As we will see in this section, the most important specifications are the isolations between antenna port, RX- and TX-port. As an example, the system planning for an IS-95/IS-98 receiver is reviewed following [57, 58]: CDMA phones operate in the full duplex mode which introduces an additional interference to the phone receiver: A signal leakage from the transmitter (TX) through the antenna diplexer. This TX leakage is generally not a problem on its own. But, in the presence of a strong jammer passing the diplexer (e.g. a signal transmitted by a nearby AMPS or TDMA base station), the modulated TX leakage signal is transferred to the jammer by the LNA nonlinearities, widening the jammer spectrum. This cross modulation (XM) contaminates the RX channel adjacent to the jammer, degrading the receiver sensitivity. The maximum allowed XM determines the linearity specifications for a CDMA LNA (since the TX leakage is filtered by the RF image-reject filter following the LNA (see Fig. 11), XM is negligible in the mixer; the mixer linearity is defined by the 3rd-order intermodulation of two *inband* jammers, see Fig. 14): The adjacent channel selectivity is a measure of the ability of the receiver to detect the desired modulated signal without exceeding a given degradation due to the presence of an unwanted signal in the adjacent channel. This is typically measured by the frame error, given by the mobile phone standard. The desensitisation characteristic[5]

[5]desensitization means a receivers unability to receive the full strength of a radio signal. This is caused by a nearby transmitter with a strong signal on a close frequency, which overloads the receiver and makes

of the receiver determines its ability to operate successfully under strong interferers. This requires an LNA with exceptional high linearity that should be achieved

1. without degrading the LNA NF and gain since the desired RX signal from a base station at maximum distance to the mobile phone is very weak, while the mobile phone in this condition transmits at its maximum output power. This is because the CDMA mobile phone sets its output power according to $P_{TX}[dBm] = -73 - P_{RX}$ in the cellular band and $P_{TX}[dBm] = -76 - P_{RX}$ in the PCS band [60], so minimum RX power always translates into maximum TX power. In addition, the signal may be jammed by a nearby AMPS or TDMA base station.

2. with a low power consumption to extend the talk time of the phone, and

3. with a low-cost technology allowing a high level of integration.

While previously GaAs MESFET front-ends containing LNA and mixer have been used, the industry meanwhile has switched to SiGe transceivers [58, 61], with RF CMOS solutions being in the pipeline [62].

3.1 Intermodulation distortion

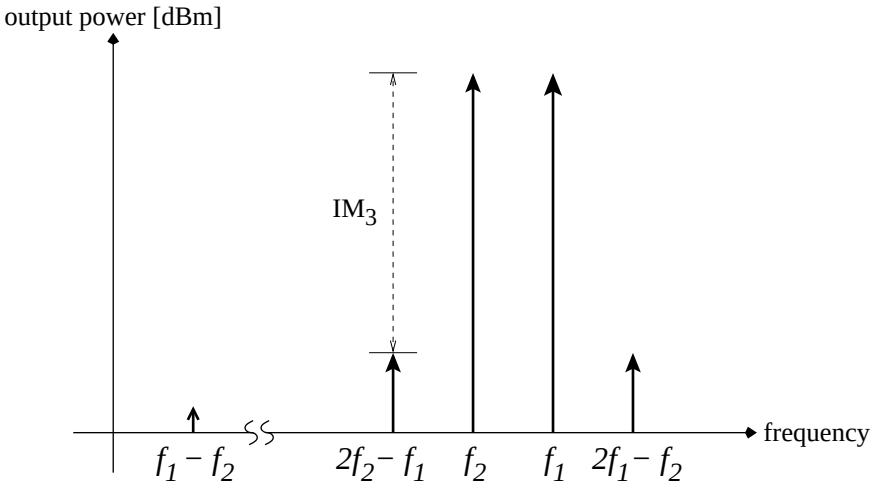


Figure 12: Applying two tones to a nonlinear device leads to intermodulation distortion.

Intermodulation distortion is the result of two or more signals interacting in a nonlinear device to produce additional unwanted signals [63]. These additional signals (intermodulation products) occur mainly in devices such as amplifiers and mixers, but to a lesser extent

it unable to fully receive the desired signal [59].

they also occur in passive devices such as ceramic SMD capacitors with a low voltage coefficient (capacitance slightly varying with applied RF voltage swing), parts containing magnetic materials such as circulators and isolators and corroded RF connectors [63]. This thesis concentrates on the reduction of intermodulation products in Low Noise Amplifiers (LNAs) and mixers. As can be found in numerous textbooks (e.g. [64, 65]) and scripts [66], the non-ideal characteristics of a weakly non-linear amplifier can be described by using the power series expansion:

$$V_{out} = K_0 + K_1 \times V_{in} + K_2 \times V_{in}^2 + K_3 \times V_{in}^3 + \ldots \tag{1}$$

Applying a one-tone excitation $V_{in} = E \cdot \sin(\omega \cdot t)$ and using $\sin(3a) = 3 \cdot \sin(a) - 4 \cdot \sin^3(a)$ and $\cos(2a) = 1 - 2 \cdot \sin^2(a)$ results in

$$\begin{aligned} V_{out} &= \left[K_0 + \frac{K_2 \cdot E^2}{2}\right] + \left[K_1 \cdot E + \frac{3 \cdot K_3 \cdot E^3}{4}\right] \times \sin(\omega \cdot t) && (2) \\ &- \frac{K_2 \cdot E^2}{2} \times \cos(2 \cdot \omega \cdot t) + \frac{K_3 \cdot E^3}{4} \times \sin(3 \cdot \omega \cdot t) && (3) \end{aligned}$$

This shows that a one-tone input signal produces harmonic distortion (Eqn. 3), as well as DC offset and gain compression (Eqn. 2, $K_3 < 0$). A two-tone input signal

$$V_{in} = E_1 \cdot \sin(\omega_1 \cdot t) + E_2 \cdot \sin(\omega_2 \cdot t) \tag{4}$$

produces harmonic distortion *and* intermodulation distortion: Combining Eqns. 1 and 4 results in

$$\begin{aligned} V_{out} = K_0 &+ K_1 \cdot \{E_1 \cdot \sin(\omega_1 \cdot t) + E_2 \cdot \sin(\omega_2 \cdot t)\} \\ &+ K_2 \cdot \{E_1 \cdot \sin(\omega_1 \cdot t) + E_2 \cdot \sin(\omega_2 \cdot t)\}^2 \\ &+ K_3 \cdot \{E_1 \cdot \sin(\omega_1 \cdot t) + E_2 \cdot \sin(\omega_2 \cdot t)\}^3 + \ldots \end{aligned} \tag{5}$$

The first term K_0 represents the DC offset of the amplifier, the second term is the fundamental signal. The subsequent terms represent the distortion of the amplifier. The 2nd order intermodulation distortion (IMD) can be found by analysing the third term of Eqn. 5 by using the identities above and $\sin(a) \cdot \sin(b) = \{\cos(a-b) - \cos(a+b)\}/2$

$$\begin{aligned} K_2(v_{in})^2 &= K_2 \cdot \{E_1^2 \cdot \sin^2(\omega_1 \cdot t) + E_2^2 \cdot \sin^2(\omega_2 \cdot t) + 2 \cdot E_1 \cdot E_2 \cdot \sin(\omega_1 \cdot t) \cdot \sin(\omega_2 \cdot t)\} \\ &= K_2 \frac{E_1^2 + E_2^2}{2} - \frac{K_2}{2}\left[E_1^2 \cdot \cos(2 \cdot \omega_1 \cdot t) + E_2^2 \cdot \cos(2 \cdot \omega_2 \cdot t)\right] \\ &\quad + K_2 \cdot E_1 \cdot E_2 \left[\cos(\omega_1 \cdot t - \omega_2 \cdot t) - \cos(\omega_1 \cdot t + \omega_2 \cdot t)\right] \end{aligned} \tag{6}$$

The first and second terms in Eqn. 6 represent DC offset and second-order harmonics. The third term is the second order IMD. This exercise can be repeated with the fourth

term of Eqn. 5 to study third-order effects.

$$\begin{aligned} K_3(v_{in})^3 &= K_3\{E_1^3 \cdot \sin^3(\omega_1 \cdot t) + E_2^3 \cdot \sin^3(\omega_2 \cdot t) \\ &+ 3 \cdot E_1^2 \cdot E_2 \cdot \sin^2(\omega_1 \cdot t) \cdot \sin(\omega_2 \cdot t) + 3 \cdot E_1 \cdot E_2^2 \cdot \sin(\omega_1 \cdot t) \cdot \sin^2(\omega_2 \cdot t)\} \end{aligned} \quad (7)$$

By using $\sin^3(a) = 1/4[3\sin(a) - \sin(3a)]$ and $\sin^2(a) \cdot \sin(b) = 1/2[\sin(b) - 1/2\sin(2a+b) - \sin(2a-b)]$ this gives

$$\begin{aligned} K_3(v_{in})^3 &= \frac{3 \cdot K_3}{4}\{E_1^3 \cdot \sin(\omega_1 \cdot t) + E_2^3 \cdot \sin(\omega_2 \cdot t) \\ &+ 2 \cdot E_1^2 \cdot E_2 \cdot \sin(\omega_2 \cdot t) + 2 \cdot E_1 \cdot E_2^2 \cdot \sin(\omega_1 \cdot t)\} && (8) \\ &- \frac{K_3}{4}\{E_1^3 \cdot \sin(3\omega_1 \cdot t) + E_2^3 \cdot \sin(3\omega_2 \cdot t)\} && (9) \\ &- \frac{3 \cdot K_3 \cdot E_1^2 \cdot E_2}{2}\{\sin(2\omega_1 \cdot t - \omega_2 \cdot t) - \frac{1}{2}\sin(2\omega_1 \cdot t + \omega_2 \cdot t)\} && (10) \\ &- \frac{3 \cdot K_3 \cdot E_1 \cdot E_2^2}{2}\{\sin(2\omega_2 \cdot t - \omega_1 \cdot t) - \frac{1}{2}\sin(2\omega_2 \cdot t + \omega_1 \cdot t)\} && (11) \end{aligned}$$

Term 9 signifies the third-order harmonics and finally terms 10 and 11 represent third-order IMD. The result clearly indicates that IMD and crossmodulation only occur on a curved transfer characteristic with cubic terms as in Eqn. 1. In contrast a transfer characteristic with a linear and quadratic portion generates the mixing products (sum and difference) and the harmonics of the input signals (see Eqn. 6) [67]. 2nd order intermodulation products are usually outside the channel and can be removed by filtering. 3rd order intermodulation products, however, for small tone spacing $|f_1 - f_2|$ fall within in the receive band and cannot be removed by filtering. Higher order intermodulation products are generally less important because they have lower amplitudes and are more widely spaced [63]. In this thesis, when talking about nonlinearity, 3rd order nonlinearity is meant, measured with a two-tone input signal of low magnitude. The 2-tone test is widely accepted in assessing amplifier linearity: The summation of the two tones with slightly different frequencies and the same amplitude V_0 leads to a time-varying envelope with peak amplitude $2 \cdot V_0$ and tests the amplifier over its whole transfer characteristics [64]. Therefore it is one of the most demanding amplifier tests available. The frequency of the envelope $\omega_1 - \omega_2$ is often referred to as *beat-frequency*.
Fig. 12 shows the power levels in logarithmic scale (e.g. in units of dBm) as seen on a spectrum analyser. The distance (in dB) between the fundamental tones and the 3rd order intermodulation products is denoted as IM_3.

The 3rd order intercept point (IP_3) can be defined as referred to the input

$$IIP_3[dBm] = P_{in}[dBm] + \frac{IM_{3\,(P_{in})}}{2}[dB] \quad (12)$$

or referred to the output,

$$OIP_3[dBm] = P_{out}[dBm] + \frac{IM_{3\,(P_{in})}}{2}[dB] \quad (13)$$

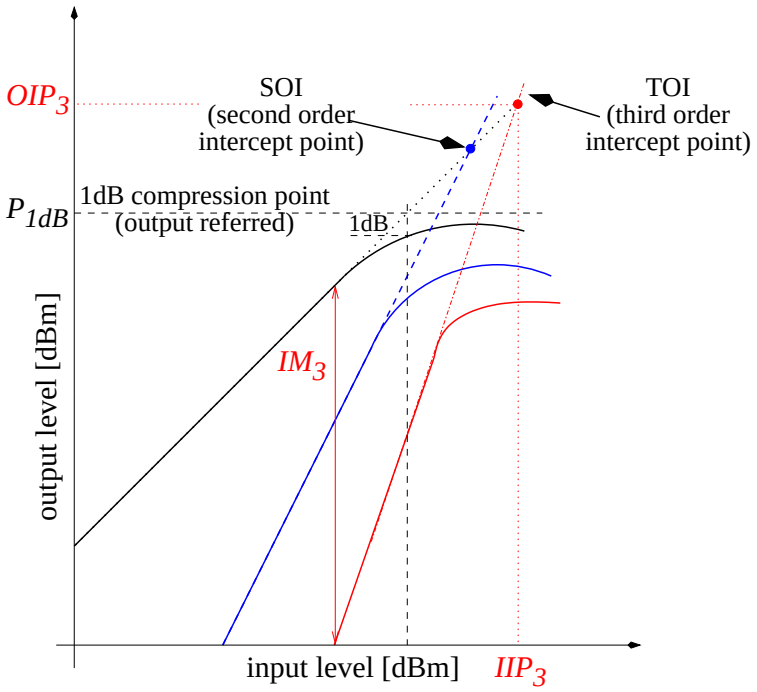


Figure 13: Definition of 1dB-compression and 2nd and 3rd order intercept point.

where P_{in}, P_{out} and $IM_{3\,(P_{in})}$ are extracted in the linear range of Fig. 13. Note that $OIP_3 - IIP_3 = P_{out} - P_{in}$ and thus equals the power gain of the device. If two strong interferers are present at the antenna, their 3rd order intermodulation products can fall inside the receive channel, masking the desired signal: As evident from Fig. 14), interference due to

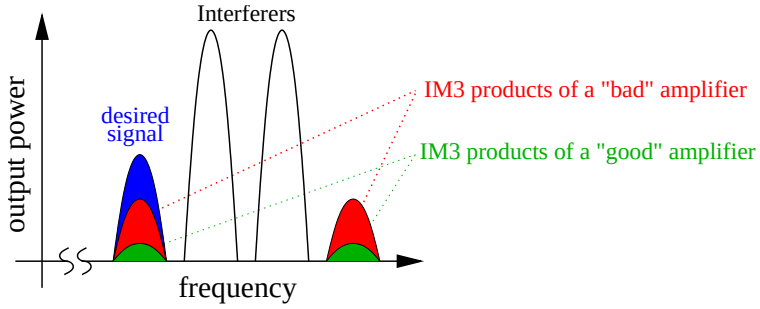


Figure 14: A third-order intermodulation product corrupts the desired channel.

intermodulation is primarily of interest at the limits of receiver sensitivity in the presence of relatively large interferers.

3.1.1 Derivation of LNA IIP$_3$ requirements

The sources of interference in a CDMA receiver include [58]

N_{RX} – the RX thermal noise,
N_{TX} – the thermal noise of the TX in the RX band, coupled through the diplexer to the LNA,
N_{Φ} – the RX LO phase noise that appears at IF after the jammer is downconverted by the RX LO (reciprocal mixing),
P_{XM} – the jammer cross modulation power in the adjacent RX channel.

In the IS-98A/95B and interim standard, the RF receiver sensitivity of the CDMA cellular mobile station is defined at the handset antenna connector. The minimum required sensitivity for the received forward channel is equal to -104 dBm. The maximum input power is -25 dBm [57]. The maximum total thermal noise power, $N_{oc,th} = N_{RX} + N_{TX}$ is set by the receiver sensitivity and dynamic range requirement of the standard, where the frame error rate (FER) must not exceed 0.5% when the received forward CDMA signal power at the antenna is $\hat{P}_{or} = -104$ dBm. This not only holds for the receive channels but for the dedicated traffic channel as well, whose ratio to the total received power is -15.6 dB. At the sensitivity limit this is $E_{c,Traffic} = \hat{P}_{or} - 15.6\,dB = -119.6$ dBm. Here $E_{c,Traffic}$ is the power per *code*. As explained in [58], to guarantee 0.5% FER for the traffic channel in average white gaussian noise (AWGN), the ratio of the average power per data bit E_b to the effective noise spectral density N_t, should be 4.5 dB or more, even for the traffic channel.

$$\frac{E_{b,Traffic}}{N_t} = \frac{128 \cdot E_{c,Traffic}}{N_{oc,th}} \geq 4.5\,dB \tag{14}$$

The factor 128 is the coding gain (see section 2.2.2). Taking the logarithm of Eqn. 14, the maximum allowed thermal noise at the antenna can be computed as

$$N_{oc,th}\,[dBm] \leq (-119.6 + 10 \cdot \log(128) - 4.5)\ dBm = -103\,dBm \tag{15}$$

With a 3 dB margin, this sets the upper limit for the *thermal noise* at the receiver:

$$N^*_{oc,th} = N_{RX} + N_{TX} \leq 10^{\frac{-106}{10}}[mW] \tag{16}$$

The maximum *total interference (noise) power*, $N_{oc,tot} = N_{RX} + N_{TX} + N_{\Phi} + P_{XM}$, is set by the single-tone desensitisation requirement, where the FER must not exceed 1% when $\hat{P}_{or} = -101$ dBm for the receive channels and $\hat{P}_{or} - 15.6\,dB$ for the traffic channel. Assuming that the total interference has a Gaussian distribution, the minimum required E_b/N_t is 4.3 dB for 1% FER. In analogy to Eqn. 15 we calculate the total interference power referred to the antenna to be

$$N_{oc,tot}\,[dBm] \leq (-101 - 15.6 + 10 \cdot \log(128) - 4.3)\ dBm = -99.8\ dBm. \tag{17}$$

The noise margin for reciprocal mixing and jammer cross modulation is therefore limited to

$$10^{\frac{-106}{10}} + N_\Phi + P_{XM} \leq 10^{\frac{-99.8}{10}}[mW] \tag{18}$$

For the single-tone desensitisation test case, the jammer is $\nu_0 = 900$ kHz away from the centre of the RX channel center. So, the RX LO phase noise that appears in the RX channel due to the reciprocal mixing is confined to a 900 kHz $\pm$ 1.23 MHz/2 = 285...1515 kHz frequency-offset range. As this is outside of the PLL loop filter bandwidth, we consider the noise of a free running VCO here which is proportional to $1/\nu^2$ with respect to the carrier in the above mentioned frequency range. Optimised, discrete CDMA VCOs show typical values of $\Phi_0 = -133.5$ dBc/Hz at $\nu_0 = 900$ kHz offset from the carrier [68].

$$\Phi_{(\nu)} = \frac{\Phi_0 \cdot \nu_0^2}{\nu^2} \tag{19}$$

Integrating this $1/\nu^2$ noise shape over the 285...1515 kHz frequency range gives

$$\eta_\Phi = \int_{\nu_1}^{\nu_2} \frac{\Phi_0 \cdot \nu_0^2}{\nu^2}\, d\nu = \Phi_0 \cdot \nu_0^2 \cdot \{-\frac{1}{\nu_2} + \frac{1}{\nu_1}\} \tag{20}$$

$$= 10^{-13.35}\, mW/Hz \cdot (900\, kHz)^2 \cdot \{-\frac{1}{1515\, kHz} + \frac{1}{285\, kHz}\} = -69.9\, dBc \tag{21}$$

Taking into account a 3 dB improvement in phase noise due to the LO frequency divider which is often used, yields -72.9 dBc. Referencing this phase noise to the P_J = -30 dBm jammer power at the antenna, we get for the receiver's LO phase noise contribution $N_\Phi = -102.9$ dBm. According to Eqn. 18, this leaves a maximum of $P_{XM} \leq -105.5$ dBm for the cross modulation contribution due to the -30 dBm jammer. Finally, using [58] and Eqn. 12, this cross modulation power is related to the LNA linearity by

$$P_{XM}\,[dBm] = P_J + 2\left(\underbrace{P_{TX} + L_{TX} - L_{TX-RX}}_{\text{TX power as seen on LNA input}}\right) - 2 \cdot IIP_3 - 2.4 \tag{22}$$

where $P_{TX} = 23$ dBm is the maximum transmit output power at the antenna, L_{TX} is the diplexer TX-antenna insertion loss and L_{TX-RX} is the diplexer's TX-RX isolation (from the PA to the LNA input) in the TX band. The correction factor "2.4 dB" takes into account that the CDMA signal is not a continuous single tone, as assumed in Eqn. 12. Note that both Eqns. 12 and 22 are valid only in dBm! Rearranging Eqn. 22 results in the following relationship between the diplexer characteristics and the LNA minimum IIP_3, satisfying the single-tone desensitisation requirement:

$$IIP_{3,min}[dBm] = P_J/2 + P_{TX} + L_{TX} - L_{TX-RX} - P_{XM}/2 - 1.2 = 59.5 - L_{TX-RX} + L_{TX} \tag{23}$$

From Eqn. 23 it is evident that the diplexer is a key part in a CDMA phone and its performance translates directly into the linearity requirements of the front-end: Assuming a TX-RX isolation of 53 dB and a TX loss of 2.7 dB, the required minimum IIP_3 is

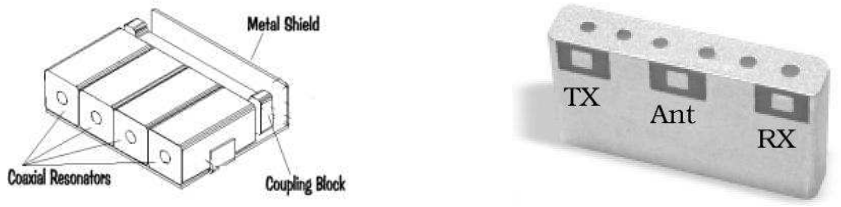


Figure 15: The diplexer is a key component in a CDMA front-end (source: Ube Electronics Limited and CTS WIRELESS COMPONENTS, INC.)

+9.2 dBm for a cellular CDMA LNA. Using the same analysis with slightly different assumptions for the technical specifications, ref. [57] calculates an IIP_3 of +7.6 dBm which is quite similar.

Eqn. 23 shows that improvements in the TX-RX isolation relax the receiver linearity requirements, resulting in a lower power consumption[6]. The diplexer itself used to be a ceramic mono-block duplex filter consisting of coupled resonators (see Fig. 15) or a SAW (Surface-Acoustic-Wave) device. Using SAW devices for diplexers is challenging, as the high TX power of up to 2 watts which needs to be handled in the thin piezo-electric layers leads to self heating [70]. In 2004, smaller diplexers using Bulk-Acoustic-Wave (BAW) or Film-Bulk-Acoustic-Resonator (FBAR) technologies have been introduced to the market [71, 72]. Currently BAW diplexers with a footprint of 3.8×3.8 mm^2 are being developed [69]. Compared to SAW devices, BAW filters offer better power handling capability, a lower temperature coefficient and can in principle be integrated onto the silicon RFIC [70], provided that AlN is used as a piezoelectric material, as other materials lead to contamination in the silicon IC process[7].
The +9.2 dBm of IIP_3 are required during a CDMA call, when the receiver is subject to the cross modulation distortion. In addition there is a low-linearity *paging* mode, which is used when the receiver monitors a forward-link paging channel waiting for an incoming call. In this idle mode, the TX power is switched off and the current of the LNA can be reduced by approximately 50%. Some receivers also have a low-gain bypass mode to handle a strong RX signal.

3.1.2 Derivation of receiver NF requirements

In the case of the receiver, there are two sources of interference that are purely white Gaussian noise [57]:

1. The receiver's input referred thermal noise power spectral density (PSD) N_0

[6]Using Eqn. 23 and the latest performance data for a BAW diplexer [69] with 57 dB of TX-RX isolation and 2.7 dB insertion loss in the TX-band, the 4 dB of additional TX-RX isolation relax the IIP_3 requirement from 9.2 dBm to 5.2 dBm.

[7]For a good overview about FBAR and BAW devices see [70].

	LNA	Image filter	1st Mixer	VGA
NF [dB]	1.7	3	6.5	15
Gain [dB]	13	-3	13	–

Table 6: IS-95 line up analysis for a total NF of 3.07 dB using H.T. Friis classical noise formula for cascaded networks [75].

2. The transmitter's thermal noise PSD in the receive frequency band N_{TX}

N_0 is determined by the receiver's noise figure (NF), and N_{TX} is determined by the amount of the transmitter's thermal noise leaking to the antenna connector of the mobile phone through the diplexer. A typical PA has an output thermal noise power spectral density in the receiver frequency band of -135 dBm/Hz[73, 74]. Assuming a minimum of 43 dB attenuation through the diplexer from the PA to the antenna input port in the receiver band, N_{TX} can be calculated as -178 dBm/Hz at the antenna connector. As discussed above, the IS95/98A standard specifies that the traffic channel requires a minimum signal strength per data bit of $[E_b/Nt] \geq 4.5$ dB for a 0.5% FER. As $-178\,dBm/Hz + (-174\,dBm/Hz) = -172.5$ dBm/Hz, the PA noise floor adds 1.5 dB of additional noise power to $k_B \cdot T$ in the RX band requiring that the $[E_b/Nt]$ needs to be increased from 4.5 dB to ≈ 6.5 dB [57]. This in turn requires that the minimum sensitivity is improved from -104 dBm to P_{actual} = -106 dBm. The noise figure for the complete front-end (referred to the antenna port) can now be calculated according to

$$NF_{receiver} = -106\ dBm - 10 \cdot \log(1000 \cdot k_B \cdot T_0 \cdot 1.23MHz) = 7.1dB \qquad (24)$$

where k_B is Boltzman's constant and $T_0 = 290$ K is the standard noise temperature. Subtracting the loss of 0.5 dB in the diplex circuit and 3.5 dB in the duplex circuit, the NF budget for the rest of the receiver front-end (LNA & mixer) is 3.1 dB. Using H.T. Friis classical noise formula for cascaded networks [75], different trade-offs can be made between LNA, mixer and VGA performance. The settings used in this work are shown in table 6.

4 Device technology

4.1 Technology selection criteria

At the beginning of the thesis, only the SiGe1 bipolar and the at46k BiCMOS process were available. The first SiGe1 product – a 1.9 GHz LNA/PA RFIC for the Digital European Cordless Telephone (DECT) [76, 77] – was available in 1998 and at that time the first commercial SiGe product on the market. SiGe1 has faster HBTs with better noise figure than at46k and comes at a lower price. Therefore most designs used this simple technology, using a 0.8μm (effective) emitter width, 2 metallisation layers (optional 3) and only 19 mask levels [2, 78]. MOS transistors turned out to be useful to allow for bypass switches in LNAs and passive FET ring mixers. Therefore at46k had been used for the design of the TETRA/TETRAPOL frontend, despite its higher HBT noise figure. This technology is described in detail in section 4.4. The SiGe2-RF process with higher f_T was projected for a 5 GHz WLAN LNA. As no MPW was available at the time of tapeout, the *power*-version of this technology (SiGe2-Power) was used and led to a much lower noise figure than simulated with the SiGe2-RF models. We later attributed this to (i) the lower base sheet resistance of the *power*-version (see table 26) and (ii) to lower interconnect resistances at the LNA input, as the tungsten plugs of SiGe2-Power allow to reinforce the base and emitter metal 1 (M1) stripes with metal 2 (M2), resulting in a lower base and emitter resistance.

4.2 SiGe1 and SiGe2 bipolar processes

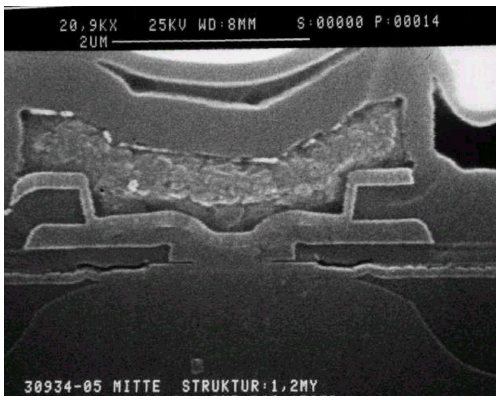


Figure 16: Scanning electron microscopy of a grinded SiGe1 wafer

Atmel's SiGe HBT technology has been reported in detail elsewhere [78, 79, 80, 81, 82, 83, 84, 85, 86]. Therefore only the key aspects of the different processes which have been used in this thesis are highlighted. In SiGe1, after buried layer (BL) implantation, device isolation is performed using *LOC*al *O*xidation of *S*ilicon *(LOCOS)*. This leads to the

characteristic "bird's beaks" at the base-collector interface (see Fig. 16) and is associated with high base-collector capacitances C_{BC}. The SiGe epitaxy is done over the complete wafer by single-wafer atmospheric pressure CVD (APCVD), where the SiGe layer grows mono crystalline onto the collector region and poly crystalline on the field oxide. The poly crystalline base contact is formed by implantation and silicidation of titanium. For small signal applications, a low collector resistance is not as important as it is for power applications and sometimes a higher collector resistance increases stability [87]. Therefore, in order to get a compact device with low base-emitter resistances and capacitances, HBTs with multiple emitter stripes but a single collector contact rotated by 90° have been used (Fig. 17).

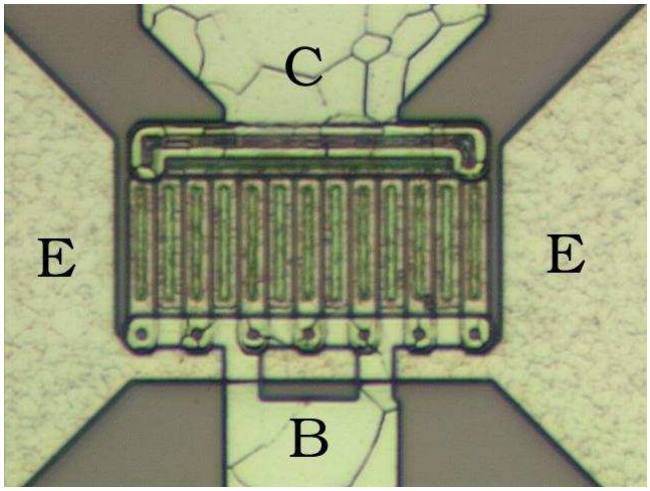


Figure 17: Layout of a multi-finger SiGe HBT with 6 emitter stripes, each $0.8\mu m \times 19.6\mu m$, 7 base contacts and one collector contact. This design shows low base and emitter resistances and moderate collector resistance and is therefore used in the LNA input stage of the GPS-LNA, UMTS-LNA and IS-95-LNA.

SiGe2-RF, announced end of 2000 [88], and SiGe2-Power are derivatives of a 2nd generation technology which uses *S*hallow *T*rench *I*solation *(STI)* rather than LOCOS to isolate devices. Together with narrow emitter stripes of 0.5 μm width (effective) this leads to higher f_{max} and 9 dB higher gain (MSG) at 5 GHz compared to SiGe1. In order to increase the current handling capability in SiGe2-Power, tungsten plugs allow for connections from metal 2 to the individual emitter stripes. In addition, the tungsten plugs enable stacked vias, so very compact layouts are feasible. The key parameters of the technologies are summarised in table 26 in appendix D.

4.3 SiGe1 model verification

In order to verify the models in Atmel's SiGe1 design kit, a thorough on-wafer characterization has been performed. As will be shown in section 6.6, the cascode configuration is

the key building block in the LNAs designed during this thesis. Therefore, rather than validating single transistors, typical LNA cascode cores, consisting of large, multi-emitter input devices (see Fig. 17), cascaded by smaller output devices, feedback from the output to the input together with the appropriate bias networks have been realized (see Fig. 18) and characterised. The small output device in common base configuration masks the large collector-base capacitance of the huge input device and makes cascodes nearly unilateral devices with very good reverse isolation ($S_{12} \approx 0$). This improves stability and makes parameter extraction easier, improving the overall model quality. As has been reported earlier [89, 90, 91, 92], bond pads shielded with a grounded metal layer at the RF input and output result in a defined parasitic capacitance of ≈ 80 fF, slightly higher than the capacitance of unshielded pads. However, as the spreading resistance of the substrate is absent due to the shield, the low residual series resistance of the metal shield leads to a high quality factor of these parasitic capacitances and they can easily be compensated by the matching networks. In addition, the reduced substrate loss of the input pad improves the LNA's noise figure. We found that the minimum NF of a 6-finger SiGe HBT at 2 GHz using shielded bond pads was 0.15 dB lower compared to an unshielded pad.

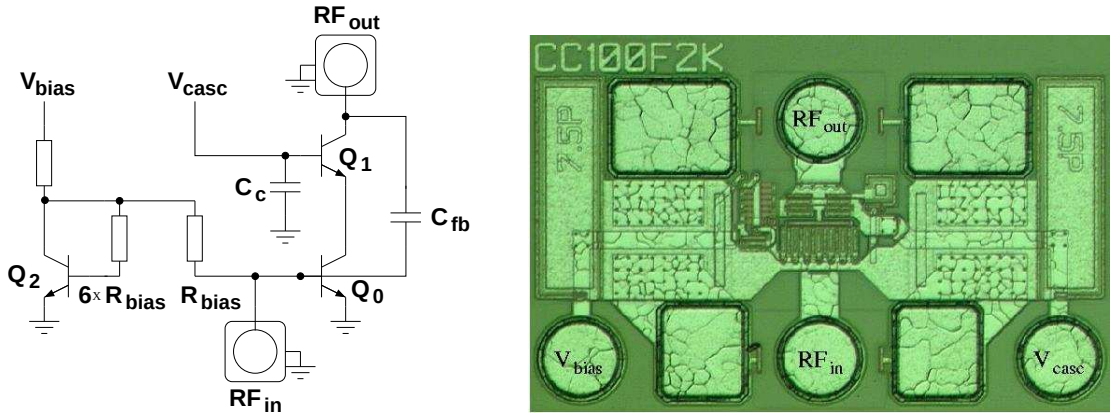


Figure 18: Schematic and layout of a typical LNA core, suitable for on-wafer characterization.

Very good agreement between measured and simulated small signal S-parameters and noise parameters was obtained for the cascodes. The slightly lower gain and reverse isolation is probably due to a deficiency in the MIM capacitor model for the small values of the feedback capacitor C_{fb} (note that the design in Fig. 18 uses a 0.1 pF capacitor): The model in the design kit uses the parallel plate equation and no fringing capacitances are considered.

The location of the source match for minimum noise figure (Γ_{opt}) is in reasonable agreement with the model, taking into account that the NP5 electronic tuner system at 2 GHz works at the lower limit of its frequency range. The measured minimum noise figure was lower than the simulated one (see Fig. 20), but NF_{min} is a strong function of current gain and base resistance, values which can strongly vary from wafer to wafer. The model-value

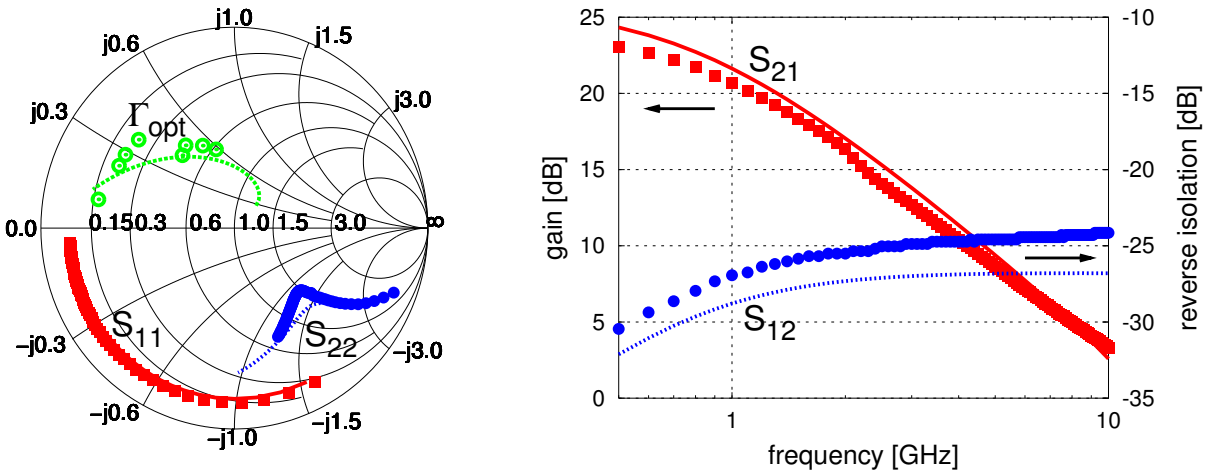


Figure 19: Measured (symbols) versus simulated (lines) S-parameters and noise parameters for an LNA core at V_{CC}=2.7V, I_{CC}=6mA. R_{bias} = 2kΩ and C_{fb}=100fF (see Fig. 18).

of h_{FE}=140 can be regarded as a worst case value but the target h_{FE}-value for SiGe1 is 180 (table 26), explaining the higher NF_{min} in the simulation. Anyway, as will be explained in appendix A, measurements of the absolute noise figure are associated with an error of at least 0.2 dB. Note that F_{min} of the 6-finger device itself as shown in Fig. 17 is 0.6-0.8 dB @ 2 GHz (depending on the wafer lot), which is superior to shrinked, pure silicon bipolar technologies with small feature sizes (e.g. 0.9 dB @ 2 GHz for Infineons's B6HF technology [93]). The degradation to the measured value of 1.1 dB @ 2 GHz in Fig. 20 is due to the additional noise contribution of the bias resistor in the current mirror of Fig. 18, which amounts to R_{bias}=2 kΩ in this example. As will be seen in section 6, higher values for this resistor (e.g. 4 kΩ) lead to a lower noise figure (Fig. 73), but degrade the linearity. Biasing using a discrete SMD inductor using the same 6-finger device (section 6.8.4) allows for the realisation of a complete LNA with $NF_{min} \approx$ 0.9 dB (Fig. 70) and a 50 Ω noise figure of 1.15 dB (Fig. 137). This shows the large influence of the bias network on the LNA's noise figure.

As the active device models were in reasonable agreement with the measurements, no bipolar modeling activities have been performed. Models of passive devices, however, either showed a large deviation from the measurements (spiral inductors) or have not been available at the beginning of the thesis (symmetrical inductors), which led to a large number of redesigns for design centering. Chapter 5 is therefore dedicated to the modeling of passive components on silicon.

In 2003 Schottky diodes[8] were added to the SiGe1 process to allow for the design of

[8]A Schottky diode is formed by a metal-semiconductor contact (e.g. an aluminium layer in contact with an n-type silicon substrate). It is named after the German physicist Walter H. Schottky, who in 1938

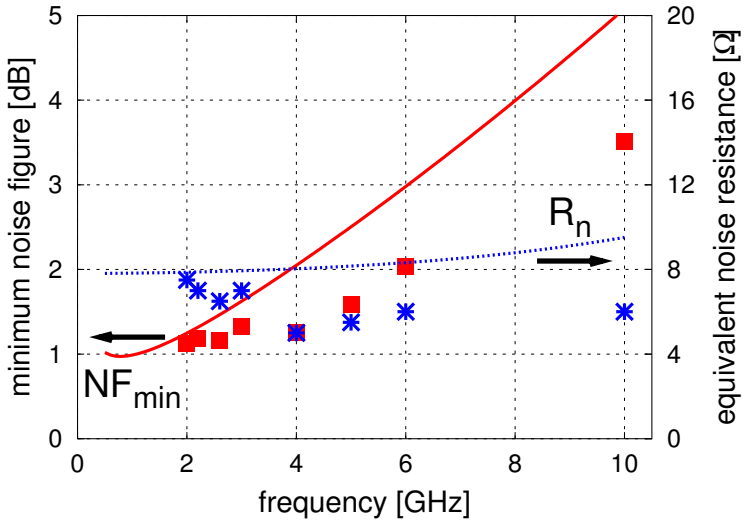


Figure 20: Minimum noise figure NF_{min} and equivalent noise resistance R_n of the LNA core of Fig. 19 (V_{CC}=2.7V, I_{CC}=6mA). At higher frequencies the measured NF_{min} is lower than the simulation as the actual base resistance is lower than modelled.

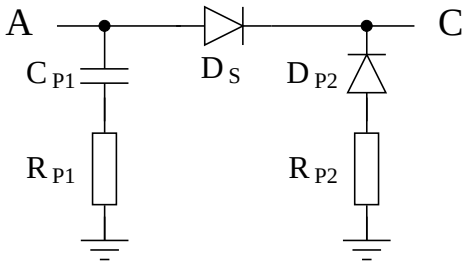


Figure 21: Equivalent circuit model of the Schottky diodes in Atmel's SiGe1 process.

power amplifiers with integrated power detectors. The models provided by Atmel had a high complexity and showed both poor agreement with the measurements (Fig. 22) and poor convergence behaviour in the circuit simulator. As the design of a diode ring mixer for the PMR front end required accurate diode models, a set of Schottky diodes of different width (40μm, 80μm, 160μm and 320μm) was realized in GSG configuration and characterised on-wafer. The simple model of Fig. 21 was able to describe the behaviour in forward and reverse direction (see Fig. 22): The anode consists of a Schottky contact of titanium silicide on the n-type silicon of the collector layer. A simple RC network C_{P1},

explained the rectifying behaviour of this kind of contact. The Schottky diode is electrically similar to a p-n junction, though the current flow in a Schottky is due to majority carriers having an inherently fast response [94]. Therefore it is used extensively for high-frequency, low-noise mixer and switching circuits, for example in automotive collision avoidance systems running at 77 [95], [96] and 120 GHz [97].

R_{P1} was sufficient to describe the shunt parasitics at this node. The cathode is formed by the buried layer which resides in the p-type wafer. Thus a reverse biased diode D_{P2} is required to model the capacitance which varies slightly with the applied voltage at this terminal. The detailed parameters of the model are summarised in table 7.

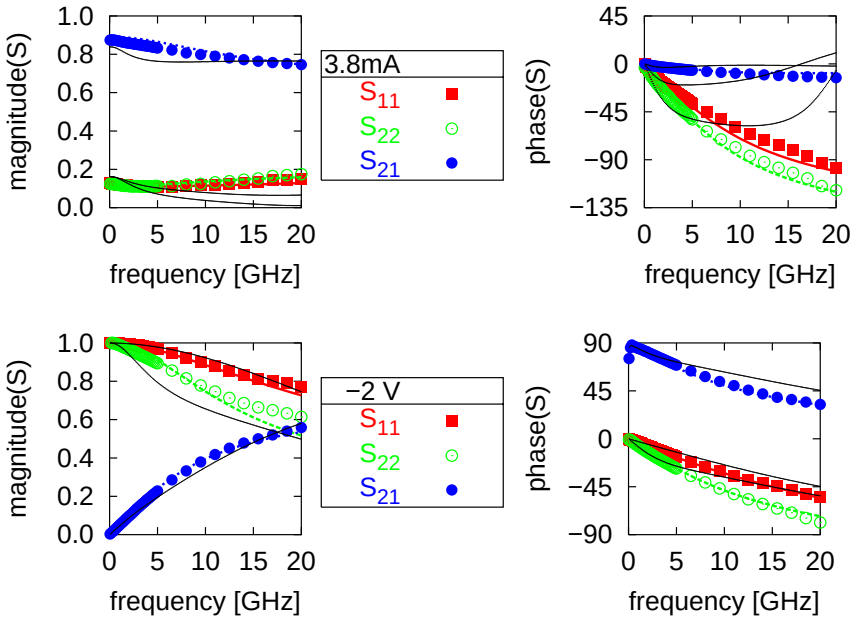


Figure 22: Measured S-parameters (points) versus scaleable model (lines) for a Schottky diode with 80μm width in forward direction (3.8 mA) and reverse direction (-2 V). The black lines indicate the poor agreement of Atmel's original model of the V5.1 design kit.

D_{P1}	series diode	$I_S = 1\mu A$, $R_S[\Omega] = 576/w[\mu m]$, $N = 1.15$ $C_{j,0}[fF] = 2.21 \cdot w[\mu m]$, $V_J = 0.18$, $M = 0.3$
C_{P1}	shunt capacitance	$C_{P1}[fF] = 0.149 \cdot w[\mu m] + 5.1$
R_{P1}	shunt resistance	$R_{P1}[\Omega] = 103/w[\mu m] + 88$
D_{P2}	shunt capacitance	$C_{j,0}[fF] = 0.76 \cdot w[\mu m] + 40$ $V_J = 0.5$, $M = 0.14$
R_{P2}	shunt resistance	$R_{P2}[\Omega] = 5360/w[\mu m] + 35$

Table 7: Scaleable model parameters of the circuit shown in Fig. 21.

4.4 at46000 SiGe BiCMOS process

Atmel's at46000 process is a SiGe BiCMOS process with 50 GHz-f_T SiGe HBTs and a 0.35 μm CMOS part (for details about the CMOS part see section 4.5). This process runs

in an 8-in fab in Colorado Springs (U.S.A) and is currently being installed in Rousset (France) as well. Compared to the bipolar processes of Atmel Heilbronn which were described in the last section, at46000 uses an AlCu (0.5% Cu) interconnect scheme with 3 or 4 metal layers, plus one 4μm thick layer of unroutable metal for thin film inductors (TFI) with a thickness of 4 μm and a resistance of just 8 m$\Omega/\square$ [98, 99]. Shallow trench isolation (STI) is used for device isolation and planarization is achieved by means of several chemical-mechanical polishing (CMP) steps. Filling procedures for both STI and metal filling applied after layout generation guarantee a homogeneous surface in order to achieve a reproducible lithography. Our measurements on several lots showed that the noise figure of at46000 HBTs is considerably higher than the NF of the HBTs in the bipolar processes, if devices with multiple emitter stripes of the same emitter area are compared (table 26). The equivalent noise resistance, R_n, is approximately twice for at46000 HBTs compared to SiGe1, pointing towards a larger base resistance. This is in contrast to an active base sheet resistance of just 500 $\Omega/\square$ and a SiGe base thickness of 135nm (including Si spacers) as cited in the design rule manual [99]. The reason for the higher NF might be problems with linking the intrinsic base to the external base contact.

4.5 Atmel's at46000 0.35μm CMOS technology

Within this thesis, RF CMOS test circuits have been designed using the 0.35μm CMOS part of Atmel's at46000 SiGe BiCMOS process. While this CMOS transistors with a gate oxide thickness of 69 Å, non-silicided gates and standard Aluminium interconnects are not as advanced as current leading edge 90 or 65nm devices using strained silicon and Copper interconnects [100, 101, 102], impressive figures of merit were achieved: A layout optimisation of these 0.35μm devices where the 20μm wide gate fingers have been contacted with metal on both sides and substrate contacts displaced to the periphery of the device improved the maximum frequency of oscillation f_{max} from 25 GHz to 60 GHz, which is better than the reported f_{max} of 50 GHz for a 0.5μm CMOS-on-sapphire process [103]. Together with an f_T of 22 GHz these devices are faster and have lower minimum noise figures than the SiGe HBTs available on at46000 (table 26). It needs to be noted, however, that this CMOS speed comes at the expense of high currents of $\approx$ 10-15 mA and gate voltages above 1 V. Minimum noise figures of sub-1dB at 1 GHz can easily be achieved. However, even with scaling of the device size, the source match Γ_{opt} to achieve this optimum noise figure is far from 50 Ω. Therefore a deviation of the source impedance from the optimum noise matching increases the noise figure considerably due to large value of the equivalent noise resistor R_n with values above 50Ω, originating from the large gate resistance of the non-silicided gates[9]. Using the BSIMv3.3 model supplied by Atmel's at46000 design kit as a core, a surrounding network of gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), drain-bulk capacitance (C_b), associated with a gate resistance and bulk resistances has been extracted from multi-bias S-parameter and noise measurements [104] according

[9]Note that R_n for a good SiGe HBT is just 6-8 Ω at 2 GHz, which considerably simplifies noise matching (table 26).

to the method of Enz [105].

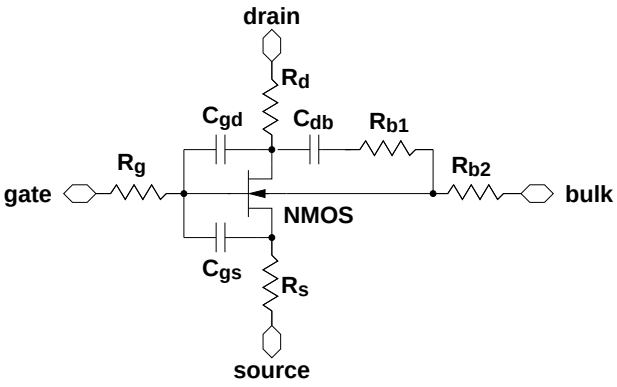


Figure 23: Large signal equivalent circuit of the 0.35μm MOS transistors using a BSIM3v3 core.

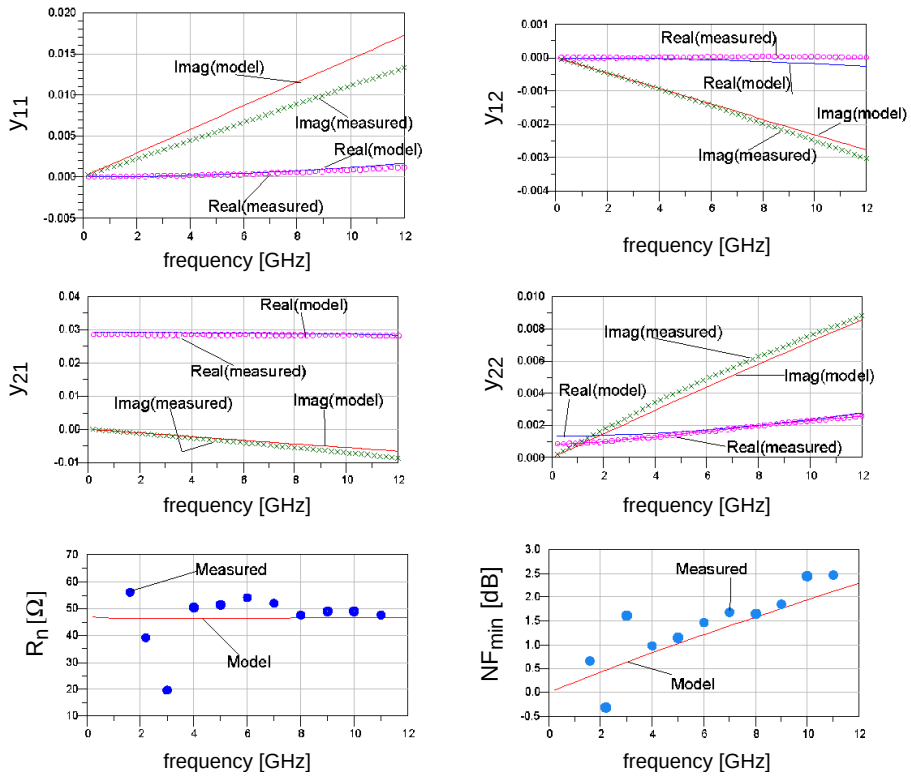


Figure 24: Modelled versus measured y-parameters, equivalent noise resistance R_n and minimum noise figure NF_{min} for a layout-optimised 8-finger NMOS device (w_{tot} = 8 × 20 μm, l_g = 0.35 μm, V_d = 2 V and I_{dd} = 7.5 mA).

The ohmic gate resistance of the MOS devices as extracted from the S-parameter mea-

surements was too small to model the large measured value of the equivalent noise resistor. A model using an equivalent voltage and current noise source was used instead.

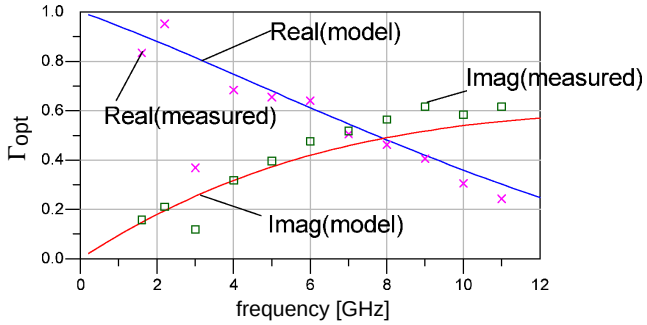


Figure 25: Modelled versus measured optimum noise reflection coefficient for a layout-optimized 8-finger NMOS device ($w_{tot} = 8 \times 20$ μm, $l_g = 0.35$ μm, $V_d = 2$ V and $I_{dd} = 7.5$ mA).

NMOS, at46000	Layout 1	Layout 2
gate length	0.35 μm	0.35 μm
Number of gate contacts	1 per 20 μm-finger	2 per 20 μm-finger
Bulk contacts	b-sgdgs-b-sgdgs-b-...-b	b-sgdgsgdgs...sgdgs-b
f_T	22 GHz	22 GHz
f_{max}	27 GHz	60 GHz
NF_{min} @ 2 GHz	2.1 dB	1.1 dB
R_n @ 2 GHz	50 Ω	20 Ω

Table 8: RF performance of 16-finger NMOS devices, 0.35μm × 20μm per finger, for two different layout versions at 15 mA (b=bulk,s=source,g=gate,d=drain).

4.6 Packaging

All ICs developed in this thesis have been evaluated on a printed circuit board (PCB) made from low-cost FR4. Just the UMTS-LNA – due to its ultra low noise figure – was evaluated on a PCB made from RO4003 material produced by Rogers Corporation. This PTFE-based material shows lower losses compared to traditional, epoxy-filled woven-glass laminates like FR4 and does not require corrections to be made to the measured NF value due to PCB losses. Most ICs have been packaged into MLF (*Micro*LeadFrame) packages from AMKOR Technology [106, 107] or QFN (Quad Flat-pack No-lead) packages from ChipPAC Incorporated (see Fig. 26), bonded with 1.0 mil (25.4μm), low-loop Au wire. Both are leadless packages where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB, instead of the conventional

formed perimeter leads. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB. Being 50% smaller in size compared to the TSSOP (Thin Shrink Small Outline Package) – which used to be the industry standard for RFICs for many years – the thermal performance improved up to 55% over TSSOP, and electrical performance (inductance and capacitance) improved 60% and up to 30% respectively over the TSSOP package [106]. While thermal considerations are not as important for our low-power receivers as they are for power amplifiers, they benefit from a low inductance to ground that can be achieved by several down-bonds in parallel onto the exposed paddle of the QFN and MLF packages (see Fig. 26). It is essential, however, to provide a good GND on the PCB itself by several through holes to the PCB's ground layer directly beneath the exposed paddle [108]. While the TSSOP package routes the IC pads to just 2 rows of pins, the QFN and MLF packages ease routing, as all four sides of the IC are accessible. As the smallest MLF or QFN package available was a 16 lead package, the UMTS-LNA had to be packaged into a TSSOP8 with exposed paddle. This solution provided a low inductance to ground, but the formed perimeter leads led to large inductances for the I/O pins. It was possible, however, to include these inductances into the matching networks (except for the supply pin, where an on-chip shunt capacitor to GND was used). Due to the low pad count of the GPS-LNA (6 pins including GND), an PLLP6 package was used which is hardly larger than a transistor package (see Fig. 101).

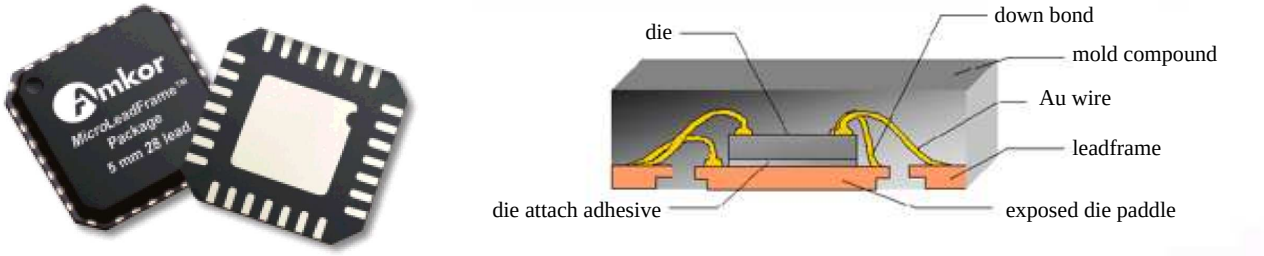


Figure 26: MLF package and cross sectional view of a mounted IC (Source: Amkor Technology [106, 107], ChipPAC Incorporated)

5 Modelling of passive components

5.1 Passive components on Silicon substrates

As high speed silicon based semiconductor processes like Si-BJT, BiCMOS, SiGe HBT, RF CMOS and SiGe HFET keep on increasing their operating speed, many applications that had been a domain of compound semiconductors like GaAs, GaInP or InP are now being served by RF integrated circuits fabricated using silicon technologies [109]. Examples include low noise amplifiers, down converters, VCOs, up converters, and power amplifiers for DECT, GSM, GPS, WLAN and Automotive radar [78].
Si-based technology – beside the lower production cost – offers the advantage of integrating additional functionality like control logic, PLLs, IF filtering, and ADCs/DACs on the chip. It becomes increasingly important to include matching components like MIMs and spiral inductors onto the IC in order to save real estate on the PCB. At higher frequencies due to the package parasitics many applications are enabled by integrated passive components. Applications for passive LC networks are (but are not limited to)

- Narrowband impedance matching networks in LNAs and PAs (see chapter 6)
- Low noise series inductive feedback in all kind of amplifiers and mixers (see chapter 6 & 7)
- LC tanks for VCOs and tuned loads in amplifiers
- To a lesser extent on chip filtering at RF frequencies (e.g. image rejection filters)
- Differential to single-ended conversion and vice versa using on chip transformers.

5.2 Lumped element circuit design

Circuit designs using resonant tanks, LC matching networks, inductive degenerations, etc., made from *lumped* elements rather than synthesising them with open and shorted transmission lines are a popular design solution in Si RFICs and MMICs [109]. While transmission line circuits are often used in III-V MMICs, lumped element circuits offer better performance on lossy Si substrates for frequencies up to approximately 24 GHz [110, 111, 112, 113, 114, 115, 20] while consuming less chip space than distributed designs [96, 116, 117, 118, 119][10]. Using reactive loads instead of resistive ones allows for higher headroom leading to high linearity at low supply voltage and low current consumption (see section 6.7.2). Accurate models of these components are essential for first-time design success ("first-time-right"). The models need to be scaleable with respect to the

[10] At higher frequencies, e.g. for 77 GHz automotive radar applications, thin-film microstrip lines are used, where the bottom metal layer effectively shields the field distribution from the lossy substrate. This technique is not considered in this thesis, as the frequency range is beyond the scope of this work.

physical geometries in order to allow for fine-tuning of the circuit designs. As popular design environments like Cadence FW2 are based on time-domain-simulators, no frequency dependent elements should be included and the models should be fully SPICE compatible. The models for spiral inductors which had been available at the beginning of the thesis in the design kits of Atmel's SiGe1 and SiGe2 processes lacked accuracy and greatly overestimated the quality factor. The quality factor Q is a measure for an inductor's energy (magnetic energy - electric energy), over the energy dissipated in its metallisation resistance and the conducting substrate (for a detailed definition of Q, see [120] and section 5.6.). The error in the inductance itself was as large as 30%. This required that many circuits, e.g. the LNAs for UMTS and GPS, were realised with several versions on one reticle with slightly different matching networks in order to get one design which is close to the specification (see chapter 6). For components like symmetrical inductors, no models have been available, leading to time-consuming trial-and-error in the design of the mixers (see chapter 7). The author hopes that this modelling work may lead to better agreement between simulated and measured circuit design results, less redesigns and reduced development costs.

5.3 Loss mechanisms of passive components on silicon

It is a common belief that the major challenge of integrating passive components into Si-based processes is the lossy silicon substrate with a specific resistance of $\zeta = 10 - 20\,\Omega \cdot cm$ for bipolar processes and $< 5\,\Omega \cdot cm$ for CMOS processes: At higher frequencies substrate currents limit quality factors of integrated inductors due to I^2R losses to approximately 5-10 [121, 122]. As explained in [123], these currents can be divided into two classes – those conducted through metal-substrate capacitances associated with individual turns of the spiral and circulating eddy currents due to magnetic fields within the substrate. For moderate substrate resistivity ($\rho = 10 \ldots 30\,\Omega \cdot cm$), eddy currents can be neglected and currents conducted through the field oxide into the lossy substrate represent a major loss mechanism [123]. Suspended inductors on a cavity etched underneath through surrounding via holes have been used in the past to reduce substrate loss and hence increase the quality factor of large-value integrated inductors on a CMOS substrate [91, 124, 125, 109], but this technique did not become a mainstream process due to concerns about the stability of the membrane[11]. In section 5.11 we examined suspended inductors realised by backside etching on SiGe2-Power and SiGe2-RF processes and came to the conclusion that etched cavities make sense for large inductors only ($2\pi f \cdot L > 50\,\Omega$, where f is the operating frequency). To reduce inter stage matching losses of power amplifiers and bipolar LNAs and mixers, however, *small* inductors ($2\pi f \cdot L < 50\,\Omega$) are required, due to

[11] Recently, techniques have been presented that transfer a fully processed silicon wafer onto a low-loss glass substrate or even a flex foil by using a substrate transfer process with removal of the lossy silicon substrate at a delamination layer like the buried oxide of a SIMOX wafer [126, 127], resulting in values for the quality factor of up to 40. Proton implantation selectively below passive structures – a method originally used for GaAs HBT isolation – can create semi-insulating ($\approx 10^6 \Omega \cdot cm$) Si layers and increases the Q factor for 5-15 nH inductors by 30-60% [128].

the low impedance levels in PAs and LNAs. Here an improvement can only be achieved with lower metal sheet resistivity. Indeed, when modelling the passive components in this thesis, frequency-dependent conductor losses turned out to play an important role in optimising inductors. Since the invention of the Si-IC technology, Al-interconnect systems on SiO_2 field oxide have been used (see Fig. 29). The rule of thumb for such kind of inductors is a series resistance of $1\,\Omega/nH$, which limits the quality factor Q at lower frequencies to $\approx 2\pi \cdot f[GHz]$. Moving into the sub-micron arena, the resistance-capacitance (RC) delays become so severe that circuit performance is often limited by the interconnects rather than by the active devices itself. Gold interconnects have been mainly limited to III-V electronics, as gold, as an impurity, forms a deep trap within the silicon band gap. Changing from aluminium to copper reduces the specific metal resistance by approximately 40%, but this is not necessarily good news for the quality factor of integrated spirals: In order to preserve a reasonable aspect ratio in these sub-μm interconnects, the copper thickness deposited by the damascene process is kept low. For a $0.13\,\mu m$, digital CMOS process this results in sheet resistances between $70\,\frac{m\Omega}{\square}$ for metal 1-4 and $40\,\frac{m\Omega}{\square}$ for the top copper layer [129], which is considerable higher compared to the values of the Atmel-SiGe processes (Fig. 29). As copper forms a dense oxide which cannot be removed by the ultra-sonic movements of the wire bonder, a top aluminium layer is sputtered to realise the bond pads. Design rules, however, often do not allow routing in this Al layer. The first IBM Cu/SiO_2 $0.25\,\mu m$ process came to market in 1998. Back end of line (BEOL) processes featuring a $4\,\mu m$ thick Cu layer on top of an additional $2\,\mu m$ Oxide have been reported that show Q-values of 24 for a $2.8\,nH$ inductor [130]. It remains to be seen, however, whether this additional post processing steps will make it into commercial products or not.
Low-k dielectrics (whether spin-on organics or vapour-phase deposited inorganics) [131] have been even slower to market, and are only now beginning to be seen in commercial products at the $0.13\,\mu m$ node [132]. Moisture absorption and material shrinkage used to be a problem of many of these low-k dielectrics. Bencocyclobutene, or BCB, commercialised by Dow Chemicals, now seems to play a strong role due to its low curing temperature and its inherently planarizing properties, which eliminates the need of expensive chemical-mechanical polishing (CMP) steps. High resistivity silicon substrates with $\rho \approx 1\,k\Omega \cdot cm$ are used for some applications where increased crosstalk due to reduced junction isolation may be tolerated [117]. As can be seen in section 5.9, due to the need of substrate contacts in an IC, the difference in quality factor between inductors on $20\ \Omega \cdot cm$ and $1\ \mathrm{k}\Omega \cdot cm$ is not very pronounced.
In this work we concentrate on the modelling of passive components for Atmel's SiGe1 and SiGe2-RF bipolar processes which use standard Al metallisation (with traces of Si and Cu) on SiO_2 dielectric.

5.4 Spiral inductors in the Atmel SiGe1 and SiGe2 processes

For the past 20 years, CMOS chip design has been primarily based on the *de facto* industry standard 'Manhattan' architecture, named for its right-angle interconnects resembling a

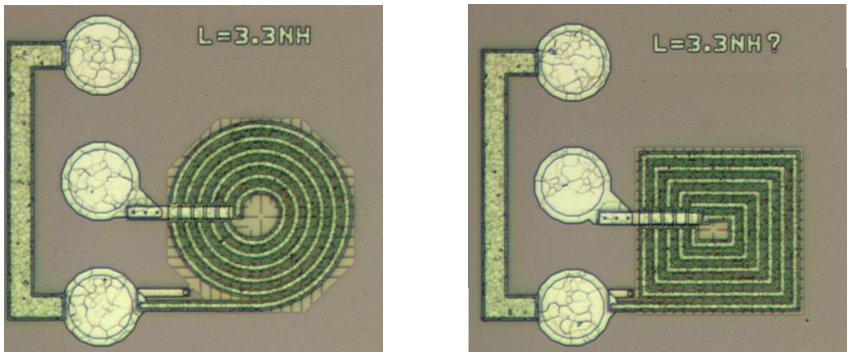


Figure 27: Round spirals (left) show a quality factor improvement of 10% over rectangular, 'Manhattan'-type inductors (right).

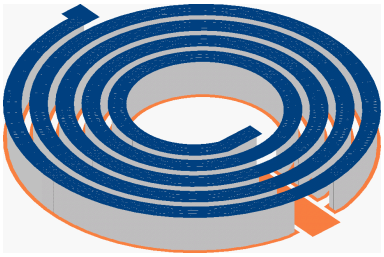


Figure 28: Cross sectional view of a spiral inductor in Atmel's 50 GHz SiGe bipolar process. For better visibility, the z-axis is scaled. The bottom metal (orange) is used for the feed through (underpass) and to reinforce the top metal (blue) in order to reduce series resistance.

city street grid. In CMOS technologies this has led to rectangular implementations of on-chip spiral inductors. In Atmel's bipolar technologies we are not limited to a 'Manhattan'-type of routing and the layout generator synthesises a round spiral inductor from semi arcs (see Fig. 28). Using test structures as shown in Fig. 27, we found that the Q-factor of round spiral inductors is 10% higher than the Q of their rectangular counterparts for comparable inductance. With respect to area consumption there is no benefit of using rectangular shapes. Improvements of the auto routing algorithms used during CMOS layout generation have led to the formation of an industry consortium called the 'X Initiative' consisting of major semiconductor manufacturers. This consortium pushes the 'X Architecture' which routes metals 1-3 in a 'Manhattan' style and rotates the primary direction of the interconnect in the fourth and fifth metal layers by 45° [133], requiring less total wire length and a lower via count. Its likely that octagonal inductors will become prevalent in CMOS layouts within a few years.

In the past a typical procedure to obtain simulation models for spiral inductors was to realise an array of inductors in a configuration suitable for on-wafer probing. After the S-parameters [134] have been taken they are de-embedded for pad and feed line parasitics

(see section C.3). The disadvantages of that procedure are

- long lead times in the range of 2 to 6 months due to layout process and wafer fabrication
- inaccuracies in the determination of R_S due to high contact resistances between the on-wafer probes and the aluminium pads, which are covered by a natural oxide
- high costs associated with mask fabrication and wafer processing.

In order to improve design efficiency, electromagnetic (EM) field simulation will finally make most of these arrays of spiral inductors obsolete. In order to rely on the simulated results, the proper simulator needs to be chosen and – even more importantly – it needs to be fed with a consistent set of technological data to correctly reproduce the measured data. It was one of the main targets of this thesis to set-up a consistent set of substrate parameters, choose the appropriate simulator and derive scaleable closed-form equations for the most commonly used passive components. The EM simulation setup was checked against measurements by realising several test arrays of spiral inductors on multiple multi-project wafer runs (MPWs) in Atmel's SiGe1 and SiGe2 processes. Data for the metallisation stack was provided through the design kits. An example is shown in Fig. 29.

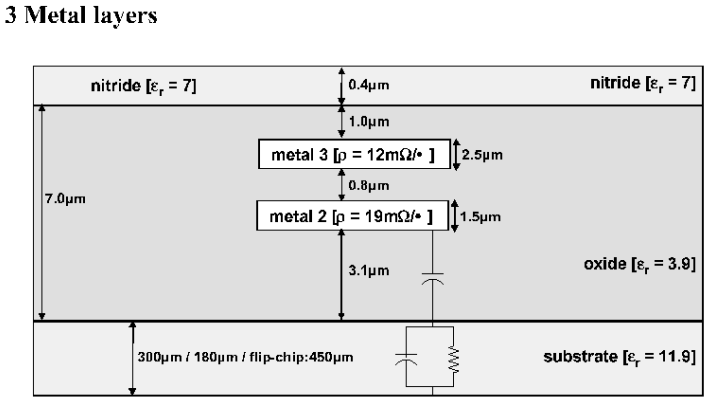


Figure 29: Schematic view of the metallisation system used in Atmel's SiGe1 process, provided that no first metal is used.

Initially simulated Q-factors differed from measured ones. Therefore wafers have been cross-sectioned as shown in Fig. 30 to check the values shown in Fig. 29. The cross-sections confirmed these values and the reason for the discrepancy has been identified within the EM simulation: As will be discussed in detail in section 5.13, the initial layer setup in the EM simulator was not appropriate so simulate the current crowding within the conductor (proximity effect) correctly (see Fig. 48).

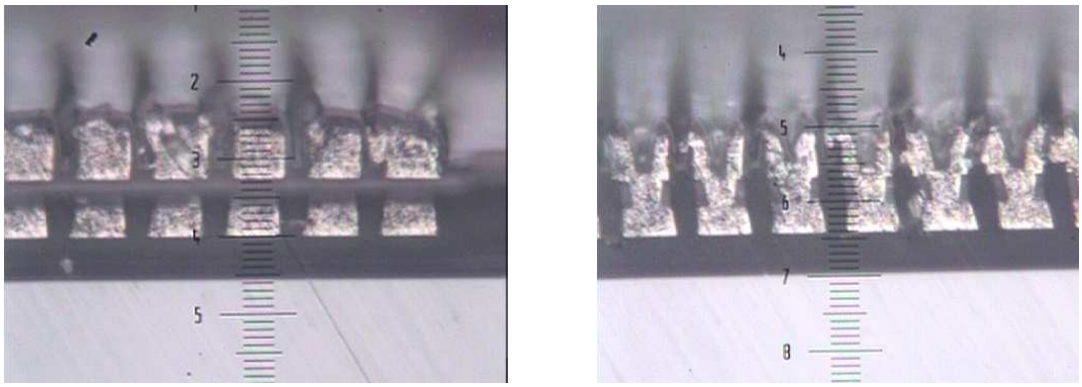


Figure 30: Left: Cross sectional view of an inductor composed of metal 2 and 3. To obtain a clearer cut, the wafer was grinded with an angle of 30° in y-direction . Y-scale is therefore $0.5\mu m$ per tick mark $\{\sin(30°) = 0.5\}$, while x-scale is $1\mu m$ per tick mark. The cross-sectional cut confirms the data provided by Atmel (see Fig. 29). Right: Cross sectional view of an inductor with metal 2 and metal 3 connected by continuous via holes. As can be seen from the figure, the SiGe1 technology uses no CMP techniques to planarise the metallisation system.

In the Atmel design kit, in order to reduce the series resistance of the Al traces, two layers of metals are shunted in parallel [109] by either continuous long-vias or circular vias placed in 90°,45°,22.5° or 11.25° segments (see Fig. 37). Metal layers 2 and 3 are used to decrease the distance from the lossy silicon substrate [135], but cost-sensitive products like the CDMA chipset shown in Fig. 3 omit the 3rd metal layer and use just metal 1 and 2 for the coil. As will be shown later, shunting 2 or more metal layers in parallel improves the quality factor for 'small' inductors, where metallisation losses dominate the overall loss. We found that 'large' inductors can be improved by routing them in the top metal only, as this decreases the oxide capacitance and hence the substrate losses. The terms 'small' are used for inductors where the operating frequency is considerably below the frequency of peak-Q and 'large' for coils that are operated close to the frequency of peak-Q. Due to this results Atmel modified the layout generator to allow for the realisation of inductors in a single, top metal layer, in addition to the stacked types used previously.
The maximum quality factors measured for Atmel's SiGe-bipolar processes are around 10 for a 4.5 turn, 2.2 nH inductor and therefore comparable to what has been published for aluminium inductors on lossy silicon substrates [136].

5.5 Equivalent circuit extraction

For the evaluation of spiral inductors and the comparison between measured and EM-simulated data, the S-parameters were separated into the single-π network of Figs. 31,32[12].

[12] Note that this simple model is not suited for implementation into CAD packages, as it contains frequency dependent quantities such as the series inductance and the series resistance. The lumped

This was necessary, as plotting different sets of S-parameters (S_{ij}, $i, j = 1, 2$) would not reveal the differences, as inductors with largely different Q-factor may have almost identical S-parameters. Therefore, in order to compare measured with simulated data or to fit scaleable models to target data sets, no S-parameters have been used directly. Instead, they have been used to extract the elements of the single-π model which allows for an accurate comparison of different data sets plus the single-ended quality factor Q defined by Eqn. 36. The elements describing the parasitics of the spirals are

1. A series resistance R_S that increases with frequency due to the skin effect and proximity effect (see Fig. 48)
2. A capacitance C_P that describes the capacitance between adjacent turns
3. Two RC networks that model the lossy substrate, where R_{sub1} and R_{sub2} are in the order of 700 Ω for a 20 $\Omega \cdot cm$ substrate with a wafer thickness of 180 μm. C_{ox1}, C_{ox2}, C_{sub1} and C_{sub2} increase with respect to the area of the coil. For inductors with patterned shields (PGS), R_{sub1} and R_{sub2} may be in the 0 – 40 Ω range (see section 5.12). Magnetic substrate currents (eddy currents) are neglected (see section 5.3).

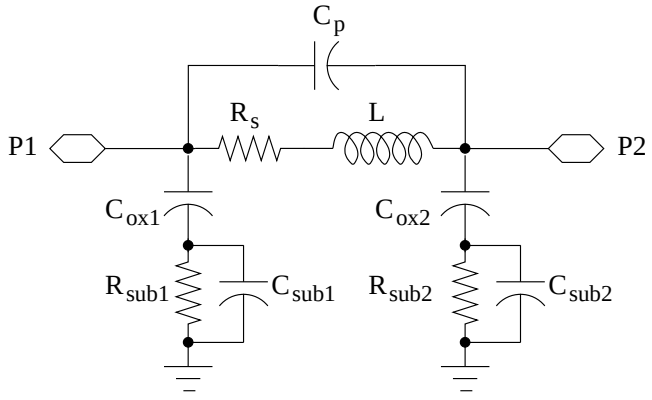


Figure 31: Physical equivalent circuit model of a lossy spiral inductor [137, 138, 139]. The frequency dependent R_S will later be modelled by an "RL+R//L" ladder circuit (Fig. 53).

According to Pfost *et al.* [140, 141], the following equation holds for a given lossy dielectric

$$R_{Sub} \cdot C_{Sub} = \rho \cdot \epsilon_{Diel.} \tag{25}$$

where $\epsilon_{Diel.} = \epsilon_r \cdot \epsilon_0$ with the vacuum permittivity $\epsilon_0 = 8.85 \cdot 10^{-12} F/m$. A substrate corner frequency f_c can be defined as

element model implemented in SPICE syntax as shown in Fig. 53 will be described in detail in section 5.15.

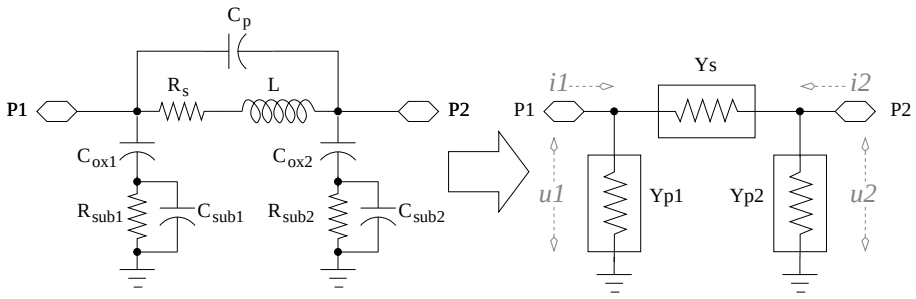


Figure 32: The equivalent circuit of Fig. 31 separates into a π-network [139]

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{Sub} \cdot C_{Sub}} = \frac{1}{2 \cdot \pi \cdot \rho \cdot \epsilon_{Si}} \tag{26}$$

which amounts to 7.6 GHz for silicon substrates ($\epsilon_r = 11.9$) with a conductivity of $\rho = 20\ \Omega{\cdot}cm = 0.2\,\Omega{\cdot}m$ ($\sigma = 1/\rho = 5\,S/m$). Extracting the substrate networks R_{Sub}, C_{Sub} for different measured and simulated inductors shows an amazing agreement with Eqn. 25. This means that Eqn. 25 can be used in both the parameter extraction and the scaleable model, allowing to calculate C_{sub1} (or C_{sub2}) from R_{sub1} (or R_{sub2}).
The remaining values for the equivalent model in Fig. 31 can easily be extracted from the S-parameters: Rather than fitting the parameters L, R_S, C_P, C_{ox1}, C_{ox2}, R_{sub1}, R_{sub2}, C_{sub1} and C_{sub2} to the 2-port S-parameters, it is easier to separate the series and shunt conductances according to Fig. 32.

$$\begin{aligned} i_1 &= Y_{P1} \cdot v_1 + Y_S \cdot (v_1 - v_2) && (27)\\ i_2 &= Y_{P2} \cdot v_2 + Y_S \cdot (v_2 - v_1) && (28) \end{aligned}$$

In matrix form this can be rewritten to

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{P1} + Y_S & -Y_S \\ -Y_S & Y_{P2} + Y_S \end{bmatrix} \times \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{29}$$

This means that it makes sense to transform the measured or simulated S-parameters into Y-parameters. Computing

$$Y_S = -Y_{21} = -Y_{12} = -\frac{Y_{21} + Y_{12}}{2} \tag{30}$$

leads for low frequencies to (see Fig. 144)

$$L = \frac{1}{2 \cdot \pi \cdot f} \cdot \Im\left[\frac{1}{Y_S}\right] \quad \text{and} \quad R_S = \Re\left[\frac{1}{Y_S}\right] \tag{31}$$

C_p may then be derived by fitting Y_S to $j \cdot \omega \cdot C_p + \frac{1}{R_S + j \cdot \omega \cdot L}$ over the full frequency range (Fig. 33).

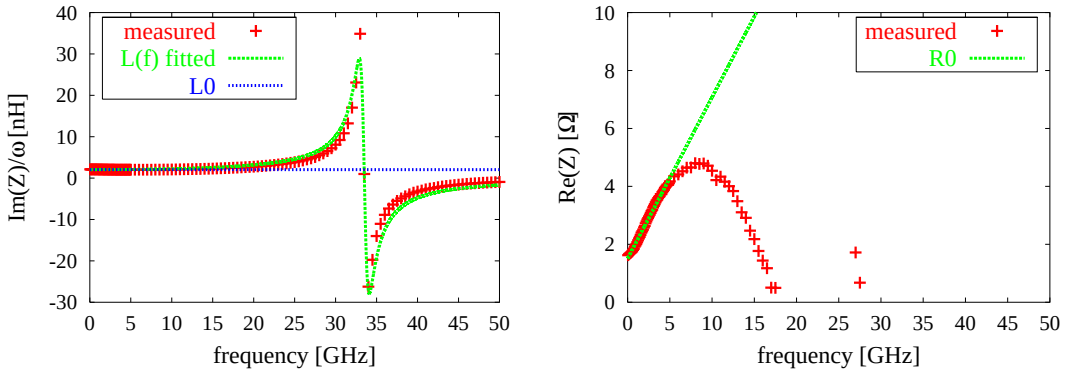


Figure 33: L_0 is extracted from $\Im[1/Y_S]$ at low frequencies, while C_P is fitted to model the resonance across the complete frequency range (left). R_S is determined by extrapolating $\Re[1/Y_S]$ towards zero frequency (right).

The substrate networks can be expressed as

$$Z_{P,i} = \frac{1}{Y_{P,i}} = \frac{1}{Y_{ii} + (Y_{12} + Y_{21})/2} \tag{32}$$

$$= \frac{1}{j\,\omega\,C_{ox,i}} + \frac{R_{sub,i}}{1 + j\,\omega\,R_{sub,i} \cdot C_{sub,i}} \tag{33}$$

with $i = 1, 2$. Using the relation 26, the substrate resistances can be obtained by fitting the real part of Eqn. 33 over the complete frequency range[13]:

$$\Re[Z_{P,i}] = \frac{R_{sub,i}}{1 + (f/f_c)^2} \tag{34}$$

The substrate capacitances $C_{sub,i}$ follow from Eqn. 25 and the oxide capacitances $C_{ox,i}$ may be obtained from the imaginary part of Eqn. 33 at low frequencies.

5.6 Definition of the 'quality factor'

The quality factor Q is a measure for an inductor's energy (magnetic energy - electric energy), over the energy dissipated in its series resistance and the substrate networks. Defined by $Q = \Im[Z]/\Re[Z]$, it depends on how the inductor is operated in a circuit.

[13]This is advantageous, as the low-frequency value of Eqn. 34 cannot be properly obtained from measurements, as the impedance of the substrate networks becomes infinite at low frequencies due to C_{ox}.

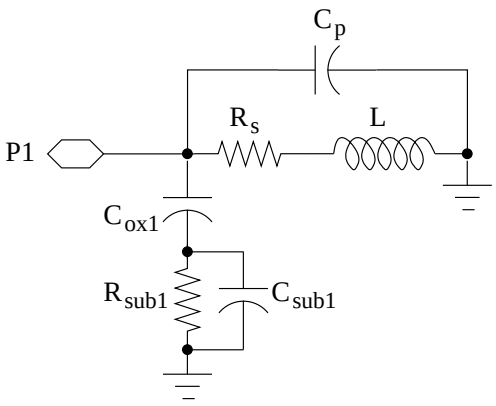


Figure 34: Definition of the single-ended quality factor Q_1

Spiral inductors are often operated with one side AC grounded (shunt inductance to GND or the supply voltage, e.g. Figs. 71, 72, 82, 87, 92, 99, 101, 120). From Fig. 34 its clear that this shorts one substrate network and that the remaining admittance is $Y_{P,1} + Y_S = Y_{11}$ (if port 2 is grounded) and $Y_{P,2} + Y_S = Y_{22}$ (if port 1 is grounded). Thus the single-ended quality factor is defined as [120]

$$Q_1 = \frac{\Im(1/Y_{11})}{\Re(1/Y_{11})} = -\frac{\Im(Y_{11})}{\Re(Y_{11})} \tag{35}$$

$$Q_2 = \frac{\Im(1/Y_{22})}{\Re(1/Y_{22})} = -\frac{\Im(Y_{22})}{\Re(Y_{22})} \tag{36}$$

For a discrete, wire wound inductor this quality factor reduces to $Q_1 = Q_2 \approx \frac{\omega \cdot L}{R_S}$. For a spiral on a lossy substrate, R_S determines Q_1 at low frequencies and R_{sub1} and C_{sub1} determine its roll-off at high frequencies (see Fig. 35). The frequency where the peak Q occurs is in between these two extremes. Peak Q itself is extremely sensitive to S-parameter accuracy: Slight deviations that are barely visible in the S-parameters of both measurements and simulation lead to large differences in peak Q. The reason is that at intermediate frequencies the real part in the denominator is still determined by R_S which is small compared to $2\pi f \cdot L$ (see Fig. 34).

As can be seen for the measured 2.1 nH inductor of Fig. 35, for an asymmetric layout Q_1 is different from Q_2. Also, the quality factor for a balanced driven coil is higher than its single-ended counterpart where one substrate network is grounded and the other driven at full voltage swing: Under balanced conditions, *both* substrate networks are driven, but with *half* the voltage swing. To derive the equation for balanced Q, for the moment we assume the equivalent circuit not to be a π-circuit but of a T-form (which is mathematically possible [142], but physically makes no sense). Due to the balanced condition, $i_1 = -i_2 = i$ and the current from the shunt impedance to GND is 'zero'. Writing [142]

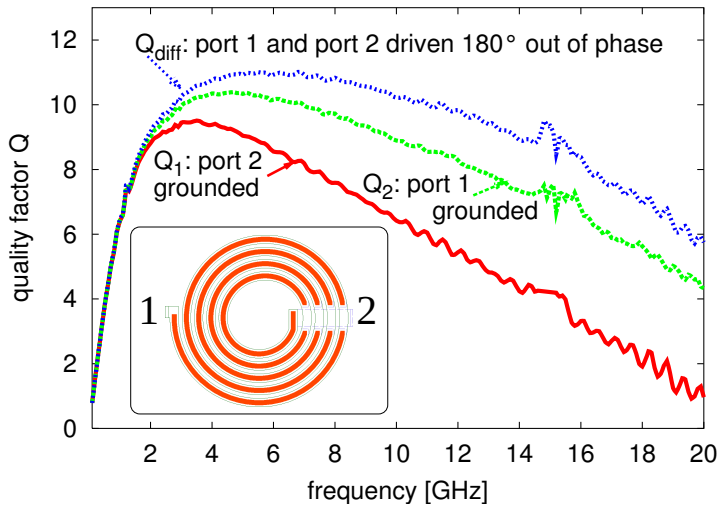


Figure 35: Due to the inequality of the substrate networks, different single-ended Q-values can be obtained, depending on the spiral configuration

$$v_1 = Z_{11} \cdot i_1 + Z_{12} \cdot i_2 = (Z_{11} - Z_{12}) \cdot i \tag{37}$$
$$v_2 = Z_{21} \cdot i_1 + Z_{22} \cdot i_2 = (Z_{21} - Z_{22}) \cdot i \tag{38}$$

The balanced impedance is therefore

$$Z_{bal} = \frac{v_1 - v_2}{i} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \tag{39}$$

leading to the definition of the balanced inductance and balanced Q:

$$L_{diff} = \frac{\Im(Z_{11} - Z_{12} - Z_{21} + Z_{22})}{2\,\pi\,f} \tag{40}$$
$$Q_{diff} = \frac{\Im(Z_{11} - Z_{12} - Z_{21} + Z_{22})}{\Re(Z_{11} - Z_{12} - Z_{21} + Z_{22})} \tag{41}$$

5.7 The choice of the metal layers

When realising inductors in an integrated semiconductor process, the first degree of freedom usually is in the choice of the metal layers. It makes no substantial difference to the *inductance* whether a single metal layer (e.g. top layer) is used, or whether several metal layers are shunted in parallel to reduce the series resistance.

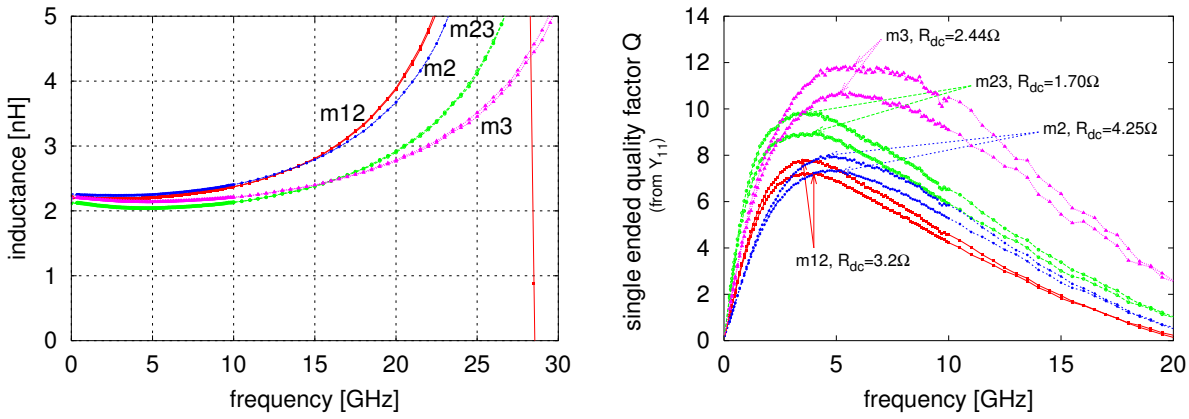


Figure 36: Extracted from S-parameter measurements, spiral inductors of the same geometry ($w = 7\mu m$, $s = 3\mu m$, $n = 4.5$, $r_i = 26\mu m$) using different metal layers show little difference in their inductances (left) but vary substantially in the value of their quality factor and self-resonance frequency (SRF, frequency of maximum Q) (right). m12 denotes a spiral routed parallel in metal 1 and 2, m23 a spiral in metal 2 and 3, and m2 and m3 spirals in metal 2 and metal 3, respectively.

Fig. 36 shows slightly *larger* inductance values for *thinner* metal layers (e.g. m2) compared to coils realised with thicker metal (e.g. m12 = m1+m2, m3, or m23 = m2+m3). Also, while the inductance from zero frequency for coils with thin metals remains virtually flat, for thicker metal layers there is a considerable drop in inductance at frequencies around 5 GHz. The reason will be explained by EM simulation in section 5.13 to be the current crowding effect, which – for higher frequencies – pushes the current towards the inner margin of the turn, except for the outermost turn, where the current is pushed to the outer margin (see Fig. 48). This effect at higher frequencies on average reduces the size of the inductor compared to its geometrical size and is more pronounced for thick metals. At lower frequencies, the Q-factor is dominated by the series resistance and benefits from using a thicker metal. At frequencies above peak-Q, it is more favourable to use only the top metal layer and move the inductor as far away from the lossy substrate as possible in order to reduce substrate losses. To show the influence of the measurement accuracy, Figs. 36 have been performed with 2 subsequent on-wafer calibrations: While there is virtually no influence on inductance, the quality factor is extremely sensitive to slightest changes in S-parameters.

5.8 Influence of the via geometry

The effect of via geometry on the performance of multilayer inductors with 2 metal layers shunted in parallel was less pronounced than expected. For the Atmel SiGe1 process, where no CMP is used, the standard *continuous* via hole (Figs. 37, right) has a slightly

lower quality factor and higher series resistance than configurations which connect the two layers only at the critical points in the layout (e.g. the underpass) (Figs. 37, left).

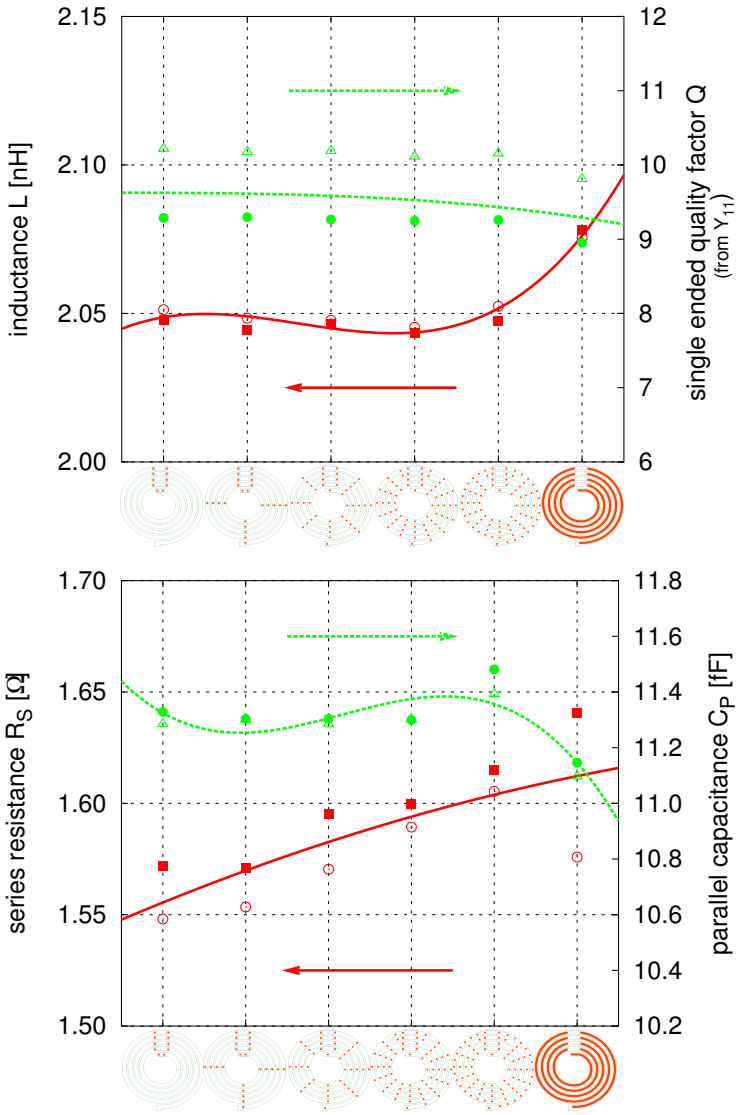


Figure 37: From on-wafer measurements, virtually no influence of the via configuration on the inductance can bee seen (left: few circular vias, right: continuous via). The slight changes in quality factor are due to variations in series resistance.

5.9 Inductors on high resistivity substrates

In the literature, high-resistivity (HR) silicon is reported to result in superior RF performance of passive components compared to standard silicon [95, 96, 116, 117, 143, 144].

While this might be true for distributed elements like coplanar and microstrip lines, the effect on the quality factor of a $2nH$ inductor was disappointing:

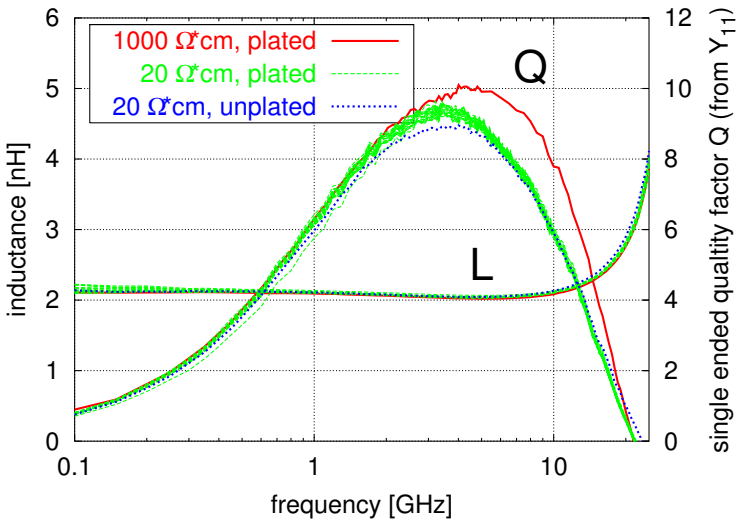


Figure 38: For frequencies up to $f_{peak}/2$, Q-factor is identical for inductors on 1 k$\Omega \cdot cm$ and 20 $\Omega \cdot cm$. The higher substrate resistance of the high-impedance substrates just allows for a slightly higher peak-Q.

As can bee seen from Fig. 38, a mere 10% of improvement in Q and a shift of peak-Q to slightly higher frequencies will usually not justify the higher cost and lower isolation performance between active devices associated with high-resistivity (HR) silicon[14]. In addition, HR material tends to lose its high resistivity properties during high-temperature semiconductor manufacturing processes [109]. Also, HR material cannot be Czochralski-grown but needs to be fabricated using the float-zone (FZ) technique [109]. In section 5.11, it will be shown that *large* inductors benefit from a *complete* removal of the silicon underneath, while the loss of small and medium sized inductors is mainly governed by the losses in the metallisation system.

5.10 The channel stopper

In all Atmel design-kit inductors the p^+ channel stopper (CS) implantation, which prevents leakage currents between adjacent n^+ wells, is blocked below the inductors. Due to the small difference in Q between standard 20 Ω·cm and 1 kΩ·cm material, an n inversion layer was believed to form on top of the HR silicon. However, DC measurements between

[14]What can also be seen is that there is virtually no difference between 20 measurements on a wafer with probe pads plated with gold (1 measurement per reticle) and a measurement on an unplated wafer. This shows the high uniformity of the SiGe-1 process and the absence of contact problems using Cascade infinity probes. For details on how to obtain reproducible on-wafer measurements, see appendix C.

n^+ wells in areas without CS showed that no such inversion layers existed. Finally the RF measurements shown in Fig. 39 have been performed to preclude the existence of an inversion layer below the inductor: With an inversion layer being present, there would have been an *in*crease in Q from the configuration to the left (CS completely removed) to the configuration to the right (CS more and more slotted). As this is clearly not the case, the evidence of an inversion layer below the inductors was ruled out. The optimum configuration was an inductor with no channel stopper below.

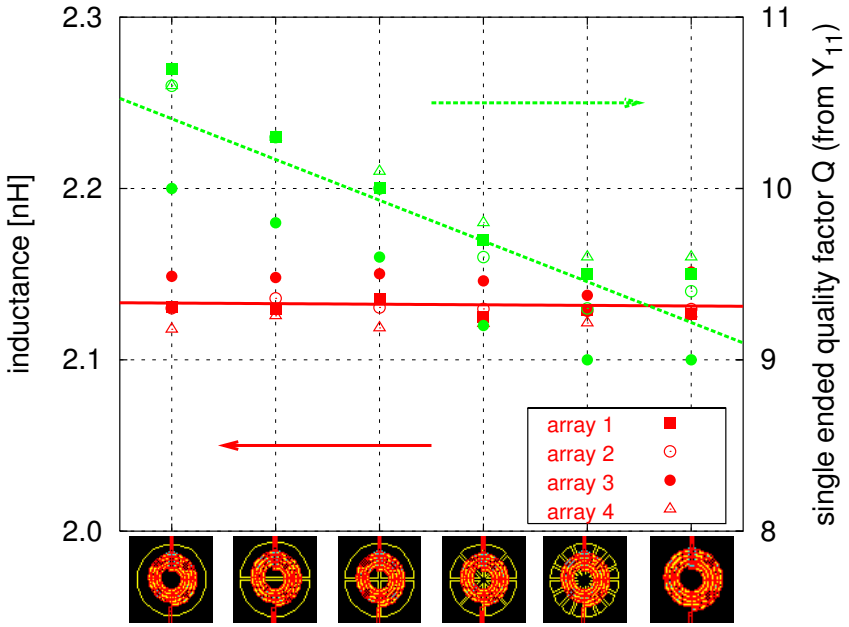


Figure 39: This set of on-wafer measurements on 4 different dies shows that omitting the p^+ channel stopper beneath the inductors does not lead to a formation of an n-inversion layer on the surface of the $20\,\Omega \cdot cm$-wafer (left: CS fully omitted, right: CS not omitted).

5.11 Influence of the substrate

In an effort to increase the quality factor of the spiral inductors, the substrate below several wafers of SiGe2-Power (1 kΩ·cm substrate) and SiGe2-RF (both 1 kΩ·cm and 20 Ω·cm substrate) has been removed by reactive ion etching (RIE) and compared to inductors without substrate removal. In order to eliminate errors due to varying metallisation thickness, both etched and non-etched inductor arrays are arranged on the same wafer in the way of a chessboard. The measured results for a 3.3 nH inductor are shown in Fig. 41.

All measured inductors showed an improvement in peak-Q of a factor of 2 (medium size inductors, see Fig. 41) to 3 (large inductors, L=30 nH). The frequency where peak-Q occurs was shifted considerably towards higher frequencies, however, and there is virtually

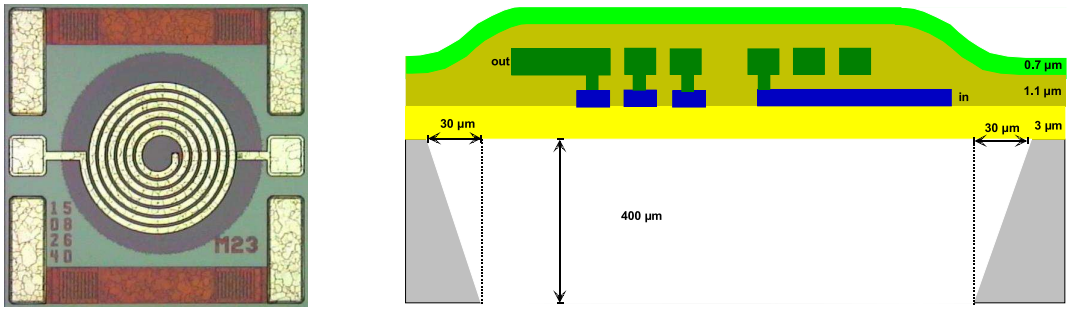


Figure 40: Inductor on a thin membrane with removed substrate.

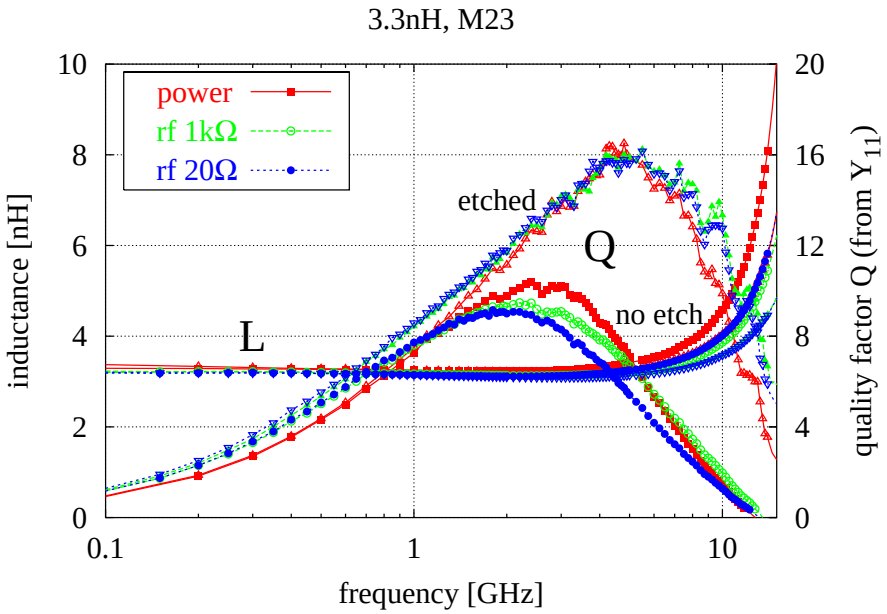


Figure 41: Inductors on a membrane with the substrate removed show a higher Q at elevated frequencies, while there is no improvement at intermediate frequencies.

no improvement by substrate removal at low and intermediate frequencies. This means that only inductors with $\omega \cdot L \gg 50\,\Omega$ benefit from substrate removal. Such inductors are typically used in on-chip filters, VCO tanks or LNA matching networks. While a high Q value is desirable in VCOs, high-Q filters and LNA output matching networks become very sensitive to process spreads in the MIM capacitors and their bandwidth is often too low for practical applications, requiring again to de-Q the passive circuit by shunting a resistor in parallel. Matching the low impedances of power amplifiers usually requires inductors with $\omega \cdot L \ll 50\,\Omega$ and such inductors benefit from a reduction in series resistance by using a thick top metal rather than by removing the substrate. We conclude that substrate removal in most cases is not a viable way to improve on-chip inductors, taking into

account the additional processing costs and the lower yield associated with this technique.

5.12 Improving Q factor and reducing crosstalk by patterned ground shields

The use of patterned ground shields (PGS) has been reported to enhance the quality factor of spiral inductors on low resistivity substrate [137, 123]. On the 20 $\Omega \cdot cm$ and 1 $k\Omega \cdot cm$ substrates used for the SiGe1 and SiGe2 bipolar processes, no PGSs have been used prior to this thesis. In order to evaluate the usefulness of PGS, an inductor array with spirals ranging from 0.6 to 4.7 nH in 2 different metal versions (M23 or M3) has been fabricated in the SiGe1 process and evaluated using an LRM+ calibration and 'Thru' de-embedding (see appendix C.2 and C.3). Two different shield geometries have been realised using either the silicided base poly layer(TiSi, 4.5 $\Omega/\Box$) or metal 1: In order to suppress currents in the PGS induced by the magnetic field, shield #1 is slotted like a pie (not shown), while shield #2 is slotted like a snow flake (see Fig. 42, left and right).

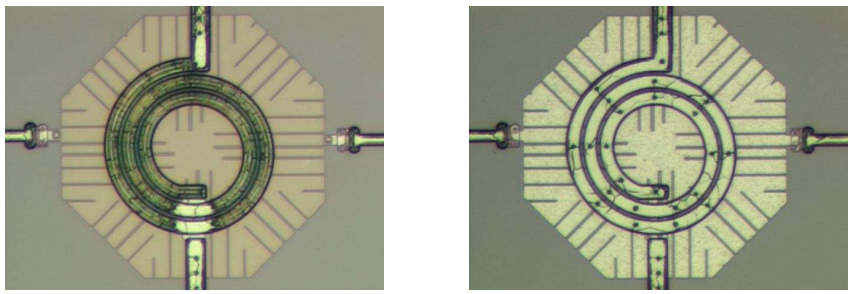


Figure 42: Spiral inductor with grounded, patterned ground shield. Left: Titanium-silicide shield, Right: Shield in metal 1

Due to the thin oxide layer between metal 1 and metal 2, the PGS realised in metal 1 led to a degradation in quality factor and strongly reduced both inductance and self-resonance-frequency (SRF). On 20 $\Omega \cdot cm$ substrate, the PGS realised in the TiSi layer led to a significant Q enhancement for the inductors routed in metal 3 at the expense of a narrower Q-vs-frequency behaviour (Fig. 43, right). For the spirals routed in M23, no enhancement in Q was observed, but the PGS led to a very narrow Q behaviour over frequency compared to the unshielded inductor (Fig. 43, left). Note that the inductance strongly *de*creases with frequency for the shielded inductors whereas it slightly *in*creases due to the turn-to-turn capacitance for the unshielded device. The fact that this effect is more pronounced for M23 with its lower oxide thickness between coil and shield shows that eddy currents induced by the magnetic field (see section 5.3) try to cancel the current flow in then coil itself. Virtually no difference was observed between shield #1 and shield #2. On 1 $k\Omega \cdot cm$ substrate, the use of PGS did not improve the quality factor but led to a strongly reduced self-resonance frequency, shifting the frequency of peak-Q towards

lower frequencies.
The following rules should be observed when using shielded inductors:

- Patterned ground shields are effective in enhancing the Q factor on low impedance substrates $\leq 20\Omega \cdot cm$ if a large oxide thickness between shield and coil is available.
- On 1 $k\Omega \cdot cm$ substrates, the reduced SRF leads to a lower frequency of peak-Q and a narrower Q-vs-frequency behaviour.
- If shielded inductors are operated close to the frequency where peak-Q occurs, the reduction in inductance compared to the DC value needs to be taken into account.

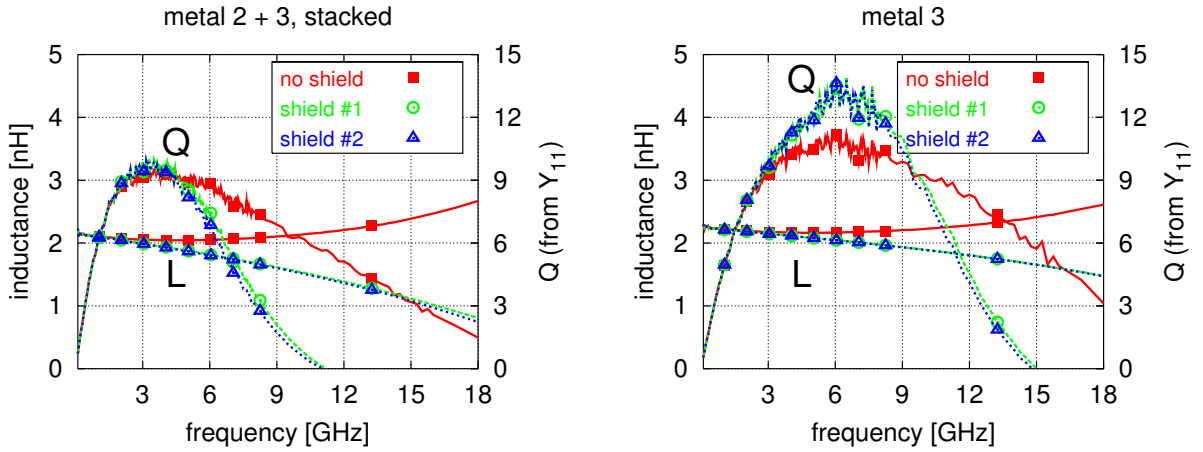


Figure 43: 4.5 turn spiral inductors on 20 $\Omega \cdot cm$ substrate. While the PGS do not improve Q for the M23 type (left), significant Q enhancement is observed for the shielded M3 type with its larger distance between coil and shield (right).

In addition to the Q-enhancement we have been especially interested in reducing crosstalk between spiral inductors using PGS. As has been explained in section 2.2.4, the strong crosstalk between the LO divider and the output inductor of the UMTS LNA precluded the LNA from being integrated into the SCUBA receive IC. In order to investigate crosstalk, an array of inductors designed by TQS in Boston was realised on a SiGe1 MPW according to the chip photograph in Fig. 44: Two inductors are shunted from port 1 and port 2 to ground, respectively. They are spaced apart by 0, 0.25, 0.5, 1, ..., 7 coil radii, measured from edge to edge. Table 9 shows the available test structures, all of them routed in metal 1 and 2. SOLT calibration has been done both using laser-trimmed standards on an impedance standards substrate (ISS) with subsequent pad removal by de-embedding as well as using less accurate on-chip calibration standards, eliminating errors due to de-embedding (appendix C.2 and C.3). The isolation-calibration routine was used to

4.5 nH			1.0 nH	
no PGS	no PGS ring of substrate contacts	grounded TiSi shield	floating BL shield	grounded TiSi shield

Table 9: Structures for characterising crosstalk between inductors

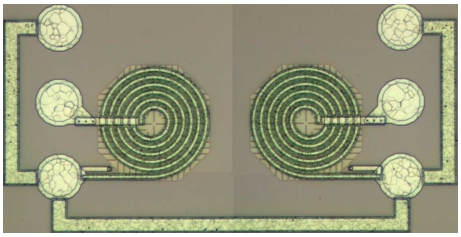


Figure 44: Test structure to measure crosstalk between shielded spiral inductors.

eliminate crosstalk via the S-parameter test set of the vector network analyser. Inductances and Q factors were extracted from S_{11} and S_{22}. S_{21}=S_{12} was a measure for the isolation between the coils.

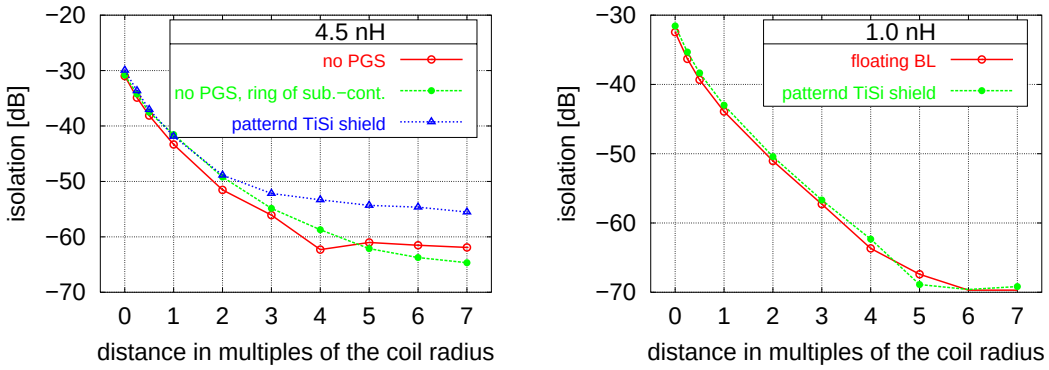


Figure 45: Results of isolation measurements at 1 GHz (left) and 3.4 GHz (right).

Generally, isolation was at its minimum (e.g. maximum crosstalk) at the frequency of peak-Q, as the voltage swing across the parallel LC circuit was maximum at this frequency. This frequency was considerable lower for the inductors using the TiSi ground shield. However, in order to get a fair comparison between shielded and unshielded inductors, we have to compare crosstalk at the *same frequency*. Therefore the values have been extracted at 1 GHz for the 4.5 nH coil, which corresponds to the frequency of peak-Q for the 4.5 nH inductor with TiSi ground shield. For the 1.0 nH coil we chose 3.4 GHz, corresponding to the frequency of peak-Q for the TiSi shielded version. Therefore the inductors using the TiSi PGS showed the highest crosstalk, considerably higher than the

unshielded versions, which were operated considerably below the frequency of peak-Q. For large distances $> 4\times$ the coil-radius (measured from edge to edge), we found a 4 dB improvement of the unshielded inductor with grounded ring of substrate contacts over the unshielded type, while there was virtually no effect at smaller distances. Peak-Q decreases by approximately 10% using a ring of substrate contacts, however.

The following three guidelines can therefore be given:

1. Use a patterned ground shield to increase the peak-Q of inductors which are spaced apart far from the lossy substrate (M3-versions in the SiGe1 and SiGe2 technologies). Take care, as the frequency of peak-Q drops and there is a strong roll-off in Q at higher frequencies (see Fig. 43).

2. Use a ring of substrate contacts to reduce crosstalk between inductors which are spaced apart by more than 4 times the coil radii. However, depending on the distance of substrate contact to the coil, the reduction in peak-Q is in the order of 10% due to reduced values of R_{sub} (see Eqn. 25).

3. To reduce coupling between adjacent coils, there is not much that you can do. Incorporate this coupling into your simulation and try to make use of it.

4. As noted by Sönmez [145], using massive metal planes with defined spacing around the inductors leads to a better reproducibility for layouts at high frequencies (e.g. 24 GHz) at the expense of reduced inductance due to the eddy currents induced in the metal planes.

It is interesting to note that both the inductance and the quality factor of the individual inductors increase slightly when the distance between them decreases. This points to a constructive coupling process and motivates the investigations towards symmetrical inductors in section 5.17.

5.13 Electromagnetic field simulation

5.13.1 2.5D simulators based on the method of moments

At the beginning of this thesis, no EM based software tools have been available that simulate inductors on lossy substrates, including metallisation loss, in short time on a fast PC or workstation with sufficient accuracy. Just at the end of this work, the tools have been powerful enough to model inductance and Q-factor accurately. Therefore, within the framework of this thesis, several 2.5D simulators and one 3D simulators have been investigated:
All of the 2.5D simulators used were based on the Method of Moments (MoM), which dates back to the work of R.F. Harrington in 1960. It is a numerical discretization technique which solves Maxwell's equations for *planar* conductors (with zero thickness) embedded

in a multi-layered dielectric substrate. The term 2.5D means that current in the plane perpendicular to the conducting XY layers can only flow in Z-direction, no current flow in ZX or ZY directions can be taken into account. Extensive evaluation was done on two 2.5D commercial tools, which differ in the way they solve these equations:

- The *Momentum™* simulator, included in Agilent technologies' *Advanced Design System™*, relies on a 4-dimensional numerical integration technique to calculate each pair-wise coupling between the mesh elements [146].
- *Sonnet™* from Sonnet Software, Inc. utilises the so-called closed-box solution in conjunction with a uniform grid which is solved using an FFT-based analysis [147].

Both *Momentum* and *Sonnet* introduced an intelligent frequency interpolation algorithm (called adaptive frequency sweep, AFS in *Sonnet*), which fitted the S-parameters of the complete frequency range to just a few EM simulated frequency points, greatly enhancing simulation speed. The term 'intelligent' means that the software autonomously decided where to set the simulation frequencies within frequency range selected by the user. This feature greatly speeds up the simulation process and it is amazing, how even narrow-band filters with several poles can be simulated with just 5–8 frequency points. For spiral inductors, however, this feature had to be used with caution: The software stopped the process of setting and simulating additional stilt frequency points, when the difference between the actually simulated result at a given frequency compared to the intelligent fit was smaller than a given Δ. While this works excellently for the *inductance* of a spiral inductor, large errors and even severe discontinuities of the Q-factor in the frequency range of peak-Q occurred! Therefore, in addition to the frequencies set by AFS automatically, the simulator had to be *forced* to simulate several additional frequencies in the region of peak-Q. The reason is the strong dependence of Q on the slightest changes in S-parameters and was explained already earlier in section 5.5. This makes the quality factor of a spiral both difficult to measure (influence of contact resistance, on-wafer calibration, de-embedding, see section C) and difficult to simulate.

5.13.2 Why a planar inductor is not a two-dimensional structure

Using the 2.5 D simulator, numerous simulations have shown that there was initially a big difference in both inductance and Q-factor between measured and simulated results:

1. The Q-factor always simulated too high compared to the measurements, a fact that first was attributed to poor measurements conditions (e.g. contact resistance) or to a degradation in substrate resistivity during wafer fabrication or to a metal thickness which could be thinner than specified.
2. The inductance always simulated too high. This was initially attributed to poor de-embedding.

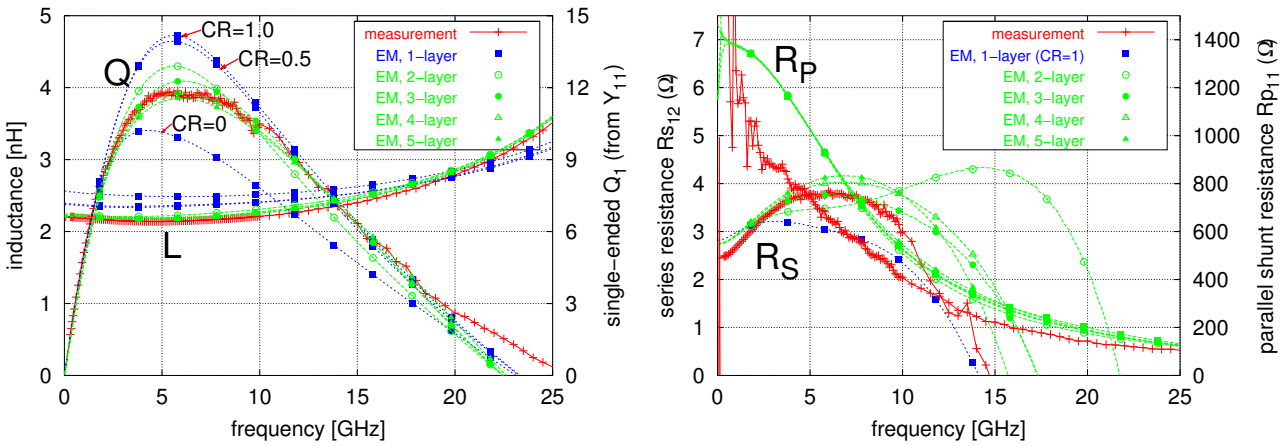


Figure 46: Modelling the metal trace of this spiral inductor in M3 (5 turns, $2.2nH$) by a single, infinitesimal thin conductor overestimates L by 10% and Q by 17% (left). The conductor needs to be split in at least 4 layers in order to model metal losses in the 2.5D simulator properly. This can be seen from the slope of the series resistance versus frequency (right).

A thorough investigation revealed that the problem was the 2.5 D simulation itself: The MoM solver uses an infinitesimal thin conductor layer (zero metal thickness) and approximates the skin effect by a built-in model assuming a straight conductor. This estimated skin effect is then overlaid to the simulated results in order to model some kind of metallisation loss. This works fine for structures, where the physical metal thickness is smaller than 10 to 20% of trace width and/or spacing (whichever is smaller). In our spirals, the spacing between the turns can be as small as 2 μm and the metal thickness of metal 2+3 is 4 μm (see Fig. 29), so this condition is not met! As can be seen in figure 46, the simulation of a planar inductor with a line-to-line spacing comparable to the metal thickness is a 3D problem and cannot straightforwardly be simulated using a planar, 2.5D simulator. The reason is that the 2.5D simulator assumes the skin effect to happen just at the top and at the bottom of a straight conductor and no current pushing to the side-walls is taken into account. Even worse, a 2.5D simulator cannot determine if the current is flowing mainly at the top or at the bottom of this artificial conductor. Therefore *Sonnet* requires the user to set a factor called *current ratio* (CR) which specifies the amount of current flowing at the top with respect to the current flowing at the bottom of the layer in order to calculate metal loss. Assuming equal current flow at the bottom and at the top (CR=1), as it would be the case in a strip line, overestimates the quality factor Q (Fig. 46, left) and simulates the slope of R_{DC} versus frequency as too flat (Fig. 46, right). Assuming that the current flows just at the bottom and that there is no current at the top (CR=0, default setting) underestimates Q. Adjusting CR for the coil Figure 46 to ≈0.2 would model Q correctly, but still simulates the inductance too high by a factor of ≈ 10%.

Its clear that Maxwell's equations should determine the current distribution within the conductor rather than the user. This can be achieved by an N-layer model [148] according to Fig. 47:

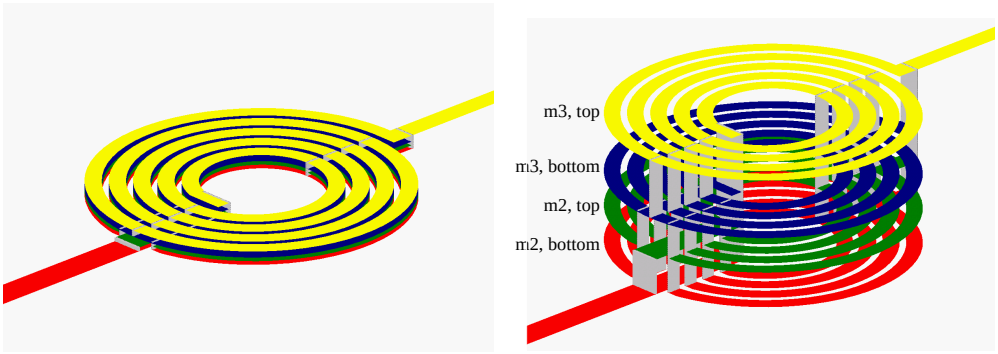


Figure 47: In order to properly model the loss in the metal traces, 2.5D simulators based on MoM require the conducting layers to be split into 2 or more layers with zero thickness, separated by vias that correspond to the physical metal thickness [149, 150, 148]. The figure on the right is scaled in z-direction for better visibility.

Here the conductor is mapped into N simulator layers during GDSII-file stream-in, spaced apart by t_{met}/(N-1), where t_{met} is the physical thickness of the conductor. Each of the N infinitesimal layers is assigned a thickness of t_{met}/N in order to maintain the correct DC resistance. I found out that a multiple sheet model should be considered [151, 152],

- if the *gap* between two lines is on the order of (or less than) the thickness of the lines and / or
- if the *width* of one line is on the order of (or less than) the thickness of the line.

Increasing the number of layers from N=1 to N=5 shows subsequent improvements in the accuracy of both L and Q (Fig. 46).
The current distribution in a 2 nH spiral inductor simulated using a 4-layer model is shown in Fig. 48. While the current flow is homogeneous at 100 MHz, there is a pronounced inhomogeneity already at 1.4 GHz, which is far below the frequency of peak-Q for this inductor (5 GHz): The current tends to be pushed inside for the inner turns and to the outside for the outermost turn. This lateral skin effect in literature is often called *proximity effect*. We found this effect to be more pronounced for "thick" conductors with a total thickness of all shunted interconnect layers of 4-5 μm compared to "thin" conductors with a total thickness of less than 2 μm. As the current at higher frequencies flows mainly at the inside of the turns, the inductor for higher frequencies becomes physically smaller than its geometrical dimensions. We believe that this is the reason for the decrease of the inductance with frequency below the frequency of peak-Q, which again is more pronounced for inductors using "thick" conductors compared to "thin" ones, which we observed both in on-wafer measurements (Fig. 36) and EM simulations (e.g. Fig. 46).

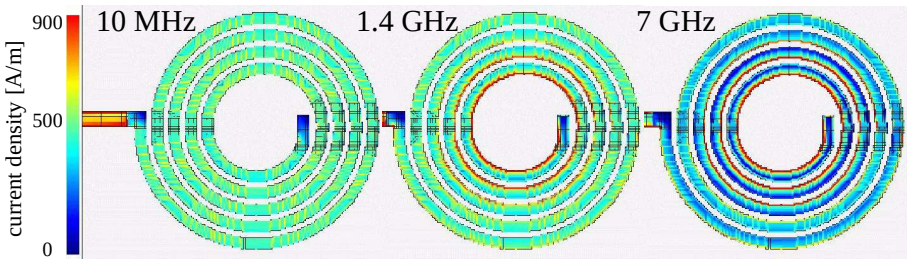


Figure 48: While current distribution is homogeneous at low frequencies, current-crowding occurs at higher frequencies, which pushes the current to the outside for the outer turn and to the inside for the inner turns (Simulation using *Sonnet* V9 with conformal mesh).

As can bee seen in Fig. 49, the classical skin effect of a straight conductor with its current extrusion to all 4 sidewalls of the conductor is virtually absent.

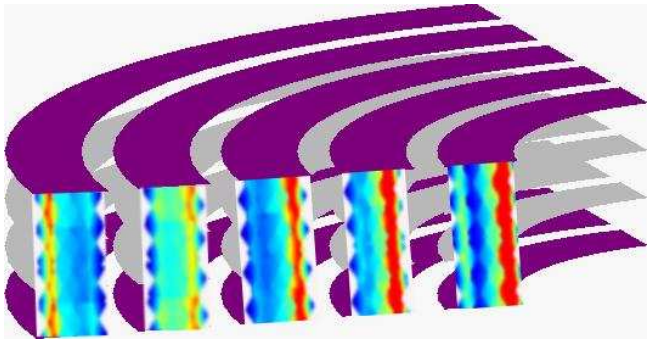


Figure 49: Cross sectional view of the current distribution in a $2\,nH$, five-turn spiral inductor at 5 GHz (z-direction not to scale). The metal strips in M3 are modelled as 4 infinitesimal thin layers in the 2.5D simulator *Sonnet* V9. The traditional skin effect which uniformly pushes the current to the edge of the conductors is virtually absent. The proximity effect pushes the current to the inside for interior turns and to the outside for the outermost turn.

To derive the closed-form, scaleable inductor models from the EM simulations, I used *Sonnet* V9 together with an N-layer model with N ranging from 2 (for large inductors > 5 nH) to 6 (for small inductors < 1 nH) so that the total amount of memory was 0.5-1.5 Gbyte and thus below the 2 Gbyte RAM limitations of our 3 GHz Pentium IV machine. Simulation times for a frequency sweep of one inductor were between 3 and 24 hours. Exceeding the RAM of the computer is possible but leads to extensive disk swapping and extremely long simulation time.

5.13.3 Sensitivity of the EM simulation

In general, with the same computational effort, higher accuracy is obtained using a coarse mesh size (e.g. 1.5 μm) combined with a larger number of layers compared to a fine mesh size (e.g. 0.75 μm) combined with a low number of N. Astonishingly, the influence of the mesh size on the simulated results of a 2.2 nH inductor with 7 μm line width, 3 μm spacing, 4.5 turns and 26 μm inner radius was very weak. Even with a grid of 2 μm – a value close to generating short circuits between the turns – the equivalent circuit parameters of the inductor are close to the final values (see table 10). At the other extreme of a small mesh grid (0.75 μm), the algorithm collapses at frequencies below 1 GHz, which seems to be a general problem of electromagnetic analysis when the cell size is very small compared to the wavelength [153].

mesh [μm]	L at peak-Q	peak Q	R_S at peak-Q	C_{ox}	C_{sub}	R_{sub}	memory [MB]	# of sub-sections	time per freq. [h]
2.0	100.2%	102.0%	97.4%	100%	100%	100.4%	86	3274	0.08
1.5	100.0%	100.0%	100.0%	100%	100%	100.0%	169	4635	0.21
1.0	99.7%	98.4%	102.1%	101%	99%	100.1%	389	7063	0.70
0.75	99.7%	98.7%	101.6%	101%	99%	98.6%	655	9170	1.55
0.5	–	–	–	–	–	–	1322	13037	42.9

Table 10: Influence of the mesh size on the simulation results of a 2.2 nH spiral inductor (*Sonnet* V9, conformal mesh). All values are normalised to the values obtained with the 1.5 μm grid.

Sonnet states that in nearly all cases the principal error source is error due to cell size [153]. The method used in table 10 is often referred to as the *Richardson extrapolation* and gives an idea about the total error of the analysis.

box size [μm]	L at peak-Q	peak-Q	R_S at peak-Q	C_{ox}	C_{sub}	R_{sub}
180	85.3%	94.1%	90.3%	102.8%	253%	46%
256	94.3%	96.7%	94.5%	100.5%	171%	67%
512	98.9%	99.0%	98.7%	99.4%	117%	90%
768	99.7%	99.9%	99.4%	100.4%	105%	96%
1024	100.0%	100.0%	100.0%	100.0%	100%	100%

Table 11: Influence of the box size on the simulation results of a 2.2 nH spiral inductor using *Sonnet* V9 with conformal mesh and a 1.5 μm grid. The outer diameter of the coil is 142 μm. All values are normalised to the values obtained with a 1024 μm box. Small boxes lead to pronounced errors.

The FFT approach used in *Sonnet* requires the circuit to exist inside a shielding box with perfectly conducting sidewalls. Therefore a sufficiently large box size is more important than a fine mesh: In small boxes a current is induced in the sidewalls in opposite direction

to the current in the coil and thus reduces its inductance (see table 11). At the same time the substrate resistances decrease and the substrate capacitances increase, leading to a slightly lower quality factor. The values for C_{sub} and R_{sub} which represent the left substrate shunt network of the equivalent circuit of Fig. 31 are depicted in table 11: The absolute values of C_{sub} and R_{sub} vary strongly with the box size. Their *product*, however, as required by theory (Eqns. 25,26) remains mainly constant as it is only related to the dielectric constant and the resistivity of the substrate, which remains constant throughout the simulations[15]. We propose to use a distance of at least 180 μm from the outermost turn to the conductive box.
In *Sonnet* V9, ports can only be placed *at the box wall*. Therefore the terminals of the passive structures are extended to the box wall using feed lines made from ideal conductors (e.g. 180 μm long). The reference plane of the ports at each sidewall can then be shifted in the layout editor to the terminal of the coil (e.g. by shifting them by -180 μm), forcing the software to correct the S-parameters for the influence of the feed lines. As has been explained earlier, a solver based on MoM does not discretize the dielectric layers but just the conductors itself. Using a larger box therefore consumes little additional memory, as the contribution of the longer feed lines usually is small compared to the number of subsections of the coil itself.
The numerical complexity of an N-layer simulation increases rapidly with the number of sheets. A similar problem occurs with 3-D, *volume* meshing EM tools like Ansoft *HFSS™* where the mesh must be small with respect to the line thickness, significantly increasing analysis time [154, 152].

5.13.4 Comparison of 2.5D and 3D EM simulators

In Fig. 50 different EM simulations have been compared to measurements of a 4.5 turn SiGe1 inductor routed in M23 ($w = 7\mu m\,, s = 3\mu m\,, r_i = 26\mu m$).

- The *HFSS* simulations using Ansoft's *HFSS* full 3D simulator have been performed by Achim Kruck of Atmel Heilbronn.
- The *Empire™* simulation [155] using the 3D Finite Difference Time Domain method (FDTD) was provided by Winfried Simon of IMST, Kamp-Lintfort/Germany.
- 2.5 D *Sonnet* and *Momentum* simulations have been performed by the author with a 4-layer model as described in section 5.13.

The 2.5D simulations show a quality factor which is slightly too high. Taking into account the error in measuring quality factor and the choice of the de-embedding method, which is easily $\pm 20\%$, the error is not too big. According to Fig. 46 the quality factor could

[15] This interesting result might be the reason why we did not find a pronounced influence of substrate contacts onto both measured and simulated Q-factors, as the roll-off of the quality factor is mainly related to the product $C_{sub} \times R_{sub}$

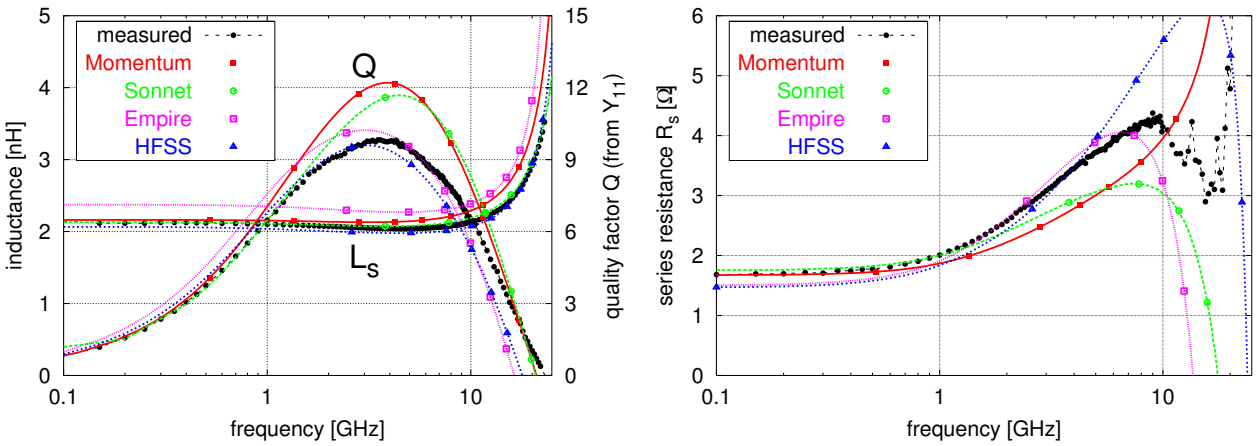


Figure 50: Comparison of different 2.5D (*Momentum*, *Sonnet*) and 3D (*HFSS, Empire*) EM simulators with measurements for a 4.5 turn inductor in M23.

be lowered by using a simulation model with more than 4 layers. The inductance and series resistance match perfectly. As has been shown on Fig. 49, determining the right current distribution is mandatory to simulate the correct Q-factor. The full 3D simulators *HFSS* (by Ansoft) and *Empire* (by IMST) seem to do a better job here, as there is a good agreement between measured and simulated Q. It is not clear why *Empire* simulated an inductance value which is too high. It could be that feed line inductance has not been de-embedded properly. Series resistance at DC simulated by *Empire* and *HFSS* is too low, which could be adjusted by choosing a lower metal conductivity. Finally, all 2.5D and 3D simulators – when properly used – give satisfying agreement with the measurement.

5.14 Analysis of process spreads

At Atmel's request, the influence of typical process spreads onto an integrated inductor has been evaluated. A 4.5 turn inductor ($w = 7\mu m, s = 3\mu m, r_i = 22\mu m$) was simulated using *Sonnet* with a 4-layer model for M3. The results are shown in Fig. 51: Changes in metal thickness have the largest influence, as the DC resistance is inversely proportional to the thickness, which is directly reflected in the DC resistance, extracted at 200 MHz. At higher frequencies the effect on the series resistance is less pronounced, as the current tends to flow at the edge of the turns (see Fig. 48). As has been expected, the effect of metal thickness on the inductance is marginal. Variations in oxide thickness influence only the peak-Q, with the remaining parameters being constant. The same is true for variations in substrate conductivity around the target value of 5 S/m (20 Ω·cm). We could not find a degradation of inductor parameters due to molding compound of plastic packages, provided that dielectric loss is negligible.

The influence of the wafer thickness on the inductor parameters was very low. The

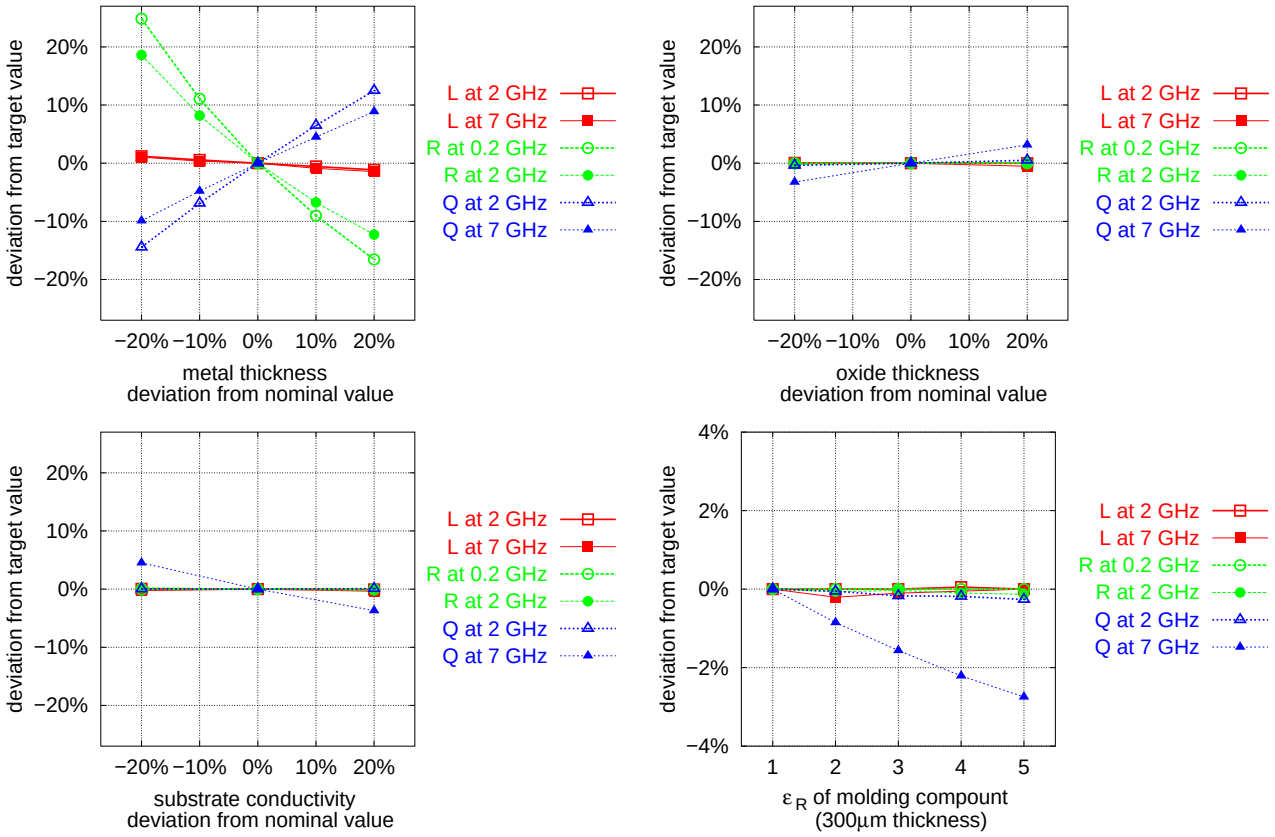


Figure 51: Influence of process spreads on inductor performance.

Wafer thickness [μm]	$C_{ox,1}$ [fF]	$C_{ox,2}$ [fF]	$C_{sub,1}$ [fF]	$C_{sub,2}$ [fF]	$R_{sub,1}$ [Ω]	$R_{sub,2}$ [Ω]
180	27.97	35.60	20.13	12.75	1162	1966
300	27.95	36.31	18.73	11.81	1250	2113
450	28.09	36.52	18.46	11.63	1272	2139
600	28.16	36.49	18.40	11.61	1278	2140

Table 12: The influence of the wafer thickness on the substrate networks is marginal.

difference between 180μm – which is used in RF power amplifiers to keep bond wire inductance low and improve heat sinking – and an unthinned, 600μm wafer merely results in slightly different substrate networks: As can be seen from table 12, the substrate capacitances $C_{sub,1}$, $C_{sub,2}$ decrease slightly with increasing substrate thickness while the substrate resistances $R_{sub,1}$, $R_{sub,2}$ increase. The effect, however, is very small and does not need to be considered in the inductor model, as the effect of the wafer thickness on peak-Q is in the order of 1%. The small influence of the substrate thickness supports the assumption of section 5.3, that the I^2R losses are dominated by currents at the substrate

surface, conducted through metal-substrate capacitances associated with individual turns of the spiral rather than circulating eddy currents due to magnetic fields within the bulk substrate.

5.15 Modelling

Up to now, the simple π model of Fig. 32 provided a convenient tool to evaluate measured and EM-simulated data. However, due to proximity and skin effect both series resistance and series inductance need to be implemented in a frequency dependent manner to model the Q factor (defined in section 34) exactly. An elegant way to model an inductance *de*creasing with frequency and a resistance *in*creasing with frequency using purely frequency independent components is the use of one or multiple ladder circuits [156, 138]. A single ladder already models both the small inductance drop versus frequency due to the proximity effect (Figs. 36 and 48) and the strong positive slope of R_s at frequencies around peak-Q and below[16] (see Fig. 54). In order to include substrate coupling between the turns (Fig. 52), a parallel RC network between port 1 and port 2 consisting of C_{12} and R_{12} has been included according to [140, 141, 157], but later omitted in the final model, as there was no improvement in model quality. The resulting model developed in this work is shown in Fig. 53. Fig. 54 shows that excellent agreement between this model and the target functions (S-parameter measurements or EM simulation) has been obtained. There was no need to use the more complicated equivalent circuits which have been reported recently [138], as a model usually becomes more difficult to scale, the more parameter it uses.

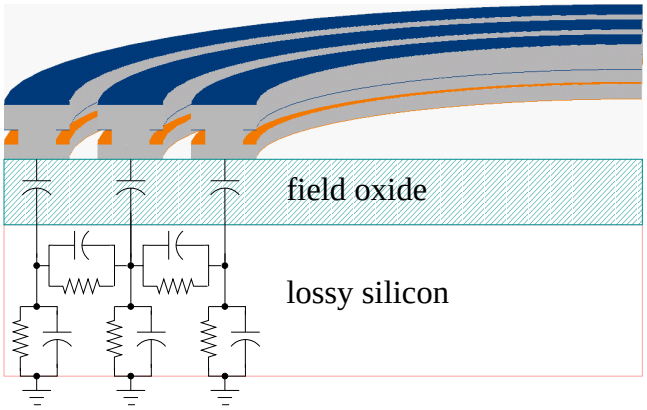


Figure 52: Substrate coupling between the turns via the field oxide.

Fitting *one* set of model parameters to *one* target (measurement or EM simulation) is relatively straightforward. In this thesis, this was done by a partner within the SCUBA

[16] As has been mentioned earlier, at frequencies above peak-Q the Q factor is not determined by the series resistance any more and modelling of R_s at these frequencies is not important.

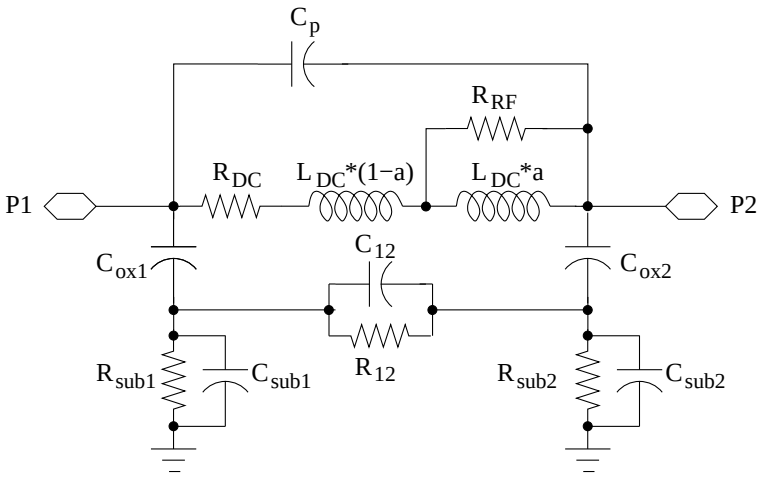


Figure 53: Inductor model taking into account the proximity effect, skin effect and substrate coupling. R_{12} and C_{12} have been omitted in the final model.

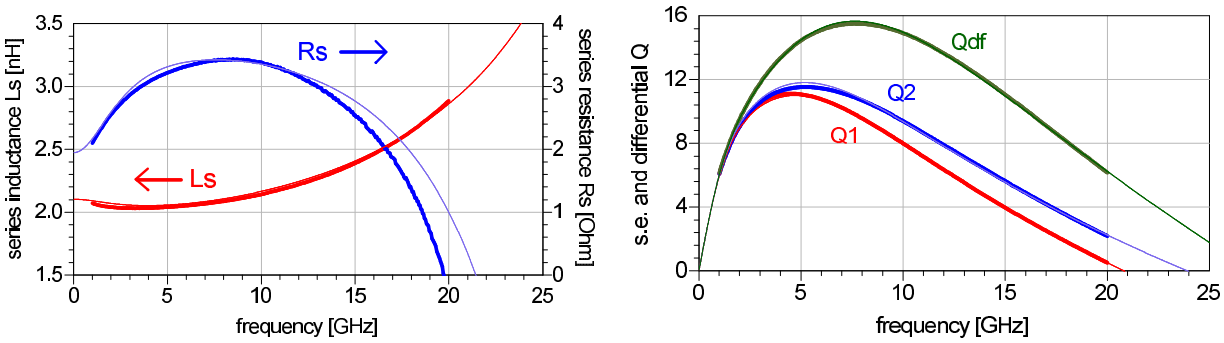


Figure 54: Using the enhanced model of Fig. 53 (thin lines), excellent agreement between the target function (EM simulation in this case, thick lines) is achieved.

project, DTS of Reutlingen/Germany [158], by using an automatic fitting procedure based on a SPICE 2G simulator (see Fig. 54). The more complex task is to derive a *scaleable* model that can predict the properties of a coil for a given technology and metal configuration with basically arbitrary geometry (e.g. number of turns, line width, spacing, radius). Rather than using a polynomial approach, it makes sense to relate as many quantities as possible to geometrical properties of the inductor. This is easy for the DC series resistance, which can be approximated by the total length of the spiral, the metal width and thickness, the geometry of the underpass and the sheet resistance of the metal. As the layout generator synthesises the spiral inductor from semi-arcs, the length of the centre line of the spiral is

$$Length_{Spi} = \frac{\pi}{2} \sum_{i=1}^{x} 2 \cdot r_i + w + (i-1) \cdot (s+w) \tag{42}$$

where x is the number of semi-arcs (x = 2·N). This computes to

$$Length_{Spi} = \pi \cdot N \cdot (2 \cdot r_i - s) + \frac{\pi}{2} \cdot N \cdot (2 \cdot N + 1) \cdot (s + w) \tag{43}$$

Dividing $Length_{Spi}$ by the line width approximates the number of squares of the metallisation system. Multiplying the number of squares with the specific resistance of the metal layer in Ω/□ (or the parallel resistance of several metal layers, if shunted in parallel) yields the DC resistance of the coil. Adding the resistance of the underpass is straightforward an results in a closed-form equation for R_{DC}. The agreement with measurements or EM simulations was so good that it was not necessary to take into account the resistance of the vias itself (see Fig. 55).

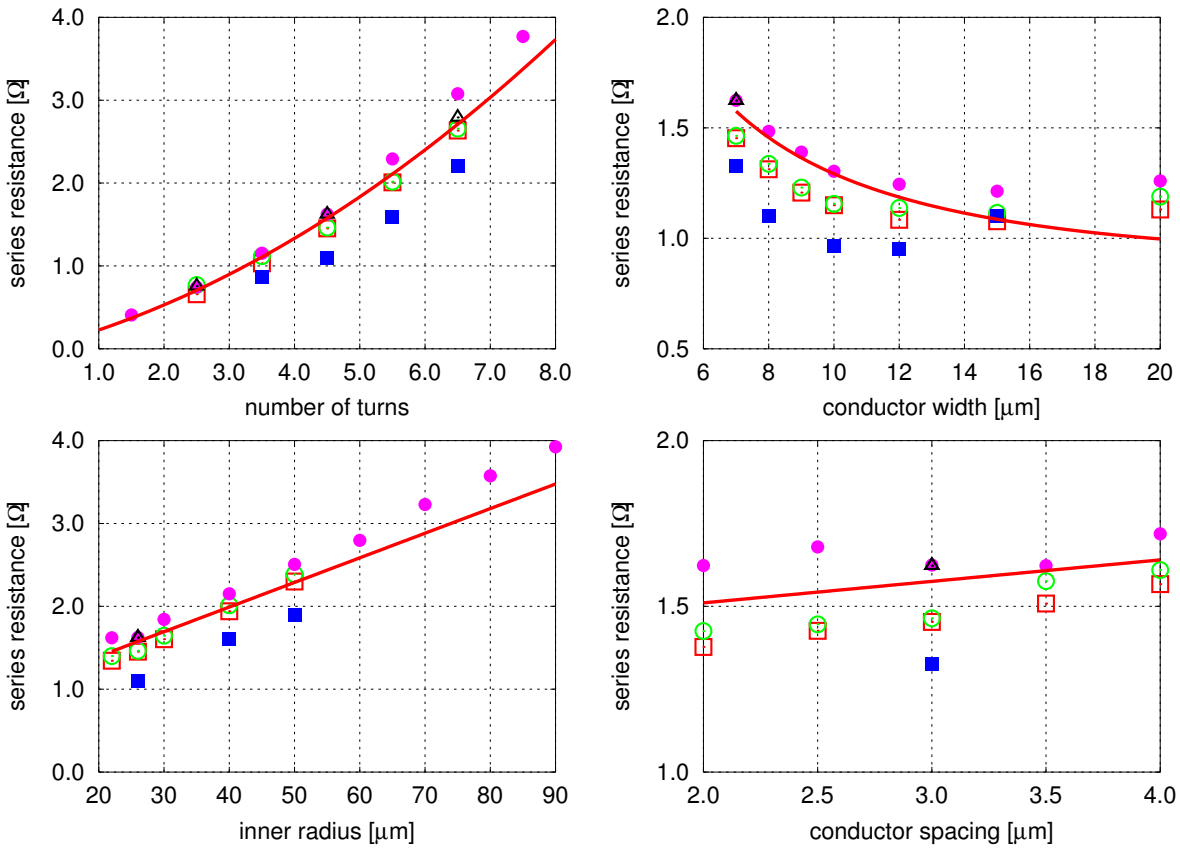


Figure 55: Closed form equation compared to measurements and EM simulations: Red, solid line: R_{DC} based on Eqn. 43. Measurements: Red □ = SOLT cal., green ○ = TNA cal. EM simulations: Blue filled □ = *HFSS* (3D), magenta ● = *Sonnet* (2.5D), black △ = *Momentum* (2.5D). Note that the *HFSS* results are rather erratic.

Inductance calculation techniques start with James C. Maxwell's seminal work, first published in 1873 [159]. 1928 – thirty years before the first silicon IC was invented – Harold

A. Wheeler presented simple analytical expressions for circular coils [160, 161, 162]. The empirically derived expressions are remarkably accurate for multi-turn, circular inductors. Wheeler gives [160]:

$$L_{Wheeler} = 31.33 \cdot \mu_0 \cdot N^2 \frac{a^2}{8a + 11c} \tag{44}$$

where $\mu_0 = 4\,\pi\,10^{-7}\,H/m$, a is the coil mean radius and c the 'thickness' of the coil, defined as shown in Fig. 56 with

$$\begin{aligned} r_{out} &= N \cdot (w + s) + r_i \\ a &= \frac{r_{out} + r_i}{2} \\ c &= N \cdot (w + s) \end{aligned} \tag{45}$$

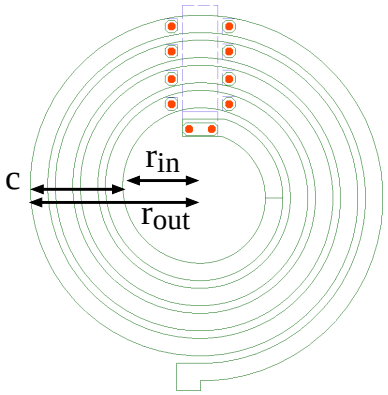


Figure 56: Illustrating the inductance formula of Eqn. 44 given by H. A. Wheeler in 1928 [160]: The average radius of the coil is $a = (r_{out} + r_{in})/2$, the average thickness of the winding is denoted as c.

Wheeler states that this formula is accurate within 5% for coils with $c > 2a$. For our standard coil with N = 4.5 turns, $w = 7\mu m$, $s = 3\mu m$ and $r_i = 26\mu m$, Wheeler's formula gives $2.12nH$, which is in excellent agreement with the $2.1 - 2.2nH$ measured for this coil for different metal configurations (see Fig. 36), although in this case $c \approx a$. A similar good agreement was found for other combinations of N, w, s and r_i.
It is amazing how many closed-form equations for L have been reported since 1928, including modifications of Wheeler's original formula. After a thorough comparison in Fig. 57, I chose the expression from Mohan, del Mar Hershenson, Boyd, and Lee [163] for the low-frequency coil inductance L_{DC} of the scaleable small-signal model in Fig. 53. Their work is based on the concepts of geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance to evaluate the self- and mutual inductances between the coils and yields

$$L_{DC} = \frac{\mu_0 \cdot N^2 \cdot d_{avg} \cdot c_1}{2} \left[\ln(\frac{c_2}{\zeta}) + c_3 \cdot \zeta + c_4 \cdot \zeta^2 \right] \tag{46}$$

where $d_{avg} = (d_{out} + d_{in})/2$ is the average diameter and $\zeta = (d_{out} - d_{in})/(d_{out} + d_{in})$ is defined as the *fill ratio* of the coil. For circular coils, the parameters are $c_1 = 1$, $c_2 = 2.46$, $c_3 =$ and $c_4 = 0.2$ [163]. The more complicated expressions published by Jenei *et al.* in

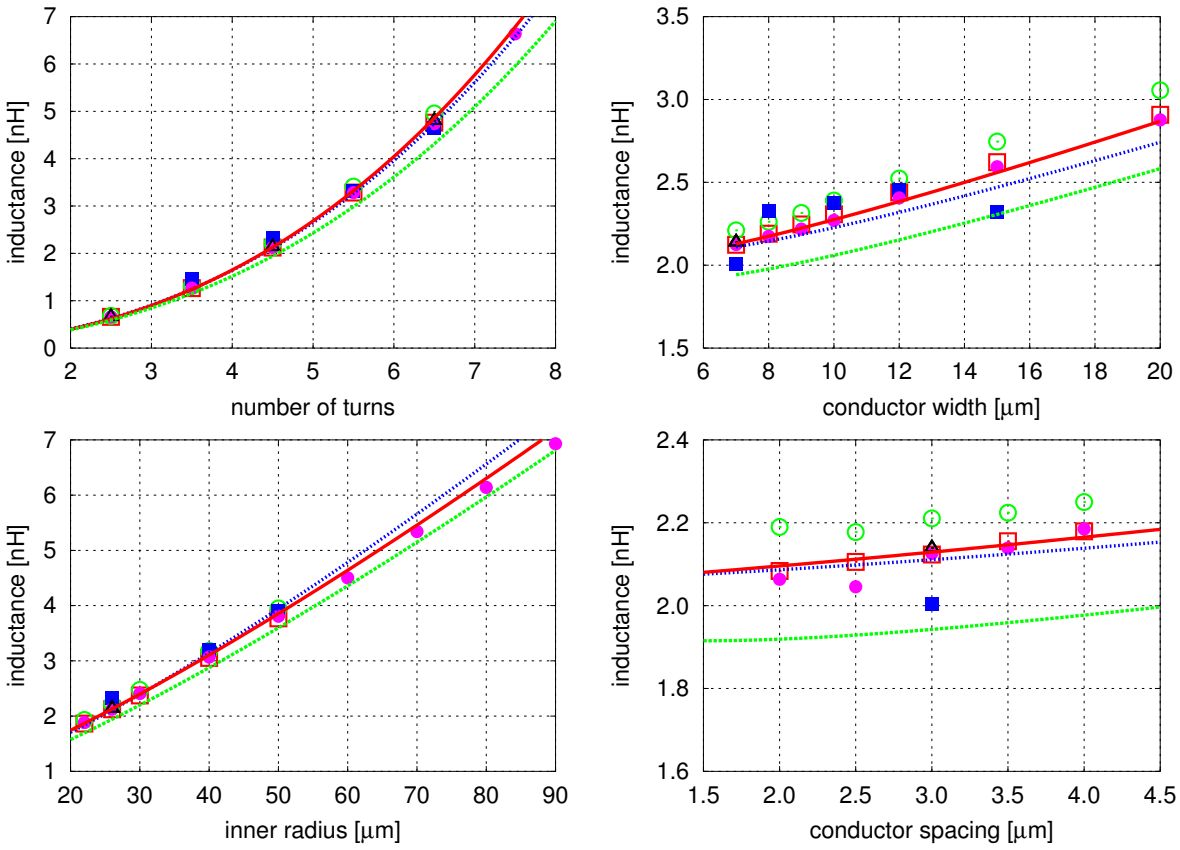


Figure 57: Closed form equations compared to measurements and EM simulations: Measurements: Red □ = SOLT cal., green ○ = TNA cal. EM simulations: Blue filled □ = *HFSS* (3D), magenta • = *Sonnet* (2.5D), black △ = *Momentum* (2.5D). Again, the *HFSS* results show a large spread. Closed form expressions (Mohan *et al.*, 1999): Blue, dotted line: Modified Wheeler (octagonal coils), Red, solid line: Geometric mean distance (GMD, round coils, Eqn. 46), Green, dotted line: Data fitted monomial, (octagonal coils). The GMD equation gives the best fit.

2002 [164]) did not result in improved accuracy.
Using the starting values for L_{DC} from Eqn. 46 and R_{DC} based on Eqn. 43, for each metal configuration and technology a set of 20-30 S-parameter files was simulated using *Sonnet* V9 for different N, w, s, r_i. This set was used as the target function to fit the scaleable model by DTS, using the automatic fitting procedure based on a SPICE 2G simulator. The substrate and oxide capacitances have been scaled to a first order with the coil area and the values of R_{RF} and a of the model in Fig. 53 have been fitted. A

detailed explanation is beyond this work and the reader is therefore referred to [158]. The models itself have been implemented in the design kits of the technologies, greatly improving the agreement between measurements and circuit design (see e.g. Fig. 88 in chapter 6).
As shown in appendix F, a software tool has been developed based on empirical formulae that – for a given inductance operating frequency – calculates all possible coil combinations and sorts them for the highest Q factor or the lowest outer diameter (see Fig. 155).

5.16 Multilevel spiral inductors

As explained by Burghartz *et al.* in [135], coils with large inductance values can be realised on a small area by using multilevel spiral inductors as shown in Fig. 58. In this way, the

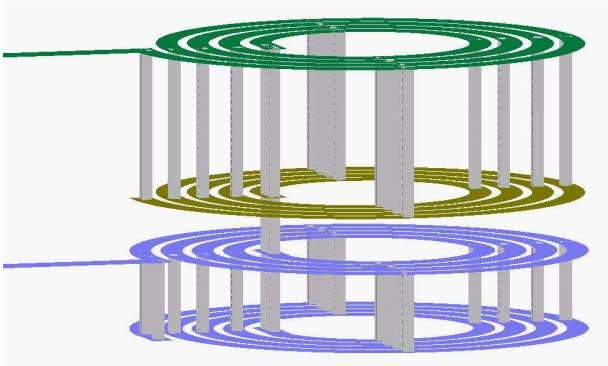


Figure 58: *Sonnet* 2-layer simulation model of a multilevel spiral inductor.

inductor is wired in M3 from the outside to the inner side (green), switches to M2 (blue) and is routed in the *same orientation* back from inside to the outside. Due to the mutual coupling, this structure achieves an inductance which is in the order of 4 times of what can be achieved on the same area using a conventional inductor (see e.g. Fig. 28). Inductors of that kind can be used where large inductance values are needed on small area and series resistance is not too critical. In single-ended applications, it is important to connect this type of inductor with AC ground to the port that connects to the *bottom* coil (blue coil in Fig. 58) and to connect the port with the large RF voltage swing to the *top* coil with the larger separation from the substrate (green coil in Fig. 58). This way the parasitic capacitance of the bottom coil has less influence on the performance. This effect is even intensified, as the part of the coil being spaced away further from the substrate, usually also has a lower sheet resistance due to the thicker metal. This can be seen in table 13, where simulated data of the multilevel spiral used in the 2.4 GHz WLAN LNA are shown. It can easily be seen that a 2-layer multilevel spiral achieves four times the inductance on the same area than a conventional spiral. Alternatively, to achieve the same inductance like with the multilayer type, a conventional spiral requires 2.5 times the area. This is in accordance to the work of Sönmez who used multilevel spirals in SiGe2-RF technology in 24 GHz multi-functional MMICs [145].

5.17 Symmetrical, centre-tapped inductors

Symmetrical, centre-tapped inductors are often used in balanced circuit design due to their high inductance per unit area. Easy biasing is achieved by the common terminal (*ct*), which is a node of virtual ground when driven by a balanced signal at port 1 and 2. Prior

	multilevel spiral	M23 spiral with **same area**	M23 spiral with **same inductance**
# of turns N	4.5	4.5	**6.5**
inner radius r_i	30 μm	30 μm	33 μm
diameter	126 μm	126 μm	**196 μm**
inductance L	5.76 nH	**1.40 nH**	5.80 nH
quality factor at 2.4 GHz	6.4*	8.3	7.5

**bottom coil grounded. If the top coil is grounded, Q reduces to 5.6*

Table 13: Performance of multilevel spirals compared to conventional spiral inductors. Line width is 6.4μm and spacing is 3μm for all 3 types (*Sonnet* simulation, SiGe2-Power technology).

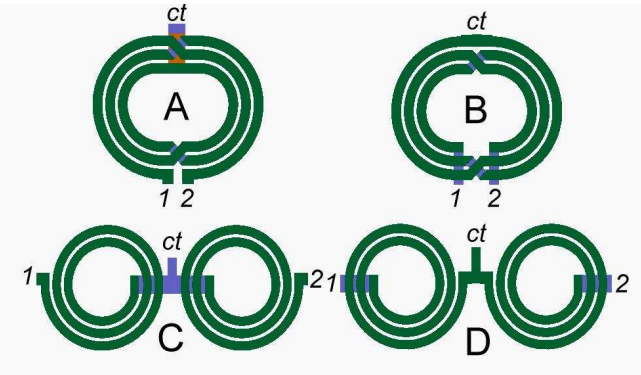


Figure 59: Different topologies which were evaluated by EM simulation.

to the extraction of a scaleable model, 4 different topologies as shown in Fig. 59 have been compared using EM simulations: Configuration A denotes a symmetrical design routed in M23, where the common terminal (ct) is fed in metal M1. Configuration B tunnels port 1 and 2 to the inner side in M2 and circles from the inside to the outside in M23. Configuration B was reported to show better performance over configuration A [165]. Finally, arranging two spirals in a balanced configuration leads to C (feed through at the ct terminal) and D (feed through at port 1 and 2). The results of the analysis are summarised in table 14: All geometries showed an inductance of $\approx$ 1.2 nH between port 1 and 2 when driven in a balanced manner. Note that there is no difference between the ct port being open or floating. The symmetrical inductors A and B show a slightly higher peak-Q compared to the two separate spirals in C and D associated with a smaller series resistance. However, the main advantage of the symmetrical type compared to two separate inductors is that its area consumption is lower by 25%. Type B shows a slightly lower Q than A, in contrast to [165]. Nevertheless, B was programmed in the layout generator as it allows for the realisation of inductors with even and odd number of turns which is not the case for configuration A. Using two separate inductors leads

to the highest SRF but comes at the expense of a higher area consumption. There is no pronounced difference if the underpass is oriented towards the common terminal *ct* or towards port 1 and 2.

Configuration	L_{diff} [nH][1]	peak-Q_{diff}	R_{diff} [Ω][2]	area [μm^2]
A	1.123	22.22 at 12.3 GHz	1.131	$148.0 \times 121 = 17908\ \mu m^2$
B	1.149	20.38 at 11.1 GHz	1.311	$148.0 \times 121 = 17908\ \mu m^2$
C	1.250	19.04 at 13.1 GHz	1.602	$235.5 \times 101 = 23786\ \mu m^2$
D	1.245	19.35 at 13.5 GHz	1.579	$235.5 \times 101 = 23786\ \mu m^2$

[1]at 5 GHz [2]at 200 MHz

Table 14: Comparing the different topologies of Fig. 59 by *Sonnet* simulation.

For the equivalent circuit of a symmetrical inductor, it is straightforward to extent the single π network for a standard spiral inductor (Fig. 31) to Fig. 60.

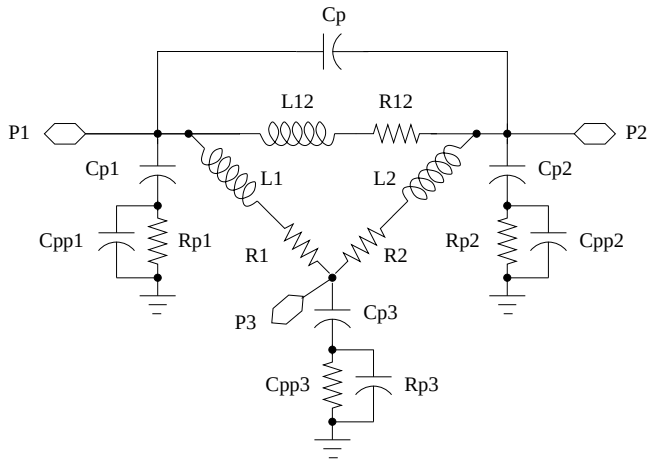


Figure 60: This equivalent circuit of the symmetrical inductor can be extracted analytically from 3-port Y-parameters.

This triple π network can easily be extracted analytically from 3-port Y-parameters: If we define $Y_1, Y_2, Y3$ as

$$\begin{aligned} Y_1 &= -Y[1,3] \\ Y_2 &= -Y[2,3] \\ Y_{12} &= -Y[1,2] \end{aligned} \tag{47}$$

then inductances and series resistances can be extracted according to

$$L_i = \frac{\Im(1/Y_i)}{\omega} \qquad \text{i=1, 2, 12}$$

$$R_i = \quad \Re(1/Y_i) \quad \text{i=1, 2, 12} \tag{48}$$

$$Y_{Pi} = \quad Y[i,1] + Y[i,2] + Y[i,3] \quad \text{i=1, 2, 3} \tag{49}$$

where Y_{P1}, Y_{P2}, Y_{P3} are used to derive oxide capacitances and substrate networks. Due to the positive coupling between the turns, L_{diff} from table 14 (the balanced inductance between port 1 and 2) is larger than $L_1 + L_2$. Therefore, L_{12} in Fig. 60 is a negative inductance, the same is true for resistor R_{12}. While this is no problem for a SPICE-based circuit simulator, some engineers prefer to substitute the negative inductance L_{12} by a coupling factor κ. That way, the three inductors L_1, L_2 and L_{12} are transformed into two inductors L_1^*, L_2^* and one coupling factor κ.

$$\begin{aligned} L_1^* &= \frac{L_1 \cdot (L_2 + L_{12})}{L_1 + L_2 + L_{12}} \\ L_2^* &= \frac{L_2 \cdot (L_1 + L_{12})}{L_1 + L_2 + L_{12}} \\ \kappa &= -\sqrt{\frac{L_1 \cdot L_2}{(L_1 + L_{12}) \cdot (L_2 + L_{12})}} \end{aligned} \tag{50}$$

with κ defined as

$$\kappa = -\frac{L_{12}^*}{\sqrt{L_1^* \cdot L_2^*}} \tag{51}$$

As an example, extracting the symmetrical inductor in Fig. 61 according to the equivalent circuit in Fig. 60, results in $L_1 = L_2 = 0,2545\,nH$ and $L_{12} = -0,876\,nH$. The balanced inductance (port 3 open) is then $[1/L_{12} + 1/(L_1 + L_2)]^{-1} = 1.215nH$. This can be transformed into two coupled inductors of $L_1^* = L_2^* = 0,431\,nH$ and $\kappa = 0,41$. The balanced inductance (port 3 open) is then $2(1 + \kappa)L_1^* = 1.215\,nH$, showing that both representations are electrically identical.

EM simulation of symmetrical inductors is straightforward, as just a 3rd port is added (see Fig. 62).

How to measure 3-port S-parameters with a 2-port test set, as well as a comparison between measurements and EM simulation is shown in appendix C.6: Fig. 145 compares on-wafer measurements to EM simulations for three different symmetrical inductors and gets reasonable agreement. Due to that, for simplicity, the models have been extracted from *Sonnet* EM simulations.

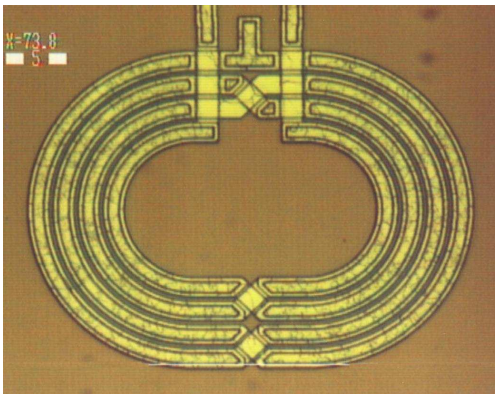


Figure 61: Symmetrical, centre-tapped inductor fabricated using the SiGe1 process

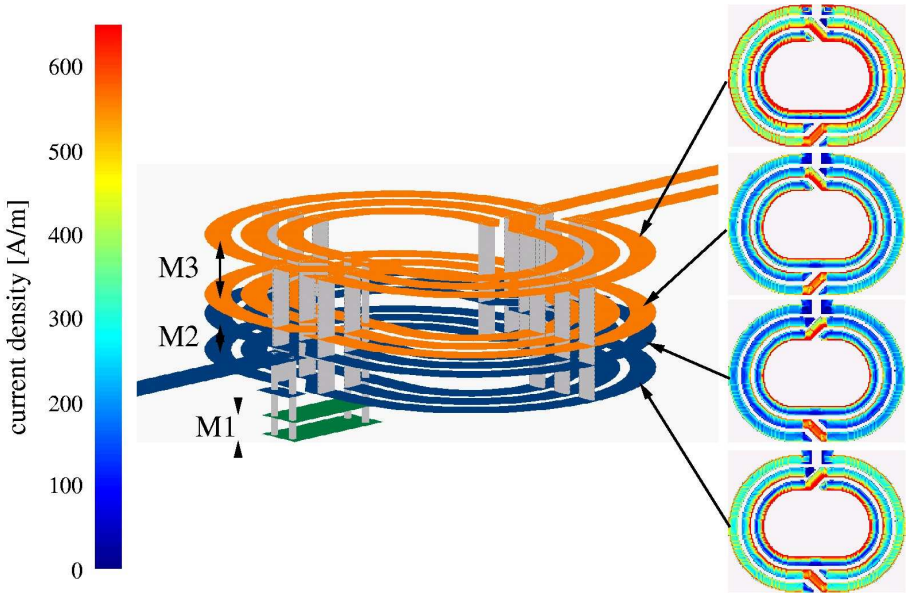


Figure 62: In analogy to Fig. 49, the proximity effect pushes the current flow in this symmetrical inductor to the inner side of the turns (except for the outermost turn). In addition there is a slight classical skin effekt, accumulating the current at the top and at the bottom (balanced drive 0°/180° with 0.5 V at 4 GHz).

6 The low noise amplifier

6.1 Harold Black and the negative feedback amplifier

Amplifiers and mixers with high linearity at all frequencies make extensive use of negative feedback. The idea of using negative feedback to reduce distortion in long distance telephone service amplifiers built upon vacuum tubes was introduced by Harold Black at the Bell Telephone Laboratories as early as 1927 and patented in 1937 [166]. The invention allowed Bell to reduce overcrowding of lines and to extend its long-distance network by means of carrier telephony. It enabled the design of accurate fire-control systems in World War II, and it formed the basis of early operational amplifiers, as well as precise, variable-frequency audio oscillators [167, 168]. Fortunately for the analog engineers, this fundamental patent and its 126 claims – which were not limited to electrical systems but applied to mechanics and acoustics as well – expired in 1954 [166]. Each modern low-noise amplifier (LNA) employs some form of negative feedback, either parallel feedback from the output to the input (e.g. section 6.2.1) or series feedback in the emitter or source connection.

6.2 Broadband LNA designs

For multiband receivers, broadband LNAs are attractive as they simplify the radios and less effort needs to be spent for antenna switches. This section discusses different broadband LNAs using negative feedback.

6.2.1 Transimpedance amplifier

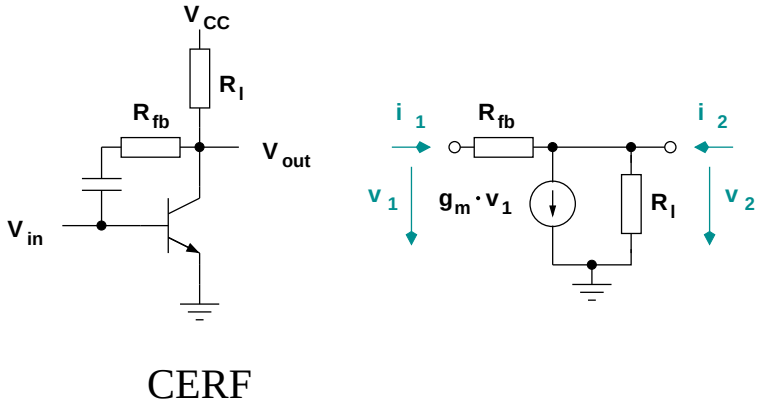


Figure 63: Common-emitter stage with parallel resistive feedback. Left: schematic, right: small-signal equivalent circuit.

The transimpedance amplifier (TIA) shown in Fig. 63 is the RF counterpart of an audio amplifier based on operational amplifiers with resistive feedback. The blocking capacitor in the feedback path allows to set the collector-base voltage larger than zero as it would be the case in the absence of this part. Its value should be large and provide a negligible reactance at the RF frequency. Due to

$$i_1 = \frac{1}{R_{fb}} \cdot [v_1 - v_2] \tag{52}$$

$$i_2 = g_m \cdot v_1 + \frac{1}{R_l} \cdot v_2 + \frac{1}{R_{fb}} \cdot [v_2 - v_1] \tag{53}$$

the Y-parameter matrix of this simple circuit is given by

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{fb}} & -\frac{1}{R_{fb}} \\ g_m - \frac{1}{R_{fb}} & \frac{1}{R_l} + \frac{1}{R_{fb}} \end{bmatrix} \tag{54}$$

Using the normalised y-parameters $y_{ij} = Z_0 \cdot Y_{ij}$ (i=1,2), the input reflection coefficient is given by [142]

$$S_{11} = \frac{(1 - y_{11})(1 + y_{22}) + y_{12} \cdot y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} \cdot y_{21}} \tag{55}$$

$$= \left[1 + \frac{Z_0}{R_l} - \frac{Z_0^2 \cdot g_m}{R_{fb}} - \frac{Z_0^2}{R_l \cdot R_{fb}}\right] / \underbrace{\left[1 + \frac{Z_0}{R_l} + \frac{2 \cdot Z_0}{R_{fb}} + \frac{Z_0^2}{R_{fb} \cdot R_l} + \frac{Z_0^2 \cdot g_m}{R_{fb}}\right]}_{=d} \tag{56}$$

and the output reflection coefficient by

$$S_{22} = \frac{(1 + y_{11})(1 - y_{22}) + y_{12} \cdot y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} \cdot y_{21}} = \frac{1}{d} \cdot \left[1 - \frac{Z_0}{R_l} - \frac{Z_0^2 \cdot g_m}{R_{fb}} - \frac{Z_0^2}{R_l \cdot R_{fb}}\right] \tag{57}$$

Both simultaneous input and output match ($S_{11} = S_{22} = 0$) can be achieved by adjusting the feedback resistor R_{fb} to $g_m \cdot Z_0^2$, independent of load resistor R_l (as long as $R_l >> 50\ \Omega$)[17]. The forward gain S_{21} is given by

$$S_{21} = \frac{-2 \cdot y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} \cdot y_{21}} \tag{58}$$

$$= \frac{Z_0}{d} \cdot \left[-2 \cdot \left(g_m - \frac{1}{R_{fb}}\right)\right] \approx -Z_0 \cdot \left(g_m - \frac{1}{R_{fb}}\right) \tag{59}$$

and the reverse isolation by

$$S_{12} = \frac{-2 \cdot y_{12}}{(1 + y_{11})(1 + y_{22}) - y_{12} \cdot y_{21}} \tag{60}$$

$$= \frac{2}{d} \cdot \frac{Z_0}{R_{fb}} \approx \frac{Z_0}{R_{fb}} \tag{61}$$

I_C	g_m	R_l	R_{fb}	S_{21}	S_{12}	S_{11}	S_{22}	k	Δ
3mA	0.118 S	300 Ω	300 Ω	13.20 dB	-17.54 dB	0.062⟨0°	0.071⟨180°	1.12	0.60
5mA	0.197 S	500 Ω	500 Ω	18.58 dB	-21.19 dB	0.046⟨0°	0.041⟨180°	1.04	0.74

Table 15: S-parameter set of a CERF LNA using an ideal transistor and Eqns. 54-61. $R_{fb} = g_m \cdot Z_0^2$ results in simultaneous input and output match. R_l has been chosen to be equal to R_{fb}.

Table 15 shows the exact results of an ideal TIA for 3 and 5 mA of bias current: As can be seen, even when using an ideal transistor, due to the strong feedback the reverse isolation is only slightly higher than the gain, leading to a very low Rollett stability factor which is given for a linear twoport by [169, 170]

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{21} \cdot S_{12}|} \quad \text{with} \quad \Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \tag{62}$$

The necessary and sufficient conditions of unconditionally stability for any combination of source and load impedance are $k > 1$ and $|\Delta| < 1$ [65]. If one of these conditions is not met (e.g. $k < 1$), the circuit is only conditionally stable (= potentially unstable) and oscillation may occur with a certain combination of source and/or load impedance presented to the transistor [65, 171]. Therefore it is essential that the k-factor is above unity for all frequencies where the device has substantial gain. Low stability is not just a problem of bipolar LNAs with parallel feedback but it also occurs for other technologies, e.g. MESFET [172, 173].
While S-parameters are useful for small-signal gain, noise and stability analysis, more reality is captured by using an ideal BJT large signal model consisting solely of an exponential current-versus-voltage characteristics

$$I_C = I_0 \cdot e^{\frac{V_{BE}}{k_B T}} \quad \text{with} \quad I_0 \approx 10^{-16} A, \tag{63}$$

infinite current gain, no dependency of collector current I_C on collector voltage (infinite Early voltage) and zero parasitic resistors and capacitances ("Level-0" model) [174]: A load resistor of 500 Ω drops 2.5 V at a current of 5 mA leads, making this circuit unsuited for 2.7 – 3.3 V circuit design. The 3 mA version – due to the low feedback resistor R_{fb} – shows already a NF of 1.41 dB even with this ideal transistor containing just collector shot noise and no ohmic resistances and no base current (see table 16). Both minimum noise figure NF_{min} and equivalent noise resistance R_n in table 16 increase further by adding a real transistor's base and emitter resistance and finite current gain. The influence on NF_{min} can be derived from Hawkins's comprehensive model for the minimum noise figure of bipolar transistors with varying collector current and frequency [175]. It shows that

[17] For reasons of voltage drop, R_l is usually chosen to be in the order of R_{fb}.

I_C (V_{CC})	50 Ω NF	NF_{min}	Γ_{opt}	R_n	IIP_3	$0IP_3$
3 mA (3 V)	1.41 dB	1.37 dB	(37.5 + j·0) Ω	5.2 Ω	-3.63 dBm	9.51 dBm
5 mA (5 V)	0.77 dB	0.74 dB	(36.5 + j·0) Ω	2.8 Ω	-5.33 dBm	13.2 dBm

Table 16: Noise parameters and two-tone linearity of a CERF LNA using an ideal transistor ("Level-0" model).

the dominant parameters for microwave noise are emitter and collector shot noise at low frequency and base resistance at higher frequencies through its thermal noise contribution. Shot noise originates from a forward-biased *pn*-junction and the emitter shot noise consists of two parts: Electron injection into the base and hole injection into the emitter. Therefore it improves with high current gain. The base-collector junction is reverse-biased and thus has no shot noise. The collector current shows shot noise only because its a delayed version of the emitter electron injected induced shot noise [176, 177]. Therefore both shot noise sources are highly correlated [177, 178, 176]. Hawkins original model is a low- to medium-frequency model: It neglects all capacitances except the base-emitter capacitance and the emitter resistance R_e (which is a reasonable assumption because base resistance $R_b \gg R_e$ for a Silicon BJT). Therefore the model was extended to HBTs by several authors, including Costa [179], Schumacher *et al.* [180], Kim and Kim [178], Yanfeng and Dexin [181], Niu *et al.* [177] and Rudolph *et al.* [176]. Assuming an ideality factor of $n_e = 1$ (which is possible for SiGe HBTs, but not for AlGaAs/GaAs HBTs), the modified Hawkins formula for the frequency and bias dependence of the minimum noise figure can be written as [178]:

$$NF_{min} = a \cdot \frac{R_b + R_e + R_{opt}}{r_e} + \frac{\alpha_0}{|\alpha(f)|^2} \tag{64}$$

with the small signal dynamic emitter resistance $r_e = V_{th}/I_C$, the thermal voltage $V_{th} = k_B T/q$, the low-frequency common-base current gain α_0, and the noise-optimal source impedance $Z_{opt} = R_{opt} + j \cdot X_{opt}$ given by ($n_e = 1$) [178]

$$X_{opt} = \frac{\alpha_0}{|\alpha(f)|^2} \frac{\omega C_{TE} r_e^2}{a} \tag{65}$$

$$R_{opt}^2 = (R_b + R_e)^2 - X_{opt}^2 + \frac{\alpha_0}{|\alpha(f)|^2} \frac{r_e(2(R_b + R_e) + r_e)}{a} \tag{66}$$

with a defined as

$$a = \frac{\alpha_0}{|\alpha(f)|^2} - 1 + \frac{\alpha_0}{|\alpha(f)|^2} \left(\omega C_{TE} r_e\right)^2 \tag{67}$$

For low frequencies ($f < 1/\tau_c$), the common-base current gain α can be described by a single-pole function [178, 181]

$$\alpha(f) = \frac{\alpha_0}{1 + j\frac{f}{f_b'}} \quad \text{with} \quad 2 \cdot \pi \cdot f_b' = \frac{1}{\tau_b + \tau_c} \tag{68}$$

with τ_b being the base transit time and τ_c the base-collector depletion layer transit time. R_n was not considered in Hawkins's original work and a simple extension to his model was added by [178], giving ($n_e = 1$)

$$R_n = R_b + R_e + \frac{r_e}{2} + \left(\frac{\alpha_0}{|\alpha(f)|^2} - 1\right)\frac{(R_b + R_e + r_e)^2}{2 \cdot r_e} + \frac{\alpha_0}{|\alpha(f)|^2}\frac{1}{2r_e}\left(\omega C_{TE} r_e (R_b + R_e)\right)^2 \tag{69}$$

with the junction capacitance C_{TE} and f_b' derived from plotting

$$\frac{1}{2\pi f_T} = r_e \cdot C_{TE} + \tau_b + \tau_c = V_{th} \cdot C_{TE}\frac{1}{I_C} + \tau_b + \tau_c \tag{70}$$

against $1/I_C$.
Using the "Level-0" model we simulated an input-referred two-tone linearity (IIP_3) at 1 GHz of -3.6 dBm (3 mA @ 3 V) and -5.3 dBm (5 mA @ 5 V), respectively, independent of the tone spacing. As expected, OIP_3 is higher for 5 mA of supply current (see table 16), but due to the higher gain, IIP_3 is lower. The IP_3 values above have been simulated using *infinite* capacitance values for the input-, output-, and feedback DC-blocking capacitors. For 1 MHz tone spacing, IIP_3 drops from -5.33 dBm (C_{source}=∞) to -6.07 dBm (C_{source}=10 nF), -11.02 dBm (C_{source}=1 nF), and finally -11.75 dBm (C_{source}=100 pF). As the difference in impedance between a 100 pF capacitor and an infinite one is just 1.6 Ω at 1 GHz and thus small compared to the 50 Ω impedance of the source, the reason is the termination of the *difference* frequency between both tones, an effect which will be discussed in section 6.8.2. Using real SiGe1 transistor models in cascode configuration (similar to Fig. 18) the values in tables 15 and 16 were confirmed. The cascode improves gain-versus-frequency response and stability at higher frequencies. Simulated noise figure was below 2.1 dB up to 900 MHz even with an ideal bias network, which is not sufficient for most of the systems in this thesis. The main contribution to the NF is due to the feedback resistance R_{fb} (0.92 nV out of 1.34 nV of noise voltage at 500 MHz with a large, 12-finger input device). The simulated gain drops from 13 dB at DC to 11 dB at 900 MHz. To fulfil our specs, this would require a 2nd stage. A 2nd active stage, however, needs to be biased at high current, otherwise it clips the signal and generates distortion. Therefore the TIA failed to fulfil our specifications of NF, linearity and power consumption.

6.2.2 Darlington circuits

Fifty years after US Patent No. 2663806 was issued to Sidney Darlington on December 22, 1953, for a variety of transistor and resistor combinations, the circuit configuration shown in Fig. 64 is still widely used in test equipment, cellular base stations and military equipment [93, 182]. The Darlington requires an external choke to separate bias and RF_{out} nodes in form of a large inductor or a high-value resistor[18] and is technically identical to the CERF LNA of the previous section (Fig. 63). Again a broadband 50 Ω termination is

[18] The latter drops considerable voltage and is therefore unsuited for 3 V designs.

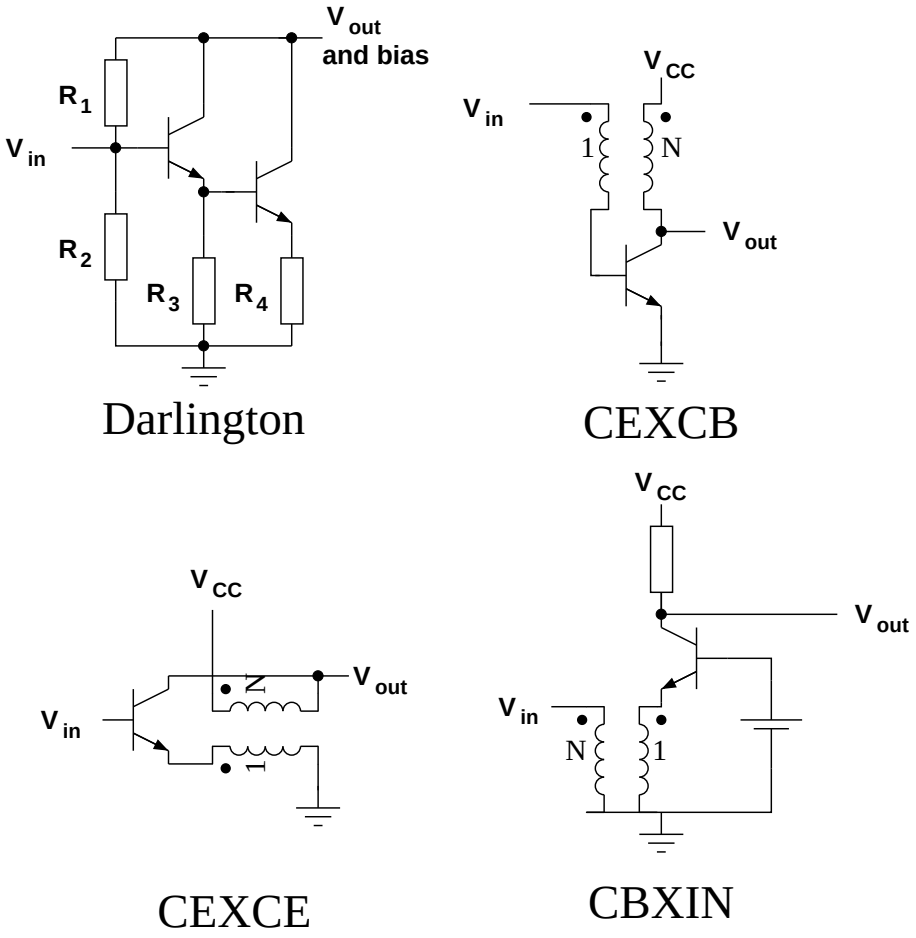


Figure 64: Various broad-band LNA topologies

achieved by setting the feedback resistor $R_1 = g_m \cdot Z_0^2$ and due to R_1 the noise figure of the circuit is typically 0.65 dB above the noise figure of the transistor itself [93]. R_3 is considerably larger than the series feedback resistor R_4 and – together with R_2 – mainly sets the bias current. The second BJT delivers the main contribution to the total transconductance. Fabricated in advanced SiGe HBT [93] or InGaP HBT technologies [182, 183], they achieve noise figures of 2.3 - 5.0 dB, gains of 16-21 dB and OIP_3's of 20-36 dBm in the 0-2 GHz range at currents ranging from 20 to 150 mA at 4 to 8 V supply voltage. For a detailed investigation of the Darlington amplifier see [93]. While Darlingtons are excellent driver amplifiers to PAs in broadband transmit systems, they did not fulfil the low-noise and low-power requirements of the LNAs to be developed in this thesis.

6.2.3 Transformer based LNAs

LNAs with excellent linearity above 5 GHz have recently been reported using on-chip, trifilar transformers [184, 185]. A study on integrated transformers in Atmel's SiGe technologies [186] revealed that the losses are too high for LNA applications below 5 GHz, even when using a small transformer tuned to the operating frequency by MIM capacitors. Therefore this section focuses on amplifiers using discrete transformers, where wideband LNAs with excellent linearity have been reported at HF/VHF frequencies for ham radio applications using trifilar transformers (e.g. the Norton amplifier [187, 188, 189][19]).
The wide band LNA using transformer feedback from collector to base (CEXCB in Fig. 64), was simulated with an IIP_3 of 16 dBm at 500 MHz and 50 kHz 2-tone spacing, a gain of 15.5 dB and sub-1 dB noise figure, consuming 6 mA from a 3 V supply. The transformation ratio of the ideal transformer was 1:N = 1:4. Using a 1:5 transformer, an IIP_3 of 10.5dBm is possible with 16.7dB of gain. This circuit features excellent NF and S_{22} properties and would have been an ideal solution for the TETRA/TETRAPOL LNA, but stability is critical and the input impedance is far from 50 Ω at low frequencies.
Using the same configuration with transformer feedback from the collector to the emitter, (CEXCE in Fig. 64), resulted in an IIP_3 of 11.3 dBm with 14.9 dB of gain at 500 MHz +/- 25 kHz while the circuit consumes 6.5 mA at 3 V. A 1:5 transformer reduces IIP_3 to 9.8 dBm but increases gain to 16.2 dB. Stability is critical, however better than using collector-to-base transformer feedback (CEXCB). Again the input impedance is far from 50 Ω at low frequencies.
In order to achieve a better input return loss across a large frequency band, we finally investigated a common-base input stage, where a broadband Z_{in} is given by $r_e + R_e = V_{th}/I_C + R_e$ with R_e being the emitter resistance and the diffusion capacitance being neglected at low frequencies. While a collector current of $I_C = 0.5$ mA leads to 50 Ω input impedance, a reasonable IIP_3 requires currents of several mA. In order to match the 50 Ω source to this low impedance, a transformer was used (CBXIN in Fig. 64). Biasing the RF stage with 4 mA, a 2:1 transformer yields an almost perfect match due to the impedance transformation of 4:1. In addition the transformer provided a current gain of 4 (6dB). NF was minimised by using three 6 finger devices but the high parasitic collector base capacitance led to an inherent gain roll off due to the formation of a low-pass at the output node, unless cascaded by an additional, smaller common-base HBT. As the common-base device has unity current gain, power gain can only be obtained by impedance transformation. This requires a large value for the load resistor, followed by an emitter follower (EF) to transfer the high voltage swing at the load resistor to 50 Ω at port 2. While the EF can provide infinite output current when the voltage goes low at its emitter node, 180° later the EF itself switches off and the current source of the follower has to sink the complete current from port 2. In order to prevent clipping of the waveform, a large current in the EF's current source is needed and linearity is therefore directly related to the current in the EF. An IIP_3 of +6 dBm required a current of 13 mA in the EF. In total, this circuit

[19] A resimulation showed that the Norton amplifier suffers from stability problems due to the low reverse isolation.

simulated 18 dB of gain but suffered from a large noise figure of 2.8 dB at 500 MHz and a high current consumption of 4 mA in the input stage and 13 mA in the emitter follower. Summarising, LNAs based on transformers did not fulfil the linearity, noise and power requirements of this thesis and suffered from stability problems.

6.3 Simultaneous noise and power match in narrowband LNAs

It turned out that narrowband LNAs using a reactive output match tuned to the operating frequency outperform broad-band designs in terms of noise figure and linearity. In narrow band designs, negative series feedback by inductive degeneration is used to increase linearity and it has been shown that the transconductance stages using inductive degeneration are more linear than those using resistive degeneration with the same current and the same transconductance [190]. They have lower noise figures, since the degeneration inductor – apart from its loss resistance – does not introduce any additional noise. To reduce the noise contribution of the input stage, large transistors with multiple emitter stripes and low base resistance are used (see Fig. 18). LNA design starts by finding the optimum bias condition for lowest noise figure (see Fig. 65).

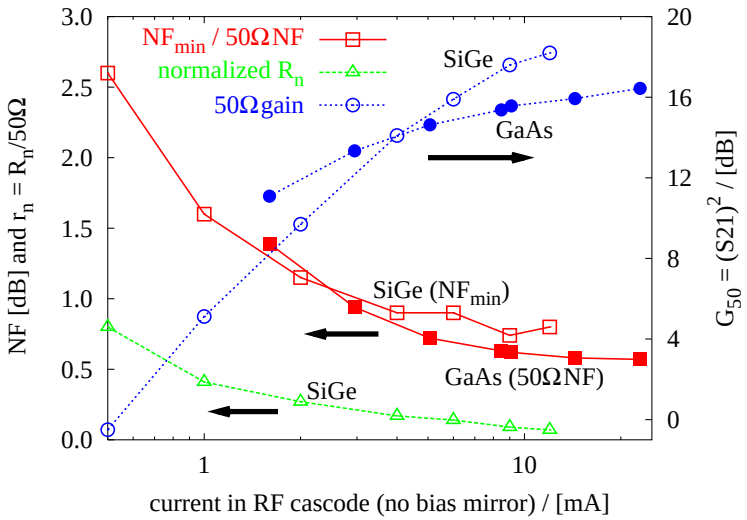


Figure 65: The optimum bias point of the SiGe LNA core of Fig. 18 for low noise operation is above 4 mA (f = 2 GHz). The low base resistance of a SiGe HBT results in a low equivalent noise resistance R_n, which in turn makes the noise figure quite insensitive to source mismatch at higher currents. For comparison, measured data of the pHEMT LNA from Fig. 149 are shown: pHEMT can deliver lower noise figure compared to SiGe HBT, but a higher operating current is needed.

Plotting Hawkins's formula for NF_{min} from Eqn. 64 against the collector current of a bipolar transistor shows a pronounced minimum at a certain current density. The region

below the minimum is governed by the shot noise $\alpha_0/|\alpha(f)|^2$, the area above by the thermal noise $\propto (R_b + R_e + R_{opt})/V_{th} \cdot I_c$. For the Atmel Sige HBTs, due to their very low base and emitter resistance, there is no pronounced minimum and low noise operation can be achieved via a wide range of collector current. For the 2 GHz LNA shown here a collector current of 6 mA has been chosen for low NF, sufficient gain and reasonable linearity (as shown later).
Achieving minimum noise figure and optimum gain at a given bias point simultaneously requires that the condition

$$\Gamma_{opt} = \frac{Z_{opt} - 1}{Z_{opt} + 1} = S_{11}^* \tag{71}$$

is fulfilled[20] at the design frequency, where Γ_{opt} is the source reflection coefficient for minimum noise (Fig. 67). Matching networks on silicon are associated with substrate losses that are considerably higher compared to GaAs-based circuits with their semi-insulating substrates (section 5.3). Therefore the design target is to match the device with a minimum amount of passive components. To achieve that, one degree of freedom is the transistor size [172], the other one the emitter degeneration impedance. Using active matching techniques [86], the emitter area of the common-emitter HBT is increased to the point that the real part of Γ_{opt} equals 50 Ω, resulting in a 6-finger device at 2 GHz (see Fig. 17). Doing so, the larger device size moves the source impedance for minimum noise figure from the high-impedance region of the Smith chart[21] towards the centre (Fig. 67). Using the emitter degeneration inductor, the real part of Z_{11} – which is typically below 50 Ω for a large bipolar transistor – can be moved towards 50 Ω. This is shown as follows: From the simple small-signal equivalent circuit of a bipolar transistor shown in Fig. 66, the Y-parameters shown in Eqn. 72 are evident.

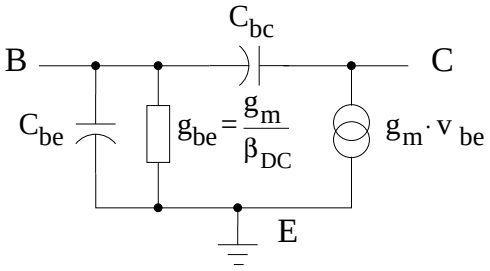


Figure 66: Simple small-signal equivalent circuit of a bipolar transistor in common-emitter configuration.

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} g_m/\beta_{DC} + i \cdot \omega \cdot (C_{BE} + C_{BC}) & -i \cdot \omega \cdot C_{BC} \\ g_m - i \cdot \omega \cdot C_{BC} & i \cdot \omega \cdot C_{BC} \end{bmatrix} \tag{72}$$

[20] assuming that the output is terminated with 50 Ω or the device is unilateral ($S_{12} = 0$).

[21] Phillip H. Smith developed the chart that bears his name in the 1930's to assist RF and microwave engineers deal with impedances along transmission lines: The impedance plane is mapped into the unit reflection coefficient (ρ) circle. Points of constant VSWR are now mapped into circles.

Using $h_{21} = Y_{21}/Y_{11}$ [142] we get

$$h_{21} \approx \frac{\beta_{DC}}{1 + i \cdot \omega \cdot \frac{\beta_{DC}}{g_m} \cdot (C_{BE} + C_{BC})} = \frac{\beta_{DC}}{1 + i \cdot \omega/\omega_\alpha} \tag{73}$$

where ω_α is the 3-dB roll-off frequency of the current gain. The unity gain cut-off frequency f_T where h_{21} drops to "1" is then defined by

$$2 \cdot \pi \cdot f_T = \omega_\alpha \cdot \beta_{DC} = \frac{g_m}{C_{BE} + C_{BC}} \tag{74}$$

For the applications covered in this thesis, $\omega \gg \omega_\alpha$ and therefore

$$h_{21} \approx \frac{\beta_{DC} \cdot \omega_\alpha}{i \cdot \omega} = -i \cdot \frac{g_m}{C_{BE} + C_{BC}} \cdot \frac{1}{\omega} \tag{75}$$

An impedance Z_E in the emitter of a bipolar transistor is seen at the base terminal as $Z_B = h_{21} \cdot \ Z_E$. For an inductive emitter degeneration, $Z_E = i \cdot \omega \cdot L_E$ and therefore

$$Z_B = \left(-i \cdot \frac{g_m}{C_{BE} + C_{BC}} \cdot \frac{1}{\omega}\right) \times (i \cdot \omega \cdot L_E) = \frac{g_m}{C_{BE} + C_{BC}} \cdot L_E = 2 \cdot \pi \cdot f_T \cdot L_E \tag{76}$$

This means that an inductance in the emitter of a transistor is transformed into a noiseless *real part* at the input terminal. It needs to be noted that f_T in this case refers to the actual operating current and is much lower than the peak-f_T of the technology, as the LNA transistor is biased at a very low current density. This technique, which is widely used in the design of bipolar LNAs (e.g. [191, 192, 78, 193, 194, 172, 173]), has previously been presented for GaAs-MESFETs [195, 172, 173] and is used in pHEMT LNA design [196] and sub-μm MOSFET design [197] as well. The LNA core of Fig. 18 uses a common-emitter input stage cascaded with a common-base stage to avoid the low pass behaviour associated with the Miller effect [195, 198]. Using measured S-parameters of this core at 6 mA, the effect of an ideal emitter inductor at 2 GHz is shown in Fig. 67. The emitter inductor raised the low real part of Z_{11} (location A) to $\approx$ 50 Ω (location B) without affecting the source termination for minimum noise figure too much (Fig. 67, left). The minimum noise figure itself is invariant against this kind of transformation (Fig. 67, right). While the total gain is reduced (right), linearity increases (not shown). In order to minimise the noise figure, this inductor is often realised by a bond wire and the inductance of the package pin, rather than using an integrated inductor with a series resistance of approximately 1 Ω per nH (see chapter 5).

With L_e at 0.5 nH (location B), a simple series inductors of $L_{in} = 2.5$ nH finally moves the remaining imaginary part of Γ_{opt} and S_{11}^* towards 50 Ω (location C), resulting in simultaneous noise and power match. This series inductor in the base of the 6-finger device is realised by the bond wire, the package pin and a thin trace on the PCB in order to avoid contributions to the noise figure by series resistances of integrated inductors.

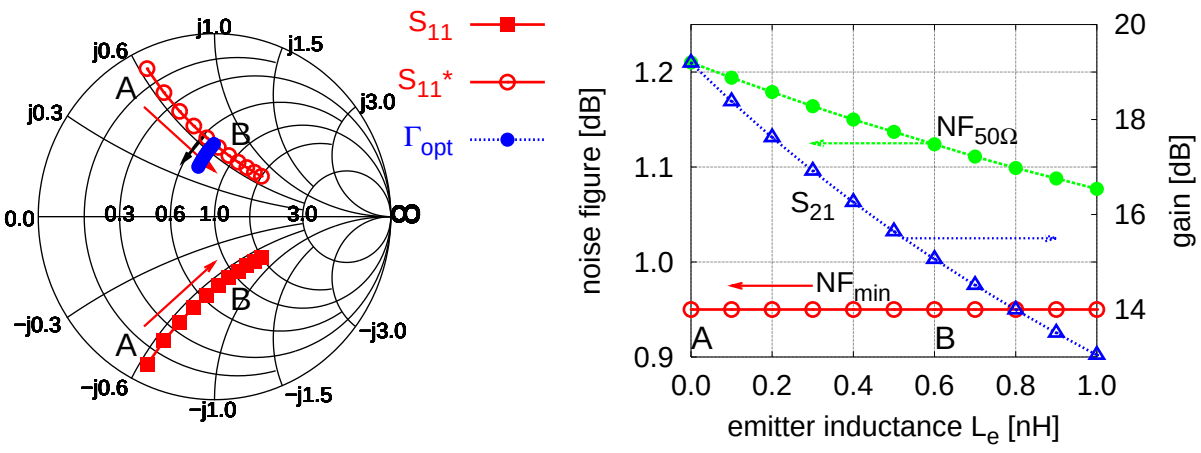


Figure 67: Inductive series degeneration at the emitter terminal raises the low real part of Z_{11} to $\approx 50\ \Omega$ without affecting the source termination for minimum noise figure too much (left). The minimum noise figure itself is invariant against this kind of transformation (right). While the total gain is reduced (right), linearity increases (not shown).

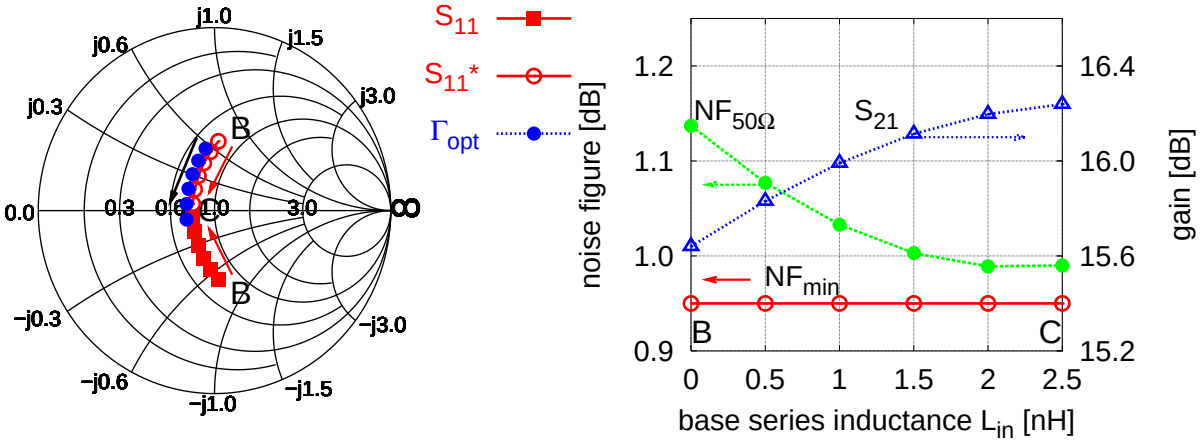


Figure 68: With L_e at 0.5 nH, a simple series inductors of $L_{in} = 2.5$ nH finally moves both the location of power match S_{11}^* and the location of noise match Γ_{opt} towards the centre of the Smith chart (50 Ω).

Targeting 30 Ω instead of 50 Ω for $\Gamma_{opt} = S_{11}^*$ results in a larger device size and lower noise figure while still resulting in reasonable input return loss (-12 dB). The complete procedure is summarised in Fig. 69.

As the noise figure is dominated by the large common-emitter device, a small 2-finger HBT

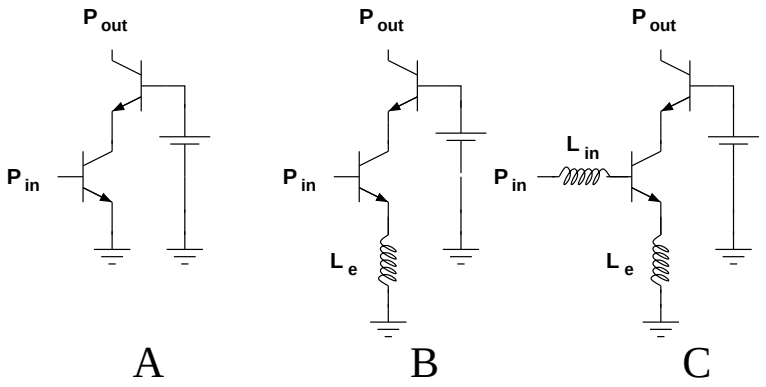


Figure 69: 3-step simultaneous noise and input match using a minimum number of reactive components.

can be used in the cascaded common-base output stage. The cascode leads to a higher isolation from the amplifier output to the input, reducing $|S_{12}|$. This unilateralization increases the stability factor k and allows to match input and output independently [173], as the common-emitter stage now drives the constant low impedance of the emitter of the common-base transistor making the amplifier insensitive to output load variations. Bandwidth is increased by reduction of the Miller capacitance defined as $C_M = C_{CB} \cdot (1 + g_m \cdot R_L)$, where C_M is the effective shunt capacitance seen at the amplifier input, resulting from the parallel collector-base feedback capacitor C_{CB}. As the load resistance R_L to the common-emitter stage is the dynamic emitter resistance of the common-base stage ($1/r_E$), the Miller capacitance is just twice the base collector capacitance and thus much lower than it would be in a normal common-emitter amplifier [199]. This comes at the expense of additional headroom and a separate pin to block the base of the common-base transistor to GND[22]. The base of this device is blocked by means of a 5 pF MIM capacitor. In order to achieve power gain, a high output impedance needs to be presented to the output of the cascode configuration. As discussed in section 6.2.3, the use of an EF for impedance transformation is prohibitive for highly linear LNAs as it would result in a very low linearity due to waveform clipping by the EF realistic bias currents. Therefore the 50 Ω output impedance is transformed to a high impedance at the cascode output by means of a passive, integrated LC matching network. In order to feed the bias current to the cascode and to have a DC block at the output, a shunt-L / series-C configuration was used, where the inductor is shunted to the supply rather than GND. As a large inductor is needed, for the GPS and SCUBA LNAs the inductor was realised in the top metallisation of Atmel's SiGe1 technology (see section 5.7) and for the 2.4 GHz WLAN LNA a multilevel spiral (section 5.16) was used. In order to become independent from inductances due to bond wires and parasitic traces on the PCB, the supply voltage

[22]If the GND of the common-emitter stage and the GND of the capacitor blocking the common-base stage are not separated, the LNA – due to positive feedback from the common bondwire inductance – turns into an oscillator.

was blocked on-chip at 2 GHz with an integrated MIM capacitor of 10 pF, in series to a 5 Ω resistor to damp low frequency resonances, which would result from interaction of on-chip inductance, bondwire and external SMD blocking capacitor on the PCB. The DC blocking capacitor at the input was not integrated due to noise reasons. As an example for this design technique, the noise figure of the UMTS SiGe LNA of the SCUBA project (see Fig. 6) as a function of the input impedance is shown in Fig. 70. The measurements have been performed using a NP5 noise tuner system from *atn microwave* at the *Zentrum für Mikroelektronik Aargau (ZMA)* in Switzerland[23]. The results confirm this LNA design technique and show a minimum NF of ≈ 0.9 dB, just slightly higher than the 0.6-0.8 dB of the SiGe HBT itself. The 50 Ω-NF was measured to be 1.15 dB (see Fig. 137 in appendix A, which is dedicated to the task how to measure low noise figures accurately).

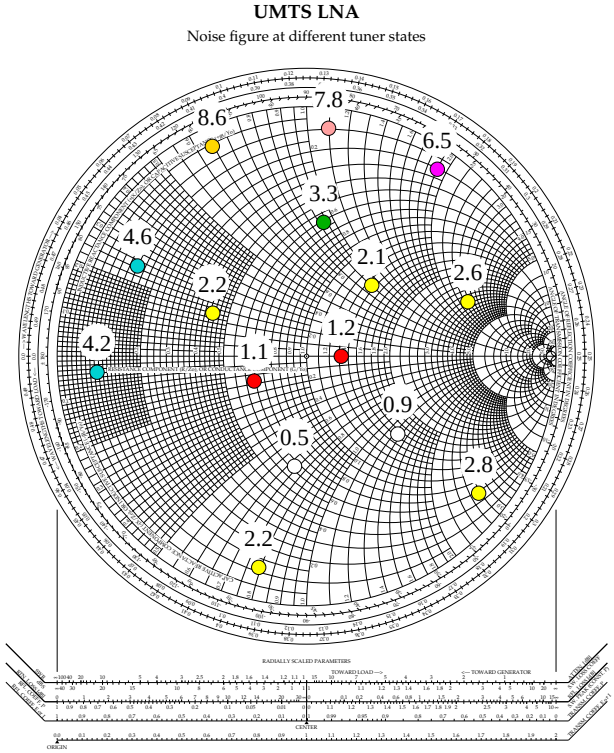


Figure 70: Noise figure of the UMTS LNA for different input impedances, measured at 1.95 GHz with a NP5 source pull system (atn microwave).

[23]The large spread of the data points originates from the fact that the diode-based *atn* tuners – due to losses in the diodes – cannot cover the Smith chart evenly and the low sensitivity makes noise measurements below 1 dB difficult.

6.3.1 Application to CMOS LNAs

The design of sub-μm MOSFET LNAs follows exactly the same design criteria as outlined before [197]. Although scaling of sub- μm gate length becomes difficult [200], it has been shown for a 0.24 μm CMOS technology that devices with minimum gate length offer the best noise performance and that the minimum noise figure NF_{min} just depends on L_g and is independent of the gate width W. So W remains as a parameter to control the size of R_n ($\propto 1/W$) and the location of Γ_{opt}: The high $Z_{opt} = 1/(G_{opt} + j \cdot B_{opt})$ needed for optimum noise performance of MOSFETS can be decreased towards 50 Ω as $G_{opt} \propto W$ and $B_{opt} \propto W$ [197]. The differences to HBT LNA design are

1. Due to the higher equivalent noise resistance R_n (see table 8) the selection of the device size of the input transistor is much more critical.

2. Due to the lower transconductance g_m the size of the cascode device is much more critical. The cascode MOS transistor can contribute up to 40% to the total MOS LNA noise figure.

3. Due to the lower operating f_T, a larger source inductance is needed to move the real part of the input impedance towards 50 Ω (Eqn. 76). Due to the higher input capacitance, a much larger gate inductance is needed to move S_{11}^* and Γ_{opt} simultaneously towards 50 Ω (e.g. 36 nH for a 900 MHz CMOS LNA [197]), making the input match more narrowband. Furthermore, this large inductance cannot be provided by a bondwire and a small inductive trace on the board, as it is usually the case for SiGe HBTs, but requires the use of a discrete, high-Q (e.g. wirewound) SMD inductor.

6.4 Bias considerations

While much attention is paid to the 2-6 fast RF transistors of a typical RFIC building block, the optimisation of the bias network is often neglected. The bias network needs to ensure a stable RF performance versus changes in supply voltage and temperature. It needs to be insensitive against process variations, as there are in a typical silicon process

- variations of the poly silicon resistors by up to ± 20 %
- variations in the MIM capacitors of up to ± 10 %
- current gains of 100-500 for a SiGe HBT and 40-100 for a Si BJT
- variations in the threshold voltage of MOS devices.

In addition the bias network needs to ensure low leakage currents in power down mode [201]. For an excellent overview about the art of biasing see [202]. Due to the high variation in a

SiGe HBT's current gain β, such a device should never be biased by forcing a base current itself without any feedback via the emitter or collector current. From the semi-empirical current-voltage relationship the strong temperature dependence of the transconductance is evident:

$$I_C = I_0 \times e^{\frac{V_{BE}}{V_{th}}}(1 + \frac{V_{CE}}{V_A}) \approx I_0 \times e^{\frac{V_{BE}}{V_{th}}} \quad \text{with} \quad I_0 = A \times j_0 \tag{77}$$

$$g_m = y_{21} = \frac{\delta(I_2)}{\delta(V_1)} \mid_{\delta V_2=0} = \frac{\delta(I_C)}{\delta(V_{BE})} = \frac{I_C}{V_{th}} = \frac{q \times I_C}{k_B \times T} \tag{78}$$

I_0 and j_0 are saturation current and saturation current density per area, respectively, which are strongly temperature dependent. From Eqn. 78 its evident that constant small signal gain versus temperature dictates the bias current to vary Proportional-To-Absolute-Temperature (PTAT). As the resulting drop of $P_{1\,dB}$ and IP_3 at low temperatures and bias currents is often undesirable, the slope of current versus temperature is typically somewhere between zero and PTAT.
The simple LNA bias circuit of Fig. 71 is often used, where the base voltage is fixed by a resistive divider and the emitter current is set by the voltage drop across the emitter resistor. If the impedance of the resistive divider is high, there is considerable voltage drop due to the base current of the transistor. The strong β-variations from lot to lot in SiGe HBTs therefore result in a large spread of the emitter current. If the impedance of the divider is too low, it increases the NF of the LNA. The strong dependence of the emitter current on the supply voltage is another drawback for this bias scheme. With respect to the temperature the bias current increases only slightly due to the decline of V_{BE} by 1.5–2 mV/K.

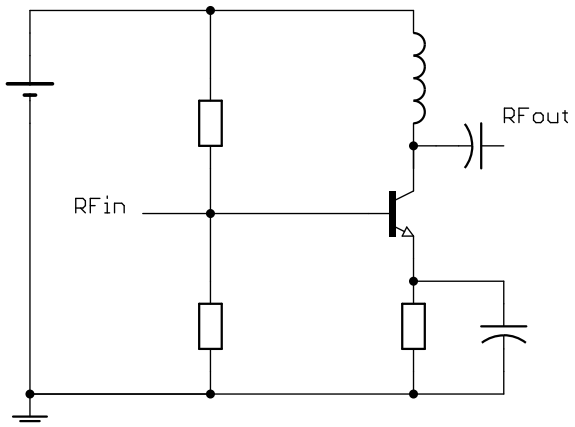


Figure 71: Simple LNA bias network.

Therefore biasing via current mirrors is usually employed (Fig. 72). Mirror ratios are commonly limited between 1:6 and 1:12, as the finite current gain of the transistors

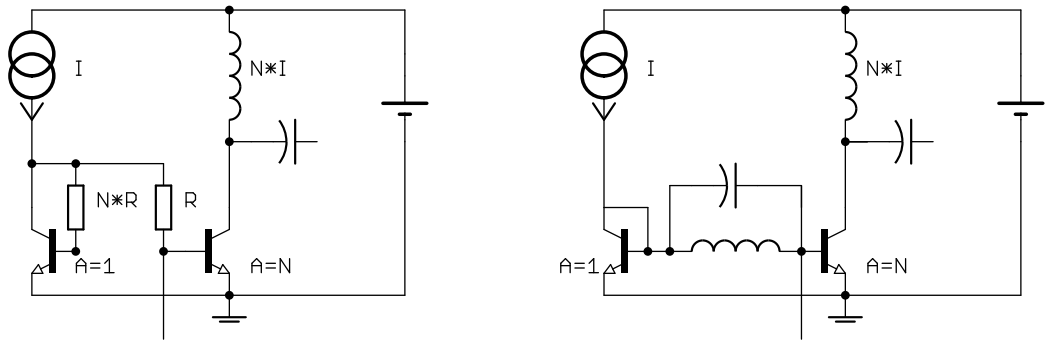


Figure 72: Current mirror bias network: Large bias resistances avoid loading of the RF stage (left). Inductive LNA biasing (right) requires the use of an external SMD inductor due to the substrate losses of the integrated inductor.

introduces an error into the mirror ratio [93]. This means that a considerable amount of DC current (8-17%) is lost in the bias branch. Using the resistive version, a trade-off between NF and IIP_3 needs to be made: While large bias resistors minimise the loading of the RF stage by the bias network and lead to a good noise figure (see measurements in Fig. 73), high IP_3 values require low impedances (see section 6.7.2). A typical value of the bias resistor for acceptable NF and medium IP_3 is 1-4 kΩ. Inductive biasing via an inductor or an LC tank is popular for PA and driver stages, as a low bias impedance increases the breakdown voltage from $BV_{CE,0}$ to $BV_{CB,0}$ (see table 26). While substrate losses of the integrated inductors (see chapter 5) are uncritical for PA and driver stages, inductive LNA biasing requires the use of a SMD inductor, as the substrate losses of the large integrated inductor increase its NF. The SCUBA LNA used this bias scheme.

The mirror-based bias circuit of Fig. 72 requires a stable reference circuit over supply voltage. The PTAT bias networks based on the Widlar bandgap reference [203, 204, 205] shown in figure 74 have been used in this thesis. Fig. 74 shows the ΔV_{BE}-cell with the area ratio N along with the regulation amplifier and its RC-feedback that ensures sufficient open-loop phase margin for stability. The all-NPN implementation (left) regulates to a 2 V reference voltage, while the BiCMOS version (right) can generate the PTAT reference current directly, which is profitable when distributing currents along long lines as it is insensitive to voltage drops[24]. Using Kirchhoff's voltage law that the voltages across a loop sum up to zero, we can easily calculate that the currents in the bandgap are indeed PTAT.

$$I_1 \times R_0 + V_{BE,A_5} = V_{BE,A_1} \quad (79)$$

$$I_1 \times R_0 = V_{th} \times \left[\ln(\frac{I_2}{j_0 \times A_1}) - \ln(\frac{I_1}{j_0 \times A_5}) \right] \quad (80)$$

[24]In pure CMOS processes, ΔV_{BE} bandgaps can be used as well, where p-well / n-well diodes with different area factors replace the bipolar transistors [206].

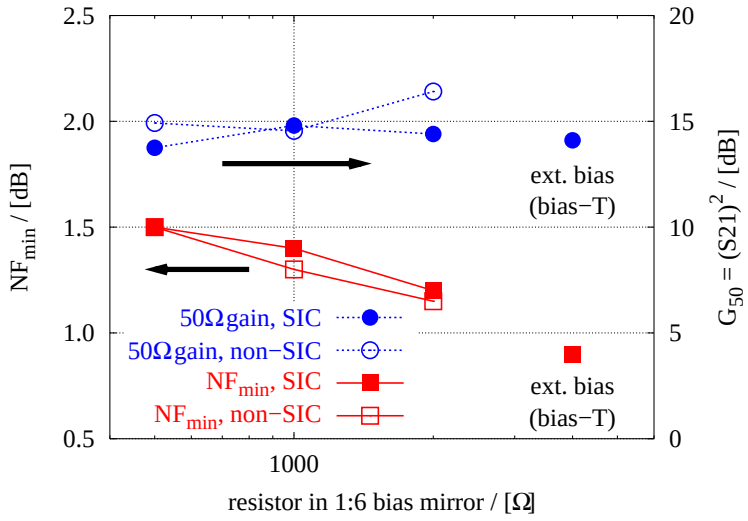


Figure 73: Increasing the bias resistor in the LNA core of Fig. 18 reduces its NF. The lowest value is obtained by using a very large inductor (e.g. bias-T).

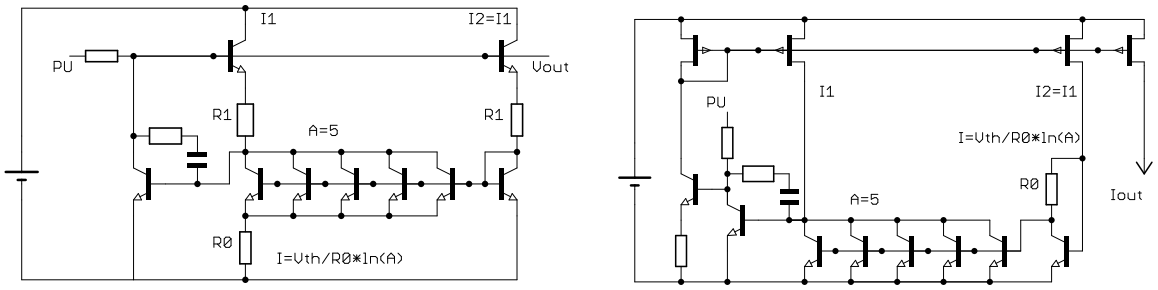


Figure 74: PTAT bandgaps based on the Widlar ΔV_{BE}-cell: Left: all-NPN implementation, right: BiCMOS version.

$$I_1 = \frac{V_{th}}{R_0} \ln\left(\frac{A_5}{A_1}\right) = \frac{k_B \cdot T}{q \cdot R_0} \ln(5) \quad \text{if} \quad I_1 = I_2 \quad \text{and} \quad \frac{A_5}{A_1} = 5 \quad (81)$$

$$V_{out} = 2 \times V_{BE} + R_1 \times I_1 = 2 \times V_{BE} + V_{th} \times \frac{R_1}{R_0} \ln(5) \quad (82)$$

Fig. 75 shows the output current of the BiCMOS current reference of Fig. 74, right.

The output current shows only little dependence on the supply voltage. To achieve a high output resistance at the output node, large PMOS transistors (L=1.5μm, W=40μm, 2 fingers) have been used in the current mirror. References of this kind with 1 V supply voltage have recently been reported [207].
Finally, bias networks based on operational amplifiers sense the collector current and compare it to an accurate PTAT reference current (Fig. 76). They are immune against

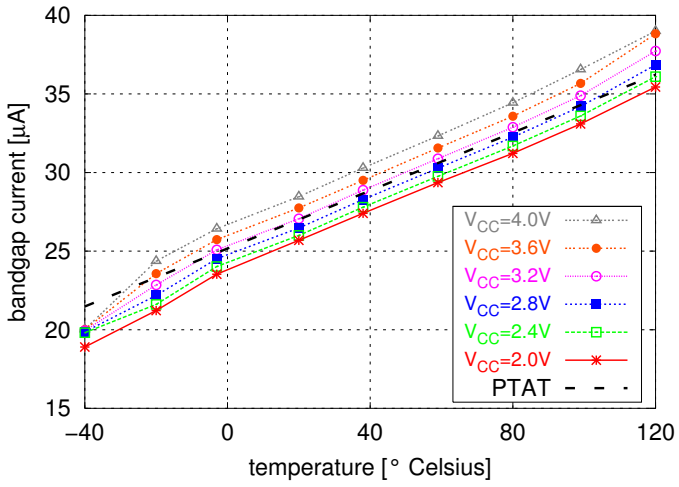


Figure 75: Current versus ambient temperature measured for the BiCMOS current reference of Fig. 74, right.

variations in device β and supply voltage. The cross-coupled, stacked-npn bias cell based on the translinear cross-quad delivers a PTAT output current with little overhead bias current. The bias current from the power-up pin is not critical in determining the PTAT output current [208]. The absence of a regulation amplifier makes the cell robust and easy-to-use as there is no ringing during start-up.

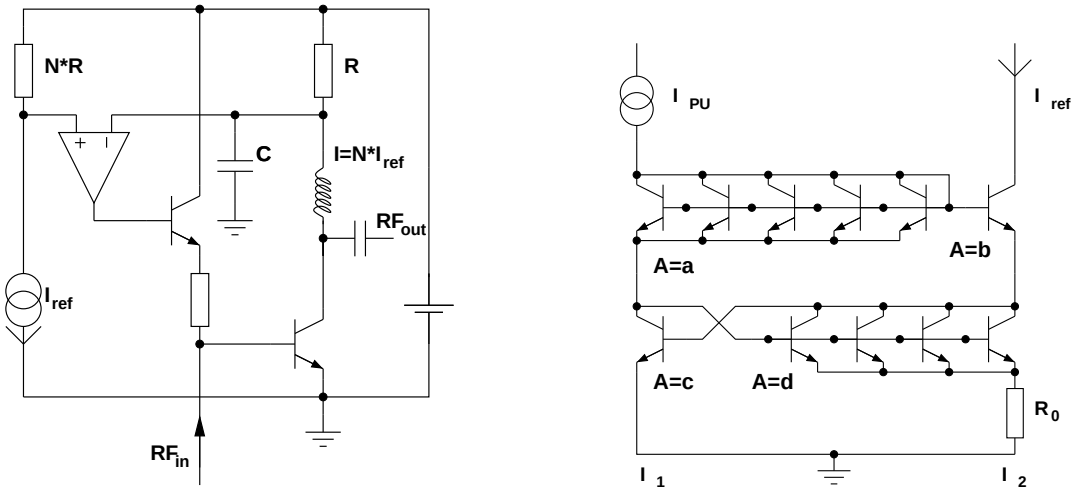


Figure 76: OP-based LNA bias network (left) and ΔV_{BE} PTAT cell using the translinear cross-quad (right) [208]. a,b,c and d denote the areas of the transistors.

Again, the output current of this translinear cross-quad can be easily calculated using Kirchhoff's voltage law, assuming that all transistors have the same current density j_0:

$$I_2 \times R_0 \;+\; V_{BE,d} + V_{BE,a} = V_{BE,b} + V_{BE,c} \tag{83}$$

$$I_2 \times R_0 \;=\; V_{th} \times \left[\ln(\frac{I_2}{j_0 \times b}) + \ln(\frac{I_1}{j_0 \times c}) - \ln(\frac{I_2}{j_0 \times d}) - \ln(\frac{I_1}{j_0 \times a}) \right] \tag{84}$$

$$I_2 \;=\; \frac{V_{th}}{R_0} \ln \left[\frac{d \times a}{b \times c} \right] = I_{ref} \qquad \text{(independent of } I_1 \text{ !)} \tag{85}$$

6.5 The influence of bias conditions on linearity

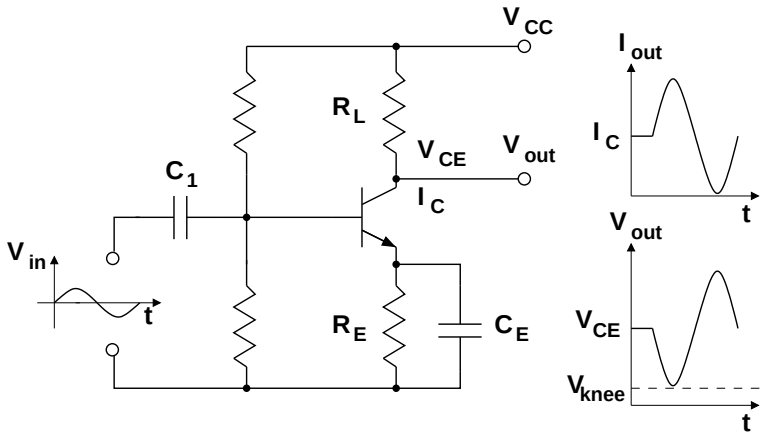


Figure 77: Class A amplifier operation.

Linearity is mainly a function of device current. Lucek and Damen [171] give the following rule of thumb for a transistor's OIP_3:

$$OIP_3\,[dBm] \;= 10 \cdot \log(V_{CE} \cdot I_C \cdot 5) \tag{86}$$

where V_{CE} is in V and I_C is in mA. This equation is derived from the loadline analysis of a BJT in class A operation (Fig. 77), where the maximum linear output power is given by

$$P_{lin,out} = V_{eff} \cdot I_{eff} = \frac{V_{CE} - V_{knee}}{\sqrt{2}} \cdot \frac{I_C}{\sqrt{2}} = (V_{CE} - V_{knee}) \cdot I_C \cdot 0.5 \tag{87}$$

Neglecting the knee voltage of ≈ 0.5 V for our SiGe HBTs compared to the collector emitter voltage V_{CE} and assuming that OIP_3 is 10 dB higher than the output P_{1dB} [209], which in turn is estimated to be equal to $P_{lin,out}$ leads finally to Eqn. 86 [210]. Eqn. 86 gives an upper bound for linearity in terms of OIP_3 which cannot be exceeded without special circuit design techniques as described in the following sections. The output-referred 2-tone IP_3 of the SiGe LNAs developed in this thesis has been plotted in Fig. 78 versus

the bias current in the *RF-stage* along with published values for a popular, enhancement-mode pHEMT from Agilent. The red line of Eqn. 86 gives an upper bound for an ideal transistor which can swing at the output from "0" to "$2 \times V_{CC}$" without any clipping ($R_L = 0$, inductive load). As all SiGe LNAs with $V_{CC} = 3$ V depicted in Fig. 78 used a cascode configuration where the common-base HBT is biased at 1.4 V, a second line is drawn which allows a full swing of just 1.6 V.

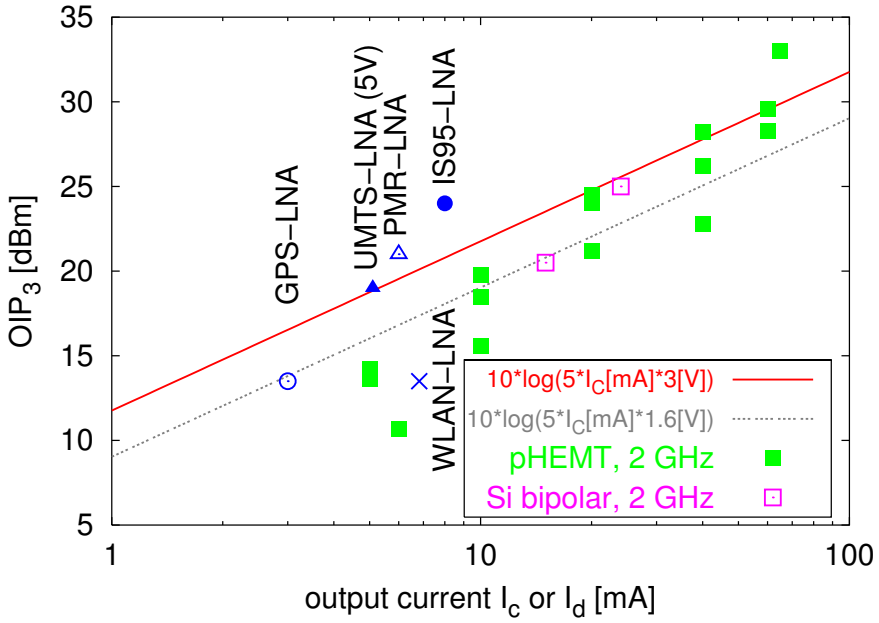


Figure 78: 3rd order intercept point (output-referred) for single stage amplifiers of various technologies at 3 V of supply voltage. SiGe HBT data are from this work, data for pHEMT are taken from [211, 212, 213], Si bipolar (Infineon BFP450) from [214] and OIP_3 rule-of-thumb according to Eqn. 86.

The following conclusions can be drawn from this figure:

1. Linearity is mainly a function of device current.

2. HEMTs do not offer better linearity than SiGe HBTs, especially not at low current levels.

3. As will be described in the following sections, (i) hitting Lucek and Damen's results of Eqn. 86 is only possible using techniques like reactively matched designs with low frequency terminations and (ii) exceeding this line is possible only using cancellation techniques.

6.6 Effect of series and parallel feedback on noise figure and linearity

As has been explained in section 6.3, the use of series feedback is mandatory to achieve noise and power match simultaneously. In addition, gain is decreased and linearity in terms of input-referred intercept point IIP_3 is increased. As can be seen in Fig. 78 and from Eqn. 86, output-referred linearity is mainly a function of the total device current [215] and cannot strongly be influenced by feedback. While inductive series feedback is used in most LNA designs, parallel feedback from collector to base is usually not used due to the following reasons:

- According to Eqn. 61, parallel feedback decreases reverse isolation leading to LO feedthrough from the mixer to the antenna[25]. This is especially unacceptable in direct conversion receivers, as it leads to DC offset at the mixer output. In addition, the stability is decreased.

- LNAs with large values of S_{12} show strong dependence of the input match Γ_S on the output match Γ_L as $\Gamma_S = S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - S_{22} \cdot \Gamma_L}$. Unilateral LNAs with S_{12}=0 are easy to match, as $\Gamma_S = S_{11}$, independent from the output reflection coefficient Γ_L and vice versa. Twoports with strong parallel feedback, however, are extremely difficult to match as the output matching network has influence on the input matching network which, in turn, depends on the output match.

- Resistive parallel feedback as shown in Figs. 63 or 133 has detrimental effects on noise figure, if the feedback resistance is low.

Iversen in 1974 [216] derived the theoretical formulae which describe the influence of parallel and series feedback on the noise figure of a twoport and and Boglione [217] *et al.* for the equivalent noise resistance R_n. As the formulae are rather involved and difficult to apply to feedback elements with parasitic networks (e.g. MIM capacitors), the effect of a MIM feedback capacitor has been measured at 2 GHz using versions of the LNA core shown in Fig. 18 with different feedback capacitor (no emitter degeneration):

As expected, the gain decreases strongly with increasing feedback, but the minimum noise figure remains constant. No reduction of the noise figure due capacitive feedback has been observed, as proposed by Cooke [218] for a common-emitter stage[26]. As has been shown

[25] This is not the case for ideal series feedback: The S-parameters for series emitter feedback with resistor R_e can be obtained from Eqns. 56-61 by setting $R_{fb} = \infty$ and replacing $g_m = I_C/V_{th}$ by the transconductance of the emitter degenerated BJT, which is $g_{m,sf} = g_m/(1 + g_m \cdot R_e)$. This way $S_{11} = 1$, $S_{22} = (R_l - Z_0)/(R_l + Z_0)$, $S_{21} = -2 \cdot g_{m,sf} \cdot R_l \cdot Z_0/(R_l + Z_0)$ and $S_{12} = 0$. Rollet's k is infinite and $\Delta = S_{22} < 1$. This means the ideal BJT amplifier with emitter series feedback has infinite reverse isolation and is unconditionally stable.

[26] Cooke points out, however, that the noise measure $M = G \cdot (F - 1)/(G - 1)$ [219], where G is gain and F is noise factor remains constant.

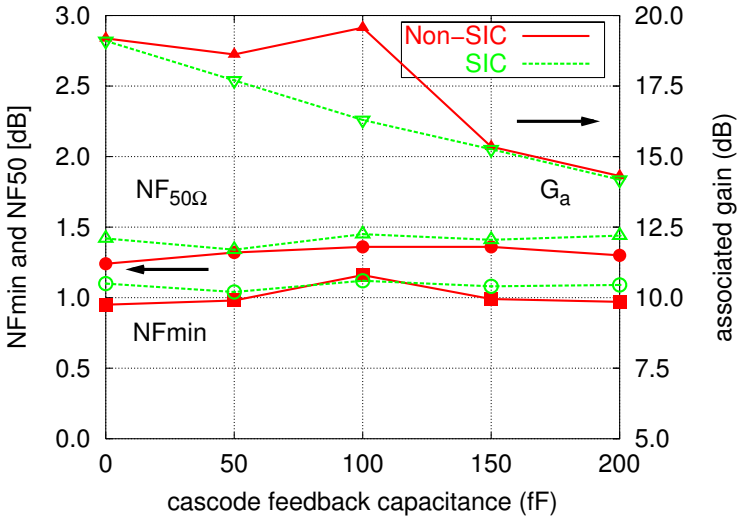


Figure 79: The measured noise figure of the LNA core of Fig. 18 is insensitive against parallel, capacitive feedback (f = 2 GHz).

in Fig. 67, NF remains constant also for ideal inductive series degeneration (L_e). It is important to note that small amount of L_e improves stability factor (equation 62) at lower frequencies, but with increasing amount of L_e, stability at higher frequencies – which means several times the operating frequency – is compromised [220]. So care needs to be taken to watch wide-band stability when using inductive series feedback. A crude but effective fix is a tiny shunt capacitor to GND at the LNA output [220].
Inductive parallel feedback has been proposed for common-gate MESFETs to cancel the drain-source capacitance [172]. However, for common-source (or common-emitter) structures, inductive parallel feedback leads to oscillations and therefore this technique was not used here.

6.7 Linearity considerations for bipolar transistors

6.7.1 Analytical considerations

Talking about linearity, the fact is that there is no such a thing like a linear device: Even capacitors, inductors and resistors exhibit some kind of nonlinearity when driven at high input power. Multilayer ceramic capacitors, when operated above their maximum rated voltage, show a nonlinear $C(U)$ characteristic, which is the reason that the large capacitor values in audio amplifiers are realised using tantalum capacitors to avoid distortion. The nonlinearity of ferrite components like isolators, circulators or inductors with an iron or ferrite core is legendary. Even RF connectors have been found to generate intermodulation at high power levels, caused by the nonlinear resistance of the contacts between dissimilar metals in their construction [65]. On the other hand, *every* device is linear if you just make

the excitation small enough (Maas' First Law of Linearity [221]). A good definition for linear devices is that the superposition principle holds for them. This definition implies that the response of a linear, time-invariant system includes only those frequencies which are present at the input (time-varying circuits, even when linear, generate mixing products between the excitation frequencies, see chapter 7) [65]. As has been shown in section 3.1, nonlinear circuits generate a large number of new frequency components. Therefore, they are easily distinguished from linear circuits.

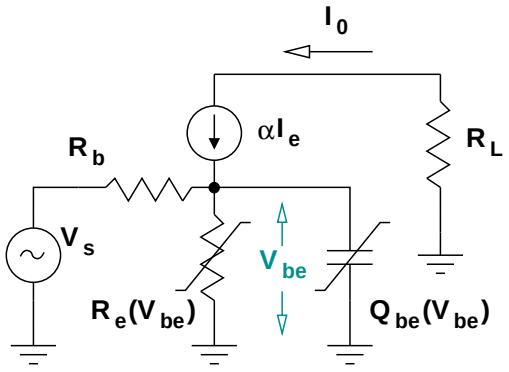


Figure 80: Equivalent circuit to illustrate the cancellation effects of diffusion capacitance and exponential nonlinearity in an HBT [222].

Distortion effects in bipolar transistors attracted the attention of researchers already more than 50 years ago, when Reynolds [223] experienced that distortion can be reduced drastically by inserting a small resistor into the emitter lead of a PNP transistor in common-base configuration. If a circuit is weakly nonlinear, techniques such as power-series (for frequency independent nonlinearities) or Volterra-series analysis (for nonlinearities that are frequency dependent), first applied to transistors by S. Narayanan of Bell Labs in 1967 [215, 224] can be used. From the strongly nonlinear, exponential transfer function of bipolar transistors one would conclude that its intermodulation (IM) behaviour is very poor. However, a Volterra-series analysis for HBTs by Maas *et al.* in 1992 came to the result that for frequencies well below f_T, IM current generated in the exponential base-emitter junction is partially cancelled by the nonlinearity generated by the junction capacitance and that this phenomena is largely responsible for the unusually good IM performance of the HBT [222]. Thus, paradoxically, it is the strong nonlinearity of both elements that causes the IM levels to be low. Without going into the complicated maths here, the cancellation effect holds for 2nd order and 3rd order intermodulation products: For 2nd order products, in the 'mid-frequency range' $\frac{1}{2\pi R_b c_1} \ll f \ll f_T$, IM current generated by the nonlinear diffusion charge

$$q_{be} = c_1 V_{be} + c_2 V_{be}^2 + c_3 V_{be}^3 \quad \text{with} \quad c_1 = \frac{\delta Q_{be}(V_{be})}{\delta V_{be}} = \frac{\delta(\tau \cdot I_e)}{\delta V_{be}} \quad \text{and } \tau = \text{forward transit time} \tag{88}$$

completely cancels IM current generated by the nonlinearity of the exponential transfer function, namely its nonlinear emitter resistance

$$i_{be} = g_1 V_{be} + g_2 V_{be}^2 + g_3 V_{be}^3 \quad \text{with} \quad g_1 = \frac{\delta i_e(V_{be})}{\delta V_{be}} = \frac{1}{r_e} = g_m \tag{89}$$

In practical devices, as junction capacitance consists of diffusion *and* depletion capacitance, the cancellation is only partial. At low frequencies there is no influence of the junction capacitance, and no cancellation takes place at $\omega_1 - \omega_2$ in a two-tone test[27]. 2nd order IM in the 'mid-frequency range' however, can be several dB better than this low-frequency value [222]. Maas proposed that it might be possible to improve the linearity of HBTs by closely tuning their capacitive and reactive nonlinearities, an effect I will make use of in section 6.8.7.
In the same way, there is partial cancellation in the 'mid-frequency range' ($\omega \gg 1/R_b c_1$) for 3rd order products [222]. Maas proposes a dedicated HBT model to predict the cancellation affects. We used the Standard Gummel Poon (SGP) model of the Atmel design kit instead, which led to slight discrepancies between measurement and simulation. In the general case of source impedances $Z_s \neq 50\,\Omega$, the cancellation effects described above occur at frequencies where the reactance of the junction capacitance is much less than $\Re\{Z_s\} + R_b$ (where R_b is the sum of extrinsic and intrinsic base resistance), and most of the nonlinear current in Fig. 80 circulates in the nonlinear emitter resistance and the junction capacitance [222].

6.7.2 Linearisation by series feedback

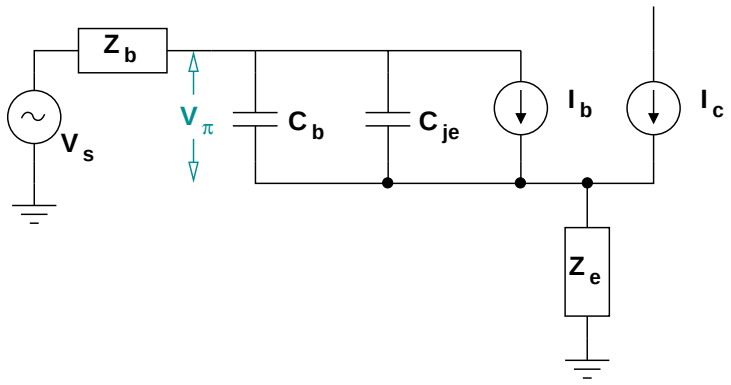


Figure 81: Equivalent circuit to illustrate the cancellation effects of diffusion capacitance and exponential nonlinearity in a HBT with series feedback [190]. Z_b is the sum of source resistance and base resistance of the device.

[27]Thus, as we will see in section 6.7.2, the linearity of HBT based amplifiers is especially sensitive to termination at this 'beat frequency' $\omega_1 - \omega_2$.

As shown in section 6.6, there is no negative effect of parallel capacitive or series inductive feedback on the noise behaviour. It does have, however, a big impact on linearity: In 1998, Fong and Meyer [190] extended Maas' approach and applied a Volterra-series analysis to transconductance stages, degenerated with series feedback (see Fig. 81):

$$I_c = A_1(s) \cdot V_s + A_2(s_1, s_2) \cdot V_s^2 + A_3(s_1, s_2, s_3) \cdot V_s^3 \tag{90}$$

V_s^n is the nth power of the voltage source signal, $A_n()$ is the Volterra series coefficient, which is a linear function of n number of frequencies and $s = j \cdot \omega$ the Laplace variable. Complicated calculations [190] using $I_c = I_Q \, exp\,(V_\pi / V_{th})$ – where I_Q is the saturation current of the HBT – and $I_b = I_c/\beta_0$ lead to $A_1(s)$, $A_2(s_1, s_2)$ and $A_3(s_1, s_2, s_3)$, where $A_1(s)$ is the small signal transconductance of the common-emitter stage:

$$A_1(s) = \frac{g_m}{[s \cdot C_{je} \cdot Z(s) + s \cdot \tau_F \cdot g_m \cdot Z(s) + g_m \cdot Z(s)/\beta_0 + 1 + g_m \cdot Z_e(s)]} \tag{91}$$

with $Z(s) = Z_b(s) + Z_e(s)$ and $g_m = I_Q/V_{th}$ (transconductance of the transistor without feedback). The IM_3 product at frequency $(2\omega_a - \omega_b)$ can be calculated by using the Volterra series coefficient $A_3(s_1, s_2, s_3)$ and letting $s_1 = s_a$, $s_2 = s_a$ and $s_3 = -s_b$. Typically the frequency difference between ω_a and ω_b is small and $s \approx s_a \approx s_b$. Using two input signals of the same amplitude V_s, the magnitude of the input-referred IM_3 products (not to be confused with the intermodulation *distance* between fundamental and IM_3) is given by

$$\begin{aligned}
|IM_3| &= \left| \frac{3}{4} \frac{A_3(s_a, s_a, -s_b)}{A_1(2s_a - s_b)} \right| |V_s|^2 \\
&\approx \left| \frac{A_1(s)}{I_Q} \right|^3 \left| \frac{V_{th}}{4} [1 + sC_{je}Z(s)] \times \left\{ -1 + \frac{A_1(\Delta s)}{g_m} [1 + \underbrace{\Delta s C_{je} Z(\Delta s)}_{\approx 0}] + \frac{A_1(2s)}{2g_m} [1 + 2sC_{je}Z(2s)] \right\} \right| |V_s|^2 \\
&\approx \left| \frac{A_1(s)}{I_Q} \right|^3 \left| \frac{V_{th}}{4} \left[1 + \underbrace{sC_{je}Z(s)}_{\text{deg.}} \right] \times \left\{ \underbrace{-1}_{\text{3rd order}} \underbrace{+ \frac{A_1(\Delta s)}{g_m} + \frac{A_1(2s)}{2g_m} [1 + 2sC_{je}Z(2s)]}_{\text{2nd order}} \right\} \right| |V_s|^2
\end{aligned} \tag{92}$$

As can be seen directly

- 3rd order intermodulation products are proportional to the cube of the ratio of small-signal transconductance $A_1(s)$ to collector current I_Q. $A_1(s)$ increases with collector current I_Q, but – depending on the feedback Z_e and the base impedance Z_b – always with a slope below I_Q (see Eqn. 91). Raising the collector current is therefore the most efficient means to improve 3rd order linearity.
- Using inductive degeneration, $[s \cdot C_{je} \cdot Z_e(s)]$ is a negative real number and cancels the '1' term partially. There is no such cancellation with resistive degeneration. Thus, common-emitter stages using series inductive degeneration are more linear than those using capacitive or resistive degeneration with the same transconductance and bias current [190].

- As shown in Fig. 68, a base inductor is necessary to achieve a simultaneous noise and power match. This results in additional IM_3 cancellation, as $[s \cdot C_{je} \cdot Z_b(s)]$ is a negative real number, too.

The 2nd order term in Eqn. 92 is typically low compared to the 3rd order term, however, it is not so small that it can be ignored. 2nd order products appear in Eqn. 92, as 2nd-order products generate 3rd order products when mixing with the fundamental tones [61]. This self-interaction is due to multiple feedbacks in the circuit: Z_e, C_{je}, $I_b(I_c)$, C_{bc} (the latter two terms were neglected here).
$|IM_3|$ can be lowered by increasing the $|A_1(\Delta s)|$ term (transconductance at low frequencies, Eqn. 91). This increases the second-order nonlinearity to cancel the third-order nonlinearity. Again inductive series degeneration is beneficial, as in that case Z_e has low impedance at low frequencies already. $|A_1(\Delta s)|/g_m$ can further be increased towards '1' by low $Z_b(\Delta s)$, e.g. a short circuit for low frequencies at the base. Therefore:

- Low impedance at base and emitter terminals at low frequencies $\omega_1 - \omega_2$ improves IP_3 as 3rd order non-linearities are cancelled partly by 2nd-order nonlinearities [190].

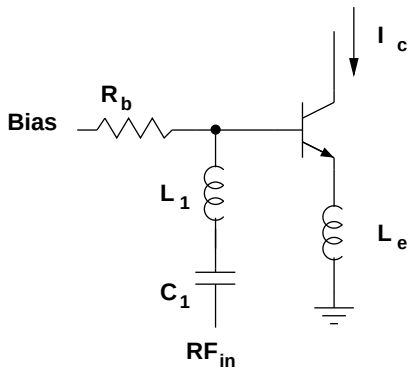


Figure 82: Inductively degenerated common-emitter transconductance stage [190].

For the example in Fig. 82, R_b is a bias resistor used to isolate the bias circuit from the RF_{in} port. At low frequency Δs, the impedance of $Z_e(\approx \Delta s\, L_e)$ is negligible and $Z_b(\Delta s)$ is dominated by R_b, as C_1 has a high impedance at low frequencies. In this case, $A_1(\Delta s)/g_m$ in Eqn. 92 reduces to $r_\pi/(r_\pi + R_b)$ where $r_\pi = \beta/g_m$ is the small-signal base emitter resistance of the transistor. Therefore, in order to increase linearity, R_b should be kept small in order to increase second-order interaction [190]:

$$R_b \ll r_\pi = \frac{\beta}{g_m} \tag{93}$$

For a typical current of 5 mA and a current gain of $\beta = 180$ (worst case: $\beta = 100$), $r_\pi = 914\,\Omega$ (worst case: $r_\pi = 508\,\Omega$). The simulation in Fig. 83 shows a clear improvement

if the bias resistor is well below this value. On the other hand, reducing the bias resistor R_b considerably below r_π leads to a large increase in NF (verified experimentally in Fig. 73). Thus, in this simple design a compromise between NF and IP_3 is necessary.
In the same way Fong and Meyer calculated a Volterra series expansion for a degenerated differential pair [190] and came to the conclusion that

1. inductively degenerated differential pairs are more linear than resistively or capacitively degenerated differential pairs

2. the IM_3 products for the differential pair are at least twice as large as the IM_3 products of the single common-emitter stage for the same bias current and transconductance. Single-ended common-emitter stages are therefore more linear than differential-pair stages with the same bias current and transconductance.

3. there is no influence of low frequency base or emitter termination on IM_3.

Thus, a common-emitter transconductance stage can be biased at a lower current than a differential-pair transconductance stage with the same linearity and transconductance [190]. Therefore, in this thesis, no LNAs based on differential pairs have been realised. Similar Volterra analysis for bipolar transistors and HBTs can be found in [65, 61, 225].
As Fong's and Meyer's computations neglected the base-collector capacitance C_{bc} (which was not done in [61]), their results are even more valid for cascode configurations.
The effect of low-frequency termination on the intermodulation performance of a TX driver amp has been studied in [226]. Aparin and Persico in 1999 presented a bipolar LNA with exceptional high linearity [61]. Their analysis revealed that shorting the base at $\omega_1 - \omega_2$ improves IIP_3, but the optimum value for the termination impedance is $\neq 0$. Such optimum nonzero sub-harmonic termination fixes the amplitude and phase of the modulation signal appearing in the bias circuit so that the product of its mixing with the input signal cancels the remaining IM_3 terms [61]. In addition, out-of-band termination at $\omega_1 + \omega_2$ – in PAs used to optimise power-added-efficiency – can lead to complete cancellation of 2nd and 3rd order contributions leading to very high IM_3. As we will see in section 6.8.7, this is very tricky and works only for amplifiers which need to operate in a very narrow frequency band.
In 2002 van der Heijden, de Graaff and de Vreede reported a balanced LNA with an OIP_3 of 20 dBm with just 2mA of bias current [227]. Again this was achieved by controlling the 2nd harmonic at the output. The result was extremely sensitive to tone-spacing, however.
It is interesting to note that low-frequency termination and harmonic termination does not seem to have an effect on the intermodulation performance of MOS and HEMT devices: Simulation results using HEMTs showed constant IIP_3 for different bias terminations. This is obviously due to the missing cancellation between 2nd and 3rd order products.

6.8 LNA circuit implementations

6.8.1 Influence of bias resistor

As discussed in the previous section, a low impedance at the base terminal of the HBT terminates the beat frequency and improves IIP_3. Fig. 83 shows simulated linearity and noise figures for the 1.93 – 1.99 GHz CDMA IS-95 LNA (described in more detail in section 6.8.7 and in [9, 10]). Up to 3 dB of linearity can be traded against up to 3 dB of

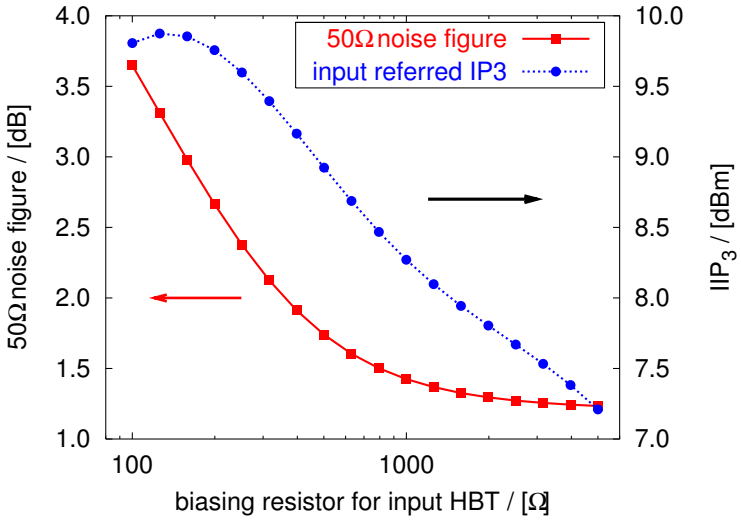


Figure 83: Tradeoff between IIP_3 and NF due to bias network impedance.

noise figure. In order to keep NF low, a value of 2 kΩ has been used in the LNAs of this thesis (except the 802.11a WLAN LNA which has lower linearity requirements and uses a value of 3 kΩ). Further methods like broadband source termination as described in the following section have been used to eliminate the remaining IM_3 degradation.

6.8.2 Broadband source termination

Eqn. 92 shows, that linearity of bipolar transistors is improved by inductive series degeneration and low $Z_b(\Delta s)$, e.g. a short circuit for low frequencies at the base. While simply reducing the bias resistor as shown in Fig. 83 increases NF, for systems with large 2-tone spacing (e.g. 900 kHz for IS-95, see section 3.1.1) the bias resistor can be shorted by the source resistor (usually 50 Ω) via a large input coupling capacitor. This is experimentally shown in Fig. 84.

Measuring 2-tone IP_3 at bipolar circuits, it turned out that different IM_3 products may occur at frequencies of $2 \cdot \omega_a - \omega_b$ and $2 \cdot \omega_b - \omega_a$, an effect called *$IM_3$-asymmetry* [61]. IM_3-asymmetry is undesirable, as it leads to two different values for IIP_3 when Eqn. 12

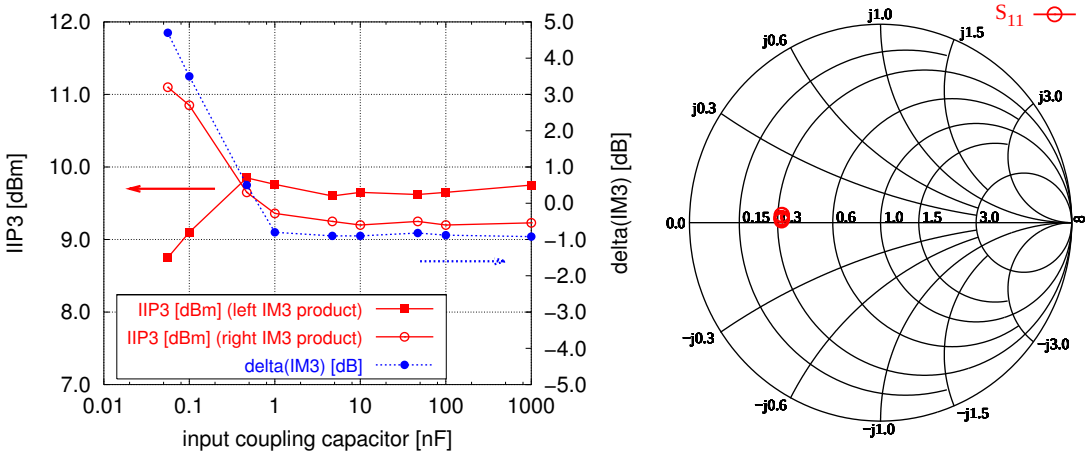


Figure 84: Using large SMD coupling capacitors at the LNA input port leads to symmetrical IM_3 products (left). Up to $1\,\mu$F may be used for the 1.95 GHz IS-95 LNA without leading to resonances in terms of S_{11} deviations at 1.95 GHz (right). Gain remains at $14.28 \pm 0.04\,dB$ and NF at $1.48 \pm 0.02\,dB$dB for all configurations.

is used. While some authors take the average of these two values, the correct way is to quote the lower of the two values. Therefore its mandatory to get equal IM_3 products as shown in Fig. 12. We have seen experimentally that IM_3-asymmetry is especially pronounced for LNAs with an input coupling capacitor which is low impedance at RF but high impedance at the beat frequency (see Fig. 84). Using a larger blocking capacitor makes the IM_3 products more equal by terminating the beat frequency with the 50 Ω impedance of the source. This method, however, is only effective, if the preceding stage (e.g. the RX filter) shows a low impedance at low frequency (e.g. 50 Ω). As can bee seen in Fig. 86 this is not always the case. An additional problem is that a large blocking capacitor C_{block} leads to large transient turn-on times, as the capacitor needs to be charged by the bias resistor R_{bias} (Fig. 72) from "0" to "$1 \times V_{BE}$". This time constant of $C_{block} \cdot R_{bias}$ may lead to problems in TDMA systems, as 100 nF and 2 kΩ amounts to 200 μs, which is nearly half of a GSM slot. Therefore this method is unsuited for TDMA systems with low tone-spacing like TETRA (table 3). In this thesis, broadband source termination is used especially for the IS-95 and the GPS LNA (see section 6.8.7 and 6.8.8), as no TDMA is used is these systems.

6.8.3 Low frequency termination using LC trap networks

A low-frequency trap network at the input of an amplifier can substantially improve the intermodulation performance of an amplifier [228]. A series LC-network is shunted from the input of the common-emitter stage to ground and the dimensions are such,

- that the inductor L_t is close to parallel resonance at the RF frequency in order avoid parasitic loading at the LNA input
- and the LC combination L_t, C_t is in series resonance at the beat frequency, providing a short to the LNA input, independent of the impedance of the preceding RX filter at this critical frequency.

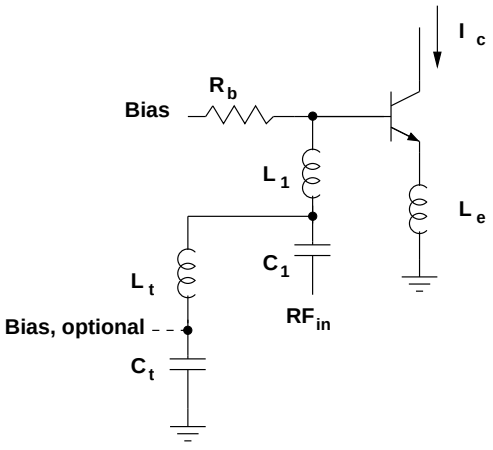


Figure 85: Inductively degenerated common-emitter transconductance stage with low-frequency trap network L_t, C_t [228].

For typical RF and beat frequencies, this results in component values in the range of several 10 nH for L_t and several nF for C_t, which precludes the use of integrated passive components. Even if the inductor could be integrated, the low quality factor of integrated inductors on lossy silicon (see chapter 5) would drastically degrade the noise figure of the LNA. Instead of being close to resonance at the RF frequency, the inductor could also be part of the input matching network if necessary [229]. As explained in the previous section, start-up behaviour due to the $R_b \cdot C_t$ time constant can be a problem when used in TMDA systems [58]. Using a low-frequency trap at the input of their discrete Si-bipolar LNAs, Fong and Szmyd of Philips achieved an impressive IIP_3 of 5 dBm and 9 dBm with currents of 4 mA and 6 mA, gains of 16.7 dB and 14 dB and noise figures of 1.0 dB and 1.1 dB, respectively, all at 2 GHz and a tone-spacing of 1 MHz [229]. The resulting OIP_3 values of 22 - 23 dBm are well above Lucek's rule of thumb in Fig. 78. Yogi and Petersen [170] got a 2.5 dB improvement in IIP_3 by optimising the LF trap at the input of their 800 MHz LNA. Using a discrete BFP620 SiGe HBT with $f_{max} = 70$ GHz and 12 SMD components, Wevers [220] of Infineon achieved an IIP_3 of +10 dBm with 14.7 dB of gain resulting in an OIP_3 of +25 dBm at 8.9 mA and 2.1 V of DC bias (the $BV_{CE,0}$ of this SiGe HBT was just 2.3 V)[28]. Wevers claims that his LF trap increases IP_3 by 5-10 dB,

[28]Reaching the +10 dBm of IIP_3 without LF trap would require a bias current of 15 mA @ 3 V using a BFP450 Si bipolar transistor [214].

while 4 dB seems to be more reasonable when comparing with Fig. 78. Note that shorting the $(f_2 - f_1)$ product as done by the LC trap does not increase the compression level of the amplifier, just IP_3. Using this technique, the general rule of thumb, stating that IIP_3 is 10 dB above P_{1dB} is no longer valid. Wevers claims to get a difference of 17.9 dB here. In summary, the disadvantage of this technique is the increase of the bill of materials due to the two additional SMD components, delays during start-up in TDMA systems [170] and its limitations to test cases where a high IP_3 is needed only at a single tone-spacing (like CDMA-IS95), although a flat IIP_3 over 1.5 decades of tone spacing can be achieved (Fig. 5 in [220]). However, the drop in IIP_3 when the tone spacing approaches "0" is pronounced, making this technique unsuited for PMR systems with low channel spacing (see table 3).

6.8.4 Low frequency termination using bias inductors and a diode

The modification of the low frequency trap, as applied in this thesis, is the inductive bias network shown in Fig. 72, right [58]: The inductor is operated close to parallel resonance at RF frequencies in order to avoid loading and noise figure degradation of the RF stage. Properly designed, the influence of the bias network on the noise figure can be eliminated completely, leading to noise figures lower than what can be achieved using practical values of bias resistors (see Fig. 73, where the very large inductor of a bias-T was used for biasing). For low frequencies, the base of the RF transistor is terminated by the dynamic resistance of the biasing diode, which is $r_e = \delta V/\delta I = V_{th}/I_{diode}$. Using an RF current of 6 mA and a mirror ratio of 1:6 ... 1:12, the current in the diode is 1.0 ... 0.5 mA resulting in an impedance of 25 ... 50 Ω which is sufficiently low to terminate the base properly (see Eqn. 93). This technique, previously known from the design of TX driver amplifiers and power amplifiers [226][29]

- provides a broad-band low frequency termination independent of the RX filter impedance at low frequency and is therefore suited for all kind of systems that require high IP_3 values within a wide range of tone spacings (e.g. UMTS)
- uses only one external SMD inductor
- due to the absence of large sized SMD capacitors is not prone to delays during start-up
- and yields excellent noise figures as it avoids resistive loading of the input resistor.

For infrastructure parts, the added cost of an external SMD inductor for biasing is not critical and therefore this technique was used within the SCUBA project, where an RX filter with high impedance at low frequencies (Fig. 86) precedes the LNA.

[29] While this technique belongs to textbook know-how, Agilent Technologies filed a patent application in 2002 for the implementation with enhancement mode FETs [230].

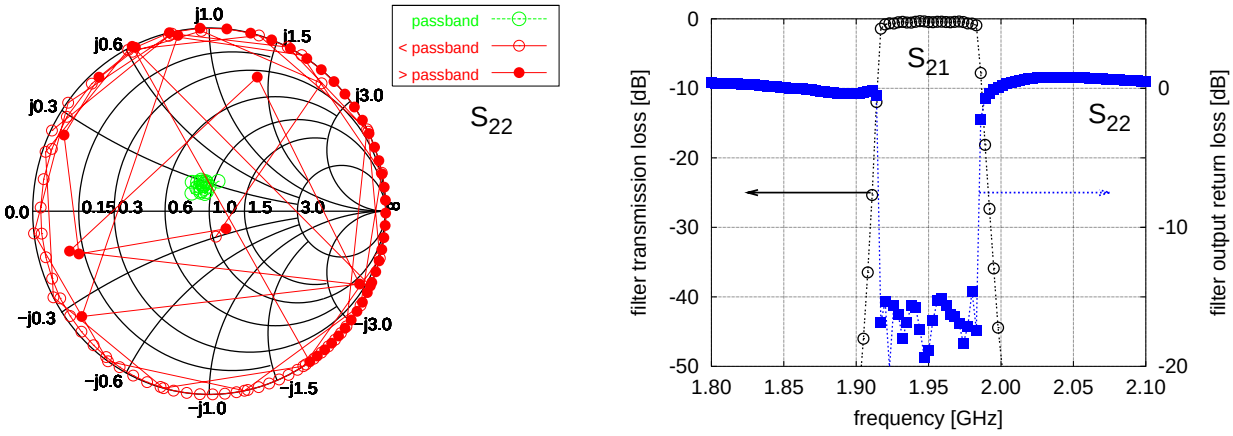


Figure 86: The UMTS base station RX filter presents 50 Ω to the LNA in the 1920-1980 MHz passband (green), but is far from 50 Ω in the stop band (red).

SCUBA LNA	50 Ω noise figure	gain (S_{21})	reverse isolation	linearity (OIP_3)	supply voltage	supply current
specification	$\leq$ 1.5 dB	$>$ 17 dB	$>$ 40 dB	$>$ 10 dBm	5 V	–
realised	1.15 dB	19 dB	45 dB	18 dBm	5 V	6.6 mA

Table 17: Compliance matrix for the UMTS LNA

Using this technique, the SCUBA LNA was designed for a base station that uses a direct conversion receiver to downconvert 4 WCDMA channels simultaneously (see chapter 2.2.4), in between an RF filter and the downconverter IC. The key specifications as well as the realised performance are shown in table 17. A high reverse isolation along with a very low noise figure was required. The high reverse isolation is necessary as the tolerated radiation of the LO signal which leaks from the mixer through the LNA to the RX antenna is just -90 dBm. In the first design iteration, the LNA was integrated onto the receiver IC which contains a 4 GHz VCO with quadrature generation (divide-by-2), IQ demodulators and base band filters [15]. This LNA, however, did not achieve the required reverse isolation and the LO signals from the divider were picked up by the on-chip inductor of the LNA's matching network, which led to DC offsets in the direct-conversion receiver. Therefore the LNA had to be realized in a separate package (Fig. 6) [16]. By omitting parallel capacitive feedback from the output to the input – which was used in the optimisation of the LNA core in section 6.8.7 – plus a dedicated grounding scheme, the target value of $|S_{12}|$ = -40 dB was exceeded by 5 dB (see Fig. 88).
A noise figure of 1.15 dB @ 2 GHz[30] – the lowest noise figure for all SiGe1-LNAs developed within this thesis – has been achieved using inductive biasing with a high-Q SMD induc-

[30]See Fig. 137 in appendix A, which explains the setup used to measure these low NF values reproducibly.

tor plus a layout optimisation of the 6-finger device shown in Fig. 17, where the seven base contacts had been contacted with additional contacts in metal M2 to reduce series resistance. This gave a 0.33 dB NF improvement compared to the 1.48 dB of the IS-95 LNA which uses the same 6-finger cascode LNA core but without layout optimisation and the traditional bias scheme shown in Fig. 72 (R=2 kΩ). The 0.3 dB improvement was already evident when optimising the cascode LNA core via on-wafer measurements (see Fig. 73). The resulting schematic is shown in Fig. 87 with full schematics in Figs. 146 and 147 of appendix E.

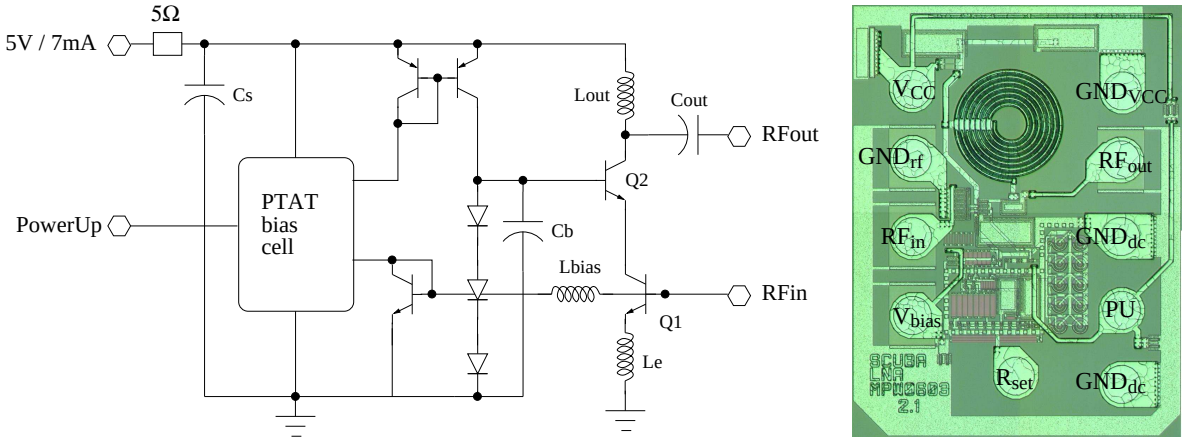


Figure 87: Schematic (left) and chip photo (right) of the 1.95 GHz UMTS LNA with inductive biasing for lowest noise figure and proper low frequency termination. To achieve a high reverse isolation, no linearization by parallel feedback was applied. The PTAT bias cell corresponds to Fig. 74 (left). Geometry of L_{out}: 7.25 turns, 8 μm wide, with 3 μm spacing and 32 μm inner diameter (nominal 7.4 nH).

A CMOS-compatible power-up pin and bias-current setting via an external SMD resistor to GND required a relatively large TSSOP8-package with exposed pad in order to provide the required pin count. The advantage of this package was a low-inductive GND_{dc} to the pad for the common-base HBT, which allowed for 45 dB of reverse isolation: Simulation showed that a value of ≤ 0.5 nH was mandatory to achieve the required 40 dB of reverse isolation. This was achieved by two downbonds to the exposed pad. As a bond array of two parallel down bonds spaced apart by 150 μm cuts down the inductance just by 37% compared to a single groundbond [231] (and not by 50% as expected), the LNA power-up pin has been routed in between the two ground bonds (see Fig. 87, right). This grounding scheme together with 5 thru-holes to the PCB ground of a 0.5 mm thick, low-loss RO4003 substrate allowed for even 45 dB of reverse isolation, corresponding to a total inductance value from die (GND_{dc}) to paddle of just 0.2 nH. The large package lead inductances of 1-1.5 nH could easily be incorporated into the design, as – with a short, inductive stripline on the RO4003 PCB – they provided just the right amount of emitter series feedback L_e for Q_1 according to Fig. 67 without the need for of a lossy

integrated inductor, thus optimising NF. At the input, the pin inductance plus a 2.2 nH SMD inductor provided simultaneous noise and power match as shown in Fig. 68. On the supply line, however, the combined inductance of pin, bond, and PCB would detune the output match of the LNA. Therefore the supply line was de-coupled on-chip via a 5 Ω resistor and a 10 pF MIM capacitor (C_s in Fig. 87) to the pad ground via a separate ground pin GND_{VCC}. The separate pin avoided feedback from the die ground GND_{dc} via the supply line and improved reverse isolation. Just on the output pin, the pin inductance was detrimental and had to be resonated by choosing a lower value for the output inductance C_{out}, which decreased the bandwidth of the output match (S_{22}). The external SMD inductor L_{bias} is connected between pads V_{bias} and RF_{in} and provides the low-frequency termination. Measured and simulated S-parameters are shown in Fig. 88

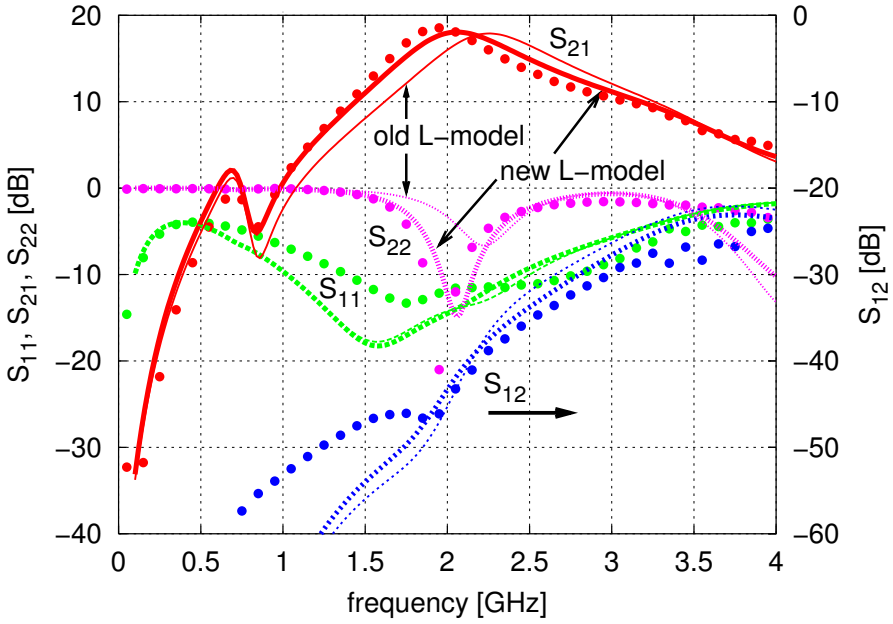


Figure 88: Measured and simulated S-parameters for the SCUBA-LNA with output match corrected by a 2.0 pF SMD capacitor. Dots are measured data, the thin lines show the simulations using the inductor model of the Atmel design kit, and the bold lines use the improved inductor model of chapter 5. While S_{11} and S_{12} are not affected, the improvement in S_{21} and S_{22} is significant.

with the reference plane moved to the package pins by using proper port extensions in the Vector Network Analyser (VNA)[31]. The following problem became evident: The inductor model of Atmels SiGe1 design kit simulated inductance values which were 30% too large, when configuration M23 was used for the output inductor. The 50 Ω output match was therefore shifted to 1.8 GHz. In order to move it to a center frequency of 1.95 GHz,

[31]This method [170] assumes that the SMA connectors and the microstrip lines on the PCB are 50 Ω with ideal transitions. No losses due to mismatch and dielectric losses are taken into account.

V2.1 w/o ESD	Measurement	ADS simulation
$I_{CC}@V_{CC} = 5.0\,V$	6.75 mA	5.95 mA (incl. bandgap)
NF_{min}	$\approx$ 0.9 dB	1.18 dB
$NF_{50,\Omega}$	1.15 dB	1.52 dB
R_n	8.5 Ω	11.5 Ω
Γ_{opt}	0.40 $\angle$-77°	0.40 $\angle$-65°

Table 18: Simulated and measured noise parameters of the SCUBA LNA. Lower NF and R_n is due to a higher current gain and lower base resistance compared to the design kit

an external SMD capacitor of 2 pF was necessary in series to the integrated 0.55 pF MIM, leading to an effective value for the output capacitor of 0.43 pF. Improved inductor models were developed as described in section 5. Resimulating the circuit using this improved model, together with the 2 pF SMD capacitor, shows superior agreement with the measurement. The remaining differences are due to an insufficient package equivalent circuit. The notch in the transfer characteristics at 800 MHz is due to a resonance in the supply line between the integrated 10 pF blocking capacitors, the bondwire and package inductance and the 100 pF SMD capacitor on the PCB. It would be even more severe if not damped by the 5 Ω resistor in the supply line (see Fig, 87, left). Using a larger value, e.g. 12 Ω in the case of the WLAN LNAs (Fig. 150), the notch is hardly visible. As explained in [192], care needs to be taken when applying on-chip decoupling to complicated transceiver designs, as – at frequencies close to resonance – isolation between adjacent blocks is reduced. The simulated and measured noise parameters are compared in table 18. Integrating the input blocking capacitor on-chip would increase the excellent NF of 1.15 dB by 0.5 dB.

OIP_3 has been evaluated for 2 boards with different emitter series feedback inductance and a supply voltage of 3 and 5 V. As the common-base device is biased at a base voltage of $3 \times V_{BE}$, at a supply voltage of 3 V the LNA is limited in output swing and the linearity is considerably lower compared to 5 V. The bias inductor terminates the beat frequency down to "0" frequency. Therefore OIP_3 versus tone spacing in Fig. 89 is extremely flat down to very low tone spacings in the two-tone linearity measurement. Due to the low-impedance termination at low frequencies, the difference between the two side-bands (USB, LSB) is low. The dip in OIP_3 around 10 MHz is due to a parallel resonance of the 47 nH bias inductor with the 10 nF blocking capacitor towards the 50 Ω source, which forms a high impedance to the beat frequency. In Fig. 90 the current of the UMTS LNA has been swept by decreasing the value of the SMD resistor that sets the bandgap current. While the optimum NF for the used transistor size is reached at low currents, gain improves with current due to $g_m = I_C/V_{th}$. OIP_3 dips at 12 mA, as above that frequency the maximum current of the 2-finger cascode HBT is exceeded.

In Fig. 91 inductive and resistive biasing is compared experimentally (I_{CC} = 6.6 mA, f = 1950 MHz, tone spacing = 5 MHz). Optimum performance is achieved with a bias

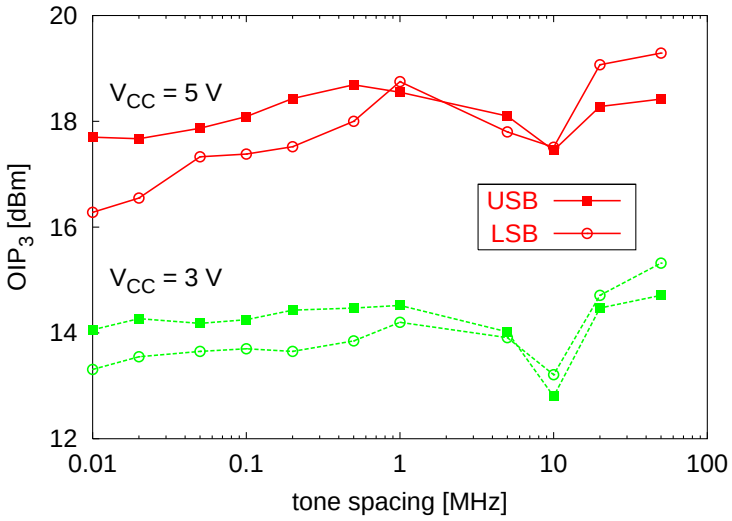


Figure 89: OIP_3 versus tone spacing at 1.95 GHz for the version with lower series feedback inductance (S_{21}=19.4 dB).

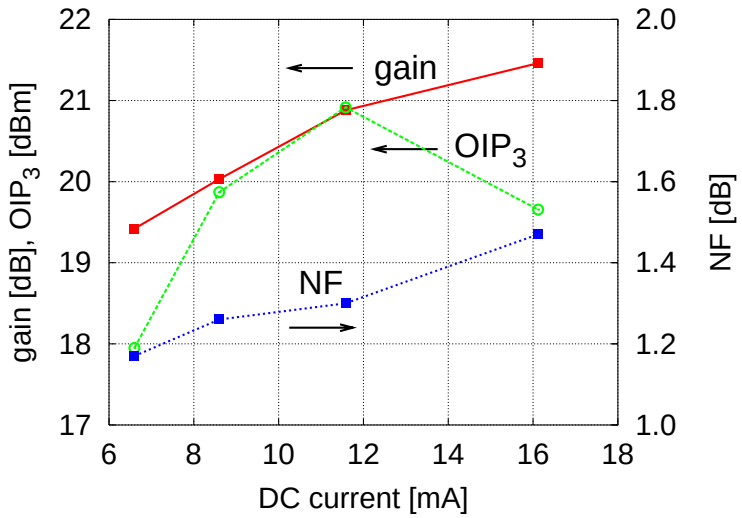


Figure 90: Gain, NF and OIP_3 versus current at 5 V supply voltage (1950 MHz, 5 MHz tone spacing). Linearity reaches an optimum at 12 mA, while the optimum current for minimum NF is below 6 mA.

inductance of 47 nH. Smaller values degrade both NF and gain. Resistive biasing should show a strong dependence of OIP_3 with resistance value (compare to Fig. 83). However, as the input DC blocking capacitor is 10 nF ($Z = -i \cdot 3.2\,\Omega$ at 5 MHz), the input in this measurement is terminated already by the 50 Ω impedance of the source.

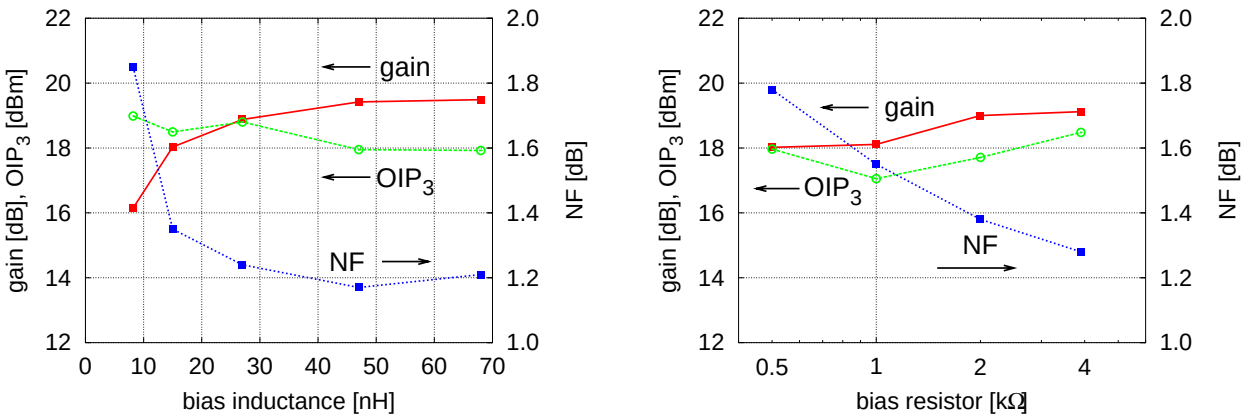


Figure 91: Gain, NF and OIP_3 versus bias inductance (left) and versus bias resistance (right) at 1.95 GHz. The improvement in NF of inductive biasing with 47 nH versus resistive biasing with 2 kΩ is 0.2 dB.

Type	SCUBA	MGA-725MA	HMC375LP3
Manufacturer	Atmel	Agilent	Hittite
Technology	SiGe1	GaAs pHEMT	GaAs pHEMT
Bias	6.75 mA @ 5 V	20 mA @ 3V	136 mA @ 5 V
$NF_{50,\Omega}$	1.15 dB	1.5 dB	0.9 dB
Gain	19 dB	15.6 dB	17 dB
IIP_3	0 dBm	10.5 dBm	17 dBm
OIP_3	19 dBm	25.6 dBm	33.5 dBm

Table 19: Different infrastructure LNAs at 2 GHz [213, 232].

The performance of the SiGe UMTS LNA is compared to pHEMT LNAs with considerable higher power consumption in table 19: The SiGe-LNA has the highest gain and its NF is in between the Agilent and the Hittite part. The Agilent LNA has better OIP_3 due to a DC power consumption which is twice compared to the SiGe LNA. Note that its OIP_3 of +20 dBm at 20 mA and 3 V is exactly as predicted by Eqn. 86 (see Fig. 78). The excellent OIP_3 of the Hittite LNA comes at the expense of an excessive DC power consumption of 680 mW.
Despite the trend towards higher integration, inductive biasing is widely used and by 2009 Infineon switched 2 of the 3 GPS LNAs available on their website to this technique [233, 234, 235, 236, 237] (see table 27). Doing this, their linearity reaches Damen and Lucek's rule of thumb shown in Fig. 78.

6.8.5 Low frequency termination using active bias networks

Low frequency termination without the need to spend an additional package pin and an additional SMD inductor can be achieved by an active bias network. These bias networks are typically based on operational amplifiers (OPAs) and compare the bias current of the RF stage to a reference current: At low frequencies, if the bias current is too large compared to the reference, the base voltage is *de*creased immediately. If the bias current is too low compared to the reference, the base voltage is *in*creased immediately. This is equivalent to a voltage source at the base with a low impedance, determined by the gain of the OPA loop. At RF, the loop gain needs to vanish, as otherwise there would be no RF gain. An active bias network, published [192] and patented [238] by Jeff Durec of Motorola is shown in Fig. 92. The key to this circuit is the generation of the temperature-

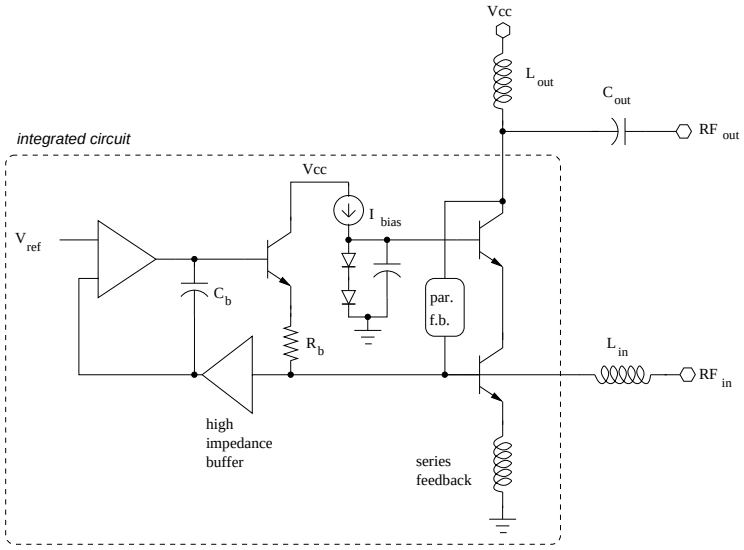


Figure 92: LNA with active bias network for low-frequency termination as proposed by Durec [192, 193, 238].

compensated reference voltage V_{ref} and the high impedance buffer in a very simple yet efficient manner. The impedance at low frequencies is basically given by R_b divided by the loop gain. At RF, due to C_b, the OPA is shorted and the impedance is nearly as high as R_b. Without degrading linearity, R_b can now be very high (e.g. 4 kΩ) resulting in excellent NF properties (see Figs. 73 and 91, right). When testing Durec's circuit of Fig. 92 for the IS-95 LNA, it turned out that the bandwidth of the original active bias circuit was too low for the IS-95 test case (900 kHz tone spacing). A modified version with a lower OPA output impedance resulted in a higher bandwidth, but – due to the high gain involved at low frequencies – had problems with stability at low frequencies and transient overshoots when turning the LNA on (see Fig. 93). While I found a simple fix to remove the current overshoot when turning the LNA off, I was not able to remove the

current spike at turn-on. Finally, also due to patent considerations, we used the more traditional biasing of Fig. 72 for the IS-95 LNA.

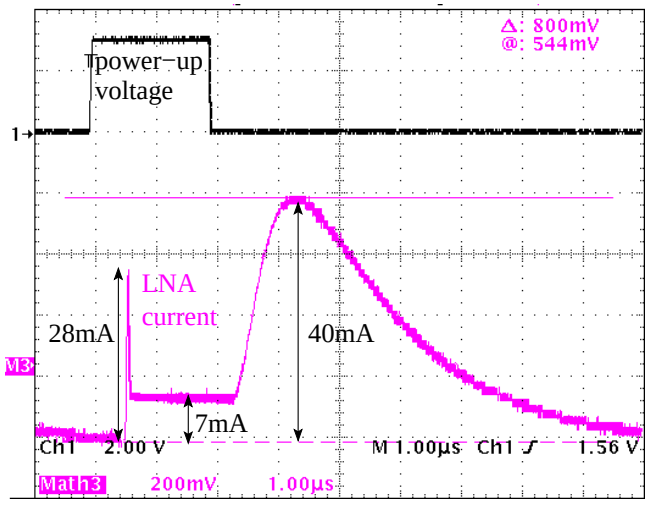


Figure 93: Active, OP-based bias networks may show heavy overshoot when turned ON and OFF (measured on a modified circuit of Fig. 92).

Due to the limited bandwidth of these bias loops we thought that it might especially be suited to provide low-frequency termination to LNAs in narrow band systems like TETRA and TETRAPOL [239] (see table 3). In contrast to broadband source termination using large blocking capacitors in the RF input (section 6.8.2), active bias networks provide a low impedance to the input transistor, independent of RX filter impedance at low frequency. Inherent to both standards is a low channel spacing of 25 kHz. This requires both LNA and mixer to be robust against two-tone intermodulation due to co-location interference in rugged environments, as interferers appear in the receive band and cannot be reduced in amplitude by a SAW filter between LNA and mixer. In order not to degrade the system linearity, the IIP_3 of the mixer needs to be higher than the IIP_3 of the LNA by the amount of the LNA gain. Therefore, rather than using a mixer of the Gilbert-type that can easily be implemented in bipolar technology [240, 241], a passive mixer known for its high IIP_3 values was used (see section 7.5.2).

System analysis requires the TETRA/TETRAPOL LNA to have an IIP_3 of +5 dBm with a gain of 17 dB and sub 2 dB NF while drawing just 6 mA from a 2.7–3.3 V supply. Again, with the low amount of current given, only a single-stage design can meet the requirements, as distributing the current on 2 stages would inevitably lead to clipping in the 2nd stage, generating excessive intermodulation (see section 6.3). A single broadband design that covers all PMR bands or at least all of the three 400 MHz bands would have been highly desirable. Extensive simulations in section 6.2.1 have shown, however, that standard broadband designs using resistive parallel feedback cannot meet the noise figure and gain requirements and that the low supply voltage precludes the use of resistive

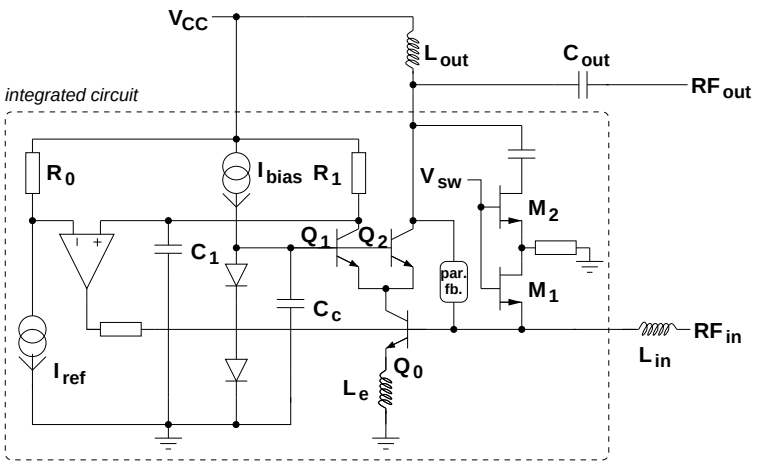


Figure 94: Switched gain LNA with active bias network for low-frequency termination as proposed in this work and used in the 400 MHz and 800 MHz PMR LNA [239].

loads. A 1-stage design with reactive LC output matching network was finally chosen, which allows to customise the 400 MHz version to the 3 different bands (380-430 MHz, 440-490 MHz and 470-520 MHz) by changing two external SMD components. A cascode structure was used to eliminate feedback due to the non-linear base-collector capacitance of the large multi-finger input device (24 fingers, 15μm each, for the 400 MHz version and 16 fingers for the 800 MHz version, respectively). Due to the high available gain at these low frequencies, extensive use of parallel RC and inductive series feedback was applied to increase linearity, limit the gain to 17 dB and limit the output impedance, as a lower transformation ratio of the LC-match increases its bandwidth. Emitter degeneration inductors were integrated on-chip to improve reproducibility. Two additional techniques were used to increase linearity:

- As IP_3 depends mainly on current (Fig. 78), a low-current bias network allows to put a large portion of the total current into the RF cascode.
- When not shorted properly, the beat frequency $f_1 - f_2$ in the two-tone intermodulation test modulates the bias point, leading to additional intermodulation products which – depending on the phase – magnify or cancel the 3rd order distortion products (section 6.7.1). To prevent this, the beat frequency, which is 50 kHz in the TETRA test case, needs to be terminated at the input with a low impedance[32].

The active bias network shown in Fig. 94 satisfies both requirements: The common-base device is split into two transistors Q_1, Q_2 with an emitter area ratio of 1:8. While the signal of Q_2 is matched to 50 Ω by L_{out} and C_{out}, the current of Q_1 drops across $R_1 = 1$ kΩ. The

[32]Note that broadband source termination using a huge input blocking capacitor is impossible in this application, as the maximum LNA start-up time is specified to be less than 1 μs, which in turn is dictated by the instant availability of a connection in PMR systems.

resulting voltage – after lowpass filtering by R_1, C_1 – is compared to a reference current I_{ref} which drops across $R_0 = 5 \cdot R_1$ and an operational amplifier (OPA) regulates the base emitter voltage of Q_0 accordingly. This loop is active from DC to $1/(2 \cdot \pi \cdot R_1 \cdot C_1) = 16$ MHz and within this regulation bandwidth provides a low impedance to the input. High loop gain leads to low Z_{in}, but care needs to be taken to maintain stability during startup. We have found, however, that this architecture leads to lower transient overshoots than Durec's circuit shown in Fig. 92. Note that I_{ref} is just $1/(5 \cdot 9)$ of the current in the RF cascode and neglecting the current of the OPA and I_{bias}, the majority of the current flows through Q_0. The translinear cross-quad used to generate I_{ref} proportional-to-absolute-temperature (see Fig. 76, right) is known for its little overhead biasing and excellent transient settling behaviour without any ringing [208].

In the presence of a strong input signal, the LNA needs a gain step to switch the gain from +17 dB to -20 dB in order not to overload the mixer. As it is desirable to save current, it was specified that the LNA current consumption is zero in the -20 dB state, which is identical with a complete shut-down of this block. The straightforward solution is the use of a bypass switch using MOS transistors (see Fig. 94) and this requires a BiCMOS technology such as Atmel's at46k (see section 4.4). In power-down, transistors M_1 and M_2 are turned on and form a T-attenuator. The LNA then acts as a 20 dB attenuator with nearly perfect input and output match[33].

Fig. 95 shows the S-parameters of the 400 MHz LNA, matched to 380-430 MHz, and the

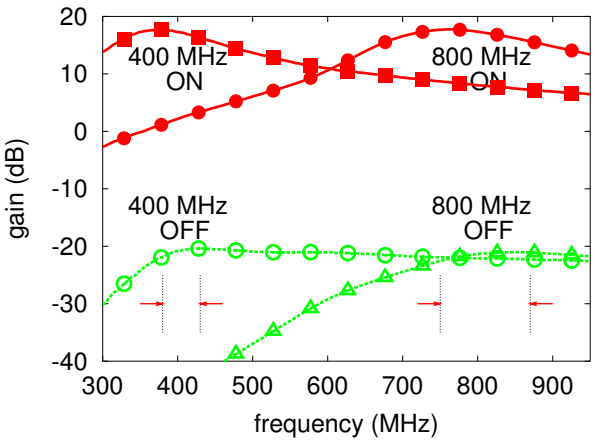


Figure 95: Gain of the LNAs in ON and OFF mode. Band edges are indicated by arrows [114].

800 MHz LNA. In OFF mode, the LNAs act like a 20 dB pad. Note the excellent return

[33] Techniques do exist to realize gain steps in a pure bipolar process, but they either consume a certain amount of DC current in low gain mode and/or use a reverse biased BC junction of a BJT [93, 242] and therefore require the supply voltage of the LNA to be switched to zero, which is an highly undesired feature as it requires a switch on the PCB to divert the LNA supply voltage from the battery to ground in low gain mode.

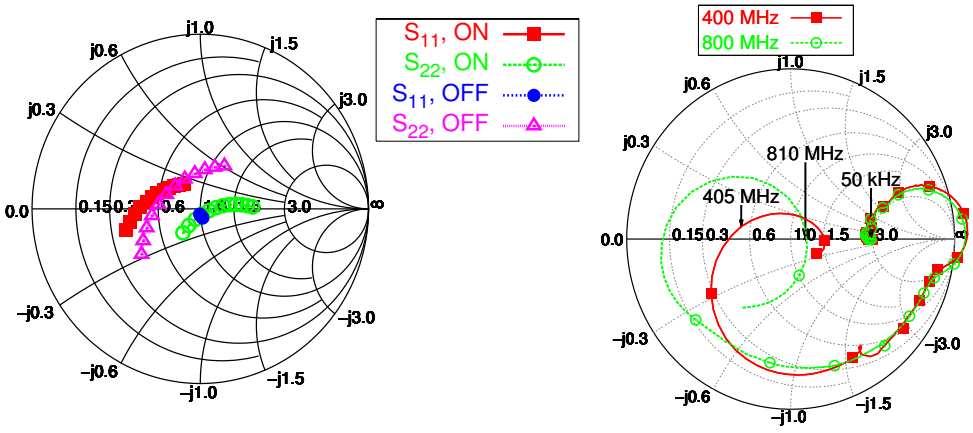


Figure 96: Left: Return loss of the 400 MHz LNA in the 380...430 MHz band (ON and OFF). Right: Using the active bias circuit of Fig. 94, low frequencies are terminated with an impedance of 150 Ω, while at RF the input impedance is close to 50 Ω. Note the problems due to instabilities at around 30 MHz.

loss in ON and OFF mode, which is shown for the 400 MHz version in Fig. 96. Reverse isolation is approximately 21 dB in all cases, which is acceptable for a super-heterodyne receiver, but – as already discussed in section 6.2.1 – implies a possible risk for oscillations. Noise figure in ON mode was measured to be 1.5 dB for the 400 MHz version and 1.8 dB for the 800 MHz version (best case values with a large spread between lots) while it is 20 dB in OFF mode for both LNAs. IIP_3 was measured to be +4 dBm at 6 mA/2.7 V with a tone spacing of 50 kHz (ON mode). Higher values can be achieved by setting the current to a higher value by means of an external SMD resistor.

6.8.6 CMOS LNA implementations

Initially it was planned to realise the TETRA/TETRAPOL front-end in a SiGe bipolar technology using the available Schottky diodes to construct a ring mixer. Due to the disappointing measurement results of this mixer (see section 7.5.1), a FET mixer was realized (see section 7.5.2), using a SiGe BiCMOS technology (at46k). The 0.35 μm CMOS part not only allowed to build a highly linear mixer, but also simplified the design of the gain switch of the LNA. As can bee seen in table 8, the minimum noise figure of layout-optimised 0.35 μm NMOS transistors in the at46k SiGe BiCMOS process is in the order of 1.1 dB at 2 GHz. Therefore test LNA circuits have been designed for TETRA using MOS technology on the at46k evaluation runs, to check if the complete front-end could be realised in a pure CMOS technology. As shown in Fig. 97, the LNA is basically a large, layout-optimised NMOS transistor with 80 fingers, each 0.35 μm × 20 μm wide (resulting in a total gate width of 1.6mm), minimised drain-source and drain-gate overlap capacitance and the gate fingers contacted at both ends. Due to the high drain-gate capacitance of such a device, a SiGe HBT was cascoded in order to avoid the Miller

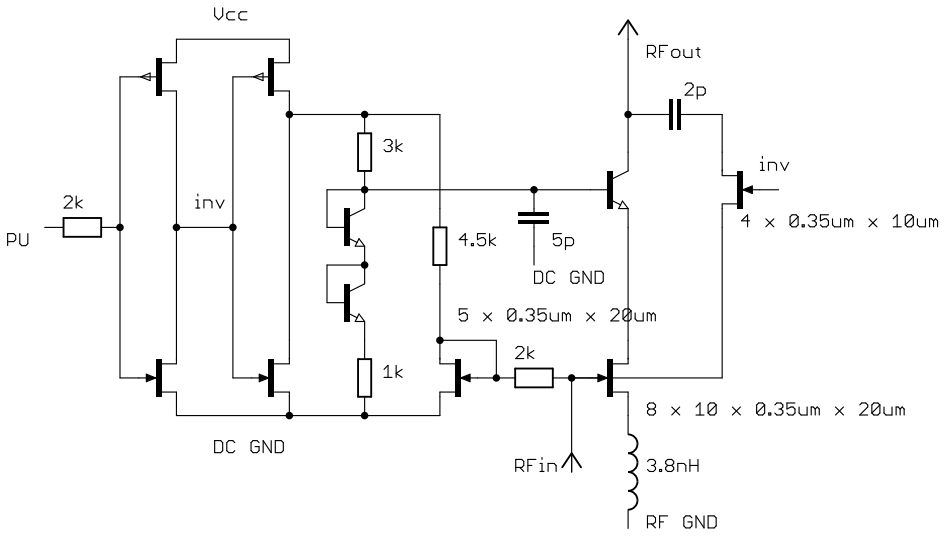


Figure 97: Schematic of the NMOS LNA with bipolar cascode and NMOS gain switch. The output match is realized using SMD components on the PCB (see table 20).

effect. Biasing was done via a current mirror topology, similar to Fig. 72, left. Source series feedback was a large 3.8nH inductor (4.25 turns, 15 μm wide with 3 μm spacing and 260 μm of outer diameter), in order to bring the low real part values of the input inductance to values between 30...50 Ω. In section 6.3 it has been shown that – regarding noise matching – the CMOS cascode behaves similar to the bipolar cascode, except that the input inductors are much larger compared to its bipolar counterparts: While we used 6.8 nH (12 nH) for the 800 MHz (400 MHz) bipolar LNAs, we had to change this to 15-18 nH (27nH) for the 800 MHz (400 MHz) NMOS LNAs. The 20 dB attenuator was realized by a simple NMOS bypass switch. Despite the high source degeneration, the gain of the NMOS LNAs with low-loss LC output matching networks was very high ($>$ 25 dB) and had to be decreased in order to achieve a high input-referred IP_3 and a stable operation without oscillations. In bipolar LNA implementations it is possible to use parallel, capacitive feedback (see section 6.6) for low-noise linearization. For the NMOS LNA, however, a feedback capacitor led to severe instability. The small signal performance of the realized NMOS LNAs is compared to their SiGe bipolar counterparts in table 20. When properly matched, the noise figure of NMOS LNAs is absolutely comparable to bipolar LNAs. However, it appeared that they are much more sensitive to mismatch and have lower linearity ($P_{1dB,input} \approx -10 \ldots -15$ dB). This is due to the lower gain, which allows for less feedback to be applied to reach the same amount of gain compared to a bipolar LNA.

Technology	NMOS	NMOS	SiGe	SiGe
Type	low-Q match (1 kΩ // 220 nH)	2 kΩ parallel feedback	150 fF parallel feedback	300 fF parallel feedback
Frequency	800 MHz	400 MHz	800 MHz	400 MHz
NFmin	1.23 dB	–	1.32 dB (1.5 with ESD)	–
NF	1.3 dB	1.65 dB	1.86 dB (1.9 with ESD)	1.50 dB
R_n	9.2 Ω	12.2 Ω	9.6 Ω (9.7 Ω with ESD)	10.9 Ω
G_{opt}	0.17 ∠ 62°	0.4 ∠ 174°	0.53 ∠ 98°	0.29 ∠ 78°
G_{ass}	16.1 dB	16.2 dB	16.2 dB	16.6 dB

Table 20: The realized TETRA/TETRAPOL LNAs at 3 V / 6 mA.

6.8.7 Cancellation by capacitive feedback in narrow band amplifiers

At its input, the LNA is tuned for minimum noise figure while preserving sufficient input return loss. Techniques to obtain simultaneous noise and power match have been described in detail in section 6.3. The output is usually conjugately matched with S_{22}^* using LC components to obtain optimum gain, sometimes with a small collector resistor to improve stability. With raising IP_3 requirements, however, gain is often traded for linearity [171, 243]: Linearity matching is widely known among high-power amplifier designers, where the load impedance is tuned for either optimum DC-to-RF efficiency or optimum linearity [244]. However, it is quite unknown so far to small-signal designers. Load-pulling can be used to plot contours of constant gain and linearity in the Smith chart. If very accurate large signal models are available (e.g. MEXTRAM [245]), load-pulling can be done by non-linear simulation (e.g. harmonic balance). Experimental load tuning can be done by either using a tuner setup as depicted in Fig. 98 or by sweeping the values of the LC output matching network on the PCB as it was done in Fig. 100. Load-tuning is

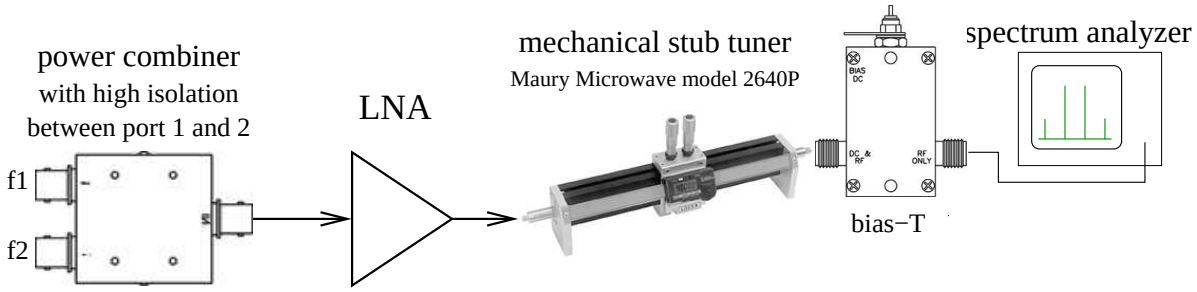


Figure 98: Measurement setup to determine the optimum output load for (a) highest gain and (b) optimum linearity.

especially effective for LNAs using a strong feedback from the output to the input, where 3rd order intermodulation products can be compensated by 2nd order products [171] by tuning the output match (Fig. 100). This was described in detail in section 6.7.

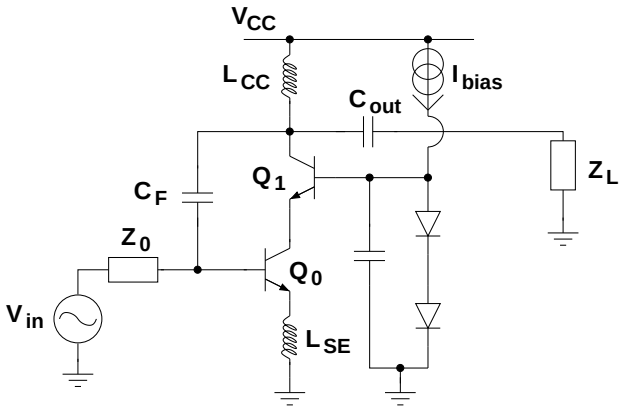


Figure 99: LNA with capacitive feedback according to [246].

f	C_F	L_{SE}	L_{CC}	C_{out}	R_L	Z_0	dB(S_{21})
1.95 GHz	200 fF	1.5 nH	7 nH	1 pF	163 Ω	50 Ω	13.57 dB

Table 21: Optimised design parameters for a 2 GHz LNA according to Fig. 99. Eqn. 94 gives an accurate expression for the gain of this LNA (compare Fig. 100, centre). R_L is the equivalent load impedance of L_{CC}, C_{out} and Z_0.

In his patent applications[34] for a LNA with inductive emitter degeneration and parallel, capacitive feedback [247, 246], Haagerats gives the following expression for the power gain:

$$S_{21} = j \times \frac{\omega \cdot C_F \cdot R_L + \frac{R_L}{\omega \cdot L_{SE}}}{1 + j \cdot \omega \cdot C_F \cdot R_L} \times \sqrt{\frac{Z_0}{R_L}} \tag{94}$$

The expression is independent of the bias current and the process used. The parallel feedback C_F reduces the high output impedance of the cascode[35] so that an LC network with a low transformation ratio can be used, allowing for a high bandwidth. As capacitive feedback according to the LNA core in Fig. 18 does not degrade the noise figure (see Fig. 79), the input transistor Q_0 can be optimised using the conventional techniques. C_F also reduces the real part of the input impedance and cancels some negative imaginary part of the input impedance, so that often no input match is needed any more. So the input match can be tuned with the output impedance, which makes the optimisation of this kind of LNA very difficult. As the current through the parallel capacitor is $\approx V_{out} \cdot \omega \cdot C_F$, it is the main purpose of C_F, to couple the signal back with such a favourable phase that IM_3 products are reduced or cancelled completely. Fig. 100 shows that tuning

[34] It needs to be noted that this circuit was patented by J.E.M. Hageraats in 2000 and 2001. Evidence exists, however, that the circuit has been used prior to the application already.

[35] Doing so replaces the non-linear base collector capacity and its associated non-linear Miller capacitance of a single common-emitter stage by a linear MIM capacitor.

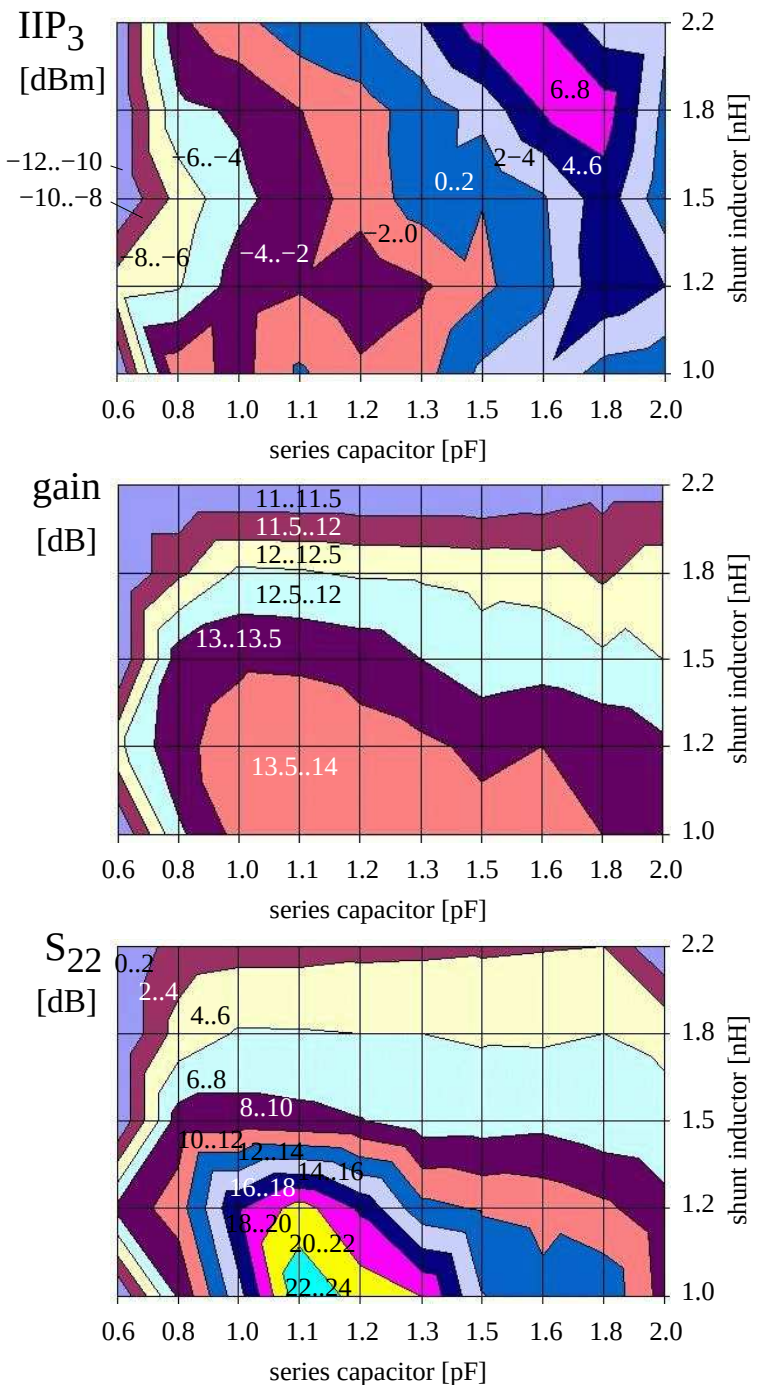


Figure 100: Linearity for this LNA with strong parallel feedback is sensitive to the output match. Optimum IIP_3 is achieved for 1.8 nH / 1.8 pF, optimum gain and output return loss for 1.2 nH / 1.1 pF. For applications with low bandwidth (e.g. 3 % for the PCS-band), gain and S_{22} can be traded against OIP_3.

the output LC match has a strong influence on the linearity (here in terms of OIP_3) as well as on output match S_{22}, gain and input match S_{11}. For applications with low bandwidth (e.g. 3 % for the PCS-band in an IS-95 application), gain and S_{22} can be traded against OIP_3. Due to the cancellation effects of 3rd order products with 2nd order products [63], a 3-6 dB improvement in OIP_3 is reported at a given supply current; or the same OIP_3 may be reached with 50% reduction in bias current [246]. Comparing the measured results of our IS-95 LNA [9, 10] with Lucek's rule-of-thumb in Fig. 78 shows that this is a reasonable assumption. The performance needs to be carefully checked over variations in temperature and component spread (especially C_F).

6.8.8 Matching networks with notch filters

For applications where a jammer occurs in a fixed frequency band only, rather than designing the LNA with a very high linearity, a notch filter can be implemented into the input matching network of the LNA. The notch is placed at the frequency of the jammer and attenuates the jamming amplitude such that the LNA can easily handle it. Using this technique a 1575 MHz GPS LNA was designed within this thesis, which is sold under the name ATR0610 [49, 50, 51]. The complete GPS chip set was introduced in section 2.5. The LNA itself uses a standard cascode configuration with series inductive emitter feedback and was optimised as described in section 6.3 and [49, 50, 51]. The absence of any parallel feedback leads to a good reverse isolation and a stability factor (Rollett's k) well above 1.2. The emitter inductance itself is realised by a package pin rather than an integrated inductor. The bandgap is according to Fig. 74, left. The schematic and chip photo of the IC is shown in Fig. 101. In a stand-alone GPS application a L-matching

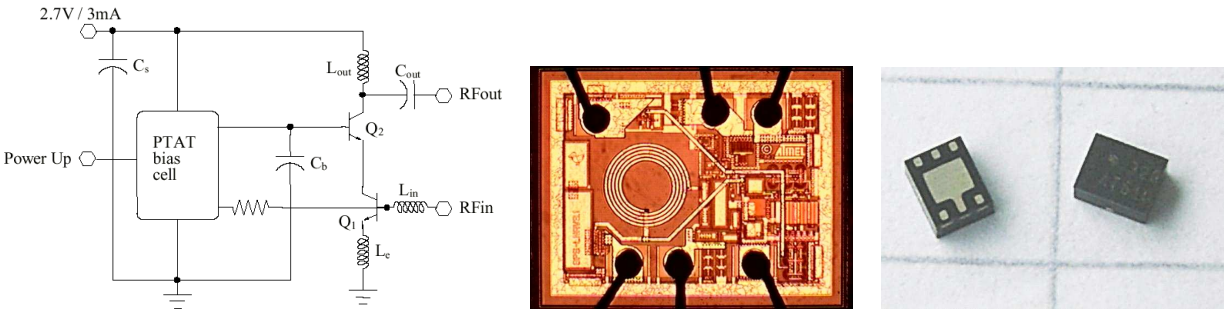


Figure 101: Schematic and microphotograph of the ATR0610 GPS LNA [50]. The miniature package (PLLP6) measures just 1.6mm × 2mm.

network is used for optimum return loss and NF properties (Fig. 102, left). The measured noise figure of 1.5 dB for this fully ESD-protected SiGe chip (1.6kV HBM) is comparable to values reported in literature for silicon BJT LNAs at higher currents and without ESD protection diodes[36]. In-band IIP_3 is -3 dBm and OIP_3 is 13.5 dBm. Comparing this with

[36] e.g. 1.4 dB NF and 20 dB of gain @ 1800 MHz for Infineon's 2-stage LNA BGA428 with a current consumption of 8 mA @ 2.7 V and IIP_3 = -9 dBm [93].

Fig. 78, this is the best what can be obtained at a bias current of 3 mA. As the power-down feature requires a separate package pin, a standard 5-pin transistor package was not an option for this device. The search for a 6-pin package with very low ground inductance for the DC and cascode ground led to the PLLP6 package, measuring just 1.6mm × 2mm. The packaged LNA requires less real estate on the PCB than a flip-chip mounted die which needs considerable spacing to adjacent SMD components for the underfill process.

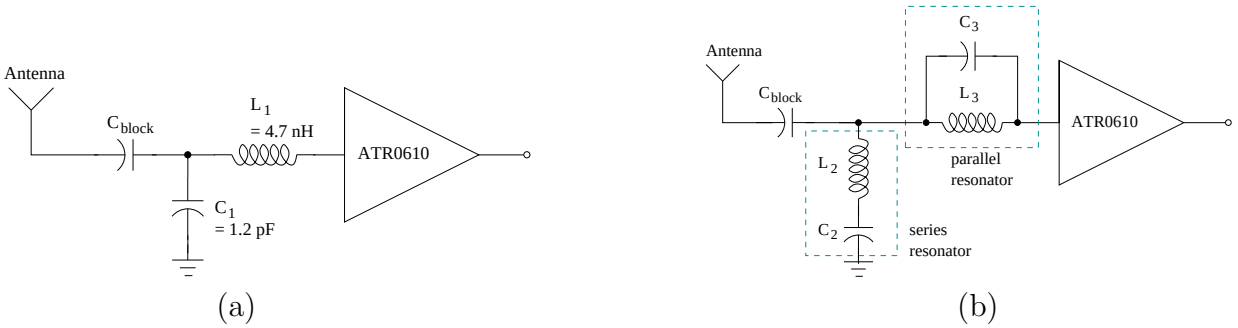


Figure 102: Input application circuitry of ATR0610 GPS LNA a) L-type network, b) 2nd order input network.

When the GPS module is integrated into a GSM mobile phone, a high jamming signal occurs due to crosstalk from the GSM1800 or GSM1900 power amplifier. The GPS receiver must be able to tolerate that jammer in order to allow for uninterrupted GPS data acquisition, even during GSM TX time slots. The matching network of Fig. 102, right, shorts the 1800 MHz jammer to GND by a series resonant tank while at the same time blocking the signal from reaching the LNA by a parallel resonant tank. At 1570 MHz the network provides the same impedance transformation like the L-match. As the notch needs to be placed at 1800 MHz while providing optimum gain at 1570 MHz, the design of the filter is critical and requires the use of high-Q SMD components with tight tolerance. The result is shown in Fig. 103: The matching network based on the notch filter suppresses the jammer by 20 dB compared to the L-type network while degrading the noise figure by just 0.4 dB. No increase in noise figure is observed up to a jammer level of -20 dBm. At CW jammer levels of -5 dBm and 0 dBm the degradation in NF is 1.1 dB and 1.6 dB respectively [49, 50]. Using this matching network, the out-of-band IIP_3 in the frequency range between 1.8 and 2 GHz is above +8 dBm with just 3 mA of current consumption.

Table 27 in appendix E compares the performance of ATR0610 with commercially available bipolar LNAs. Maxims MAX2654 [248], a 135 transistor device built upon Maxim's GST-3 SiGe HBT process [249] with a transit frequency f_T of 35 GHz has the same integration level as the ATR0610, except that the power-up pin is multiplexed with the RF output, requiring a choke to separate the signals on the board. Compared to the ATR0610, however, it shows 4 dB lower linearity at twice the current consumption. While the device at 1575 MHz shows a low NF_{min} of 1.30 dB, the equivalent noise resistance R_n is high

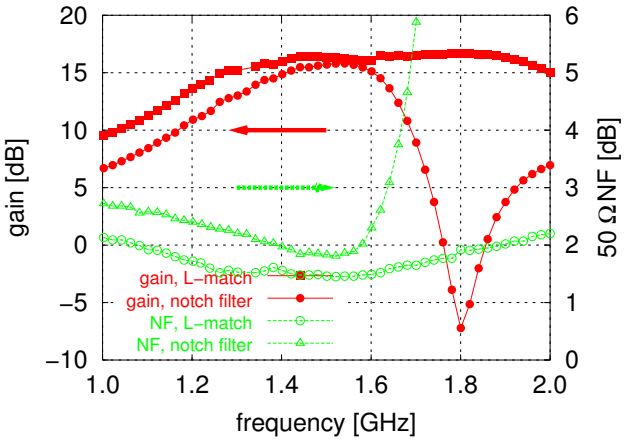


Figure 103: The suppression of the GSM1800 signal by the notch filter comes at the expense of a slightly higher NF.

(39.9 Ω) [250]. Together with a Γ_{opt} of 0.29 ∠ 114°, this makes noise matching difficult. For comparison: The ATR0610 has a comparable NF_{min} of 1.4 dB, Γ_{opt} of 0.38 ∠ 150°, but an equivalent noise resistance of just $R_n = 5.5\ \Omega$, which makes it a much more robust device against antenna mismatch, which is often encountered when customers use ceramic GPS patch antennas with a ground plane which is too small. The high R_n of Maxim's SiGe technology is also evident in the MAX2648 5 GHz WLNA LNA (see table 29). The BGA622 [251] uses Infineon's 70 GHz f_T Silicon Germanium technology and is a wideband amplifier with pre-matched input and output and a low gain bypass stage. As the power-up pin is multiplexed to the RF output pin, an inexpensive 4-pin SOT343 package can be used. Due to its wideband nature, the gain at 1.575 GHz is quite low, but the linearity is remarkable for a broadband design. If a low-gain mode is needed, the BGA622 is definitely a good choice, but the device is ESD sensitive. The JRC GaAs HBT LNA has a lower NF, but this is due to the absence of any ESD protection. Furthermore, it requires 3 SMD inductors and 1 supply blocking capacitor. The μPC8211TK, finally, is a general purpose SiGe HBT LNA from NEC Electronics which can be matched to different applications using SMD components. The GPS implementation requires the usage of 3 inductors, 7 capacitors and 1 resistor, requiring a large board space which cannot be compensated by the tiny 1.3 × 1.5 mm^2 lead-less minimold package. While the NF performance is 0.2 dB better compared to the ATR0610, the linearity is 9 dB lower, while drawing the same amount of bias current [252, 253].
Table 28 in appendix E compares the performance of ATR0610 with FET LNAs. The 0.5μm-MESFET models shown in table 28 are self-biased depletion-mode devices, non-ESD protected, and come in a huge SOIC-8 package. AM50-0002 is a three-stage MESFET LNA with low NF, but huge current consumption (20 mA) and relatively low linearity. The application note proposes to match the high input impedance to 50 Ω using a very narrowband strip-line matching network, which is very sensitive. MAAM-12021 is a

cascode design, which is optimised for 5 V applications and offers poor linearity at supply voltages of 3 V. Simulations using state-of-the-art, discrete pHEMT enhancement-mode devices ATF541 [254, 255] show noise figures of 0.5 dB with linearities comparable to the ATR0610[37]. An harmonic balance simulation using the advanced Curtice quadratic model provided by Agilent delivered OIP_3 values for 3.7 and 6.4 mA bias current which are in line with Fig. 78 (table 28). As there was no influence of any low frequency termination on the linearity, the fundamental nonlinearities of FETs seem to be completely different from those of the BJT. The schematic is shown in Fig. 149 and uses a common-source configuration with reactive LC output matching. The chosen device showed a minimum NF of 0.4 dB at 1.6 GHz with $R_n = 2.5\,\Omega$ at a bias current of 9 mA which compares well with the measured noise figure of 0.5 dB. As the reverse isolation of the transistor itself was already critical, no parallel feedback has been used: The stability of the amplifier is very marginal with $k < 1$ over a wide frequency range. Therefore the device needs to be terminated properly at input and output. The shunt inductor at the input provides a return loss of $|S_{11}|^2 = 7.2$ dB as well as ESD protection and moves the optimum source match towards 50 Ω. Output return loss is better than 14 dB.

Nearly the same NF was achieved by a SiGe test design, similar to the production version

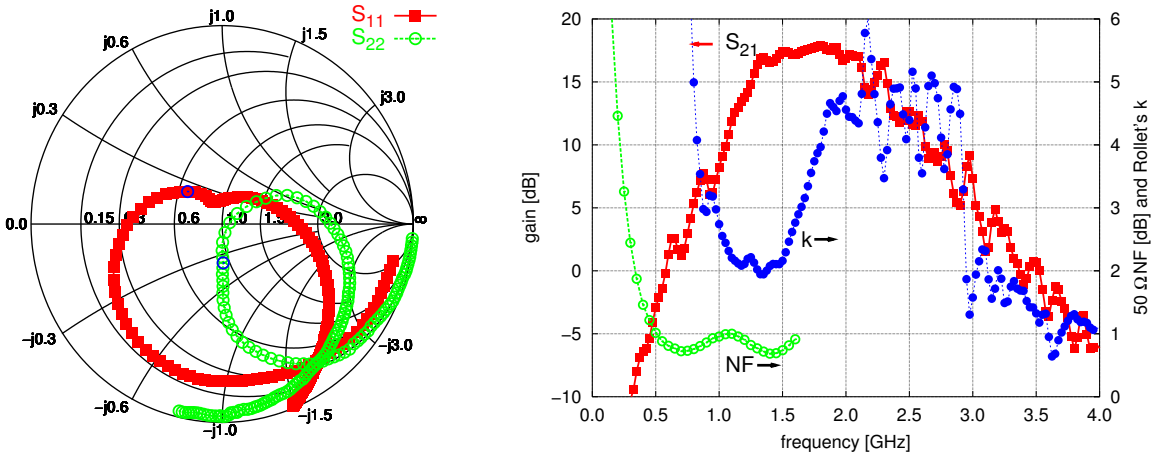


Figure 104: LNA similar to the design in Fig. 101, but realized in SiGe2-Power technology

shown in Fig. 101 but using the SiGe2-Power process. It achieved a NF of 0.8 dB at GPS frequencies with a much better input return loss ($|S_{11}|^2 > 12$ dB) while drawing just 50% of the pHEMT's bias current (including bandgap and power-down circuitry). The cascode

[37] For e-pHEMT devices, at low currents densities the drain current varies nearly exponentially with gate-source voltage (V_{gs}=0.35V @ 3.7mA, V_{gs}=0.38V @ 6.4mA). This makes the biasing very difficult and requires to connect the gate via a resistive voltage divider to a resistor in the drain, which drops around 1 V across the drain resistor in order to stabilise the drain current by negative feedback (see Fig. 133). The alternative are active bias controllers, which tend to oscillate when not designed properly. Biasing of enhancement mode FETs seems to be a general problem and thus explains that Agilent filed a patent application for the well known bias circuit of Fig. 72, right (see [230] and footnote 29).

RF stage with on-chip output match ($|S_{22}|^2 > 14$ dB) provided excellent stability. Using the GaAs pHEMT LNA instead of this advanced SiGe LNA would lead to 0.3 dB more GPS sensitivity, however at the expense of stability and at twice the power consumption. Compared to the implementation losses of typical GPS antennas, the 0.3 dB difference in sensitivity are negligible.
These results show that SiGe HBT technology can deliver similar noise and linearity performance with better stability at lower supply voltages and lower current consumption than GaAs MESFET and pHEMT.

6.8.9 Comparison of the circuit design techniques for linearization enhancement

For the WLAN system described in section 2.4 a broad-band LNA was designed according to the specifications of table 22.

Frequency range	4.9 - 5.9 GHz
Noise figure	< 2 dB
Gain	10 dB (min.)
$P_{1dB,in}$	-14 dBm (4.9-5.4 GHz) -12 dBm (5.4-5.9 GHz)
IIP_3	-4 dBm (4.9-5.4 GHz) 0 dBm (5.4-5.9 GHz)
Power consumption	7-8 mA @ 3V

Table 22: Target specification for the 4.9-5.9 GHz WLAN LNA [37].

Simulations using the SiGe2-RF design kit showed that the 2 dB NF is the main difficulty in reaching the specs of table 22, although Erben *et al.* [86, 92] in 1998 reached NF_{min} values of 1.6 dB on-wafer at 5.7 GHz for a 2-stage common-emitter LNA using TEMIC's pre-production SiGe1 process. As discussed in section 2.4, a single-ended design was requested as its easier to interface to the TX/RX switch. For the required bandwidth of 19%, a transimpedance stage would be appropriate, but the resistive feedback deteriorates the NF and a resistive load at a supply voltage of 3 V strongly reduces linearity. A narrow band amplifier architecture has finally been chosen, with the Q of the LC matching reduced by a 500 Ω resistor to reach the required bandwidth. A simple common-emitter stage showed the lowest noise figure, but at the band edge of 5.9 GHz delivered just 9.5 dB of gain. Finally, a cascode structure was used as in [45], as it increased the NF by less than 0.05 dB, but allowed for a higher gain margin. The common-emitter HBT is a 4-finger SIC device ($0.5 \times 15\mu m^2$ each) which is cascaded by a 2-finger non-SIC device. For biasing, a PTAT bandgap based on the Widlar ΔV_{BE}-cell was used similar to the one shown in Fig. 74. Compared to the previous designs in Figs. 87, 94, 99, 101, however, the base of the cascode was not connected to a 1.4 V reference (2 diodes), but was connected directly to the 2 V rail of the Widlar bandgap via a 1.5 kΩ / 3 pF low pass: Besides reducing the

Technique	IIP_3 [dBm]	OIP_3 [dBm]	gain [dB]	NF [dB]	NF_{min} [dB]
bias resistor 4 kΩ	3.28	15.87	12.58	1.76	1.64
bias resistor 3 kΩ	**3.56**	**16.16**	**12.59**	**1.80**	**1.66**
bias resistor 2 kΩ	3.86	16.43	12.56	1.86	1.71
bias resistor 1 kΩ	4.33	16.47	12.40	2.00	1.81
bias resistor 0.5 kΩ	4.95	17.02	12.06	2.26	1.98
ideal 10nH bias inductor	4.91	17.44	12.53	1.75	1.59
3 kΩ / BBST (100 pF)	3.64	16.24	12.59	1.81	1.66
3 kΩ / BBST (1 nF)	5.40	18.00	12.59	1.81	1.66
3 kΩ / BBST (infinite capacitance)	5.82	18.42	12.59	1.81	1.66
3 kΩ / LF trap, centred at 1 MHz	6.22	18.67	12.45	1.85	1.66

BBST = broadband source termination

Table 23: Simulated results of different LF termination techniques at 5.5 GHz (3 V / 8 mA), 1 MHz tone spacing). Coupling capacitor to the source is 27 pF if not otherwise noted.

overhead bias current, this way enough base current is supplied to the cascode HBT even under heavy compression and therefore P_{1dB} is improved. The full schematic is shown in Fig. 150. For linearity optimisation, different methods of low frequency termination are compared by harmonic balance simulation in table 23: Reducing the resistor value in the current mirror of Fig. 72 improves linearity, but at the expense of an increased noise figure. Terminating the input HBT with the source impedance using a large coupling capacitor improves linearity by approximately 2 dB, if the capacitance is large enough (e.g. 1 nF → Z = 159 Ω at 1 MHz) and if the source impedance is 50 Ω down to low frequencies (which is usually not the case in practical applications). Finally, a low-frequency trap network consisting of a 10 nH inductor in series with a 2.5 μF capacitor provides a short circuit at the beat frequency (1 MHz) and gives 2.5 dB improvement without compromising NF and gain. As the simulated linearity was well above the required value of 0 dBm (table 22), we optimised the circuit for NF (3 kΩ bias resistor) and lowest bill-of-material (no low-frequency trap network). While a first test version with small GSG pads for on-wafer probing used a 0.4 nH on-chip emitter inductor (see Fig. 105, right), the final IC was slightly modified for chip-on-board (COB) mounting (see Fig. 105, left): The emitter degeneration inductor ($L_e = 0.45$ nH) and the base inductor were replaced by bond wires, the number of GND pads was reduced from three to two and the output capacitor was reduced from 0.33 to 0.25 pF in order to accommodate the output bondwire. Initially we had been worried about combining the GND pad for the cascode GND and the GND to which the supply voltage is blocked into one bond pad, as we expected lower reverse isolation and hence worse stability. However, due to the use of a double bond pad which allows for two bonds with 90° orientation, we obtained an excellent reverse isolation of 34 dB for 6 samples mounted COB (see Fig. 106, right). A 10 $k\Omega$ shunt inductor at the

output provides some ESD protection for the sensitive MIM capacitor. The result of 6

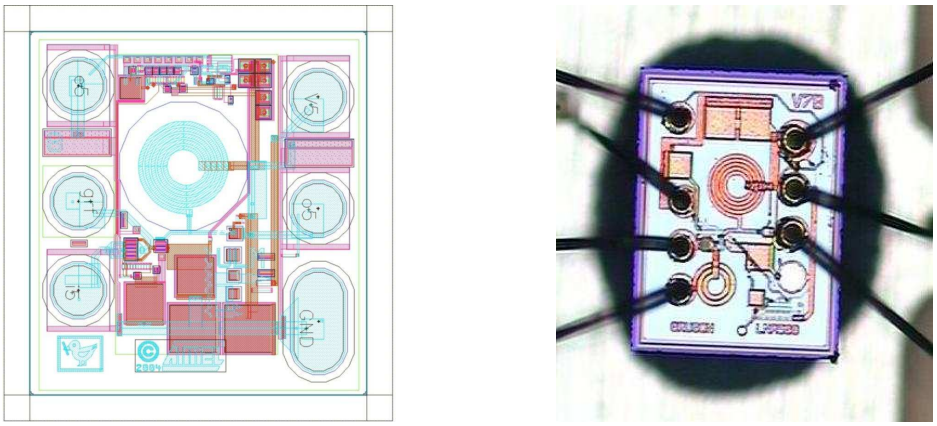


Figure 105: Final layout of the 802.11a LNA (left, 0.6 × 0.64 mm^2) and test version in a PLLP6 package (right).

ICs from one SiGe2-Power lot, mounted on a RO4003 substrate of 0.2 mm thickness is shown in Fig. 106. The fully integrated LNA requires just a 27 pF blocking capacitor (0201 size) at the input. Enable and supply voltage were blocked by 100 pF on the board to avoid noise pickup via the cabling (similar to Fig. 9). As the supply is blocked internally with 10 pF, external blocking might be obsolete in the final application. The SMA-to-microstrip transitions had only ≈ 10 dB of return loss and thus the calibration was done using a test PCB with an 'Open', 'Short', 'Load' (2 × 100Ω [SMD] in parallel) and 'Thru' instead of the LNA die. This moved the reference plane to the place where the aluminium bonds touch the board. Although the ICs had been mounted manually, they show very consistent performance: The return loss is around 15 dB in the band of interest (4.9...5.8 GHz). Compared to the on-wafer measurement, the gain dropped by 1 dB to 12 dB and shows little variation via the 4.9...5.8 GHz band. The reverse isolation is 34 dB, which is an excellent value for a bonded 5 GHz device. The small notch in the transfer function at 1.1 GHz is due to a resonance of the on-chip 10 pF to GND, and the supply bond wire, damped by a 12 Ω on-chip resistor in series to the supply bond wire.

The measured data are compared to literature data in table 29 in appendix E. Compared to the balanced SiGe1-LNA of the HG-Dat project (in high-gain state), the improvement due to the SiGe2-Power technology is evident. Maxim's MAX2648 [256] uses Maxim's GST-3 SiGe HBT process [249] and is packaged in a 1 mm × 1.5 mm ultra chip-scale package (UCSP™). As the output is an open-collector transistor, the DC bias and RF matching network need to be realized off-chip using 7 SMD components and a stripline [256], which is a tricky thing to do at 5 GHz [257], as this is close to the self resonance of off-the-shelf SMD components. For the usage in a front-end module, the required board space is impractical. In contrast, the ATR7158 requires just a 27 pF input blocking capacitor. While the noise figure is comparable to this work, the high R_n of 58.5 Ω makes the noise figure of the MAX2648 extremely sensitive to source mismatch. This is especially true,

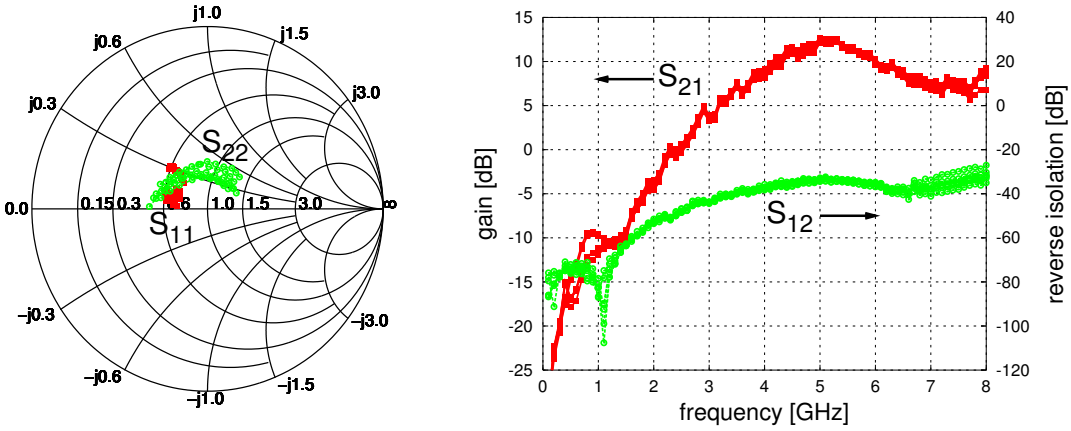


Figure 106: 6 different ICs from the same lot, mounted chip-on-board (COB) onto 0.2 mm-RO4003. Left: return loss at 4.9. . .5.8 GHz, right: gain and reverse isolation.

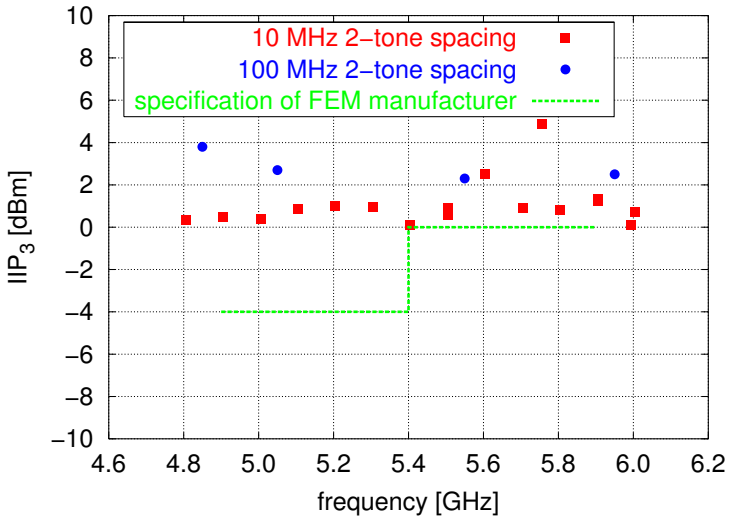


Figure 107: 3rd order intercept point of the 5 GHz SiGe LNA for different tone spacing. The specification of the front-end module manufacturer is easily met.

as Γ_{opt} is far from 50 Ω.
Finally, three 5 GHz CMOS LNAs are listed in table 30 [258, 259, 260]. Operated at the maximum allowable supply voltage of 1.2 V of the 90 nm CMOS technology, the design by Linten *et al.* from IMEC uses a shunt inductor as part of the input matching network to achieve an ESD level of 2 kV (HBM). As in all CMOS LNA implementations, a cascode with LC output matching network is used [261]. The high noise figure of 3.0 dB (2.7 dB for the device without ESD protection) can be attributed to the use of a large (4.3 nH) on-chip series inductor in the input match. Satou *et al.* of Fujitsu uses a 0.11 μm CMOS process to achieve 1.6 dB of noise figure with modest linearity. The lowest NF of 1.4 dB

is obtained with the "largest" gate length of 0.18 μm by Mohammadi *et al.* at a very low current of 2.5 mA and a remarkable linearity. LNA implementations using sub-μm CMOS technologies have two problems:

1. Due to the high cost of the mask set, CMOS LNA designs make only sense in large integrated transceivers, which run in very high volumes. They are not suited for front-end modules, as the overall cost is too high.

2. While the minimum NF is usually low (see table 8), the high equivalent noise resistance R_n makes them extremely sensitive to source mismatch.

The 2.4 GHz design of the dual-band LNA ATR7124 uses the same architecture as the 5 GHz circuit, except that the size of the input HBT is doubled ($8 \times 0.5 \times 15$ μm^2). The 5.8 nH load inductance is realized by a multi-level coil [135] in order to minimise chip real estate (see section 5.16). Figure 108 shows return loss and gain for a device mounted chip-on-board with a relatively large emitter bondwire. Correcting for board

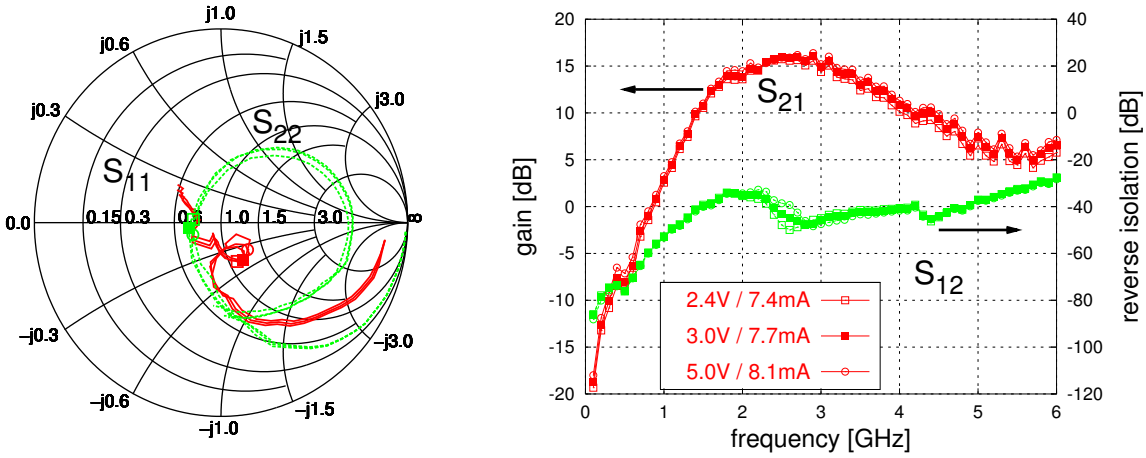


Figure 108: 2.4 GHz (chip-on-board) LNA at 3 different supply voltages. Left: Bold dots are at 2.4 GHz. Right: Extremely good power supply rejection due to integrated bandgap circuitry.

parasitics, a noise figure below 0.9 dB was achieved with 16.5 dB of gain (Fig. 109). The measured data are compared to commercially available HBT LNAs in table 31 of appendix E. The BGA622 uses Infineon's 70 GHz f_T Silicon Germanium technology and is a wide-band amplifier with pre-matched input and output and a low gain bypass stage. Due to its wideband nature, the gain at 2.4 GHz is low. The SiGe HBT LNA MAX2644 from Maxim [262] has similar linearity at the same power consumption, but the NF is 2.0 dB. The RF2373 from RFMD [263] is an open-collector AlGaAs HBT LNA and can be configured to any frequency between 400 MHz and 3 GHz using LC output and input match by SMD components. While the NF is moderate, the linearity is 2 dB above Lucek's rule-of-thumb in Fig. 78 (24.5 dBm of OIP_3 for 13 mA).

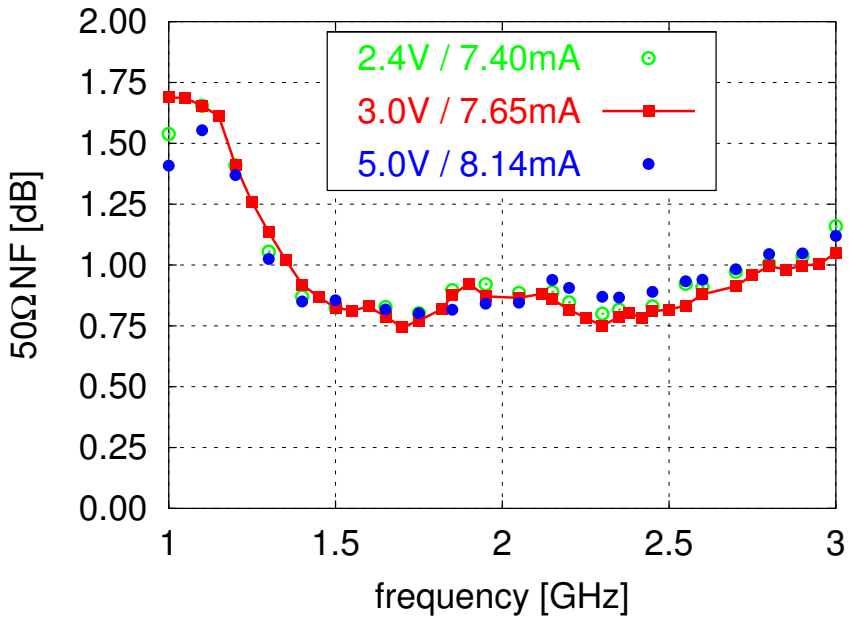


Figure 109: Noise figure of the 2.4 GHz chip-on-board LNA for a 2.4 to 5 V supply.

7 The downconverter

7.1 Super-hetero and direct-conversion receivers

Since the invention of the superheterodyne receiver[38] by Walter Schottky of Siemens in 1918 [94] and Edwin Armstrong in 1920 [261], radio front-ends make extensive use of frequency downconversion from radio frequency transmitted over the air to an intermediate frequency (IF). At this early level in the front-end there is no fundamental difference whether the input signal is modulated in an analog fashion or a digital one. The IF frequency is usually fixed which allows for the use of a very steep passive filter using ceramic resonators or filters based on surface-acoustic-wave (SAW), film-bulk-acoustic-resonator (FBAR) or bulk-acoustic-wave (BAW) technology [70, 71, 72]. To downconvert one of the various RF channels of the system, the local oscillator is stepped across the channels using a voltage-controlled oscillator (VCO) which is locked to a quartz reference using a phase-locked-loop (PLL) circuit. A direct conversion receiver (DCR) downconverts the modulated RF signal directly to baseband, eliminating the need for an IF SAW filter at the expense of power-hungry active base band (BB) filtering. DCRs are more difficult to implement due to the following problem [264, 265]:

- In a superheterodyne receiver, DC offset – generated by imperfections in the mixer – can easily be removed by AC coupling.
- In a DCR – as the VCO runs at the RF centre frequency – LO signal leaking back through the mixer and the LNA to the antenna is reflected at a mismatched antenna, fed back via the LNA to the mixer and downconverted; leading to a DC offset at the output of the mixer (self-mixing). This high amount of DC offset often *cannot* be removed by AC coupling but needs an active DC offset canceler resulting in increased power consumption [265]. This problem of self-mixing is reduced by using a LNA with a high reverse isolation (see section 6.8.4), a mixer with a high LO-to-RF isolation and a careful PCB design.

In the transmit path the mixer modulates the baseband signals back onto a RF carrier. This upconversion process can be a direct one (direct conversion) or take place via an IF frequency which allows for additional filtering before the final upconversion to RF happens. IQ modulators are usually used in digitally modulated systems.
In most of the systems described in this thesis, the superheterodyne approach has been favoured over the DCR:

- Narrowband CDMA (IS95), as described in sections 2.2.2, 2.2.3, and 3, is a challenging system, and some phones even today still use a superhet receiver. The reasons are (i) strong blockers, after passing a highly linear LNA and mixer frontend, may

[38] Superheterodyne receiver: Radio receiver that converts all radio frequencies to a fixed intermediate frequency to maximise gain and bandwidth before demodulation.

be filtered easier using an IF compared to doing so at base band frequencies (ii) the small channel bandwidth does not allow for the removal of the DC offset by AC coupling (as it is the case in UMTS receivers), and finally (iii) the superhet has always a lower power consumption, as filtering is done on the IF using passive filters, rather than using active filters at BB frequencies.

- Professional mobile radios (section 2.3) are high-performance devices with very high linearity requirements, while cost is a minor issue.
- As has been described in section 2.5, the GPS signal is well below the noise floor and needs to be amplified – despite the high coding gain – at RF and IF frequencies. To the author's knowledge, no GPS DCR has been reported so far. Two superhet architectures are currently used: The double conversion receiver with 2 IF frequencies and the single conversion receiver with direct subsampling at the IF. Due to its very low power consumption, the latter is used in Atmel's ANTARIS™GPS chip set, despite the high NF associated with the subsampling architecture [261].
- In UMTS, described in sections 2.2.4, DCRs dominate over the superhet in mobile devices. Also the base station receiver, developed within the SCUBA framework, uses DCR in order to down-convert 4 channels simultaneously (see Fig. 4).
- Due to the price war for WLAN (section 2.4) devices, most of the solutions on the market use a DCR architecture, with a trend to an all-CMOS implementation.

Frequency mixers are key components in both superhets and DCRs. The first implementations used a single vacuum tube to realize oscillator, mixer and amplifier in a single device (e.g. Armstrong [261]), a technique which is still applied using IMPATT or Gunn diodes at sub-millimetre frequencies. Also the first transistor radio, the Regency TR1 used this approach in order to minimise the usage of the expensive Ge transistors [261]. In the next section we will have a look on the fundamentals of mixing operation, classify mixers in non-linear and commutating devices and give some examples.

7.2 Mixing operation

Using simple trigonometric analysis, a frequency converter ("mixer") analytically is often treated to be a multiplier:

$$\begin{aligned} V_{IF} &= A_{RF} \cdot \sin(2 \cdot \pi \cdot f_{RF} \cdot t) \times A_{LO} \cdot \cos(2 \cdot \pi \cdot f_{LO} \cdot t) \\ &= A_{RF} \times A_{LO} \cdot [\sin(2 \cdot \pi \cdot [f_{RF} - f_{LO}] \cdot t) + \sin(2 \cdot \pi \cdot [f_{RF} + f_{LO}] \cdot t)] \end{aligned} \quad (95)$$

An ideal mixer generates the *difference* and the *sum* of the input frequencies, while suppressing the input frequencies completely. In a down-conversion mixer, the sum of the input frequencies, $f_{RF} + f_{LO}$, is usually easily suppressed by low-pass filtering. While Eqn. 95 is a handy expression, it strictly only holds for frequency multipliers, where the

output amplitude is proportional to the *product* of the input amplitudes. Such devices do exist as products, but they suffer from a low conversion gain and a high noise figure and are rarely used. Mixers, on the other hand, should be as "linear" as possible in the sense that doubling the amplitude of the input signal exactly doubles the amplitude of the output frequency, but they should be insensitive to variations in LO amplitude in order to get rid of both AM noise and amplitude variations of the VCO. Eqn. 95 therefore can only give an indication of how a mixer works. The difference between a mixer and a multiplier is graphically shown in Fig. 110.

7.3 Mixers utilising device nonlinearities

While a mixer should be linear in amplitude from RF to IF, it cannot be built upon a single linear element, as a linear circuit cannot lead to frequency conversion. Therefore frequency conversion is often referred to as being a nonlinear process, making use of the nonlinear transfer function of a semiconductor device. This is true for a first kind of mixer often used in the design of MMIC mixers at elevated frequencies, exploiting the nonlinearities of Schottky diodes, MESFETs or HEMTs. Three-port device mixers as shown in Fig. 112 have advantages over diode mixers here, including higher conversion gain, wider dynamic range, and better isolation between the ports [266]. The cascode MESFET mixer [267] as shown in Fig. 112, right, is suited for low frequency applications, as it does not need passive couplers: The LO is usually fed to the gate of the upper FET (or the 2nd gate of a dual-gate device) and the RF is fed to the gate of the lower FET. The IF can be deduced from the drain. Fuente *et al.* reported high conversion gain (13 dB) and high linearity (IIP_3 = 7 dBm) along with 20 dB port-to-port isolation for a 600 - 1800 MHz mixer with +7 dBm of LO drive using 0.5 μm × 300 μm GaAs MESFETs [267]. NF and power consumption were not reported.

7.4 Switching mixers

A simple switching mixer has been proposed by Maas [65]: It consists of a single FET, operated in resistive mode ($V_{DS} = 0$). The LO is fed to the gate and switches the FET ON and OFF periodically. RF is feed to the drain and at the same node the IF is deduced. When the LO signal is "high", the FET provides a short circuit at the drain, when the LO signal is "low", the FET is in its high impedance state. In the ideal case, the FET would resemble a pure relay (0 Ω in ON state, no shunt capacitance in OFF mode). The circuit can be operated single-ended and does not need any transformers or baluns. A GaAs implementation for a 500 - 2500 MHz mixer reached 5.7 dB conversion loss, +24 dBm of IIP_3 and 6 dB of NF at a power consumption of 6 mA at 3 V [268]. As already pointed out by Maas [65], the difficulty is in the realisation of the matching networks. As RF and IF are both taken from the drain node, the mixer cannot provide isolation between them. Maas recommends to provide a short circuit for the LO frequency at the drain, which is difficult to realise as $f_{LO} \approx f_{RF}$. Instead, following [268], we used a series resonant

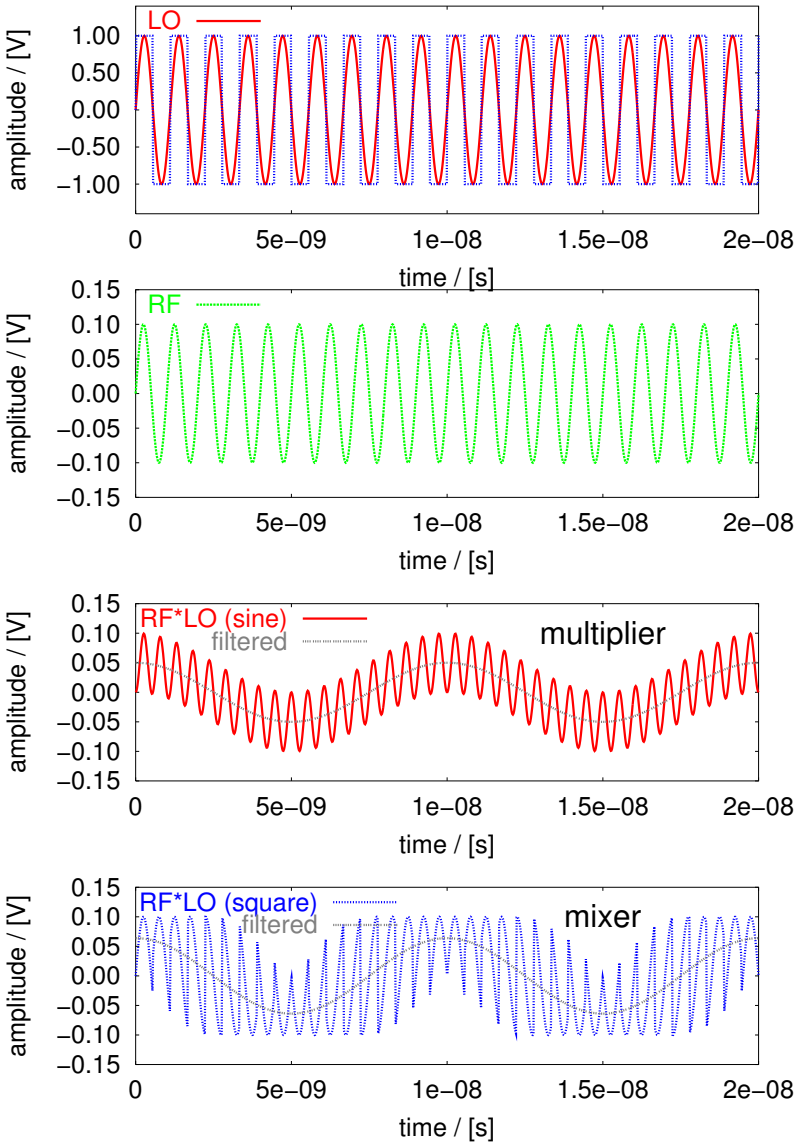


Figure 110: A multiplier *multiplies* two sinusoidal signals, RF (green) and LO (red), whereas in an ideal mixer the RF signal is *commutated* with a rectangular LO signal (blue), leading to lower conversion loss (-3.9 dBV versus of -6 dBV in this example) and lower noise figure (RF = 1 GHz, LO = 0.9 GHz).

tank at the input, tuned to the RF frequency of (62 nH in series to 2.7 pF) and at the output a parallel tank tuned to the LO frequency (1.5 pF in parallel to 100 nH) , in order to block the 460 MHz LO frequency from reaching the IF port. At the IF frequency of 50 MHz, the parallel tank has the admittance of a 98.5 nH inductor, which is matched to 50 MHz using a 100 pF capacitor. A 2-stage CMOS buffer was used to amplify the LO input power (-5 dBm) into a rail-to-rail signal before being fed to the 16 × 0.35 μm

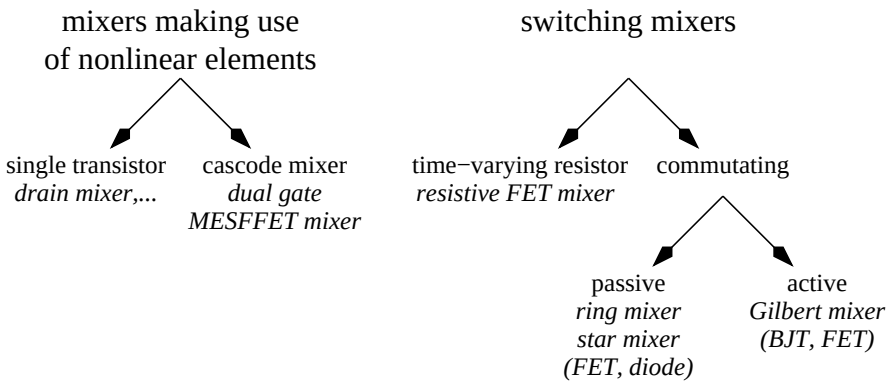


Figure 111: Mixers may be classified into nonlinear and switching types.

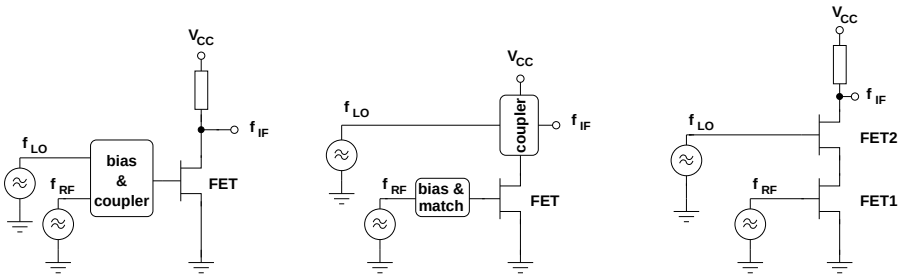


Figure 112: Three-terminal mixer based on MESFETs: Left: Gate mixer, centre: drain mixer [266], right: cascode (or dual-gate) mixer [267].

$\times$ 20 μm NMOS transistor. For symmetry in g_m, the inverter of the 1st LO buffer stage uses a NMOS with 20 μm gate width and a PMOS with 40 μm gate width. The feedback resistor biases the inverter close to $V_{CC}/2$ so that a small LO input power is sufficient to toggle it. The gate width was doubled in the 2nd buffer stage in order to drive the gate of the 320 μm wide shunt NMOS. The mixer was realised using Atmel's at46k technology and the results are depicted in Fig. 114. The strong point of that circuit design is that

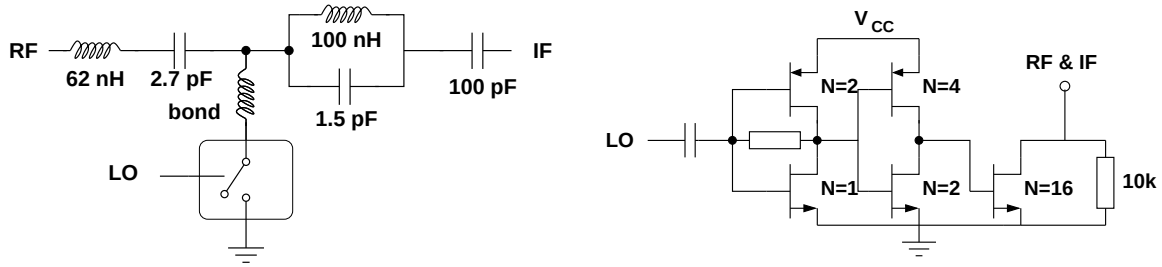


Figure 113: Resistive FET mixer [65] applied to a 400 MHz PMR front-end. Left: Filters and matching, right: core circuit.

it needs virtually no current (just the AC current needed to charge/dis-charge the MOS transistors). Having a look on the simulated and measured results, however, the result is disappointing (Fig. 114): The simulated IIP_3 characteristics is not a smooth function of

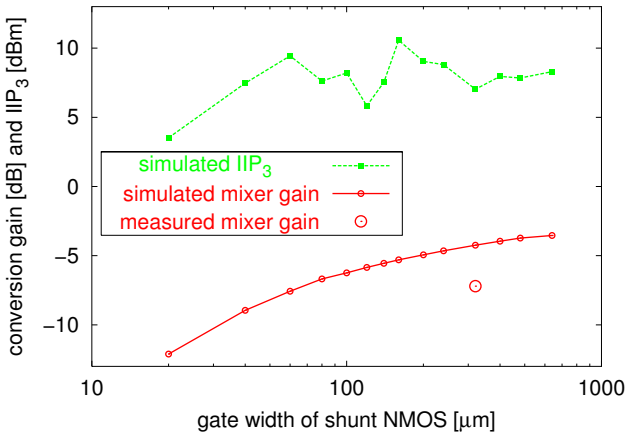


Figure 114: Simulated vs. measured conversion loss and linearity for the resistive FET mixer of Fig. 113 (f_{RF} = 410 MHz, f_{LO} = 460 MHz).

the switch's gate width. The reason is a severe IIP_3 asymmetry, which might be due to convergence problems in the HB simulator. The measured conversion loss is 3 dB worse than the simulation. As the circuit was extremely sensitive to the filter and matching circuits, no further optimisation was done.

7.5 Commutating mixers

At RF frequencies, rather than using single-diode or 3-terminal mixers, commutating mixers proved to be useful. The operational principle of a commutating mixer is shown in Fig. 115: RF and LO signal are fed as balanced signals. During one alternation of the LO

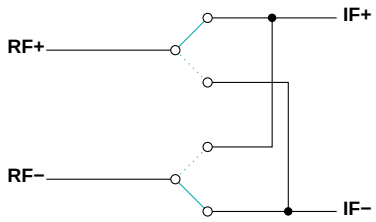


Figure 115: Operational principle of a commutating mixer.

signal, RF+ is switched to IF+ and RF- is switched to IF-. During the next alternation of the LO signal, RF+ is switched to IF- and RF- is switched to IF+. The result is

displayed graphically in Fig. 110, bottom: Compared to a multiplier, the conversion gain of a commutating mixer is higher and its noise figure is lower. Commutating mixers can be both passive (using Schottky diodes or FET transistor as switches) or active. The latter is based on Barrie Gilbert's ingenious invention and is the heart of any modern mobile phone.

7.5.1 Passive commutating mixer using Schottky Diodes

The commutating mixer shown in Fig. 115 is realised as a ring mixer as depicted in Fig. 117, using either diodes or FET transistors. Both are reported to offer low noise figure, low conversion loss (6-7 dB, respectively) and high linearity. A disadvantage of these balanced circuits is that they need several broadband transformers, namely 2 for the diode mixer (one of them centre-tapped to derive the single-ended IF) and 3 for the FET mixer (for RF, LO, and IF port). In a diode mixer, Schottky diodes [269] are used due to their high speed (see section 4.3). The penalty for the high linearity is that commutating passive mixers need to be driven at a very high LO drive level: A level-10 mixer requires +10 dBm of LO input power and typically delivers +20 dBm of IIP_3, which drops to typically +10 dBm of IIP_3 for a level-7 mixer (+7 dBm of LO input power). While these LO power levels are available in base stations, they are difficult to realize

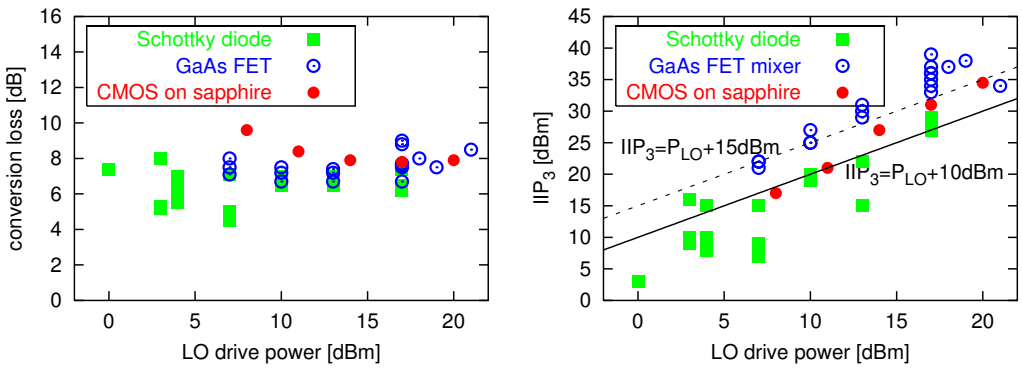


Figure 116: Conversion loss and IIP_3 for commercially available passive ring mixers with integrated transformers in the 0 - 2 GHz range (Source: MiniCircuits, Cougar, wj communications, Peregrine).

in mobile terminals due to power consumption constraints and problems with crosstalk. Therefore, this kind of mixer is typically used in base stations, as the high linearity and high compression level allows to use a LNA with very high gain. Together with the 6 - 7 dB mixer NF, the NF of the receiver is mainly determined by the loss of the antenna filter and by the LNA. For the PMR system as shown in table 3, even for the handset this approach was chosen, as due to the very low channel spacing the jammers occur in-band. Therefore the IIP_3 of the mixer needs to be in the order of the LNA's IIP_3 (6 dBm) plus the LNA gain (17 dB) minus the loss of the RX filter ($\approx$ 3 dB) in order not to degrade

the linearity of the overall system. As can bee seen from Fig. 116, left, a 6 dB conversion loss is difficult to achieve. This is confirmed by a simulation with ideal transformers and ideal diodes (no parasitic resistances and capacitances) which delivered a conversion loss of 5.5 dB already. Adding device parasitics and transformer loss (0.5 - 1.0 dB for a wire wound type at 400 - 800 MHz) allows for little margin. As the LO drive level was specified to be 0 dBm for the PMR handset, a LO buffer amplifier needed to be integrated, in order to reach an IIP_3 of +20 dBm.

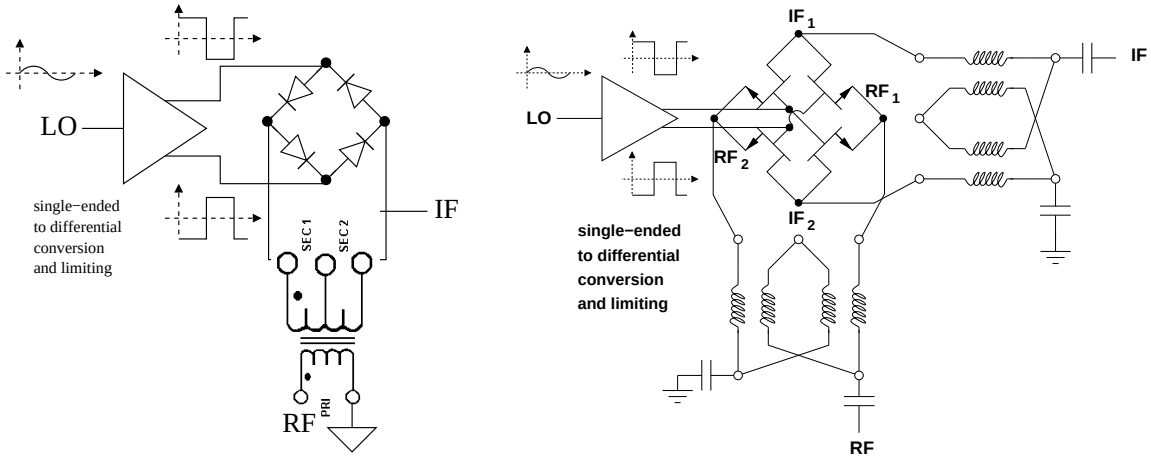


Figure 117: Ring mixers used in the 400 MHz and 800 MHz PMR front-end: Left: Diode mixer, right: FET mixer.

The first TETRA/TETRAPOL design was a passive diode mixer using the Schottky diodes available in the SiGe1 technology. As explained in section 4.3, they consist of a TiSi Schottky contact (external base connection) on n-type silicon (collector layer). These diodes have primarily been developed for use in power amplifiers with integrated power detectors. Indeed, as shown in table 7, their threshold voltage is as low as 0.18 V, which makes them suited for detector applications, but not ideal for mixing applications, were diodes with medium or high barriers are required. The difficulty in designing the LO buffer, which provides the necessary balanced drive to the diodes, is the very low impedance of a diode so that a large amount of current is necessary to drive the diode quad. A single-ended to balanced converter similar to Fig. 153, left, has been used, followed by a differential, limiting pair and emitter followers with large bias current in order not to clip the signal. The schematic is shown in Fig. 117, left. The wire wound, centre-tapped balun which was used at the RF port was larger than the LNA/Mixer IC itself. While the realised SiGe1-LNA had a good performance regarding NF and linearity [270], the results of this mixer were poor: Consuming 9.2 mA of DC current from a 3 V supply, the conversion loss was 8 dB and IIP_3 was a disappointing +6.5 dBm at 650 MHz RF frequency. As the optimum performance was reached at a LO power of -8 dBm, the gain of the LO buffer was not the problem. However, when increasing the supply voltage to 4 V, which increases the bias current from 9.2 mA to 15 mA, the

conversion loss was improved to 6.5 dB [271]. We concluded that the current drive of the diodes from the emitter followers was too low. In order not to increase the quiescent DC current of the emitter follower, a push-pull stage as shown in Fig. 151 was used. In addition, the models of the Schottky diodes themselves were improved (see section 4.3). Simulations using this buffer showed that the conversion loss target could be reached

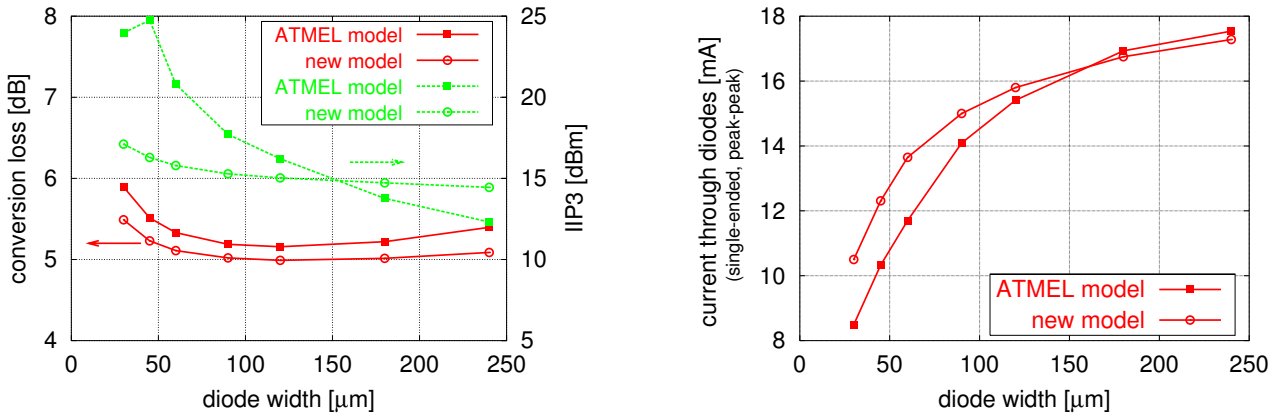


Figure 118: Diode mixer with push-pull LO buffer. Left: conversion loss and IIP_3 (2 MHz tone spacing), right: current through diodes.

using 100 ... 200 μm diodes. The new model, however, predicted much lower linearity than both the Atmel design-kit model and the specification. The required current just to drive the diodes would have been more than 12 mA, which is twice what the specification allowed for. Therefore we moved to a FET mixer design and switched from SiGe1 to the at46k SiGe BiCMOS technology.

7.5.2 Passive commutating mixer using FET (NMOS) transistors

The 0.35 μm CMOS part allowed for the implementation of a quad-FET mixer as shown in Fig. 117, right, and also helped us realising the low-gain state of the LNA (see Fig. 94). The mixer uses a quad-FET ring mixer consisting of 4 NMOS transistors, 0.35 μm $\times$ 150 μm each [65] (Fig. 117, right). The mixer's RF is fed to the ring via a passive transformer. The transformer at the LO port is substituted by a high gain limiting amplifier similar to Fig. 113: A differential BJT pair transforms the single-ended input (-10 dBm) into a differential one which is subsequently amplified and limited by a balanced chain of 3 NMOS/PMOS inverters with increasing MOS width. Due to the high impedance of the FET gates a rail-to-rail signal at the LO port of the ring mixer is achieved with just 4 mA at 400 MHz and 6 mA at 800 MHz. While in the diode mixer the IF is derived at the centre tap of the RF transformer, a 2nd transformer at the IF side is necessary for the FET mixer. If a balanced IF filter is available, the signal can be routed to the IF IC

in a balanced configuration, eliminating the need for this transformer. The layouts of the ICs are shown in Fig. 7. As can be seen from Fig. 119, the measured linearity reached

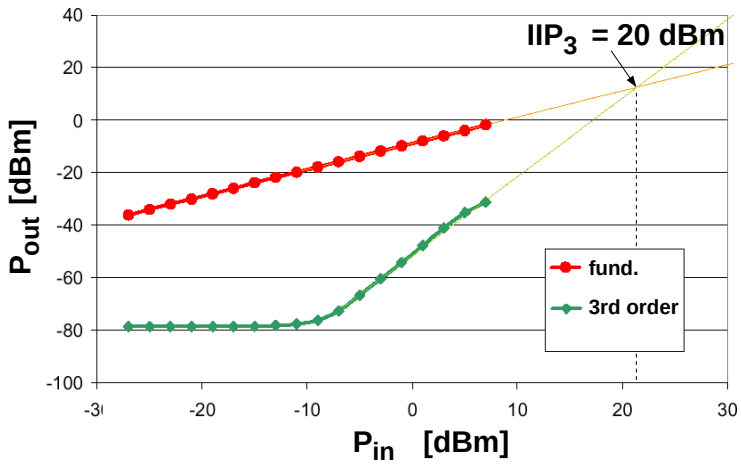


Figure 119: Measured IIP_3 of the FET mixer of Fig. 117, right [239].

+20 dBm in the first shot.

7.6 The Gilbert mixer: An active, commutating mixer

Systems integrated monolithically often use a topology called the Gilbert mixer, which dates to the mid-1960's [240, 241]. The Gilbert cell mixer is a commutating mixer, where *currents* are commutated rather than *voltages*. The RF input stage transforms the input voltage into currents which are then fed to the commutating unit and further to the IF load. Due to this, the mixer exhibits conversion gain rather than the 6 - 8 dB conversion loss of passive commutating mixers. This RF input stage, however, sets fundamental limits to the attainable dynamic range. Furthermore, it does not provide an accurate match to the source, so impedance-transformation methods are required. Usually resistor or transistor current sources are used to bias the RF input stage. A transistor current source with resistive series feedback requires a voltage drop of around 1 V, a resistor current source can reduce that drop the several hundreds of mV. To further reduce this voltage drop, in the design used for the IS-95 CDMA mixer in the American PCS band (1930 MHz - 1990 MHz), the high impedance current source was replaced by an LC tank L_t, C_t, resonating at 1.95 GHz. This allows for maximising the headroom for the IF tank (L_1, C_1 and L_2, C_2) in order to achieve maximum linearity. The simplified schematic is shown in Fig. 120. Inductive emitter degeneration L_a, L_b is used for the input stage Q_1, Q_2 in order to achieve a high linearity at low noise figure and to minimise voltage drop. L_a, L_b are realized in form of a symmetrical, centre-tapped inductor (see Fig. 61, section 5.17) The local oscillator is fed from pins V_{lo}, V_{nlo} to the switching quad Q_3 - Q_6 from a limiting buffer amplifier. Fig. 121 shows results of a harmonic-balance simulation

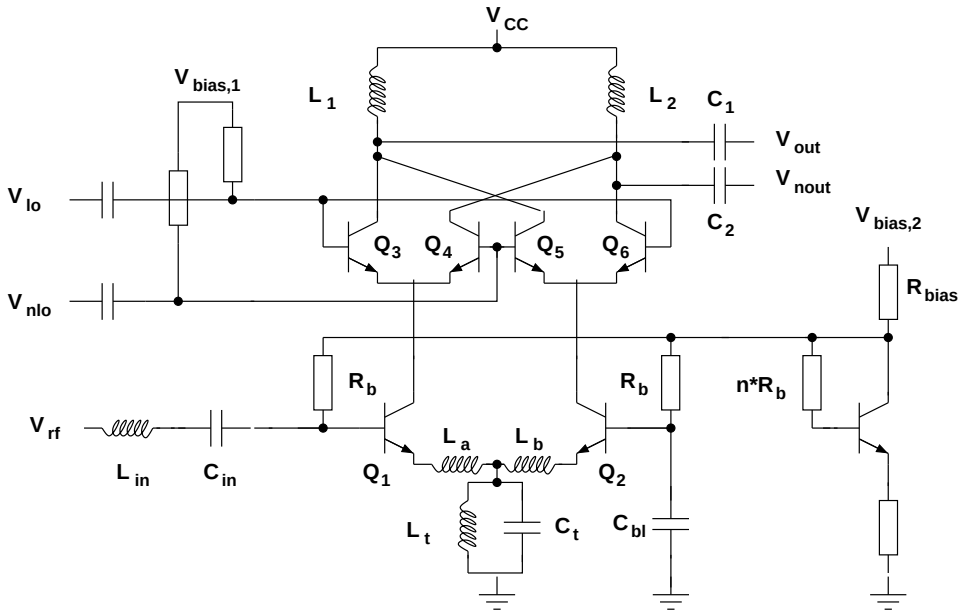


Figure 120: Inductively degenerated Gilbert cell mixer with LC tank L_t, C_t as current source.

for different LO drive levels, using a sinusoidal and a rectangular LO drive. It is evident that the rectangular LO drive, at a given drive level, leads to lower noise figures and higher gain than the sinusoidal LO drive. A value of 400 mV_{pp} (100 mV single-ended LO amplitude) is sufficient to achieve 16.5 dB of gain and 6.8 dB NF. This agrees well with the measured values in Fig. 122. This shows that hard-switching with a minimum cross-over time (where the four transistors of the switching-quad are balanced) is more effective than using a sinusoidal LO. The mixer is driven from a single-ended RF source, which is the SAW filter in the CDMA front end (see Fig. 11). The other port of the emitter coupled pair is AC grounded by C_{bl}. A series inductor L_{in} is used to provide impedance transformation to 50 Ω. The current source (LC tank) could also be placed asymmetrically, e.g. at the emitter of Q_2. However, in that case the DC voltage drop across the series resistance of L_a, L_b would lead to differences in base-emitter voltage for Q_1 and Q_2, which would be difficult to compensate. The measured values are shown in Fig. 122 for $V_{CC} = 2.75$ V, $f_{LO} = 1.75$ GHz at -6 dBm and $f_{IF} = 200$ MHz. Using 13 mA of current (mainly in the mixer stage itself), a N=3:1 transformer at the output (450 Ω load) and a high impedance LC tank, the mixer achieves a conversion gain at room temperature of 16 dB with a NF of 7.0 - 7.5 dB which is in good agreement with the simulated values in Fig. 121. The input-referred 3rd order interception point is an excellent +4 dBm, which leads to an output-referred IP_3 of +20 dBm. This is considerably higher than the OIP_3 of the commutation FET mixer (13 dBm) in Fig. 119. The noise figure of 7 dB is comparable to a passive mixer (right).

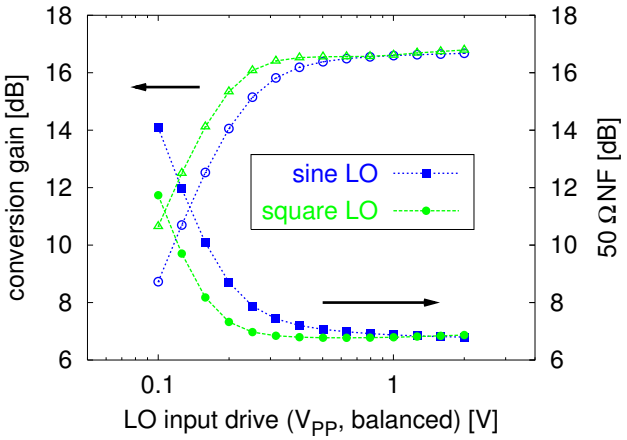


Figure 121: Conversion gain and NF of the Gilbert mixer show in Fig. 120.

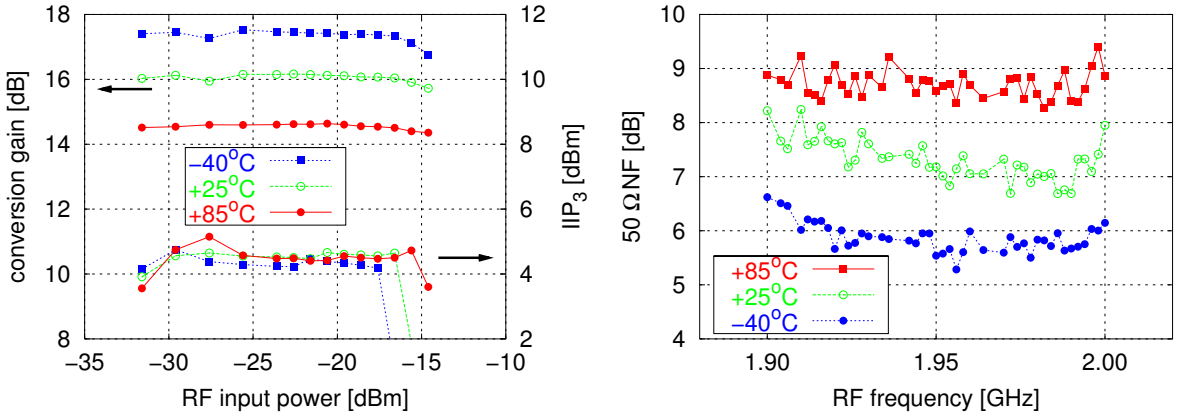


Figure 122: Left: Conversion gain and IIP_3 of the CDMA mixer. Right: NF.

Therefore, active Gilbert cell mixers are widely used in portable devices like cellular and corded phones, GPS receivers, and WLAN due to their ease of integration (requires just BJTs or MOSFETs + passive components), the low LO drive requirements (400 mV_{pp}, balanced) and the high conversion gain at moderate NF. The drawback compared to a passive mixer is the lower input-referred IP_3, which limits the amount of LNA gain that can be used in front of the mixer. This leads to a higher overall NF of the system.

7.7 Image rejection mixers

For low-cost applications like WLAN (see section 2.4), DCR or image reject (IR) mixers are used in order to save an external RF SAW filter. A single mixer downconverts both

the actual signal (RF) and its image, located at the opposite side of the LO frequency, to the same IF frequency, thus making the signal information indistinguishable from any interferers in the image band. In the presence of a weak image signal the signal quality is deteriorated and a strong image can even completely overrun the signal. The image-reject mixer based on the Hartley architecture [272] is widely used in recently published receivers, e.g. [27, 273, 274, 275]. It is a single-sideband mixer which downconverts the RX signal and suppresses the signals at the image frequency to a certain extent. A high image suppression relaxes the requirements on the RX filter. In an image-reject mixer the signal is fed to two identical mixers, which in turn are driven by LO signals which are 90° out of phase[39]. If the IF signals of one mixer are again shifted by 90° and added to the in-phase IF signals in a summation amplifier, the image frequency is suppressed and the RX signal doubled in amplitude. The weakness of the Hartley principle is in the difficulties of the phase shifter implementation. To obtain an image suppression of 40 dB, a phase error of only 1° or an amplitude imbalance of up to 0.1 dB can be tolerated [27]. External 90° hybrids in the IF path have been used in the literature [27], which is not acceptable in a product due to the increased bill-of-materials. Polyphase RC - CR filters have been used extensively to provide quadrature [27, 274, 276, 275]. Since the amplitude and phase errors of 1-stage RC - CR filters are highly sensitive to absolute variations of the R and C values, multi-stage polyphase filters with a loss of 6 dB per stage are required [273]. A 2-stage filter is a good compromise between conversion loss, phase accuracy and amplitude balance versus RC variations [273, 275] (Fig.123).

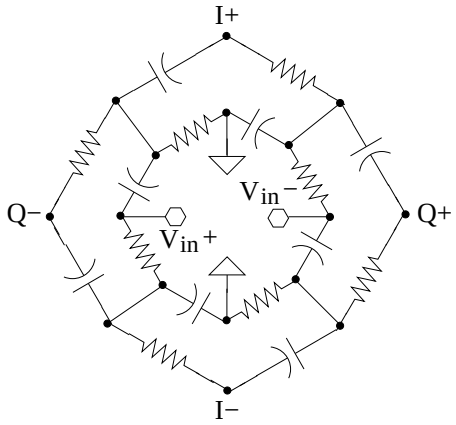


Figure 123: 2-stage polyphase filter for quadrature generation.

While there is no alternative to the polyphase circuit in the IF (or RF) path due to linearity considerations, this circuit is not the optimum solution for providing LO quadrature: In order to obtain optimum performance, the polyphase filter needs to be driven by a sinusoidal LO signal, however LO signals are usually square waves due to a limiting

[39]Instead of providing quadrature in the LO path, the RF signals can be phase-shifted. Due to noise figure and linearity considerations, this variant is rarely used, however.

amplifier. In addition, the 12 dB conversion loss requires two completely identical buffer amplifiers to boost the LO signals back to the 400 mV_{pp} required to drive the Gilbert-cell mixer (see section 7.6). Alternatively, quadrature VCOs have been used to obtain in-phase and quadrature signals directly at the expense of a larger chip area and higher power consumption [264, 277, 124, 278, 33]. Finally, frequency dividers can provide quadrature while acting as limiting amplifiers at the same time. As this solution requires a VCO in the range of 9 - 12 GHz for the WLAN radio, frequency doublers have been used to circumvent this [27]. Frequency doublers, however, are known to produce even harmonics (besides the target frequency) and DC offsets. As can be seen in Fig. 125, this has a detrimental effect on the phase error. Furthermore, each frequency doubling process is associated with an increase in close-in phase noise by 6 dB, which is another argument against this. The circuit used in this thesis therefore consists of a fully integrated X-band VCO, a frequency divider, a broadband modified Gilbert-cell mixer and a 2-stage polyphase filter in the IF branch. The divide-by-two acts as a phase shifter and improves the close-in phase noise by 6 dB, however for a fair comparison it needs to be noted that MMIC VCOs at higher frequencies show inherently higher phase noise due to lower resonator Q and higher 1/f noise of the faster transistors which are required. In order to cover the various WLAN bands in Europe, Japan and the US, broadband operation was achieved by using a fully integrated X-band VCO at 10 GHz in conjunction with a master-slave divider rather than using a polyphase filter or a quadrature VCO for generating the 0°, 90°, 180° and 270° LO signals. While consuming less chip-area than competing solutions, we achieved an excellent image suppression of 40 - 45 dB without any post-tuning. This values were obtained by minimising the content of even harmonics in the VCO output spectrum. The modified Gilbert mixer with a common-base input stage allows for a broadband RF operation from 2.5 - 6 GHz at a low supply voltage of 3 V. The block diagram of the fully integrated receiver is shown in Fig. 124.

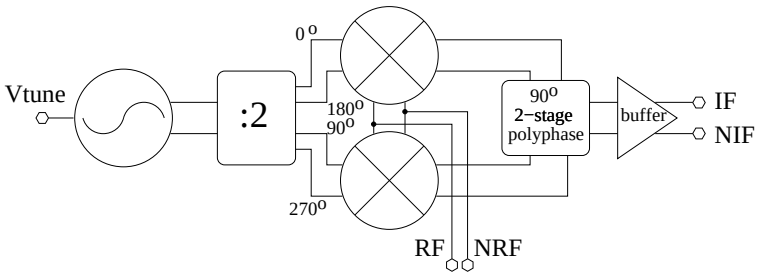


Figure 124: Block diagram of the 5 GHz WLAN receiver

The balanced X-band VCO is followed by a digital divide-by-two using master-slave flip-flops realized in emitter-coupled logic to deliver the in-phase and quadrature signals while providing amplitude limiting at the same time. IF phase shifting is done by a 2-stage polyphase RC - CR filter centred at an IF of 500 MHz. A buffer amplifier allows the circuit to be measured on-wafer in a 50 Ω environment. In Fig. 125 the process of quadrature generation is depicted: While one flip-flop triggers on the rising edge of the input signal,

the other triggers on the falling edge. What designers are often not aware of is the fact that a phase difference of 90° can only be obtained, if the duty-cycle of the input signal is exactly 50 %, which is equivalent to the absence of DC offsets and even harmonics in the VCO signal.

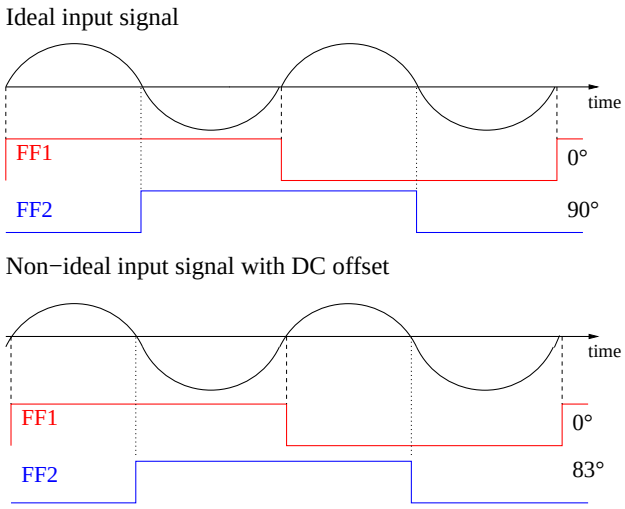


Figure 125: Input signals to the divider with a duty cycle of 50% lead to ideal quadrature outputs (top), while signals containing even harmonics and DC offsets (bottom) lead to phase errors.

While DC offsets may be removed by capacitive coupling, even harmonics can only be suppressed by a balanced circuit design and a very symmetrical layout. The VCO itself uses a standard capacitively cross-coupled topology [279] with a core current of 9 mA in conjunction with a symmetrical, centre-tapped inductor and pn tuning diodes.

The IQ mixer in Fig. 126 is a modified version of the classical Gilbert-cell mixer [240]: In order to achieve broadband operation and a constant input impedance versus frequency, transistors $Q_1 - Q_4$ are operated in a common base configuration, blocked by capacitor C_1. To minimise the external component count, resistive loads associated with a large voltage drop have been used rather than an LC tank centred at the IF. In order to allow for 3 V operation, headroom was gained by the use of an LC tank which is centred at 5.5 GHz and acts as the current source. A symmetrical spiral was used in order to minimise chip area. Q_0 together with $Q_1 - Q_4$ form a current mirror, where the resistor R_0 compensates the resistive voltage drop in L_{1a}, L_{1b}. It is imperative to have as good mutual matching between the two mixers as possible for achieving a high image reject ratio. Therefore a common input stage was used for the I and Q mixer, which minimises parasitic capacitances at the input, too. The exactly identical tail currents are then steered to the individual switching quads using a current mode approach. As V_{BE} matching is essential for $Q_1 - Q_4$, the HBTs are drawn very close to each other in the die layout (Fig. 127). The mixer core consumes 8 mA from a 3 V supply.

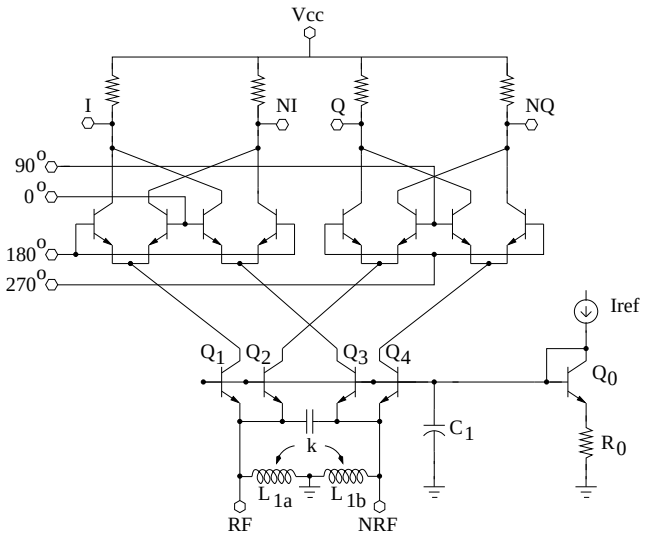


Figure 126: Simplified schematic of the IQ mixer using a common base input stage and an LC current source.

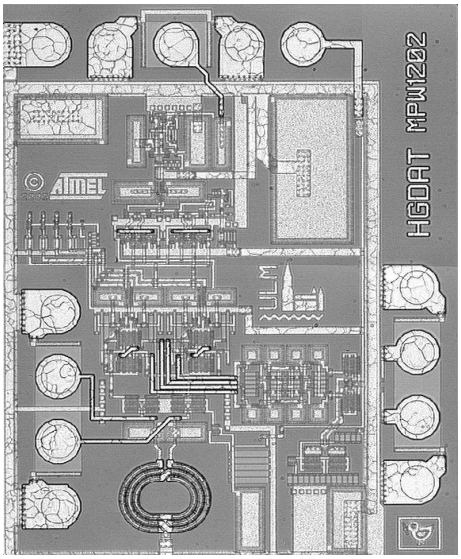


Figure 127: The layout of the WLAN IR mixer (bottom left) with LO frequency divider (top) and IF polyphase filter (right) is extremely compact and measures just 700 μm $\times$ 760 μm (including pads).

The measurements have been performed using on-wafer probes. In order to facilitate characterization, the VCO has been realized separately with its own output buffer (measuring just 275 μm $\times$ 275 μm, excluding pads) and the divider was driven using a synthesizer via a dedicated single-ended-to-differential amplifier. VCO measurements using a double-arrow 180° hybrid combiner showed that the critical 2nd harmonic is suppressed by more

than 50 dBc. The tuning range of the VCO is 600 MHz and the output power is 2 dBm and very uniform across a 6" wafer (Fig. 128). Mixer measurements have been performed

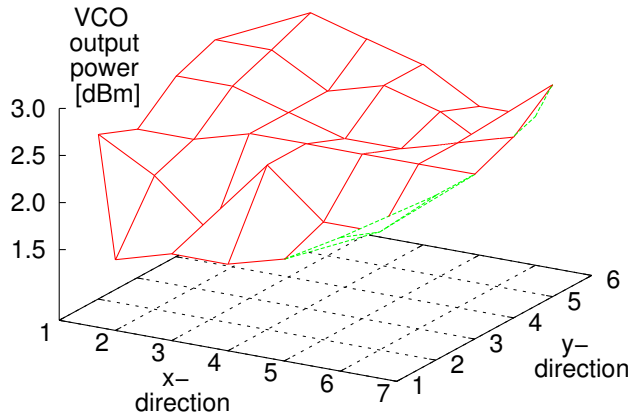


Figure 128: Mapping the output power of the 10 GHz VCO across the wafer reveals the high uniformity of the production-line SiGe technology.

using a VNA with frequency translation mode. The RF input was driven with by a 2 - 8 GHz double-arrow 180° hybrid combiner with a phase error of less than 5°. Sweeping the IF frequency at a fixed LO frequency of 10 GHz / 2 using LO low-side injection showed that the 2-stage polyphase filter is exactly centred at 500 MHz. An image suppression of 45 dB was achieved without any post tuning (Fig. 129). The image suppression is nearly independent of the LO input power to the divider. The gain of the IR mixer including the 12 dB loss of the polyphase filter ranges from 5 dB at f_{IF} = 100 MHz to -5 dB at f_{IF} = 1000 MHz. Sweeping the RF frequency from 2.5 GHz to 6 GHz shows a very flat gain response and an image suppression of more than 40 dB in the frequency range of interest (4.9 - 5.5 GHz) (Fig. 129, right). The image rejection is therefore equal or better than the 29 - 40 dB reported in literature (e.g. [274]). It is equal to the result of [275] which, however, uses a 3-stage polyphase filter and operates at a much lower RF frequency of 700 MHz. We achieve comparable results like the work in [27] which uses an off-chip IF hybrid and tuning in the LO phase shifters.

7.8 Mixer summary and conclusions

For high-volume applications requiring a high level of integration, the Gilbert mixer is the optimum choice for a high linearity mixer. Using optimised circuit design techniques, an output-referred IP_3 of +20 dBm at 1.9 GHz has been reached with 16 dB of gain (section 7.6). This OIP_3 is considerably higher than the +13 dBm of the NMOSmixer

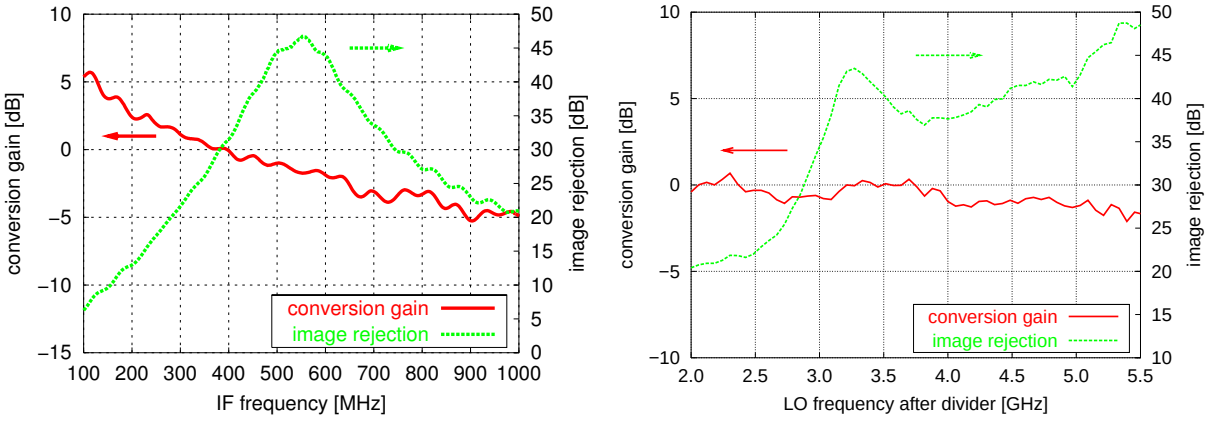


Figure 129: Left: Conversion gain and image suppression versus IF frequency for f_{LO} = 10 GHz / 2. The polyphase filter is centred at an IF of 500 MHz. Right: Conversion gain and image suppression versus RF frequency at an IF of 500 MHz.

(section 7.5.2). The drawback of the Gilbert mixer is, that only moderate system noise figures can be achieved. The reason is not the noise figure of the mixer itself (which reached an excellent value of 7 dB) but the limited amount of LNA gain that can be used in order not to compress the mixer: According to the noise formula of cascaded networks, an active mixer's noise figure contributes more to the system noise figure compared to a passive mixer that can tolerate a higher LNA gain due to its higher input-referred IP_3. For special high-linearity applications like short-range automotive radar, the LNA is even skipped and the antenna directly fed to the Gilbert mixer [280].
Image reject mixers have a higher noise figure but save cost as they do not require a SAW or BAW filter for image suppression.
Passive mixers are used in high end applications like base stations, PMR terminals and long-range automotive radar. At microwave frequency (e.g. in 24 or 77 GHz radar applications), the diode mixer frequency shows undefeated performance. These diodes, however, use dedicated Silicon or GaAs Schottky processes. Integration of Schottky diodes into a standard SiGe process was not successful, not even for a 400 MHz application (section 7.5.1). For this application, the NMOS mixer is the optimum choice due to the easy integration into a standard CMOS process and the low LO power drive level requirements.

8 Conclusion

This thesis was carried out at the Competence Center for Integrated Circuits at Ulm University. It is a response to the high requirements in linearity of systems like UMTS, CDMA, GPS, TETRA and WLAN compared to its predecessors and arises from the demands for higher data rates and higher cell capacities. Several development projects within the department targeted receive front-ends with high linearity. While the specifications varied slightly, the need of new design techniques was common to all these projects. So rather than concentrating on *one* such system, this work reviews available circuit architectures and linearization techniques and chooses the methods best suited for each problem. All circuits have been designed using production line Silicon-Germanium bipolar and BiCMOS processes of Atmel Heilbronn (now TELEFUNKEN Semiconductors [1]) and Atmel Colorado Springs.

Theoretical considerations, extensive simulations and measurements showed that SiGe HBT technology – despite its exponential current-versus-voltage characteristics – offers higher linearity than pHEMT at low current consumption. For a given supply current, the most linear SiGe HBT LNA uses a single-stage cascode design with narrow band reactive load and inductive series feedback. In order to achieve a high 3rd order intercept point (IP_3) in the two-tone test, the difference frequency (often called 'beat frequency') needs to be shorted properly. Different low-frequency termination techniques like broadband source termination, LC trap networks, inductive bias networks and active bias networks based on operational amplifiers have been evaluated and the optimum solution was chosen, depending on the application. For very narrowband applications, cancellation of intermodulation products by using capacitive parallel feedback can be exploited, leading to high IP_3. All realised LNAs have been benchmarked with published results and are close to the theoretical optimum in linearity.

Both passive mixers and active Gilbert cell mixers have been optimised with respect to linearity. For systems where the interferers appear out-of-band of the SAW filter between LNA and mixer, an optimised Gilbert cell mixer is generally the best compromise in system noise figure, linearity and power consumption. For systems with strong in-band jammer (e.g. professional mobile radio terminals), a NMOS ring mixer with high peak-to-peak LO drive shows high input-referred linearity and allows for high LNA gain resulting in a very low system noise figure.

Accurate models of passive on-chip components were critical for the success of this work, and therefore one chapter is dedicated to the characterization, simulation and modeling of planar structures on Silicon. Starting from investigations for repeatable on-wafer calibrations and measurements, different 2.5D and 3D EM simulators have been evaluated and it has been shown that a planar inductor on silicon is not a 2-dimensional electromagnetic problem: Accurate simulation results for inductance and quality factor can only be obtained when taking into account current crowding effects between the metallisation layers, modelling the current flow in their actual physical thickness. Choosing the correct input parameters for the simulator is more important than selecting a special vendor's software. Different closed-form equations for inductance calculation have been evaluated

and good agreement has been found, even for 'historic' work. By that, scaleable inductor models, accurate in both inductance and quality factor, have been derived for the SiGe1, SiGe2-RF and SiGe2-Power design kits.
For the future, highly integrated RF CMOS tranceivers will dominate all mass-market applications, allowing for lower supply voltages (1.2 . . . 1.8 V instead of the 2.7 . . . 3.3 V used in this thesis). SiGe HBT technology will find niche applications in front-end modules and responds to this demand with higher device speeds (> 100 GHz) and lower parasitic capacitances by improved isolation techniques, allowing for simple common emitter stages instead of cascode designs used in this thesis. This niche applications, however, will not enable sufficient volume for state-of-the art 8 inch SiGe HBT and SiGe BiCMOS wafer fabs. Currently dominated by GaAs HBT and pHEMT technology, automotive radar at 22 - 29 GHz and 77 - 81 GHz (for short-range applications) and 76 - 77 GHz (for long-range radars) will switch to SiGe HBT for cost and reliability reasons and higher integration levels [280, 281, 282, 283]. Thus, automotive radar will be the next killer application for SiGe HBT technology.

Frank J. Gruson, June 2010

Acknowledgement

At this point I would like to thank my supervisor Prof. Dr.-Ing. Hermann Schumacher for his support and advice since October 2000. He handled many administrative tasks silently in the background, which allowed me to focus on my technical work. He was always there to discuss technical questions when necessary.
I am grateful to Prof. Dr.-Ing. Joachim Burghartz, head of the Institute of Nano and Microelectronic Systems at the University of Stuttgart, for serving as assessor and for reviewing this voluminous thesis in detail. Thank your for your advice and the excellent discussions we had.
The team at the Competence Centre for Integrated Circuits at the Ulm University assisted me in many ways: I am especially grateful to Kai Boris Schad, Ertugrul Sönmez and Ferdinand Sigloch for their assistance in all computer and software related problems. Ursula Spitzberg assisted me in on-wafer RF measurements. Sven Hettich designed and populated most of the PCBs and he did a great job in supporting me within the SUPERSTAR project.
The amount of people that supported me at Atmel in Heilbronn and Ulm barely fits onto this page: I appreciate many excellent discussions with Dr. Günther Bergmann, Dr. Udo Karthaus, Holger Schulz and Dr. Uwe Erben. The layout teams supported many of my designs and I would like to give my tanks to Jacqueline Lückert, Irene Logemann, Petra Bögel and Siggi Semmler in Ulm and Martin Averweg in Heilbronn. Dr. Andreas Schüppen, Harry Dietrich, Dietrich Zerrweck, Peter Brandl and Dr. Jürgen Berntgen did a great job in running the SiGe wafers and provided me with an abundant amount of silicon (germanium), assisted by Dr. Wolfgang Schwerzel and Klaus Gratzke who cared for wafer logistics – thanks ! It is impossible to count the number of ICs which Gerhard Kutscher and his team in Heilbronn and Dieter Griesinger in Ulm packaged for me. Many thanks to Matthias Bopp and Winfried Rabe for managing the research projects.
The cooperation with the Boston Design Center of TriQuint Semiconductors was a real pleasure for me. I enjoyed working with you guys and my special thanks go to Xinwei Wang and Wen Chen. I spent a wonderful summer in Boston in 2002 and I would like to thank Greg Henderson and Dilek Barlas and their families for that.
To all those people whom I have not named explicitly or inadvertently left out, thank you.
This work would not have been possible without the full support of my family and I would like to thank Heike for her continued support and encouragement. The understanding of Sarah and Theresa that their dad spent innumerable evenings, weekends and holidays for his thesis was extremely helpful. Finally, I would like to thank my parents that enabled me to pursue my technical studies and always supported me.

Frank J. Gruson, June 2010

Method	Suitable applications	Advantage	Disadvantage
Gain Method	Very high gain or very high NF	Easy setup, very accurate at measuring very high NF, suitable for any frequency range	Limited by spectrum analyzer's noise floor. Cannot handle DUTs with low gain & NF.
Y Factor Method (using Spectrum Analyser)	Wide range of NF	Can measure wide range of NF at any frequency regardless of gain	When measuring very high NF, error could be large.
Y Factor Method (using a Noise Figure Meter)	Super low NF	Convenient, very accurate when measuring super low NF (0 - 2 dB)	Expensive equipment, frequency range limited

Table 24: Three methods of measuring noise figure [285].

A Noise figure measurements

A.1 General considerations

Although professional equipment for measuring noise figure is available since more than 50 years, NF measurements are still tedious and the result is often frustrating and unreproducible. J.C. Greene in his satirical article *"Noisemanship – The Art of Measuring Noise Figures Nearly Independent of Device Performance"* [284] already noted in 1961, that noise figure measurements can yield very high values (e.g. when measuring NF on competitor's devices) or very low values (preferably when measuring your own devices). In today's competitive environment where NF differences of less than 0.1 dB decide about a design win, Greene's conclusions are true now more than ever. The following appendix gives an overview about noise figure measurement techniques.
For measuring noise figure, there exist at least three methods [285] which are depicted in table 24. All methods work for amplifiers, where input and output frequency are the same, as well as for frequency translating devices like mixers. As the LO's contribution to the noise figure is not removable by any kind of calibration, it is very important to use a generator of high spectral purity and low phase- and AM-noise (e.g. tube oscillator or quartz-oscillator) [286]. For poor LO-generators, a narrow-band filter yields a significant improvement.

A.2 The Gain Method

Noise factor F and noise figure NF contain the important information about the noise performance of an RF system. The basic definition is [209]:

$$\begin{aligned} F &= \frac{[\text{Total } \textit{output} \text{ noise power}]}{[\textit{Output} \text{ noise power due to input source only}]} \\ NF &= 10 \cdot \log(F) \end{aligned} \tag{96}$$

The Gain Method – which requires just a frequency source and a spectrum analyser – directly uses this definition:

- The noise power at the output N_{out} is measured.
- Assuming that the input noise is purely thermal noise, due to Brownian motion, the available noise power of the input source is $k_B \times T \times \Delta f$ where $k_B = 1.38 \cdot 10^{-23} J/K$ is Boltzmann's constant, T the absolute temperature in Kelvin and Δf the bandwidth of the noise receiver (noise bandwidth in Hz). By definition, all noise figure values are referred to $T_0 = 290\,K = 16.8°C$ and thus the noise power density (per 1 Hz) is -174 dBm/Hz. Adding the system gain we obtain the output noise power due to the input source only.

Thus we have the following equation:

$$\begin{aligned} NF = 10 \cdot \log(F) &= N_{out} - [-174 \text{ dBm/Hz} + 20 \cdot \log(BW) + \text{gain}] \\ &= ND_{out} + 174 \text{ dBm/Hz} - \text{gain} \end{aligned} \tag{97}$$

if ND_{out} is the measured noise density at the output per 1 Hz. To use the "Gain Method" to measure the noise figure, the gain of the DUT needs to be pre-determined. Then the input of the DUT is terminated with the characteristic impedance (50 Ω for most RF applications, 75 Ω for video/cable applications). Then the output noise power density is measured with the noise marker of a spectrum analyser. The "Gain Method" can cover any frequency range covered by spectrum analyser. The biggest limitation comes from the noise floor of the spectrum analyser: The low noise amplifiers developed in this work feature noise figures between 0.5 and 2 dB with gains between 10 and 20 dB. This would require the measurement of noise densities at the output of the DUT in the range of -160...-150 dBm/Hz, which is below the noise floor of most spectrum analysers. The "Gain Method" is therefore suited for systems with either high gain or high noise or both (table 24).

A.3 The Y Factor Method

Due to the low noise figure of the devices realized in this thesis, noise figure measurements are done using the Y-factor method [287], which uses a noise source with a known excess noise ratio (ENR), typically an avalanche diode [209] followed by an attenuator. The

ENR describes the difference in noise temperatures between 'hot' (noise source ON) and 'cold' (noise source OFF) [287, 288, 289, 285].

$$ENR_{(dB)} = 10 \cdot \log\left[\frac{T_h - T_c}{T_c}\right] \tag{98}$$

Using this technique, noise figure is measured by injecting an accurately known amplitude of noise T_h into the amplifier (DUT) and finally into a receiver (see Fig. 130). This is compared with injecting ambient temperature noise T_c into the same setup.

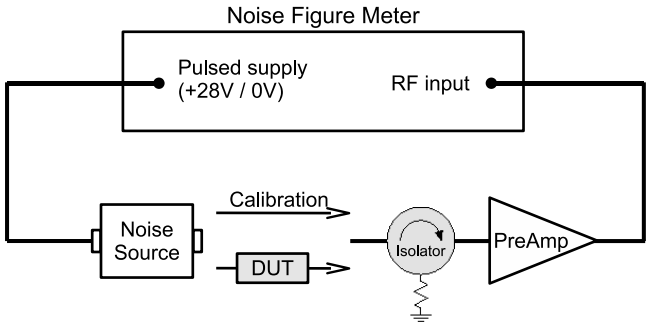


Figure 130: Setup for RF noise measurements [290].

As the noise source in OFF state – due to the built-in attenuator – represents a pure 50 Ω resistor, ENR is easily converted to noise spectral by the following equation [289]

$$-174 \text{ dBm/Hz} = 0 \text{ dB ENR} \tag{99}$$

The ENR of the noise source is tabulated at spot frequency points throughout the specified frequency range and is interpolated in between these frequency points. For the input noise temperatures of T_h and T_c, the measured output noise powers are referred to as N_h and N_c, respectively. These two noise powers, when expressed as a ratio, represent the Y-factor value given by

$$Y_{Fact} = \frac{N_h}{N_c} \tag{100}$$

The noise figure is then calculated by [285]

$$NF_{(dB)} = ENR_{(dB)} - 10 \cdot \log\left(Y_{Fact} - 1\right) \tag{101}$$

In space applications, instead of NF often equivalent noise temperatures are given. Such an equivalent input noise temperature T_e can be assigned to the DUT via its (linear) noise factor F using the equation

$$F = 1 + \frac{T_e}{T_0} \quad \text{with} \quad NF_{dB} = 10 \cdot \log(F) \tag{102}$$

Automated equipment like the hp8970B noise figure meter or a spectrum analyser with noise figure personality (see table 24) is available to record the Y-factor versus frequency, to calculate the gain as well as F, T_e and NF and to perform the 2nd stage error correction which corrects the measured noise temperature by the influence of the noise figure equipment [288].
From Eqn. 101 it is evident that the accuracy of the noise figure measurement is only as good as the accuracy of the calibrated ENR value of the noise source, specified by the supplier with an error of ± 0.15 ... ± 0.18 dB. The accuracy of the noise receiver for measuring the ratio of the noise powers (Eqn. 100) can be as low as ± 0.05 dB [291, 292]. Each noise figure measurement is therefore associated with an unavoidable measurement error in the order of at least ± 0.2 dB, which is mainly due to the uncertainty of the ENR calibration data [287]. If the measurement was not done properly, the measurement error can easily be higher. The following precautions are necessary:

- Spectrum analysers with noise figure personality may be used to measure noise figures (see table 24, middle). While spectrum analysers are excellent devices to cover a power range of 80 dB with medium accuracy, they are not optimised to measure the ratio of two power levels with high accuracy. *Agilent* gives a total error of 0.24 - 0.46 dB for its spectrum-analyser based NF measurement system (including the ENR impreciseness of the noise diode) [293]. Noise figure analysers (see table 24, bottom) like the hp8970B should be preferred over spectrum analysers, as they are linearised and optimised for the limited power range of a noise figure measurement.

- The signals delivered by the noise source to the DUT are extremely small. To prevent the DUT picking up interferers, the measurement environment needs to be shielded by a Faraday cage against radiation from fluorescent lamps, computer and measurement equipment, nearby basestations or TV and radio transmitters. Swept measurements should be preferred over fixed frequency measurements in order to identify such interferers.

One of the most important contributions to measurement accuracy is a good match (low VSWR) between the noise source output and the device connected to it (DUT or test setup) [290, 286], an error which becomes especially pronounced at noise figures below 6 dB (Fig. 3 in [287]). During measurement, a small amount of noise power is reflected at the DUT input (or at the test setup during calibration) (see Fig. 131).

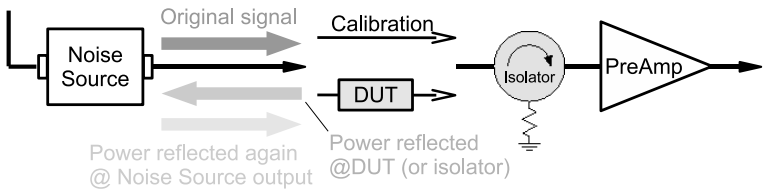


Figure 131: Reflected power during noise figure measurements [290].

Some of this reflected power is reflected again at the noise source output with unpredictable phase, thus changing the measured power of the signal in an uncertain way. The preferred setup for noise figure measurements at RF frequencies is shown in Fig. 130. The isolator and preamplifier are added to reduce measurement uncertainty. An isolator like the one shown in Fig. 132 reduces reflected power between the DUT and the test setup and makes sure that the noise figure meter sees exactly the same impedance during calibration (DUT removed) and NF measurement (DUT in place). This is vital when removing the influence of isolator, preamplifier and noise figure meter during the 2nd stage error correction. The preamplifier reduces the noise figure of the test setup. This preamplifier is often integrated into the noise figure meter, but in the case of the hp8970B has a noise figure of 6 - 9 dB. As isolators are inherently narrowband, for the wideband case it is reported to replace the isolator with a low VSWR attenuator of approximately 6 to 10 dB [286]. This was not done in our measurements, as the attenuator results in an increased NF of the measurement system, and therefore increases the influence of the 2nd stage error correction. Instead, a low noise preamplifier with excellent wideband input match S_{11} was designed (section A.4). The high reverse isolation of the device makes S_{11} insensitive against mismatch of the noise receiver (see figure 135).

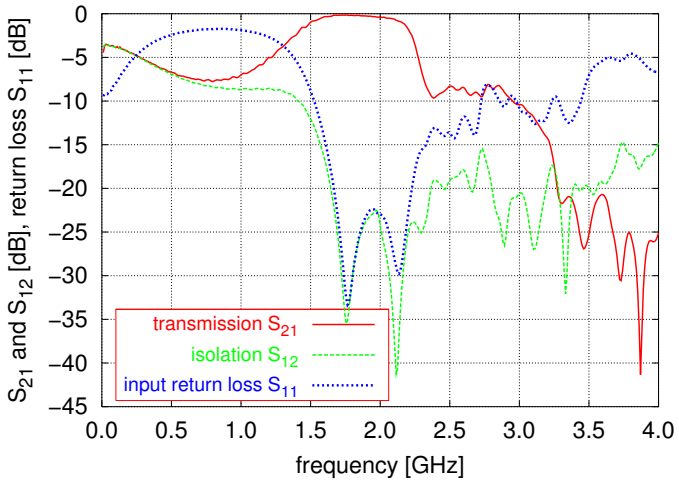


Figure 132: Due to the high isolation, isolators provide excellent input match (>23 dB) independent of the output load, while attenuating the signal by as little as 0.3 dB (Ditom D3C0120 isolator, 1.7-2.0 GHz).

Noise sources are commonly available with nominal ENR values of 15 dB and 6 dB. In the 15 dB source, the raw ENR of the GaAs avalanche diode of typically 25 dB is attenuated by 10 dB, in the 6 dB source by approximately 20 dB [289]. The 6 dB source therefore shows a return loss of at least 40 dB, independent from the noise diode being 'on' or 'off'. This means that there is less difference in impedance between 'hot' and 'cold ' compared to the 15 dB source. If the noise source changes impedance when turned on, the DUT sees a different excess noise than is calibrated for the noise source [290]. Therefore it is

Expected Noise Figure [dB]	Noise Source Nominal ENR	Typical NF Uncertainty [dB]	Typical Gain Uncertainty [dB]
0 to 10	5	± 0.24	± 0.83
10 to 20	10		
20 to 35	15	± 0.41	± 0.83

Table 25: Rule of thumb for ENR versus expected noise figure of the DUT [289] and typical measurement uncertainties of a commercial measurement setup (10 MHz-3 GHz) [293].

necessary to use a 5 - 6 dB ENR noise source when measuring noise figures up to about 10 dB and particularly to minimise measurement uncertainties

- when the noise figure of the DUT is very low and the DUT is sensitive to changes in source impedance (e.g. has a large equivalent noise resistance R_n).

The use of a source with low ENR has the following advantages:

- Errors due to non-linearities within the noise figure meter are reduced, if the difference in noise power between *hot* and *cold* (Y_{fact}) at the instrument is lower (note that $Y_{fact} - 1$ is always lower than the ENR, see equation 101).
- Many automatic noise figure analysers switch attenuators in order to handle higher noise power levels. This increases the NF of the measurement system and the influence of the 2nd stage error correction will be more pronounced. With a low ENR source the instrument will use less attenuation, resulting in a lower instrument noise figure. The influence of the 2nd stage error correction will be lower, which reduces measurement uncertainty (see table 25). Using a 15 dB noise source together with a 10 dB pad instead of a 5 - 6 dB noise source is possible [286], but the uncertainties of ENR and pad attenuation sum up in this case.

A.4 Improving measurement accuracy by a low-noise preamplifier

The disadvantage of noise diodes with low ENR is that the noise signal might be too low for the noise figure meter, especially if the DUT has a low amplification (e.g. the TETRA/TETRAPOL LNA in low gain mode). In that case the noise figure meter cannot choose the voltage swing to be in the optimum linearity range of its voltage detector as it needs to switch its IF attenuators to the state with the lowest attenuation. To overcome this problems, a broad band, low noise preamplifier for the hp8970B noise figure meter has been designed under the following constraints:

- The gain should be flat across the frequency range of 0.3 - 3 GHz.
- A good input match is required to allow for broad band measurements without using isolators or at frequencies where isolators are difficult to get (e.g. < 800 MHz)
- In order to make this input match independent from the match of the noise figure meter, a high reverse isolation is required so that $S_{21} \cdot S_{12} \ll 1$. This in turn leads to a stable amplifier with high Rollett factor, which is a desirable side effect.
- The noise figure should be well below the noise figure of the hp8970B (6...9 dB) in order to lower the cascaded noise figure considerably.
- No attempt was made to optimise the large signal behaviour ($P_{1\,dB}$ and IIP_3).

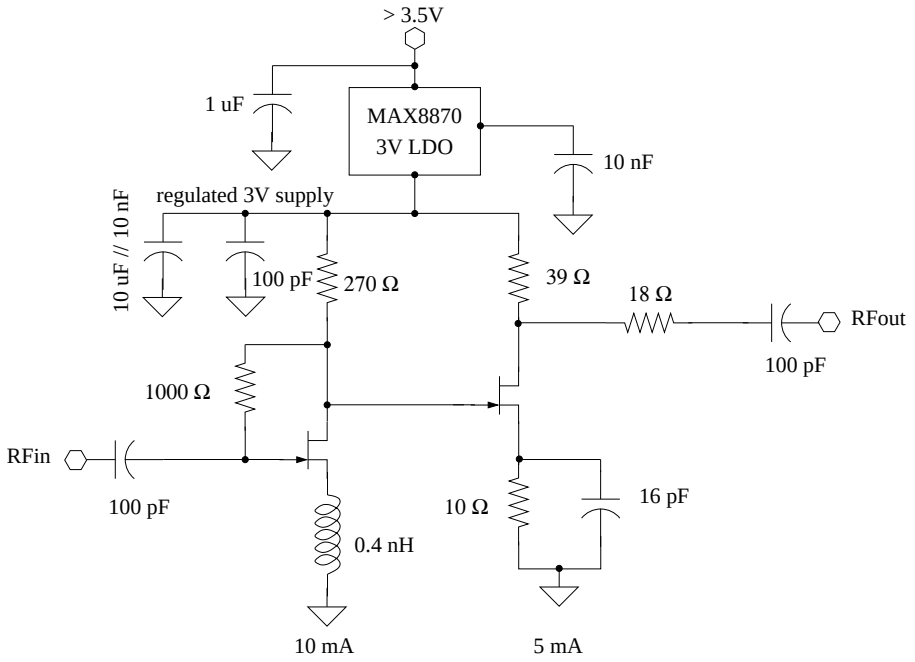


Figure 133: Broadband pre-amplifier for the hp8970B noise figure meter realized using e-PHEMTs.

State-of-the-art 0.15 μm enhancement-mode, pseudomorphic GaAs HEMTs (e-pHEMTs) available from *Agilent Technologies* with the type number ATF-551M4, housed in a thin miniature leadless package with low lead inductances were used in the design, as the low input capacitance of FETs allows for a broad-band design [294, 255, 87]. Resistive parallel feedback was used in the first stage for achieving a good broadband input match. In order not to deteriorate the low NF of the e-pHEMTs too much ($NF_{min} = 0.41$ dB @ 2 GHz for 10 mA and 2.7 V with 17.9 dB of associated gain), the feedback resistor was maximised under the S_{11} constraint, resulting in a value of 1 kΩ at a 270 Ω load. Inductive source degeneration of 0.4 nH, realized as a short line on the 0.5 mm thick RO4003 substrate,

helped to move Γ_{opt} towards 50 Ω. The resulting low-pass behaviour was compensated by a 2nd stage with high-pass characteristics. Excellent broad-band output match was achieved by the 39 Ω load in conjunction with a 18 Ω series resistor (Fig. 133). This 2nd stage does not use any parallel feedback in order to achieve the high reverse isolation. The parallel feedback of the 1st stage together with the 270 Ω load sets the current to 10 mA with a 3 V supply voltage. The second stage is DC coupled to the first stage and the 10 Ω source resistor reduces the current of this stage to 5 mA. The resulting amplifier was realized using low-cost SMD components in 0402 size and packaged into a metal housing (Fig. 134). The measured S-parameters show a flat gain of 22 dB, good reverse isolation (47 dB up to 2 GHz) and good input and output return loss (Fig. 135).

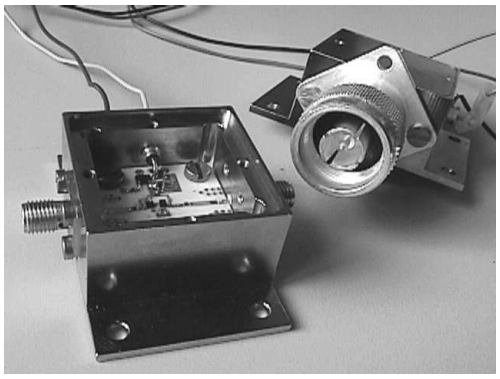


Figure 134: The preamplifer is realized on RO4003 substrate and packaged into a metal housing stuffed with either SMA or N-connectors.

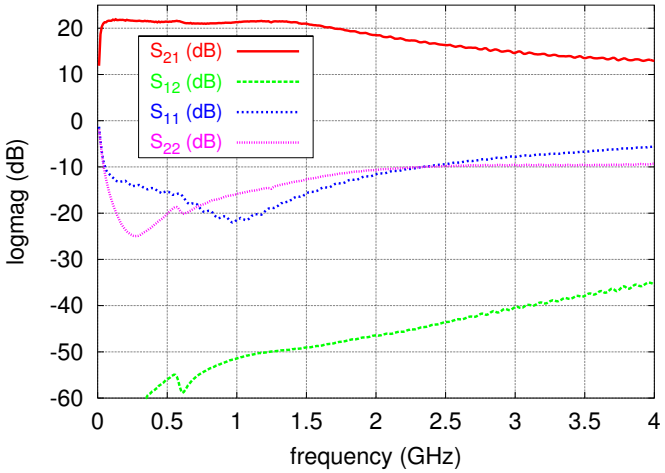


Figure 135: Measured S-parameters of the preamplifier: The circuit was optimised for a flat gain and good input and output return loss. The good reverse isolation makes the input return loss independent of the match of the following stage.

Usually a high number of averages needs to be used when calibrating the noise figure setup, as any jitter in the calibration step will add to the measurement uncertainty of all subsequent measurements [293]. Therefore a long averaging time should be used for calibration in order to reduce this source of uncertainty to a negligible level. As this preamplifier (Fig. 134) reduces the noise figure of the measurement system from 6. . .9 dB to just 1.2 dB, we got more repeatable NF results with a lower amount of averaging and even for devices with low NF and low gain: According to Friis' formula for cascaded networks [75], due to the 1.2 dB NF of our measurement setup the influence onto the NF of the DUT is small, so that errors due to the 2nd stage error correction do not play a dominant role.

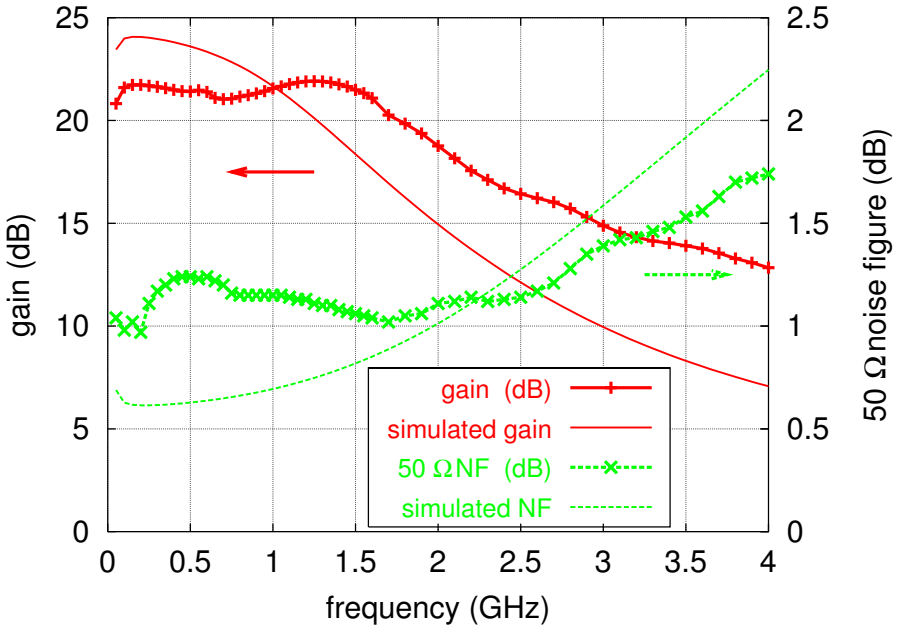


Figure 136: The noise figure of the preamplifier is flat up to 2.5 GHz and is determined by the 1 kΩ feedback resistor of the first stage (see Fig. 133).

A.5 Example

The Scuba LNA with inductive biasing is one of the DUTs with the lowest NF in this thesis. A set of measurements under different conditions has been made and plotted in Fig. 137:

- The green and the red curve show measurements with two different calibrations and using the preamplifier to the hp8970B NF meter as shown in Fig. 134. Due to the high gain of the preamp, the influence of the second order correction performed in the hp8970B is negligible and the curves are virtually identical.

- The blue curve uses a calibration, where a 1.7 - 2.1 GHz isolator (Ditom D3C0120, see Fig. 132) was inserted in between the DUT (SCUBA LNA) and the preamp. This improves the input return loss of the preamp from 10 dB to 23 dB. The results are identical to the previous curves, as a return loss of 10 dB is already good enough, especially for a DUT which has itself a high reverse isolation and the noise match at the input is absolutely independent from the output. Note that this is not the case for amplifiers with parallel feedback and hence bad S_{12}.

- Finally, the hp8970B was forced to perform its 3 calibration sweeps with IF gains of +20 / +10 / 0 dB (the settings were +10 / 0 / -10 dB before, due to the high gain of the preamplifier). Again there is no difference to the previous results, showing the excellent linearity of hp8970B's A/D converter.

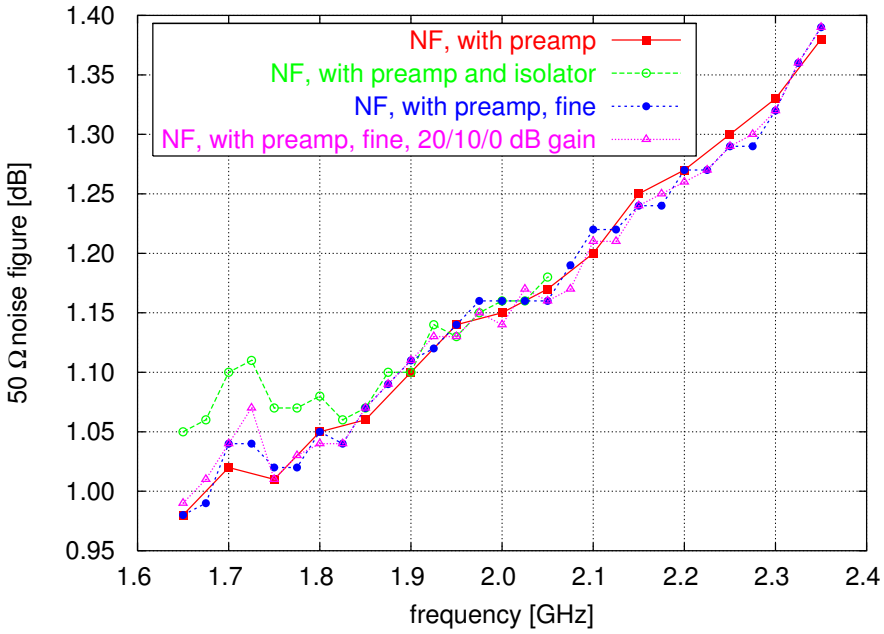


Figure 137: SCUBA LNA V22, V_{CC}=5V, 2.0 pF series cap at output. 10/0/-10 dB IF gain in hp8970B if not otherwise stated.

This investigation shows that NF measurements can indeed be reproducible and accurate, as long as some precautions are taken. It should be noted, however, that the absolute accuracy of a NF measurement can never be better than the specified ENR error of the noise diode used.

B Measuring intermodulation distortion products

B.1 Combining the sources

Linear amplifiers like the IS-98 LNA require an IIP_3 of +10 dBm to be measured with two input tones at -30 dBm, spaced by 900 kHz in frequency. According to Eqn. 12 this requires a 3rd order intermodulation distance of 80 dB! While it is easy to simulate such a scenario in a frequency domain simulator, it is a challenge for the measurement setup to accomplish this. Aside from the dynamic range of the receiver (which is typically a spectrum analyser), two very clean sources with very low spurious tones are required. Combining such sources using a matched network is typically done using a star network resistive combiner (see Fig. 138) [63, 295, 296].

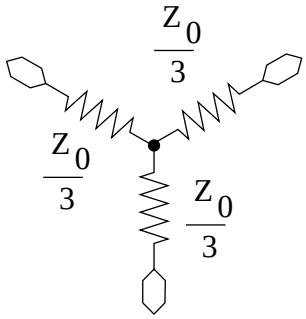


Figure 138: Using a star combiner for combining two signal generators results in a transmission loss of 6 dB and an isolation between the sources of 6 dB only.

Star combiners are broadband devices and ensure that the generators are correctly matched, but they offer only very little isolation (6 dB) between the two signal generators: The signal from the output of one signal generator will be injected into the output of the other signal generator. The presence of the signal from one generator at the output of a second generator will cause its output level to modulate [295]. If the beat frequency (tone spacing) is within the signal generator's Automatic Level Control (ALC) bandwidth the signal generator will try to remove it by generating AM onto the desired signal, thus cancelling the intermodulation caused by the foreign signal. This results in the signal generator no longer producing a single signal at the required frequency, but also producing side bands (beat nodes) at an offset from this signal [63]. As this offset is equal to the difference between the desired and unwanted signals this makes those ALC distortions indistinguishable from intermodulation products that may be generated by the device under test. There are several ways in which the test setup can be altered in order to minimise these distortion problems:

- Isolation between the two sources can be enhanced by including an isolator between the combiner and the signal generators. Adding only little to the transmission loss

from the source to the combiner, it prevents signals being reflected back into the sources [63]. These devices, however, are inherently narrowband and under certain conditions they may generate their own intermodulation products.

- Reactive, hybrid combiners can be used in place of resistive combiners. The device which was used in most of the measurements of this work was the ZESC-2-11 from mini-circuits [297] (see Fig. 139). Due to its broadband nature, it is assumed that this hybrid is based on transformers using ferrite cores similar to the 6 dB hybrids presented in [295]. Despite of being a low-cost part, it offers significant advantages over the star network of Fig. 138.

- As ferrites themselves show intermodulation at high input drive level, for amplifiers with very high linearity they should be replaced by Wilkinson-type 3 dB splitters based on air-core inductors [295] (for lower frequencies) or striplines (for higher frequencies). The drawback of this devices is their limited bandwidth.

- For mixer testing, a low pass filter should be inserted between the combiner and the device under test to reduce harmonic levels. Any harmonic distortion from the mixer is indistinguishable from that of the generator [63, 295, 296].

B.2 Setting up the spectrum analyser

Spectrum analysers produce intermodulation products if operated incorrectly [63]. When choosing a proper analyser, the intermodulation free dynamic range needs to be considered. As a rule, spectrum analysers are designed to operate at their best with -30... -40 dBm at the analyser's mixer input. This means that increasing the internal attenuation needs to be considered. As the attenuation level is increased so the noise floor rises and potentially hides any intermodulation products. The measurement bandwidth must therefore be reduced in order to reduce the noise floor [63]. As a quick check, if the intermodulation product displayed by the analyser is real, its level relative to the carrier will not be affected by slightly varying the input attenuation of the spectrum analyser. When working with very low input levels, the input attenuation may be decreased. As the mixer of the spectrum analyser typically is poorly matched, at least 6 dB of attenuation is required to provide sufficient return loss to the DUT. This is especially true for the narrow-band LNAs developed in this work, as their IP_3 is very sensitive with respect to changes in the load.

B.3 Using a frequency translating vector network analyser

From October 2002, a vector network analyser with frequency translation mode was available [298]. This allows to sweep the input frequency quickly over the frequency band, while the analyser records one of the fundamental output tones and one of the intermodulation

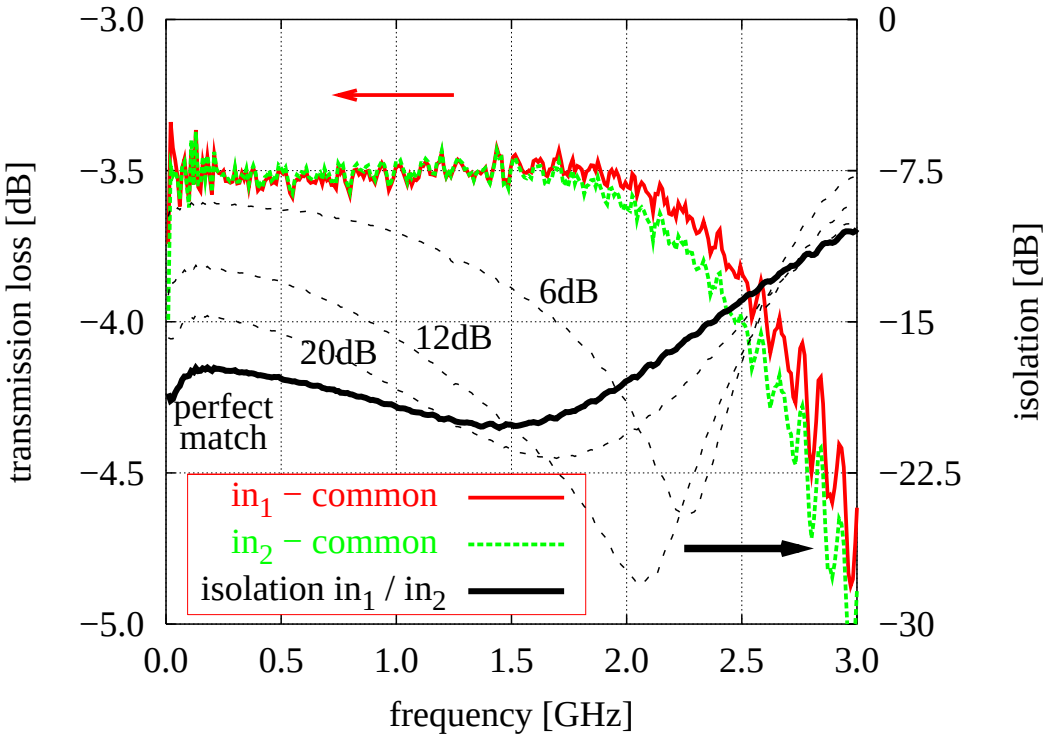


Figure 139: Hybrid combiners show transmission losses close to the theoretical value of 3 dB. The isolation for this low-cost 0 - 2000 MHz part (ZESC-2-11) is better than 15 dB, provided that the common port is matched to better than 20 dB.

tones. Care needs to be taken to check that the worst case intermodulation distance is used if the DUT shows some asymmetry here.

C On-wafer characterisation of inductors - the measurement challenge

C.1 Getting the right contact

When performing on-wafer measurements, the biggest problem initially was to get adequate contact on the aluminium pads. This pads form a thin layer of naturally, insulating aluminium oxide as soon as they are exposed to the atmosphere. Depending on how much overtravel was used, the Picoprobe or Cascade air-coplanar probes slid on the pads, leading to arbitrary values for the series resistance and the Q-factor in turn. While the standard wafer probes are made from an alloy of beryllium and copper to provide good electrical contact on gold pads, special probes existed with harder tungsten tips for aluminium pads. Despite of the considerable higher price of these probes, the problem remained the same, as tungsten also oxidises and the aluminium and aluminium oxide accumulates on the probe tips after a few contacts, significantly increasing the contact resistance and hence resulting in poor measurement repeatability. Finally, the pads of numerous wafers were electroplated with a thin layer of nickel gold to allow for good contact. Now reproducible measurements were possible, leading to consistent results. In 2003, a breakthrough in probe tip technology occurred, when Cascade Microtech announced a series of wafer probes called 'Infinity probes' [299]. The revolutionary feature of these tips was that rather than scratching away the oxide, they puncture it by using very sharp tips ($12 \times 12 \mu\text{m}^2$) at the end of an otherwise blunt probe. This small size and the required small overtravel minimises the damage to the aluminium pad. Claiming a typical contact resistance below 0.05 Ω on aluminium pads, they also allow to reduce the diameter of the pads to below 40 μm, which reduces pad capacitance and hence the error when de-embedding the pads from the DUT (see section C.3). In addition, the construction of the coaxial-to-microstrip transition confines fringing fields more tightly than conventional flexible coplanar tips. Better field confinement reduces unwanted coupling to nearby devices or other probe tips and thus allows to shrink the separation between individual devices. As can be seen in Fig. 38, this new series of wafer probes, on non-plated pads, delivered nearly the same Q-factor as a conventional probe on gold plated pads.

C.2 Influence of the coaxial calibration technique

Using my simplified 'Thru' de-embedding technique, which is described in section C.3, I compared 4 different types of *full 2-port* on-wafer calibration procedures which all led to identical values for the inductance, but varied in the results for the quality factor Q (see Fig. 140):

- *SOLT-hp* denotes the SOLT calibration procedure as built into Agilent's hp8510C vector network analyser. For the common SOLT ('Short', 'Open', 'Load', 'Thru')

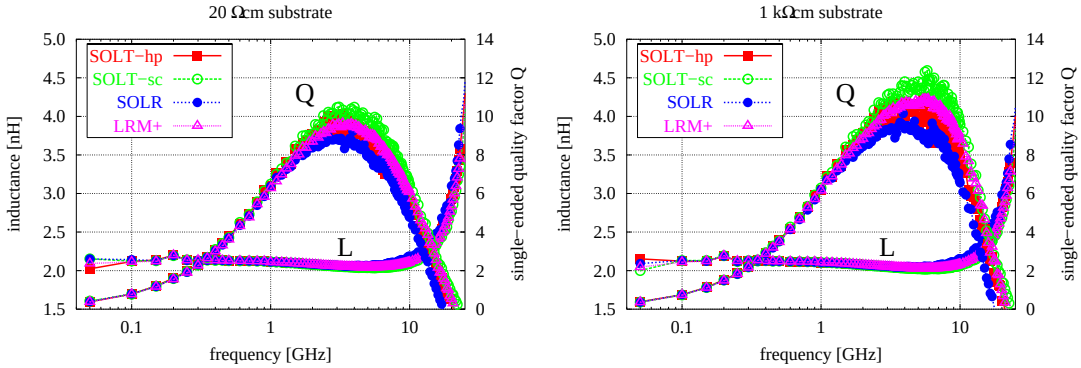


Figure 140: Four different calibration methods lead to four different values for the Q factor. For 20 Ω·cm substrate (left) the differences are less pronounced compared to the 1 kΩ·cm substrates shown on the right. Süss Microtec's LRM+ calibration yields the smoothest Q curves.

calibration [300, 301, 302] all of the standards must be fully known and specified [303]: The 'Open' has a capacitance (often negative) and 'Short' and 'Load' are inductive. It performs reasonably well if accurate models of calibration standards can be determined, which is typically the case below 26 GHz. These parameters are, however, subject to the exact placement of the probes onto the standards by the operator, so reproducibility is the biggest problem of this technique. Another problem arises, when the user designs its own calibration standards and needs to determine the parasitic networks himself (Fig. 144). Nevertheless, the 8510's SOLT calibration was used in most of the measurements in this work, as more advanced calibration software was not available before the final phase of this thesis.

- *SOLT-sc* refers to the same SOLT procedure, but coded in Süss Microtec's SüssCal software [304].

- *LRM+* ('Line', 'Reflect', 'Match') uses the same standards as SOLT, but does not require a careful specification of the 'Short' and the 'Open' used as reflect standards [305]. The reflect itself just requires $|S_{11}| = 1$ and may be either an 'Open' or a 'Short'. LRM only requires the specification of the 'Thru' delay and loss, and the DC resistance of one 'load' standard, which sets the impedance of the calibration (in contrast, SOLT uses the impedance of the 'Thru' to determine Z_0). The result is that LRM+ is less sensitive to probe standard overtravel. In addition it solves the "Ports Asymmetry" problem caused by the slightly different values of the two laser-trimmed match (load) elements. LRM+ is the version as patented by Süss Microtec. This calibration technique delivered the smoothest curves and shows a good long-term stability of the calibrated VNA.

- *SOLR* ('Short', 'Open', 'Load', 'Reciprocal') does not need any knowledge of the 'Thru', except the fact that its *reciprocal* ($S_{21} = S_{12}$ when driven with the same port impedance) [306, 307]. This technique is especially useful if measurements are performed with the probe tips oriented in an angle other than 180°.

Often standards are probed after the calibration is completed in order to verify the calibration quality. To ensure that one performs a calibration *verification* and not a connection *repeatability* test, standards need to be used that are different from those used during the calibration process [308]. For that purpose, 200 Ω shunt resistors have been realised on lossy silicon within GSG on-wafer structures.
The most accurate on-wafer calibration method, the TRL calibration (a method by the U. S. National Institute of Standards and Technology), was not used in this work, as it uses multiple transmission lines as standards (e.g. three lines for a calibration from 2...18 GHz) and cannot perform measurements down to zero frequency. In addition, its standards need to be on the same wafer as the DUT, which is difficult on silicon due to the high transmission line losses [303, 305]. Calibrations techniques like LRRM [300] with automatic load inductance calculation are beyond the scope of this thesis.
From Fig. 140 its hard to say which calibration is the *best*. SOLT shows different results, depending whether SüssCal is used or the 8510C's built-in routines. SüssCal's LRM+ shows the smoothest Q-curve and thus has the lowest systematic errors. Anyway, the lesson to be learnt here is that the quality factor cannot be determined more accurately than ±10% for a 2 nH inductor on silicon, as it is influenced by the slightest changes in S-parameters. This can also be seen in Fig. 141, where the frequency dependence of the extracted series resistance is plotted, which is closely linked to the Q-factor. Above the frequency of peak-Q, the behaviour of R_s is completely undetermined: SLR with the lowest Q-value (Fig. 140) extracts the highest R_s (Fig. 141), SOLT as implemented in SüssCal yields the highest Q-value and extracts the lowest R_s.

C.3 Pad removal techniques (de-embedding)

Prior to the extraction of the inductor's equivalent circuit, the parasitic elements of both pads and feed lines need to be subtracted from the measured inductor data, a procedure often referred to as *de-embedding* (see Fig. 143). De-embedding is especially important for small inductors and the associated error can be minimised by using the smallest pads and shortest feed lines that can be realised practically. De-embedding usually starts with stripping the pad parasitics from the device-under-test (DUT). As the pads are in parallel to the inductor itself (see Fig. 142), the Y-parameters of the pads add to the Y-parameters of inductor & feed line. Therefore, the pads can be removed by subtracting the Y-parameters of the pads (measurement of an 'Open' structure, which includes only the pads) from the Y-parameters of the inductor measurement (including pads), a method called *pad removal* [309]. The pads finally used for inductor characterization are a shrinked version of the low-noise pads used in the LNA design of section 6 and are shielded to

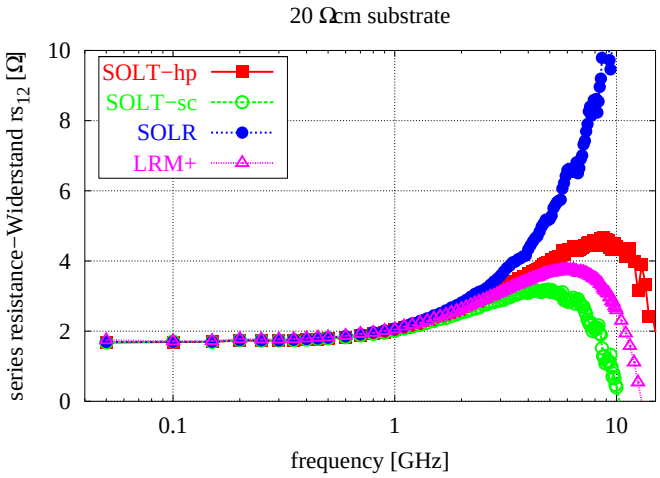


Figure 141: Frequency dependence of the extracted series resistance for 4 different *full 2-port* calibration techniques.

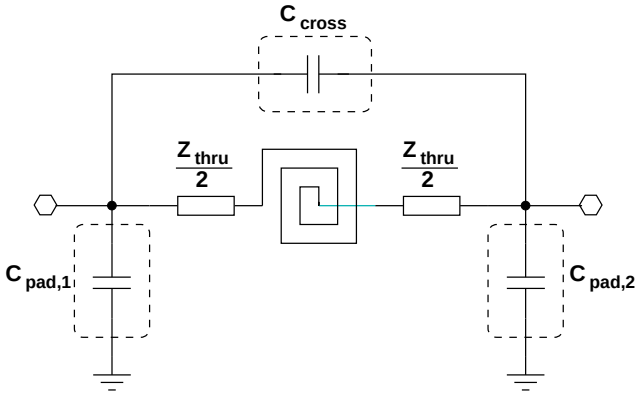


Figure 142: Pad removal and de-embedding of the feed lines.

ground with a silicided poly layer, giving a reactance which is purely capacitive and very reproducible. This leads to better reproducibility in the subsequent de-embedding process. Starting with 60 μm pads for the conventional probes (pad capacitances in the order of $C_{pad,1} \approx C_{pad,2} = 40\,\text{fF}$), this value dropped to $C_{pad,1} \approx C_{pad,2} = 15\,\text{fF}$ when the small contact area of the 'Infinity' on-wafer probes allowed to shrink the probe pads to 40 μm in diameter[40]. The crosstalk is usually extremely small ($C_{cross} < 0.2\,\text{fF}$). To remove the parasitics of the feed line, three methods exist:

1. After pad removal from the 'Thru', the remainder is converted to Z-parameters.

[40]This is a significant improvement in measurement accuracy, as the substrate capacitance of a 2 nH inductor itself is in the order of 15 fF.

Z_{thru} is extracted and the Z-parameters of the inductor are obtained by

$$Z_{ind} = Z_{\{ind-open\}} - \frac{Z_{thru}}{2} \times \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{103}$$

This method, however, assumes that the feed lines consist of inductance and series resistance only and have no shunt networks.

2. To overcome this limitation, I invented a 1-step de-embedding method which disassembles the S-parameters of the 'Thru' into a π-network, where the shunt elements are the sum of pad capacitances $C_{pad,1}$, $C_{pad,2}$ plus the shunt networks of the feed line itself. These shunt networks of pads and 'Thru' are then stripped from the Y-parameters of the DUT in 1 step. The feed resistance and inductance are then removed as in Eqn. 103. Note that this method requires just the knowledge of the 'Thru' S-parameters. No measurement of an 'Open' is required.

3. The mathematically correct method starts after pad removal and expresses the feed line as a chain matrix [310, 311]:

$$\begin{array}{rcll} v_1 & = & v_2 + Z_{thru} \cdot & (-i_2) \\ i_1 & = & & (-i_2) \end{array} \tag{104}$$

The resulting $\mathcal{A}$-matrix of the 'Thru' is then

$$\vec{\mathcal{A}}_{thru} = \begin{bmatrix} 1 & Z_{thru} \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & Z_{thru}/2 \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} 1 & Z_{thru}/2 \\ 0 & 1 \end{bmatrix} = \vec{\mathcal{A}}_{thru/2} \times \vec{\mathcal{A}}_{thru/2} \tag{105}$$

In practice, $\mathcal{A}_{12}$ is $\neq 0$ due to the shunt networks of the feed line[41], but Eqn. 105 remains approximately valid if $\mathcal{A}_{12} \ll \mathcal{A}_{21}$. The $\mathcal{A}$-matrix of the inductor itself is then obtained from the pad-removed $\mathcal{A}$-matrix $\mathcal{A}_{\{ind-open\}}$ according to

$$\vec{\mathcal{A}}_{ind} = \vec{\mathcal{A}}^{-1}_{thru/2} \times \vec{\mathcal{A}}_{\{ind-open\}} \times \vec{\mathcal{A}}^{-1}_{thru/2} \tag{106}$$

Due to the complexity of the matrix inversion and multiplication, this method has not been implemented into our standard de-embedding software.

It is needless to say that the 'Thru' structure needs to have exactly the same length like the length of the feed lines of the inductors and needs to consist of the same metal combination and width. It is convenient to lay out all inductors with the same length of feed lines, which requires just one 'Thru'. However, the author has seen many test arrays, where each inductor had its own 'Thru' structure and each 'Thru' structure was useless, as it had the same *pad distance* between port 1 and port 2 as the inductor and thus was much too long. A inductor de-embedded with the three techniques is shown in Fig. 144.

[41] It can be shown that $\mathcal{A}_{12} \approx 2 \cdot Y$, where Y is the shunt conductance of the π network of the 'Thru'.

C.4 Wafer level calibration as an alternative to de-embedding

The alternative to the de-embedding procedure is to move the reference plane of the calibration to the location where the DUT is located by means of an on-wafer calibration with custom-built standards (see Fig. 143, right). This calibration can either be one of the methods sketched in section C.2 or a dedicated technique which is more suited for silicon calibration standards like TNA.

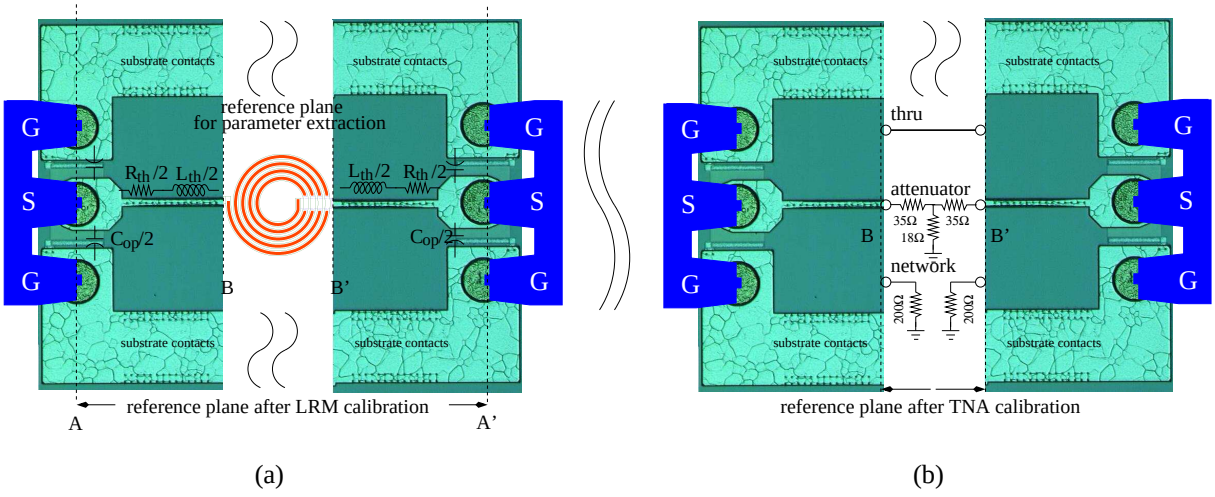


Figure 143: On-wafer measurement configuration: (a) de-embedding of pad capacitance C_P and feed elements (L_{th}, R_{th}) after on-wafer calibration using an ISS. (b) An on-wafer calibration using standards realised on silicon in the actual DUT environment eliminates the need for de-embedding (example: TNA calibration).

Several different de-embedding methods have been evaluated and the results are plotted in Fig. 144: The following techniques did not require any de-embedding, as the system was calibrated directly to the reference plane of the DUT (Fig. 143, right), using calibration standards which are integrated as small lumped elements onto the silicon:

- SOLT calibration *on silicon* (purple curve), where 50 Ω resistors, 'Open' and 'Short' are realised on-wafer in test structures at the same location where the coil is connected (similar to Fig. 143, right). This makes de-embedding of pads and feed lines obsolete, as it moves the reference plane directly to the coil itself. The drawback is that the SOLT requires the exact knowledge of the parasitics of these cal standards (see section C.2): The reference impedance is set to the value of the on-chip 50 Ω device which is not well defined, as resistor values in a typical silicon process may vary up to ±20 %, which reduces the return loss from -∞ to -19 dB. As inaccuracies in reference impedance translate directly into inductances, resistances and capacitances, this technique lacks accuracy.

- The blue curve shows an on-silicon calibration using Rohde & Schwarz's patented 'Thru-Network-Attenuator' (TNA or TAN) technique, built into its ZVX series of vector network analysers. TNA is especially suited for planar circuits and uses three two-ports as calibration elements, namely a reflectionless connection ('Thru', T), a reflectionless two-port ('Attenuator', A) with unknown transmission coefficients (S_{21} between -5 dB and -55 dB) and a symmetrical two-port ('Network', N) with unknown S-parameters, but equal reflection coefficients at VNA test ports 1 and 2 [312, 313, 314, 315, 316]. A T-attenuator with 15 dB of attenuation has been realised on silicon (Fig. 143, right). As TNA derives its reference impedance from the attenuator, resistor inaccuracies result in a similar return loss error as in SOLT: $\pm$20 % of resistor error reduces the return loss from -∞ to -20 dB, while the attenuation remains accurate within 0.1 dB. A 'Thru' connection was realised by simply connecting the feed lines of the inductors together. This results in the (required) defined electrical length, which is simply 'zero'. For the 'Network' standard any arbitrary network may be used, just featuring reflection symmetry and a reflection coefficient different from zero. The only information needed is the approximate character of the reflecting network, i.e. if it is approximately 'Open' or approximately 'Short'. In practice, already open cables or an open test fixture fulfils this requirements and thus no standard is needed. We used two 200 Ω shunt resistors. To check the calibration, 50 Ω shunt resistors have been probed. Unfortunately, due to process and layout tolerances, the 15 dB pad showed a 42 Ω input impedance. Therefore all S-Parameters had to be converted with a factor of 50/42 in order to correct the results.
  Regarding the standards required for a TNA calibration, the following advantages can be pointed out:

  1. Instead of 4 standards for the classical SOLT, just 3 standards are required (in practice, just 2 standards are necessary, as the 'Network' standard may be realised by an open cable or test fixture). This way, a 'Short' (which is not used during calibration) may be used to verify the quality of the calibration.
  2. Exact knowledge of the parasitics of the standards is not needed. For instance the 'Network' standard prevents the complicated design and description of a 'Short' or an 'Open'. Therefore, the TNA calibration procedure makes it easy to design calibration standards for special test fixtures and to verify the quality of the calibration, as just 2 standards are required which are partially unknown.

  This makes the TNA calibration ideally suited to avoid de-embedding procedures on silicon.

Fig. 144 shows the results of two different measurement approaches. For comparison, the following results have been measured using a VNA which was calibrated to the end of the probe tips using a SOLT calibration (Fig. 143, left) and differed in the de-embedding process:

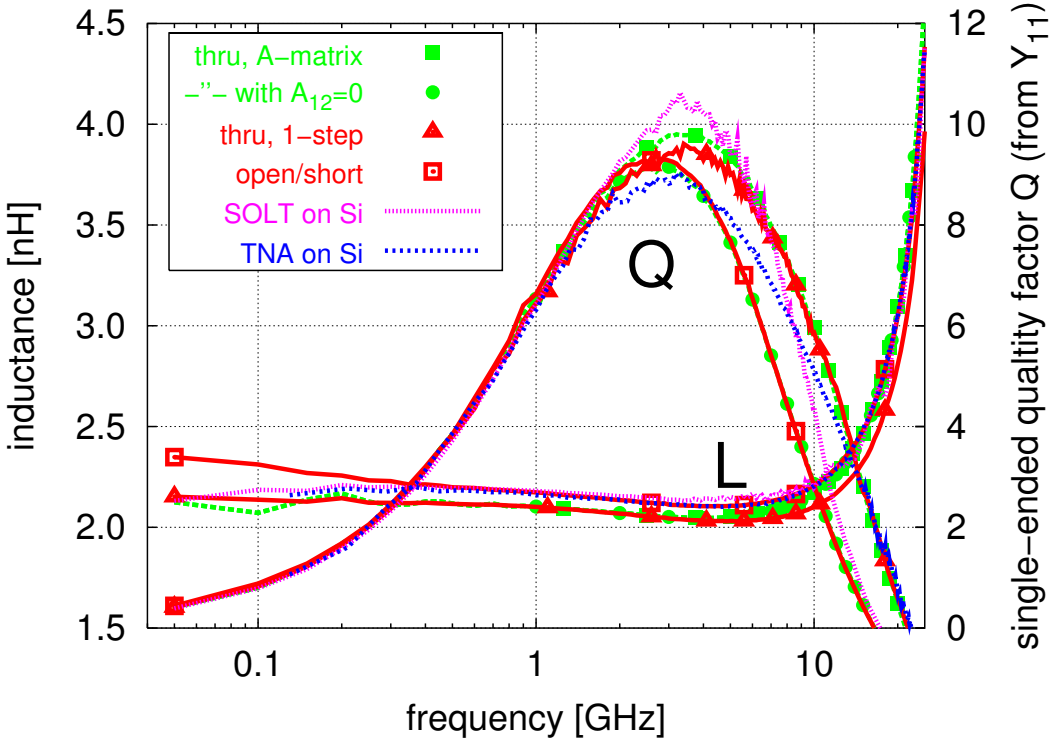


Figure 144: Different de-embedding techniques (see text).

- The green curves show a 2-step de-embedding which strips the pads using the Y-factor method (from a measurement of the 'Open') and the feed lines ('Thru') using the A-matrix method. While curve (□) uses the full A-matrix, in curve (•) A_{12} – which is 70 dB below A_{21} – was set to zero, resulting in a remarkable difference in Q. Data are taken using a SOLT calibration using laser-trimmed standards on an impedance standards substrate of type *CS-190* from Cascade MicroTech (see section C.2).

- △ refers to my 1-step de-embedding method, where the pad parasitics are taken from the shunt networks of the 'Thru' and stripped from the coil via Y-parameter subtraction. The series network (feed inductance L=0.3 nH, series resistor R=0.3 Ω, frequency dependent) are then extracted and stripped using Z-parameter subtraction. This methods requires just the S-Parameters of the 'Thru' and no 'Open' measurement is required. The result is identical to the analytically correct method using A-matrices. Calibration is as above.

- □ refers to data from the same calibration, where the pads have been stripped using 'Open'-data. However, inductance and resistance of the feed lines were not stripped using 'Thru' data, but have been extracted from 'Short' measurements. Note that these data are identical to setting $A_{12} = 0$, as both methods neglect the shunt

capacitance of the feed line (not visible in a 'Short' measurement due to the low impedance).

C.5 Choosing the right technique

Section C.2 compared different VNA error correction techniques, all using a calibration referenced to the probe tips based on a ceramic ISS. Using such a calibration, in section C.3 the reference plane has been shifted to the DUT by using different de-embedding techniques for pad-removal and feed line stripping. I found that a LRM+ calibration on an ISS, followed by a simplified 1-step de-embedding using just a 'Thru' measurement is easier to use and more consistent compared to a two-step method where first the pad-capacitances are extracted from an 'Open' measurement and in a 2nd step inductance and resistance of the feed lines from a 'Short' or 'Thru'. This 1-step 'Thru' de-embedding technique resulted in virtually the same results for inductance and quality factor like the mathematically correct treatment using the *full* transfer ($\mathcal{A}$) matrix and needs only one de-embedding structure (a 'Thru' with exactly the same length as the feed lines of the inductor). The often used 2-step 'Open/Short' method resulted in substantial differences, as it neglects the shunt parasitics of the feed lines and thus attributes them to the inductor itself, leading to a Q-factor being too small. The same error is introduced by using the technique based on a transfer matrix with $\mathcal{A}_{12} = 0$. More complex three step de-embedding techniques have been described recently [317], but we believe that our 1-step 'Thru' de-embedding technique is sufficiently accurate and at the same time easy to use. Section C.4 compared ISS- and de-embedding-based approaches to 2 wafer-level calibration techniques, which make de-embedding obsolete and avoid the errors being introduced by it. Compared to a SOLT wafer-level calibration, TNA is simple to use but still suffers from generating an accurate reference impedance using commercially available silicon processes and would require laser trimming for the resistors.

C.6 On-wafer characterisation of 3-ports

In section 5.17, symmetrical inductors have been optimised and models have been generated from EM simulated or measured 3-port S-parameters. To get 3-port inductors by on-wafer measurements using a 2-port S-parameter test-set like the hp8510C, three approaches can be used:

1. The balanced inductance and Q-factor can simply be obtained by connecting to port 1 and 2 and letting the 3rd port (*ct*) open. In this case, however, it is not possible to extract the 3 substrate networks and the coupling factor k.

2. Each symmetrical inductor can be laid out 3 times:
   (i) port 1 is terminated with an on-chip 50 Ω resistor and port 2 and port 3 are routed to on-wafer probes.

(ii) port 2 is terminated with an on-chip 50 Ω resistor and port 1 and port 3 are routed to on-wafer probes.
(iii) port 3 is terminated with an on-chip 50 Ω resistor and port 1 and port 2 are routed to on-wafer probes.
From the three 2-port measurements (2 x 2 matrices), the 3 x 3 matrix of the full three port is constructed. As, for symmetry reasons, the results of (i) and (ii) should be identical, two measurements need to be performed. As the parasitics of the 50 Ω on-chip resistor cannot be de-embedded, it needs to be as perfect as possible.

3. The same procedure as in 2.) can be used, but the circuit is laid out as a three-port and the unused port is terminated by a 3rd on-wafer probe with a coaxial 50 Ω resistor connected to it. The drawback is that this approach can only be used at low frequencies, where the parasitics of the 3rd on-wafer probe can be neglected.

Fig. 145 compares 3-port on-wafer measurements to EM simulations for three different symmetrical inductors and gets reasonable agreement.

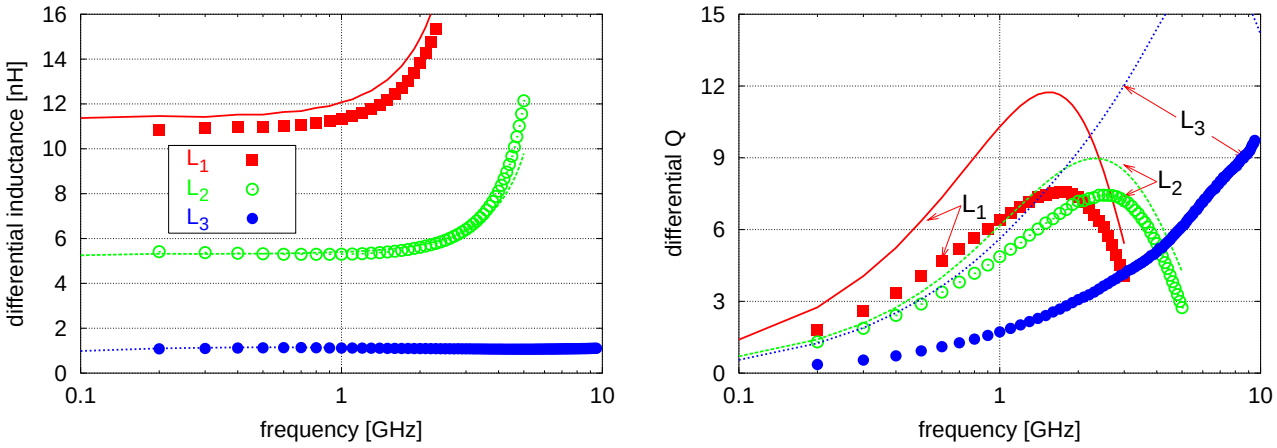


Figure 145: Inductance (left) and quality factor Q (right) of symmetrical coils when driven with balanced ports. Symbols: measurement, lines: EM-simulation.

D Details about the SiGe processes

technology	SiGe1		SiGe2-RF		SiGe2-Power		at46000	
	non-SIC	SIC	non-SIC	SIC	non-SIC	SIC	non-SIC	SIC
f_T [GHz]	30	50	50	80	33	42	35	50
f_{max} [GHz]	50	50	90	90	90	90	50	50
BV_{CE0} [V]	6	3.5	4	2.5	6.3	4.5	5.0	3.0
BV_{CB0} [V]	15	12	11	9.5	16	15.5	16.8	10.1
current gain	180		250		180		180	
base resistance [$\Omega/\square$]	1500		2200		1350		500	
substrate [$\Omega \cdot cm$]	20 or 1000		20 or 1000		1000		19	
device isolation	LOCOS		STI		STI		STI	
minimum device [μm^2]	0.8×1.2		0.5×1.2		0.5×1.2		0.8×1.6	
number of metals	2 (opt. 3)		3		3		3 or 4 + TFI	
metal pitch / spacing [μm]	5 / 3		3 / –		3 / –		1.33 / 0.49	
tungsten plugs	no		no		yes		yes	
inductor stackup	M12, M23		M23, M3		M123,M23,M3		TFI layer	
metal-TiSi cap	$1.1\frac{fF}{\mu m^2}$		opt., $1.1\frac{fF}{\mu m^2}$		no		yes[1]	
high-Q metal-metal cap	no		$0.93\frac{fF}{\mu m^2}$		$0.93\frac{fF}{\mu m^2}$		$1.1\frac{fF}{\mu m^2}$	
varactor	option		option		option		hyperabrupt	
LPNP	option		option		option		gated LPNP	
NFmin @ 1.6 GHz [dB]	0.6 – 0.8						1.2 – 1.5	
R_n @ 1.6 GHz [Ω]	6 – 8						12 – 15	

[1]double poly ($1.9\ fF/\mu m^2$) and MOS capacitors ($4.0\ fF/\mu m^2$)

Table 26: Overview of the SiGe processes used in this thesis.

Table 26 shows an overview of the SiGe processes used in this thesis. Devices with selectively implanted collector (SIC) have higher speed (f_T, f_{max}) at the expense of reduced breakdown voltage (BV_{CE0} for base at high impedance, BV_{CB0} for base at low impedance) compared to non-SIC devices. LOCOS isolated technologies separate individual devices by *LOC*al *O*xidation of *S*ilicon, while *S*hallow *T*rench *I*solation (STI) is used in more advanced processes. For the bipolar technologies, inductors are built by shunting several metal layers in parallel (e.g. M123 for a parallel combination of metal 1, 2 &3). For the BiCMOS technology, a separate *T*hin *F*ilm *I*nductor (TFI) layer exists. Lateral PNPs (LPNPs) have been used for biasing in bipolar processes, where no PMOS transistors existed. All data have been taken from [1, 99], except NFmin and R_n which have been measured by the author for a device with $94\mu m^2$ emitter area (e.g. Fig. 17) at I_C = 3 - 6 mA.

E Detailed schematics and benchmarks

Throughout this thesis, circuits have been shown using simplified circuit schematics in order to facilicate readability and make the main thoughts clear. This appendix lists detailed schematics of selected circuits including all component values.

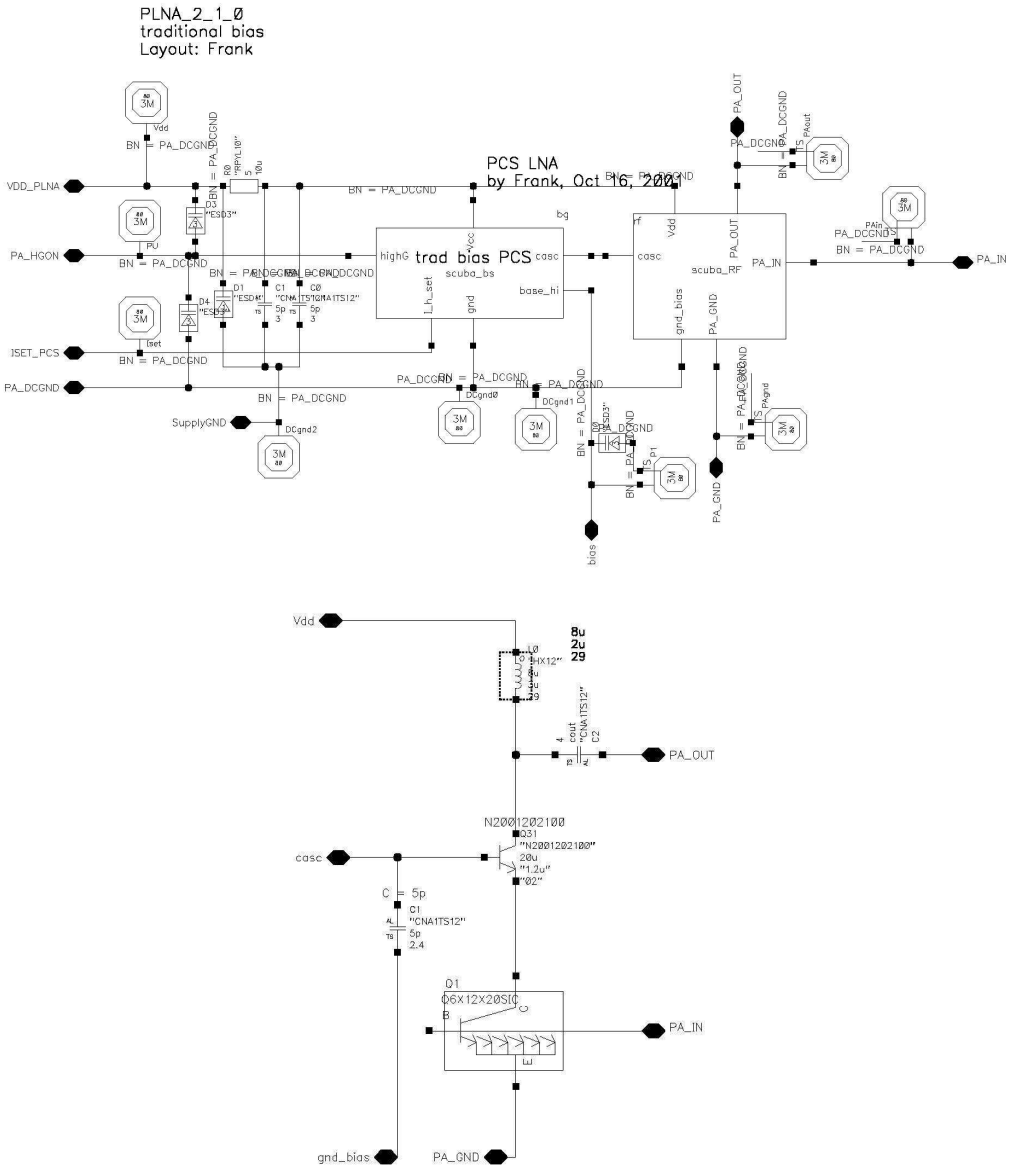


Figure 146: 1950 MHz LNA of the SCUBA receiver (MPW-run MPW0603-SiGe1): Top schematic (top), RF cascode (bottom), ...

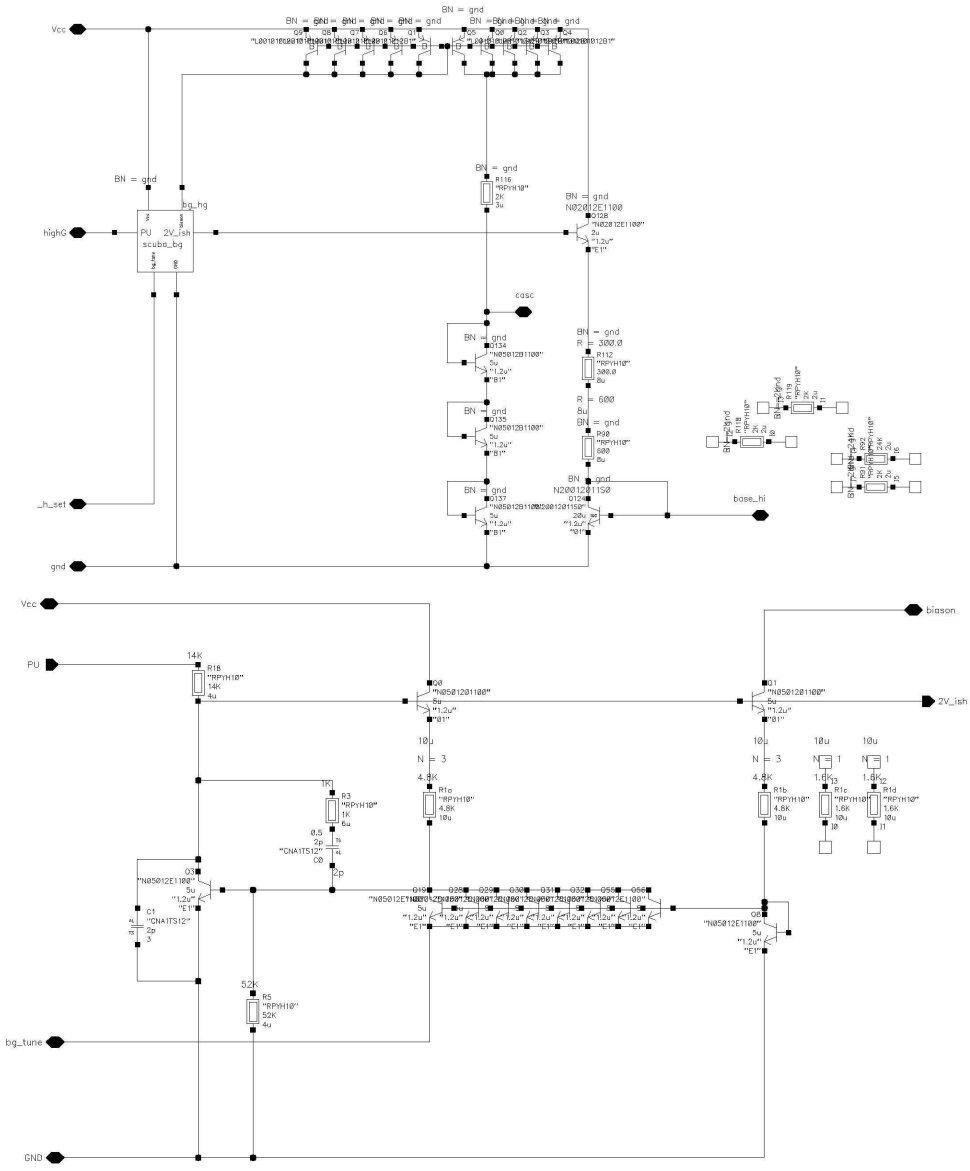


Figure 147: ... bias network (top) and Widlar bandgap (bottom).

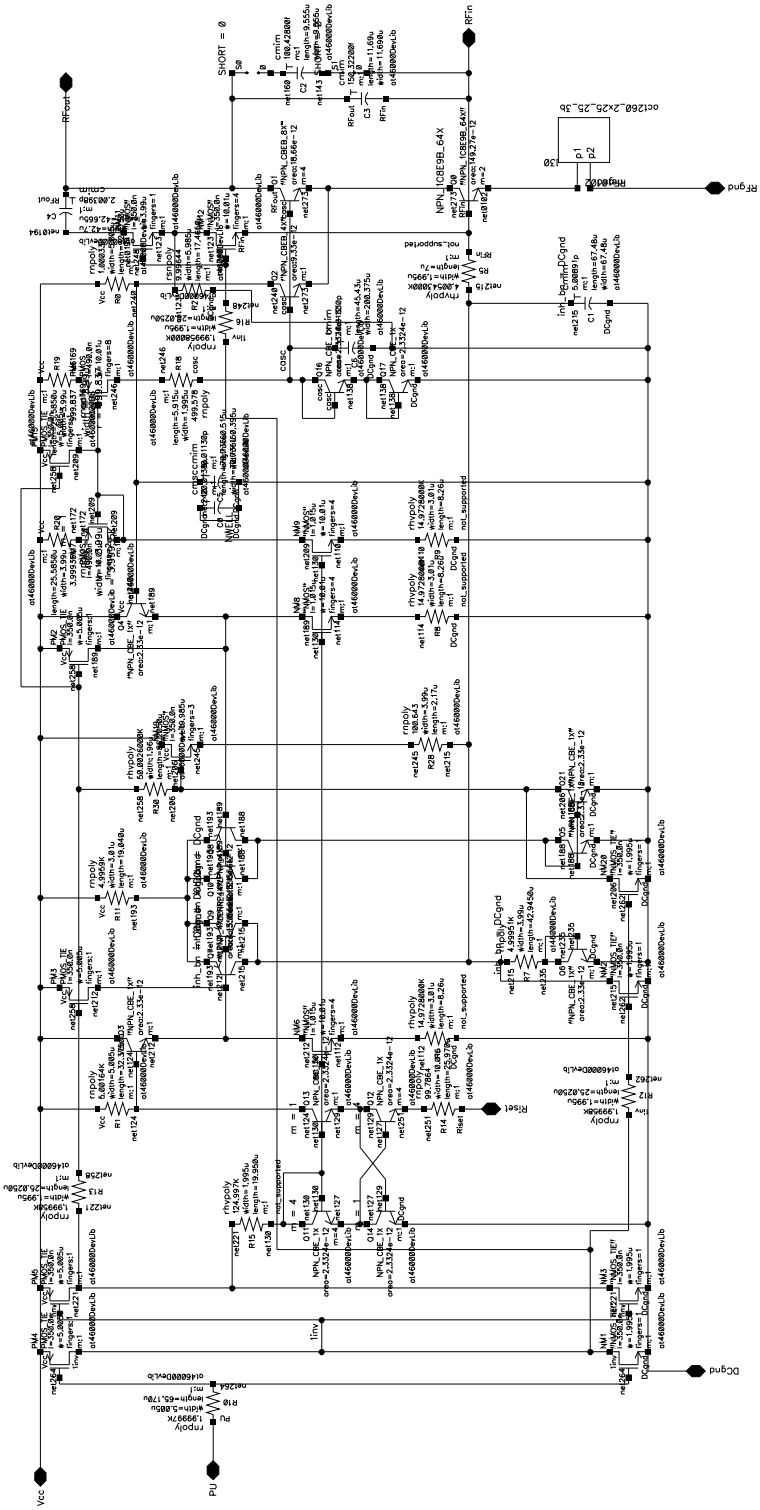


Figure 148: 800 MHz LNA of the TETRA/TETRAPOL receiver (MPW-run at46018).

model manufacturer reference	ATR0610 Atmel this work	MAX2654 Maxim [248]	BGA622 Infineon [251]	BGA615L7 Infineon [233, 234, 235]	BGA715L7 Infineon [236, 237]	NJG1103F1 JRC [318]	μPC8211TK NEC [252, 253]
technology	SiGe HBT	SiGe HBT	SiGe HBT	SiGe HBT	SiGe HBT	GaAs HBT	SiGe HBT
gain [dB]	16.5	15	15	18.5	20	16	18.5
50 Ω NF [dB]	1.5	1.5	1.0	0.9 / 1.1	0.75	1.2	1.3
IIP_3 [dBm]	-3	-7.2	0	-4 / -1	-7	-4	-12
OIP_3 [dBm]	+13.5	+7.8	+15	14.5 / 17.5	+13	+12	+6.5
current [mA]	3	5.8	5.8	5.6	3.3	3	3.5
supply voltage [V]	2.7 – 3.3	2.7 – 5	2.4 – 3.2	1.5 – 3.6	2.7 – 3.3	2.5 – 4.5	3

Table 27: ATR0610 compared to other GPS HBT LNAs. ATR0610 is the optimum compromise with respect to power consumption, bill-of-materials, NF, linearity and price.

model manufacturer	ATR0610 Atmel	MAAM-12022 M/A-COM	MAAM-12021 M/A-COM	AM50-0002 M/A-COM	ATF541 Agilent †	
technology	SiGe HBT	MESFET	MESFET	MESFET	pHEMT	
gain [dB]	16.5	14	20 (3V)...21 (5V)	27	11.7	12.5
50 Ω NF [dB]	1.5	1.85	1.55	1.15	0.52	0.46
IIP_3 [dBm]	-3	–	-8 (3V)...-2 (5V)	-14*	3.4	6.7
OIP_3 [dBm]	+13	–	+12 (3V)...+19 (5V)	+13*	15.1	19.2
current [mA]	3	5	8	20	3.7	6.4
supply voltage [V]	2.7 – 3.3	3 – 5	3 – 5	3 – 5	3.0	

* at V_{cc}=5 V † simulated values using ATF541 large signal model

Table 28: ATR0610 GPS LNA compared to commercially available GaAs MESFET and pHEMT LNAs [319, 320, 321, 254].



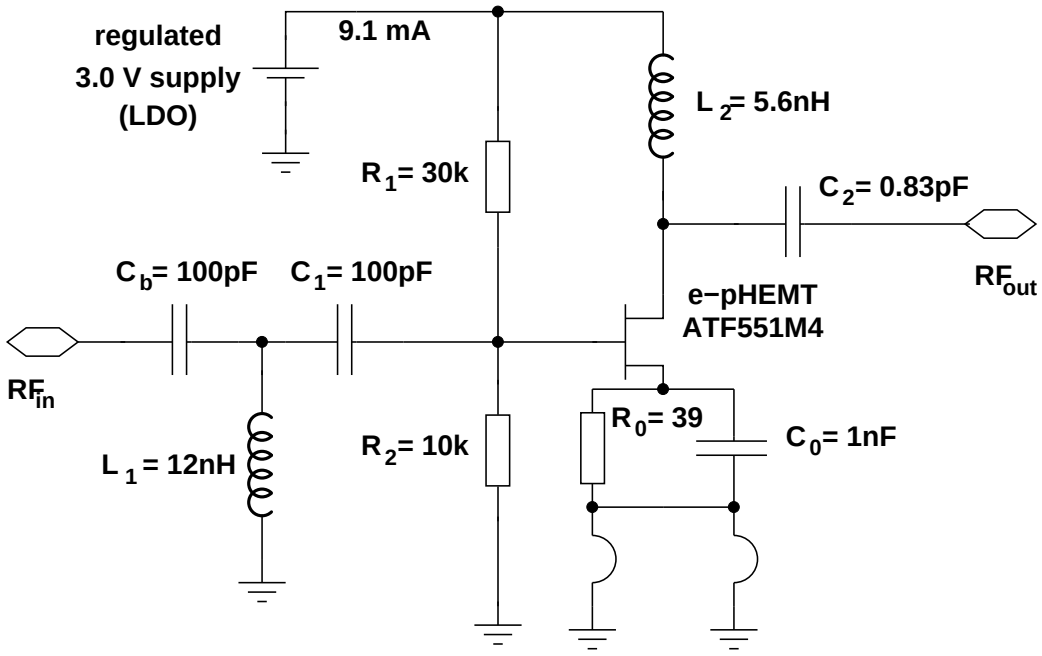


Figure 149: GPS LNA using a discrete enhancement-mode pseudomorphic HEMT transistor in common-source configuration with reactive LC output matching on a low-loss substrate, packaged in a metal housing (top). Biasing is via a high-impedance resistive voltage divider at the gate and a resistor current source in the source leads, which is bypassed at RF frequencies.

Type	ATR7158	HG-DAT	MAX2648
Author	this work	Erben [45]	[256]
Manufacturer	Atmel	Atmel	Maxim
Technology	SiGe2-Power	SiGe1	SiGe GST-3
Package	chip-on-board	on-wafer	ChipScale
Supply voltage [V]	3	3	3
Supply current [mA]	8	13.2	12
Gain [dB]	12 (13.5†)	15	16.2
NF (50 Ω) [dB]	1.65 (1.35†)	2.5	1.8
NF_{min} [dB]	1.30†	–	1.65
Γ_{opt}	0.175 ∠ 70°†	–	0.70 ∠ 162°
R_n [Ω]	8.8†	–	58.5
P_{1dB}, input [dBm]	-11	-6	-11.1
IIP_3 [dBm]	0.5	–	0.1

† on-wafer version with smaller pad size

Table 29: Performance of the ATR7158 WLAN LNA at 5.5 GHz compared to other SiGe HBT LNAs [45, 256, 257].

Author	ATR7158	Linten	Satou	Mohammadi
	this work	et al. [258]	et al. [259]	et al. [260]
Manufacturer	Atmel	IMEC	Fujitsu	Philips
Technology	SiGe2-Power	90 nm CMOS	0.11 μm CMOS	0.18 μm CMOS
Package	chip-on-board	on-wafer	on-wafer	on-wafer
Frequency [GHz]	5.5	5.5	5.3	5.8
Supply voltage [V]	3	1.2	1.2	1.8
Supply current [mA]	8	8.1	10.4	2.5
Gain [dB]	12 (13.5†)	13.3	17	16.7
NF (50 Ω) [dB]	1.65 (1.35†)	3.0 (2.7 w/o ESD)	1.6	1.4
P_{1dB}, input [dBm]	- 11	-11.5	–	-15.6
IIP_3 [dBm]	0.5	-2.7	-8.8	-2.6

† on-wafer version with smaller pad size

Table 30: Performance of the ATR7158 WLAN LNA compared to CMOS LNA implementations [258, 259, 260].

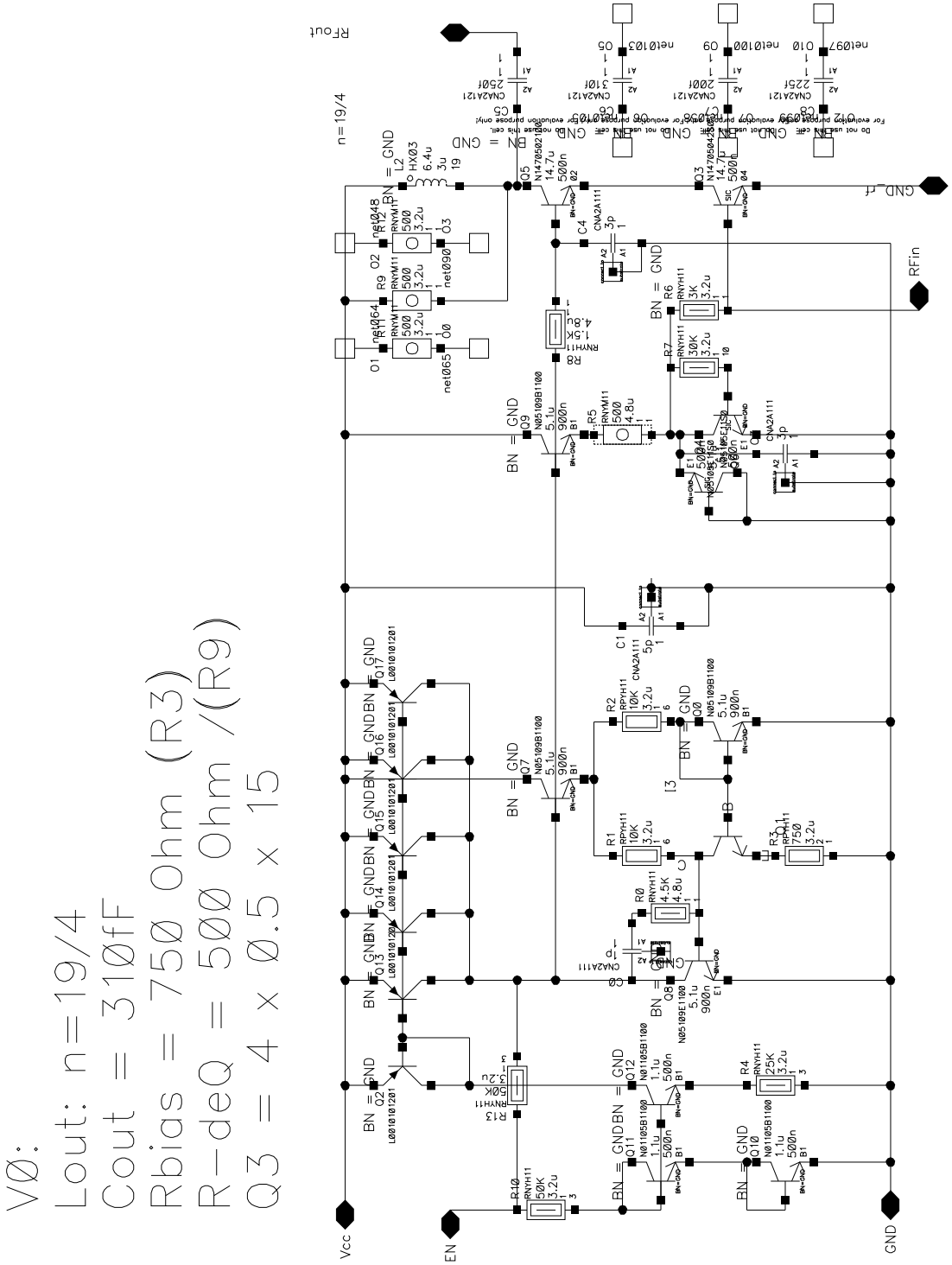


Figure 150: 4.9 - 5.9 GHz WLAN LNA (SiGe2-Power technology)

Type	ATR7124	BGA622	MAX2644	RF2373
Author	this work	[251]	[262]	[263]
Manufacturer	Atmel	Infineon	Maxim	RFMD
Technology	SiGe2-Power	SiGe HBT	SiGe HBT	GaAs HBT
Package	chip-on-	SOT343	6 SC70	SOT
Package	board	+ SMD parts		+ SMD parts
Supply voltage [V]	3	2.75	3	3.3
Supply current [mA]	8	5.8	7	13
Gain [dB]	16.5	12.7	17	15
NF (50 Ω) [dB]	0.9	1.15	2.0	1.3
P_{1dB}, input [dBm]	-12	-12.4	-13	-3.5
IIP_3 [dBm]	–	≈ 3	-3	9.5

Table 31: Performance of the 2.4 GHz part of the ATR7124 dual band WLAN LNA compared to commercially available HBT LNAs.

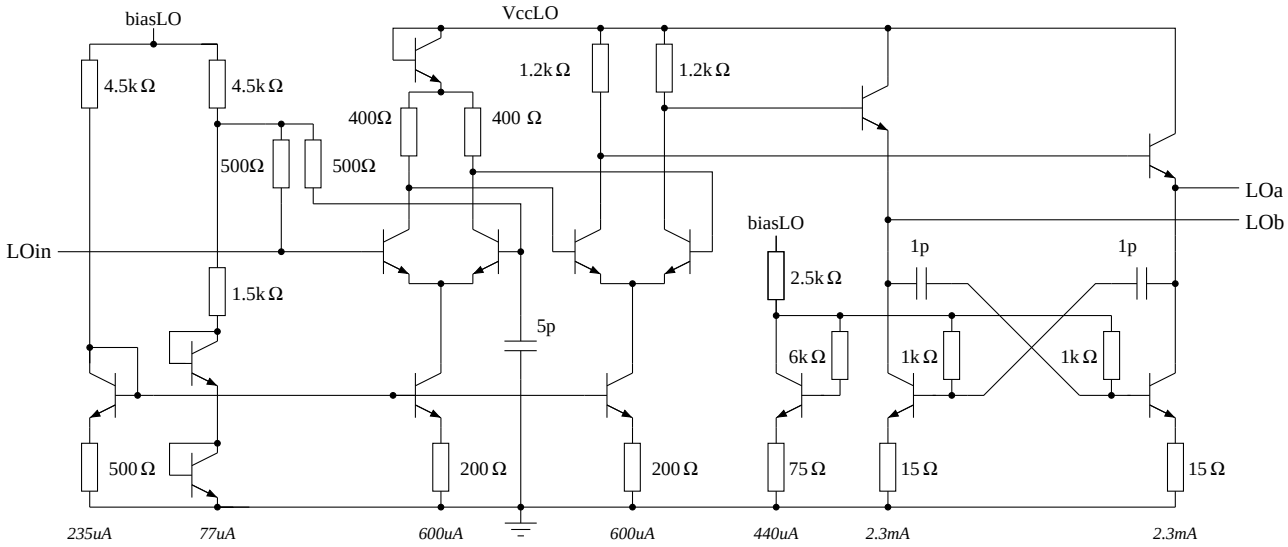


Figure 151: Push pull buffer to drive the quad diode ring mixer of the TETRA/TETRAPOL receiver (MPW0203-SiGe1).

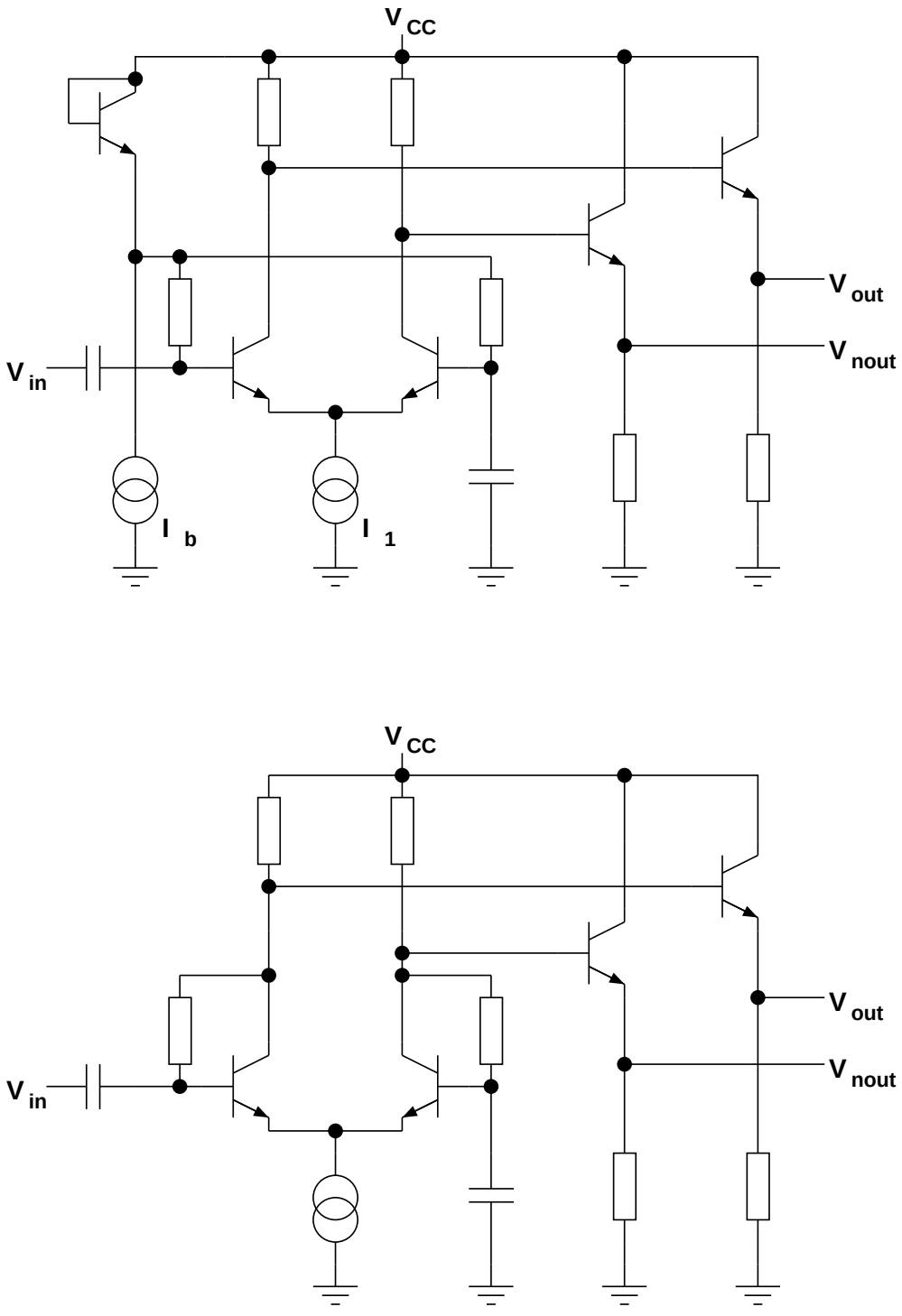


Figure 152: Standard single-ended to balanced (SE2D) limiting buffer amplifier as used in the TETRA project (top) and variant with increased bandwidth (bottom) [322].

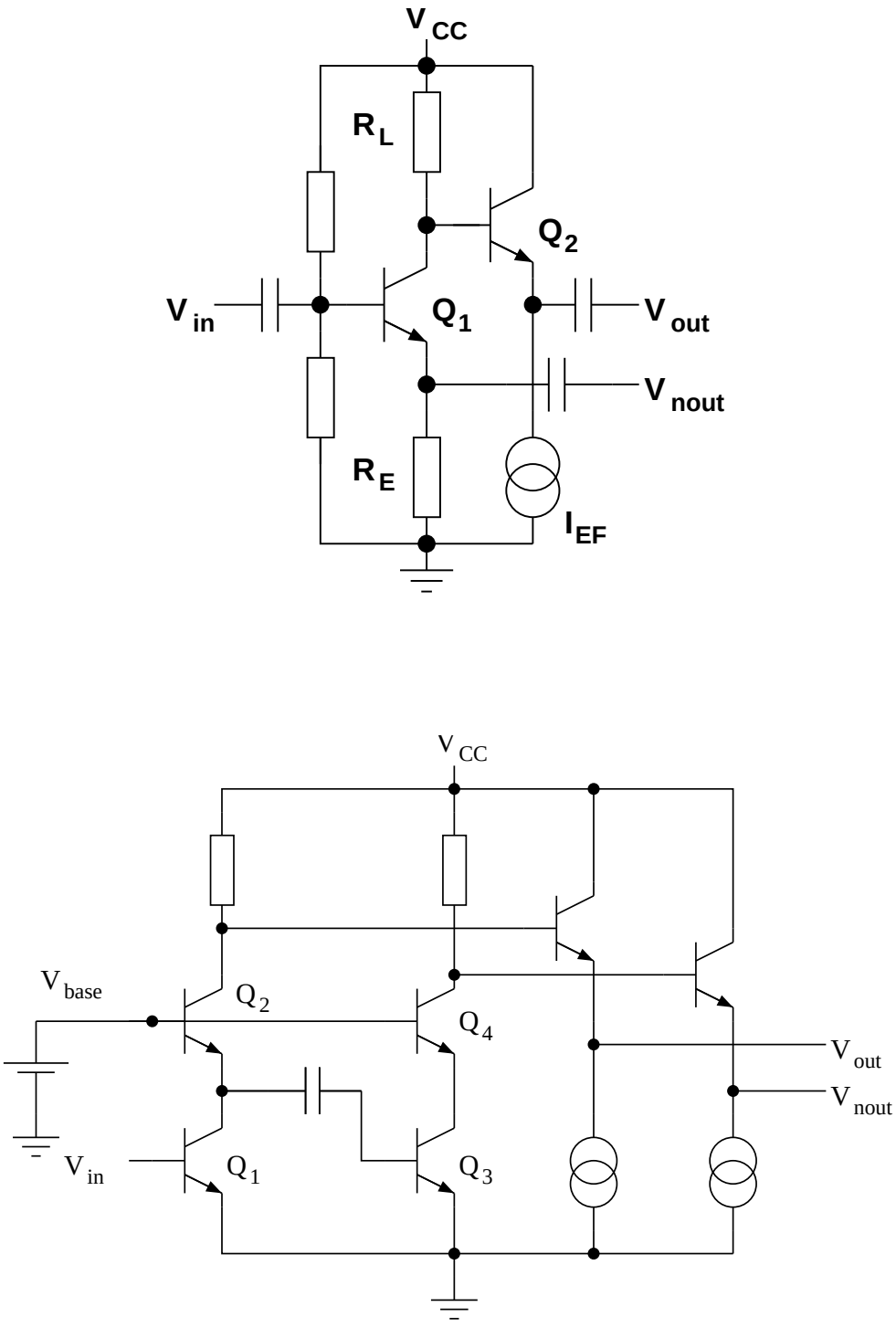


Figure 153: Simple, non-limiting, SE2D buffer amplifier as initially used in some versions of the TETRA mixer at 800 MHz and below (left) and high-speed cascode SE2D buffer used at frequencies of 5 GHz and above (right).

F Dimensioning spiral inductors

As shown in section 5.13, numerous EM simulations have shown that with the correct settings one can accurately predict the values of series inductance, series resistance and shunt reactances. As the quality factor is very sensitive to slight changes in S-parameters, however, it is difficult to calculate using simulation, especially if interpolation techniques like ABS or AFS are used. For the designer it is very important to chose for a given frequency and inductance value the implementation with the highest quality factor. Therefore the experimental data of Q have been fitted to the semi-empirical expression of Eqn. 107, where f denotes the frequency in GHz. For small frequencies, $Q \approx \frac{\omega \cdot L}{R_S} = 2 \cdot \pi \cdot \frac{L}{R_S} \cdot f$. The term '$\beta \cdot f^2$' models the influence of both skin and proximity effect. In our case β varies from 0.021 for a small inductor to 0.091 for an inductor with a very wide trace width of 20 μm. The term in the denominator models the influence of the substrate capacitance. A least squares fit has shown that Q_b only depends on the trace width (0.29 for w = 7μm) and that α remains nearly constant at 1.39. The expression for α, β, Q_b are given in Eqn. 110 for inductors of type M23 and in Eqn. 113 for M3-type inductors.

$$Q_1 = 2 \cdot \pi \cdot \frac{L_{DC}}{R_{DC}} \cdot 10^9 \cdot \frac{f - \beta \cdot f^2}{1 + Q_b \cdot f^{\alpha}} \tag{107}$$

for spirals in M23

$$\alpha = 1.388 \cdot \left[\frac{w}{7\,\mu m}\right]^{-0.140} \cdot \left[\frac{s}{3\,\mu m}\right]^{0.0708} \cdot \left[\frac{n}{4.5}\right]^{0.949} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{0.387} \tag{108}$$

$$\beta = 0.044 \cdot \left[\frac{w}{7\,\mu m}\right]^{0.729} \cdot \left[\frac{s}{3\,\mu m}\right]^{0.277} \cdot \left[\frac{n}{4.5}\right]^{1.755} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{0.873} \tag{109}$$

$$Q_b = 0.285 \cdot \left[\frac{w}{7\,\mu m}\right]^{1.614} \cdot \left[\frac{s}{3\,\mu m}\right]^{-0.337} \cdot \left[\frac{n}{4.5}\right]^{-1.056} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{-0.342} \tag{110}$$

for spirals in M3

$$\alpha = 1.358 \cdot \left[\frac{w}{7\,\mu m}\right]^{-0.032} \cdot \left[\frac{s}{3\,\mu m}\right]^{0.0556} \cdot \left[\frac{n}{4.5}\right]^{0.933} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{0.583} \tag{111}$$

$$\beta = 0.0445 \cdot \left[\frac{w}{7\,\mu m}\right]^{0.489} \cdot \left[\frac{s}{3\,\mu m}\right]^{0.0218} \cdot \left[\frac{n}{4.5}\right]^{1.475} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{0.573} \tag{112}$$

$$Q_b = 0.0776 \cdot \left[\frac{w}{7\,\mu m}\right]^{1.844} \cdot \left[\frac{s}{3\,\mu m}\right]^{-0.961} \cdot \left[\frac{n}{4.5}\right]^{-1.882} \cdot \left[\frac{r_i}{26\,\mu m}\right]^{-0.574} \tag{113}$$

Using equation 107, a simple *VisualBasic™* program has been developed that calculates, for a given inductance, technology and turn spacing, all reasonable geometries in terms

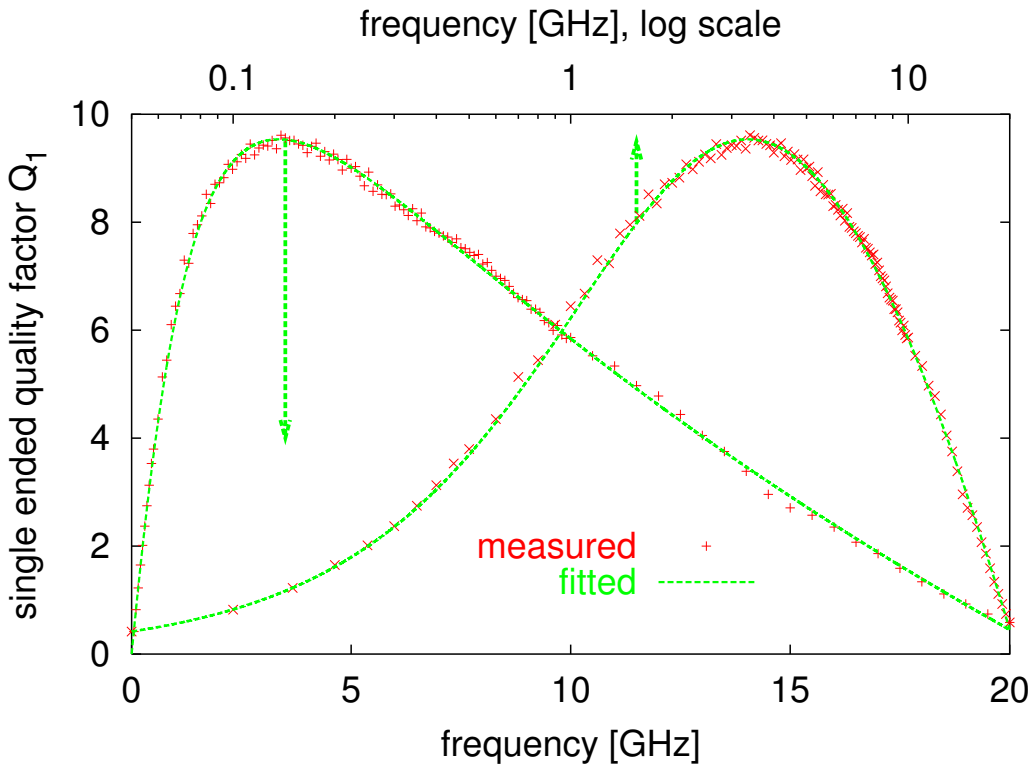


Figure 154: The single-ended quality factor Q_1 fits perfectly to the semi-empirical expression 107, both for low (logarithmic x-axis) and high frequencies (linear x-axis).

of (i) number of turns (ii) line width and (iii) inner radius. At the chosen frequency, all Q factors are listed as well so that the circuit designer can easily identify the geometry with the highest Q-factor and a reasonable area consumption.
Using the algorithm for inductance calculation from Mohan *et al.* [163] which we found to be extremely accurate for Atmel's round spiral inductors, a tool was developed that searches for all possible geometrical combinations of conductor width, conductor spacing, number of turns and inner radius that yield a given inductance and sorts them for highest Q or lowest outer diameter. Equations 107, 110, and 113 of chapter 5 have been used to calculate the quality factor at a given frequency.

We found this tool to be useful for the first dimensioning of a spiral inductor when a circuit is started from scratch. Its clear, however, that this tool cannot substitute the full, scaleable equivalent circuit models developed in section 5.15 which include frequency dependent resistive and capacitive losses.

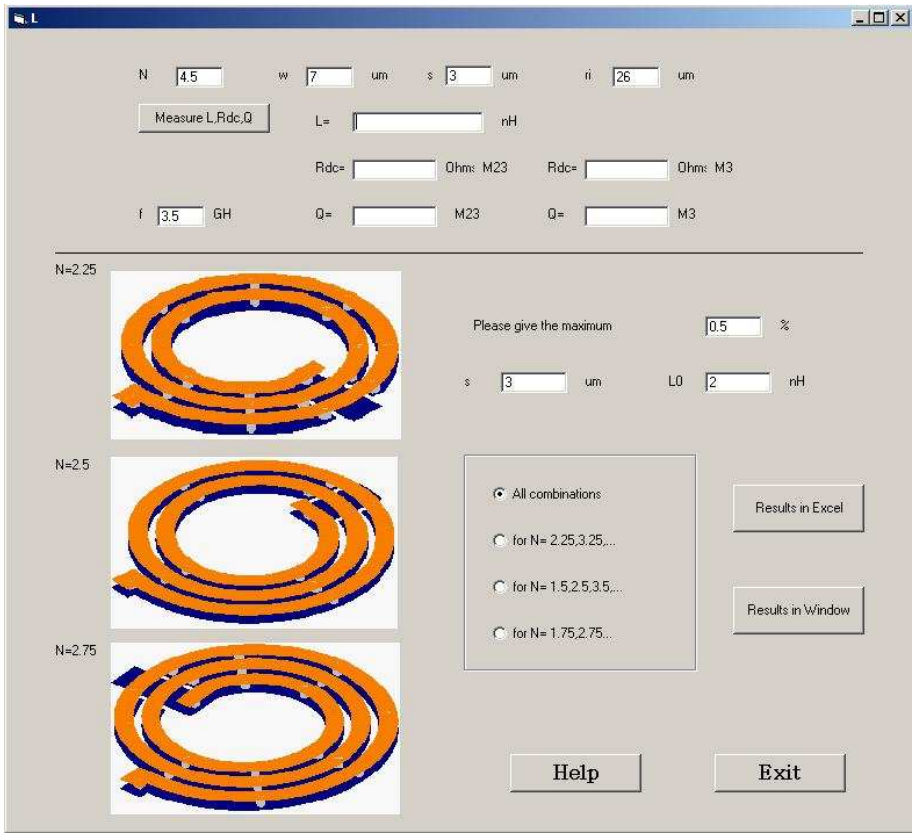


Figure 155: This tool developed within this thesis, searches for all possible geometrical combinations that yield a given inductance and sorts them for highest Q or lowest outer diameter.

G Glossary of terms

Acronym	Explanation
1G	1st generation mobile technology (analogue)
2G	2nd generation mobile technology
3G	3rd generation mobile technology
A	Emitter area of a transistor
AC	Alternate Current
AC coupling	Transmission of →RF or →IF signals via a coupling capacitor
ADS	Advanced Design System
ALC	Automatic Level Control
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone System (→1G analogue standard in the US)
APCO	Association of Public Safety Communications Officials International
AWGN	Average White Gaussian Noise
BAW	Electromechanical filters using piezoelectric Bulk-Acoustic-Wave technology
β	Current gain of a bipolar transistor
BER	Bit Error Rate
BiCMOS	semiconductor process using → bipolar and → CMOS transistors
BJT	Bipolar Junction Transistor
BL	Buried Layer
BOM	Bill Of Materials
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CCK	Complementary Code Keying
CDMA	Code Division Multiple Access
cdmaOne	IS-95 standard-based CDMA system (→2G), deployed mainly in USA and Asia
cdma2000	cdmaOne derivative, accepted as →3G standard
CMOS	Complementary →MOS transistors (NMOS and PMOS)
CMP	Chemical-Mechanical-Polishing
COB	Chip-on-board mounting of a bare →die onto a →PCB
CSP	ChipScalePackage: Package having barely larger dimension than the semiconductor →die
CVD	Chemical Vapour Deposition: Technique to deposit a chemical species from a gaseous mixture (for example silicon from silane = SiH_4)
DCR	Direct-conversion receiver

Die	Piece of semiconductor containing the IC after separating the wafer
DUT	Device Under Test
DQPSK	Differential →QPSK
DSSS	Direct Sequence Spread Spectrum
Diplexer	Device that allows bi-directional (duplex) communication over a single channel
Early	Voltage, that models the influence of collector voltage on collector current in a → BJT
EF	Emitter follower
EGNOS	European Geostationary Navigation Overlay System (overlay to → GPS)
ESD	ElectroStatic Discharge
ETSI	European Telecommunications Standards Institute
FBAR	Filters using thin-Film-Bulk-Acoustic-Resonance technology
FDD	Frequency Division Duplex
FDMA	Frequency Division Multiple Access system
FER	Frame error rate
FET	Field Effect Transistors
FFT	Fast Fourier Transformation
FIR	Finite Impulse Response filter
FM	Frequency Modulation
f_{max}	Maximum frequency of oscillation, where the power gain drops to '1'
f_T	Transient frequency of the device, where the current gain drops to '1'
FSK	Frequency Shift Keying
Γ_{opt}	Source impedance for optimum noise performance
GaAs	Gallium-Arsenide
GDSII	Database file format which is the de facto industry standard for data exchange of IC layout artwork
GPS	Global Positioning System
g_m	Transconductance of a transistor
GMSK	→MSK with Gaussian filtering
GSM	Global System for Mobile Communication, worldwide →2G standard
HBT	Heterojunction Bipolar Transistor
HBM	Human Body Model (impact of →ESD of the human body onto an IC)
HEMT	High Electron Mobility Transistor
h_{FE}	Current gain of a transistor
HPSK	Hybrid Phase Shift Keying
HiperLAN	High Performance Radio LAN, specified by →ETSI
HR	high-resistivity

IC	Integrated Circuit
IF	Intermediate Frequency
IIP_3	$\rightarrow$ IP_3, referred to the input of an amplifier
IM	Intermodulation distortion
IP_3	3rd order intercept point
I/Q	In phase / Quadrature
IS-95	Interim Standard for US $\rightarrow$CDMA ($\rightarrow$2G standard)
ISS	Impedance Standard Substrate
ln	Natural logarithm to the base of e
LNA	Low Noise Amplifier
LRM	On-wafer calibration using 'Line', 'Reflect', 'Match'
LO	Local Oscillator
log	Logarithm to be base of 10
MIC	Millimeter wave Integrated Circuit
MLF	MicroLeadFrame package, leadless package similar to the $\rightarrow$ QFN package
MMIC	Monolithic Millimeter wave Integrated Circuit
MOS	Metal-Oxide-Semiconductor transistor using a metallic gate isolated by a thin oxide layer to control current flow in a lateral way
MoM	Method of Moments
MPW	Multi Project Wafer run
MSK	$\rightarrow$FSK with a phase shift of $\pm\pi/2$
NF	Noise Figure
NF_{min}	minimum Noise Figure
NMT	Nordic Mobile phone Technology, $\rightarrow$1G standard deployed in Scandinavia and Eastern Europe
NPN	Bipolar transistor with np/pn junctions
OFDM	Orthogonal Frequency Division Multiplexing
OIP_3	$\rightarrow$ IP_3, referred to the output of an amplifier
OPA	Operational amplifier
OVSF	Orthogonal Variable Spreading Function
PCB	Printed Circuit Board
PMR	Professional Mobile Radio
PNP	Bipolar transistor with pn/np junctions
PSD	Power Spectral Density
PSK	Phase Shift Keying
PTAT	Proportional To Absolute Temperature
PTFE	PolyTetra-Fluor-Ethylen
Q	Quality factor of an inductor

QAM	Quadrature Amplitude Modulation
QFN	Quad Flat-pack No-lead package: Leadless package similar to the → MLF package
QPSK	Quadrature Phase Shift Keying
ρ	Specific resistance in units of $[\Omega \cdot cm]$ or $[\Omega \cdot m]$. $\rho = 1/\sigma$
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RIE	Reactive Ion Etching
σ	Conductivity in units of [S/m]. $\sigma = 1/\rho$
SAW	Electromechanical filters using piezoelectric Surface-Acoustic-Wave technology
SGP	Simple Gummel Poon model for bipolar transistors
SE2D	Single-Ended to Differential converter
SiGe	Silicon-Germanium alloy
SMD	Surface Mount Device
SOLT	On-wafer calibration procedure using 'Short', 'Open', 'Load', 'Thru'
SPICE	Simulation Program with Integrated Circuits Emphasis
SRF	Self Resonance Frequency
STI	Shallow Trench Isolation, technique to isolate active devices on the wafer from each other
T	Absolute temperature in Kelvin
TAN	→ TNA
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TETRA	TErestrial Trunked RAdio (formerly 'Trans-European Trunked RAdio')
TIA	Telecommunications Industry Association
TIA	Transimpedance Amplifier
TNA	On-wafer calibration using 'Thru', 'Network', 'Attentator'
TSSOP	Thin Shrink Small Outline Package
UMTS	Universal Mobile Telephone System (→3G →W-CDMA standard)
U-NII	Unlicensed National Information Infrastructure bands (USA)
VNA	Vector Network Analyser
VSWR	Voltage Standing Wave Ratio
V_{th}	Thermal voltage $q \cdot T/k_B$ ($25.4mV$ at room temperature)
WCDMA	Wideband →CDMA, →3G proposal
WLAN	Wireless Local Area Networks (license exempt system for data transmission)

H List of symbols

Acronym	Explanation
A	Ampere or Area
$\mathcal{A}$	chain parameter
β	current gain
C	capacitance
c_0	speed of light in vacuum
dB	Decibel
δ	differential operator
Δ	difference operator or matrix determinant
E_b	energy per data bit
ϵ_R	relative permittivity
ϵ_0	dielectric contant or vacuum permittivity
	$\epsilon_0 = 1/(\mu_0 \cdot c^2) = 8.854187817... \cdot 10^{-12}$A·s/(V·m)
f	absolute frequency
f_T	maximum transient frequency (current gain = 0 dB)
f_{max}	maximum oscillation frequency (power gain = 0dB)
ν	frequency offset with respect to a carrier
g_m	transconductance $g_m = \frac{\delta I_{out}}{\delta V_{in}}$
Γ_{opt}	generator impedance to achieve minimum noise figure NF_{min}
h	hybrid parameter (h_{21} = small signal current gain β)
I	large-signal current
i	small-signal current
$\Im[\quad]$	imaginary part
j	$\sqrt{-1}$
j_0	current densitiy per area
K	Kelvin
k	Rollet´s stability factor
k_B	Boltzmann constant ($k_B = 1.3806504 \cdot 10^{-23} J/K$)
κ	coupling factor between two inductors
μ_0	magnetic constant or vacuum permeability
	$= 4\,\pi\,10^{-7} N/A^2 = 1.2566370614... \cdot 10^{-6} H/m$
L	inductance
N	number of turns
N	noise power
nH	nano Henry
NF	noise figure

NF_{min}	minimum noise figure
ω	$2\,\pi f$
Ω	Ohms
P	power
q	elementary charge ($1.602176487 \cdot 10^{-19}$ coulombs)
Q	quality factor
ρ	specific resistance in units of $[\Omega \cdot cm]$
$\Re[\quad]$	real part
R	resistance
r	radius
S	scattering parameter
s	scattering parameter (normalized to Z_0)
s	spacing
σ	specific conductance in units of $[S/m]$ ($\sigma = 100/\rho$)
t	thickness
t	time
T	absolute temperature
V	Volt
V	large-signal voltage
v	small-signal voltage
V_{th}	thermal voltage ($V_{th} = \frac{k_B \cot T}{q} = 25\text{mV}$ at T=295K)
w	width
Y	admittance parameter
y	admittance parameter (normalized to Z_0)
Z	impedance parameter
z	impedance parameter (normalized to Z_0)
ζ	fill ratio of a coil

References

[1] `www.telefunkensemi.com/#PageTop`, last visited Dec. 2009.

[2] "SiGe Bipolar Silicon Germanium – High-speed Technology for Communications Applications," `www.telefunkensemi.com/_assets/Pages/PT-SiGe1.html`, last visited Dec. 2009.

[3] "Digital Modulation in Communications Systems - An Introduction," Application Note 1298, Hewlett-Packard Company, 1997.

[4] F. Kostedt and J. C. Kemerling, "Practical GMSK Data Transmission," Application Note 20830067.002, MX COM, INC., 4800 Bethania Station Road, Winston-Salem, NC, USA, 1998.

[5] "Orthogonal frequency-division multiplexing," `www.en.wikipedia.org/wiki/OFDM`, last visited Dec. 2009.

[6] H. Johnston, "DoCoMo announces trial of 4G system," *wireless europe*, p. 12, July 2003.

[7] "CDMA - Multiplexing von UMTS," `www.umtslink.at/index.php?pageid=wcdma`, last visited Dec. 2009.

[8] Koninklijke Philips Electronics N.V., "2005 Worldwide Wireless Communication Standards," Dec. 2004. order number 9397 750 14105.

[9] X. Wang, W. Chen, G. Henderson, G. Bergmann, U. Karthaus, and F. Gruson, "SiGe RF Receiver Front-end for Cellular CDMA/GPS Applications," in *IIC-China 2003: 8th Annual International IC-China Conference & Exhibition*, Mar. 2003.

[10] X. Wang, W. Chen, G. Henderson, G. Bergmann, U. Karthaus, and F. Gruson, "SiGe RF Receiver Front-end for Cellular CDMA/GPS Applications," in *ICC'03: 2003 IEEE International Conference on Communications*, 2003.

[11] "T0351 – 2.8 V Dual-mode RF receiver for CDMA / AMPS," data sheet, Atmel Germany GmbH, `www.atmel.com`, Nov. 2002.

[12] "T0352 – 2.8 V Dual-band/Dual-mode RF receiver for CDMA / AMPS," data sheet, Atmel Germany GmbH, `www.atmel.com`, Nov. 2002.

[13] "T0353 – 2.8 V Tri-mode/Quad-mode RF receiver for CDMA / AMPS / GPS," data sheet, Atmel Germany GmbH, `www.atmel.com`, Oct. 2002.

[14] "T0354 – 2.8 V Dual-band/Dual-mode RF receiver for Cell CDMA / AMPS," data sheet, Atmel Germany GmbH, `www.atmel.com`, Nov. 2002.

[15] U. Karthaus, F. Gruson, T. Bitzer, H. Vogelmann, G. Bergmann, N. Alomari, K. Weese, and A. Pascht, "Fully integrated, 4-channel, direct conversion SiGe receiver IC for UMTS base stations," in *Proc. Eur. Conf. Wireless Technologies 2003, Munich, Germany*, pp. 213–216, Oct. 8-10 2003. ISBN: 0-7803-8333-8.

[16] U. Karthaus, F. Gruson, G. Bergmann, and A. Pascht, "Improved four-channel direct-conversion SiGe receiver IC for UMTS base stations," *IEEE Microwave and Wireless Components Letters*, vol. 14, pp. 377–379, Aug. 2004. ISSN: 1531-1309.

[17] S. Reynolds, B. Floyd, T. Beukema, T. Zwick, U. Pfeiffer, and H. Ainspan, "A direct-conversion receiver IC for WCDMA," in *Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 61–64, 2002.

[18] J. Jussila, J. Ryynanen, K. Kivakas, L. Sumanen, A. Parssinen, and K. Haionen, "A 22 mA 3.7 dB NF direct conversion receiver for 3G WCDMA," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 284–285, 2001.

[19] T. Bitzer, U. Karthaus, A. Pascht, and K. Weese, "Realisation of a SiGe-HBT Direct Down Conversion Receiver for UMTS Base Stations," *IEEE Int. Symp. on Electron Devices for Microwave and Optoelectronic Applications, Manchester, UK*, pp. 83–88, Nov. 2002.

[20] F. Gruson, G. Gaborit, P. Abele, and H. Schumacher, "A broadband SiGe mixer for 5-GHz WLAN applications with X-band quadrature generation and high image-rejection," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers, Fort Worth, Texas, USA*, pp. 523–526, June 6-8 2004. ISBN: 0-7803-8333-8.

[21] Tetra MOU, "The Madrid tragedy – In the aftermath of disaster, communications are the key to efficient response," *Tetra News*, no. 2, p. 5, 2004. `www.tetramou.com`.

[22] "Sprachlos im Katastrophen-Einsatz - Sicherheitskräfte sollen zuverlässigen Funk bekommen (in german).," *Süddeutsche Zeitung*, Feb. 28 2004.

[23] "Terrestrial Trunked Radio," `www.en.wikipedia.org/wiki/Terrestrial_Trunked_Radio`, last visited Dec. 2009.

[24] "Project 25," `www.en.wikipedia.org/wiki/Project_25`, last visited Dec. 2009.

[25] P. Lunness, "P25 Radio Systems," Training Guide TG-001 Rev. 2-0-0, Daniels Electronics Ltd., 43 Erie Street, Victoria, BC Canada V8V 1P8, Jan. 2007.

[26] B. Ellis and C. Komatas, "Will WLAN put 3G in the dark ?," *wireless europe*, pp. 17–18, July 2003.

[27] J. P. Maligeorgos and J. R. Long, "A Low-Voltage 5.1-5.8-GHz Image-Reject Receiver with Wide Dynamic Range," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1917–1926, Dec. 2000.

[28] IEEE Computer Society, "IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications," June 2007. IEEE Std 802.11™-2007.

[29] "HiperLAN," `www.en.wikipedia.org/wiki/HIPERLAN`, last visited Dec. 2009.

[30] "HiperLAN2Resource Center," `www.palowireless.com/hiperlan2/about.asp`, last visited Dec. 2009.

[31] M. Zargari, D. K. Su, C. P. Yue, S. Rabii, D. Weber, B. Kaczynski, S. S. Mehta, K. Singh, S. Mendis, and B. A. Wooley, "A 5-GHz CMOS transceiver for IEEE 802.11a Wireless LAN Systems," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1688–1693, Dec. 2002.

[32] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS Wireless LAN Receiver Front End," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 765–772, May 2000.

[33] T.-P. Liu and E. Westerwick, "5-GHz CMOS Radio transceiver Front-End Chipset," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1927–1933, Dec. 2000.

[34] J. Browne, "CMOS Yields High-Speed 5-GHz WLAN Chip Set," *Microwaves & RF*, p. 156, Nov. 2000.

[35] "High Frequency Circuit Materials Product Selector Guide," Tech. Rep. 92-601, Rogers Corporation, 2002.

[36] Maxim Integrated Products, "Single-Chip, 802.11a/b/g Dual-Band RF transceiver Delivers Best Sensitivity," *Analog Design Solutions*, 2004.

[37] P. Heide, "Specification for EPCOS WLAN module." private communications, Jan. 2004.

[38] P. Heide, "WLAN-Frontend-Module in LTCC Technologie: Größe durch Miniaturisierung," *components - your direct link to EPCOS*, vol. 3, pp. 8–10, 2006. EPC:50027.

[39] P. Naraine, "Predicting the EVM Performance of WLAN Power Amplifiers with OFDM Signals," *Microwave Journal*, vol. 47, pp. 222–226, May 2004.

[40] Anadigics, "Dual-band WLAN power amp," *Microwave Engineering Europe*, p. 36, Dec/Jan 2005.

[41] "Medium Power Amplifier for 5.1 to 5.3 GHz Applications using the MGA-425P8," Application Note 5085 5989-1507EN, Avago Technologies, Aug. 2004. `www.avagotech.com`.

[42] "SKY65205: WLAN 802.11b/g RF Front-End Module," preliminary data sheet, Skyworks Solutions, Inc., Dec. 11 2003.

[43] "SKY65202: WLAN 802.11a RF Front-End Module," preliminary data sheet, Skyworks Solutions, Inc., Oct. 9 2003.

[44] A. Nakatani and L. Williams, "Automating and Optimizing High Performance LTCC Design," *Microwave Journal*, vol. 47, pp. 176–188, Sept. 2004.

[45] U. Erben and E. Sönmez, "Fully differential 5 to 6 GHz low noise amplifier using SiGe HBT technology," *Electronics Letters*, vol. 40, pp. 39–41, Jan. 8 2004.

[46] G. Heinrichs, "Galileo – Das neue Europäische Navigationssystem," in *EEEf-COM04: Hochfrequenz- und Mikrowellen-Elektronik, Komponenten und Module, FH Ulm*, May 26-27 2004.

[47] F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour, A. Kheirkhahi, M. Nariman, M. Conta, and S. Bhatia, "A Fully Integrated Low-IF CMOS GPS Radio With On-Chip Analog Image Rejection," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1721–1727, Dec. 2002.

[48] F. Gruson, "COVER FEATURE - GPS : How to design a high-performance GPS receiver," *Microwave Engineering Europe*, pp. 16–19, Aug./Sept. 2006.

[49] H. Schulz, H.-J. Golberg, F. Gruson, M. Durler, and S. J. Spiegel, "GPS low noise amplifier with high immunity to wireless jamming signals and power control option," *Advances in Radio Science*, vol. 2, pp. 195–197, 2004. `http://www.adv-radio-sci.net/2/195/2004/`,ISSN = 1684-9965.

[50] F. Gruson, H. Schumacher, H. Schulz, H.-J. Golberg, M. Durler, and S. J. Spiegel, "GPS low noise amplifier with high immunity to wireless jamming signals," in *2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers*, (Atlanta), pp. 77–80, Sept. 2004. ISBN: 0-7803-8703-1.

[51] H.-J. Strobel, W. Bischof, S. Gerlach, H. Schulz, K.-F. Becker, E. Jung, K.-D. Lang, H. Mokrani, and S. Spirkovitch, *New Combination of SiGe RF Amplifier ICs with High-Q MEMS Components for Wireless Communication Radio transceivers*, pp. 97–109. MicroNano Integration, Springer, Berlin, 1 ed., Jan. 2004. ISBN 3-540-20252-8.

[52] E. Alexander, "Leading-edge SAW Filters for Short Range Devices," *Microwave Journal*, vol. 47, pp. 236–242, May 2004.

[53] "Galileo (Satellitennavigation)," `http://en.wikipedia.org/wiki/Galileo_(satellite_navigation)`, last visited Dec. 2009.

[54] Clemens Bürgi, Eric De Mey, Andrea Orzati, Andreas Thiel, "Highly-Integrated Solution for Ultra-fast Acquisition and Precise Tracking of Weak GPS and Galileo L1 Signals," in *ION GNSS 19th International Technical Meeting of the Satellite Division*, pp. 226–235, Sept. 2006.

[55] European Space Agency, "Galileo satellite launch in view," *Microwave Engineering Europe*, pp. 22–23, Oct. 2004.

[56] G. W. Hein, J. Godet, J.-L. Issler, J.-C. Martin, P. Erhard, R. Lucas-Rodriguez, and T. Pratt, "Status of Galileo Frequency and Signal Design," in *Proceedings of the 15th International Technical Meeting of the Satellite Division of the Institute of Navigation ION GPS 2002*, pp. 266–277, Sept. 24-27 2002.

[57] "Triple/Dual/Single-Mode CDMA LNA/Mixers," data sheet, Maxim Integrated Products, Sept. 2000. ANJLQ400.03, Rev. B.

[58] V. Aparin, E. Zeisel, and C. Persico, "Highly Linear SiGe BiCMOS LNA and Mixer for Cellular CDMA/AMPS Applications," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 129–132, 2002.

[59] "Desensitization (telecommunications)," `www.en.wikipedia.org/wiki/Desensitization(telecommunications)`, last visited Dec. 2009.

[60] I. Kipnis, "Refining CDMA Mobile-Phone Power Control," *Microwaves & RF*, pp. 71–76, June 2000.

[61] V. Aparin and C. Persico, "Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits," *IEEE MTT-S Dig.*, vol. 3, pp. 977–980, June 1999.

[62] V. Aparin and L. E. Larson, "Modified Derivative Superposition Method for Linearizing FET Low Noise Amplifiers," *2004 IEEE RFIC Symposium, Fort Worth, Texas, USA*, no. MO1C-3, 2004.

[63] T. Carey, "Intermodulation Distortion," Application Note 46891-846, IFR Systems, Inc., 2000.

[64] P. B. Kenington, *High-linearity RF amplifier design*. Artech House microwave library, Artech House, Norwood, MA, 2000. ISBN 1-58053-143-1.

[65] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Artech House, Inc., 2nd ed., 2003.

[66] H. Schumacher, *Monolithic Microwave ICs in High-Speed Systems*. Ulm University, 2002. lecture notes.

[67] C. Henn, "Intermodulation distortion (IMD)," Application Bulletin SBOA077, Burr-Brown, 6730 S. Tucson Blvd., Tucson, AZ 85706, U.S.A., Apr. 1994.

[68] "W-CDMA 2.3 GHz VCO using BFR360F and BBY58-02V," Application Note Rev. 2.0, Infineon Technologies AG, 81726 München, Germany, Nov. 2006.

[69] "BAW Duplexer - Serienfertigung gestartet," *components - your direct link to EPCOS*, vol. 3, p. 2, 2006. EPC:50027.

[70] R. Aigner, "RF-MEMS Filters Manufactured on Silicon: Key Facts about Bulk-Acoustic-Wave Technology," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 157–161, Apr. 2003.

[71] J. Browne, "FBAR Filter, Duplexer Isolate PCS Signals," *Microwaves & RF*, p. 118, Feb. 2004.

[72] "BAW filters set to sweep the board," *Microwave Engineering Europe*, pp. 19–20, Nov. 2004.

[73] "2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers," data sheet, Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA, U.S.A., Feb. 2001. 19-1524; Rev 3.

[74] "AWT6309 - HELP2™AWS/KPCS CDMA 3.4V/28dBm Linear Power Amplifier Module," data sheet, ANADIGICS, Inc., 141 Mount Bethel Road, Warren, New Jersey 07059, U.S.A., May 2009. Rev 2.4.

[75] H. Friis, "Noise figures of radio receivers," *Proceedings of the IRE*, vol. 32, pp. 419–422, 1944.

[76] "Silicon-Germanium HBTs Merge With Mainstream CMOS Process," *Electronic Design*, p. 97ff, July 10 2000.

[77] M. Bopp, M. Alles, M. Arens, D. Eichel, S. Gerlach, R. Götzfried, F. Gruson, M. Kocks, G. Krimmer, R. Reimann, B. Ross, M. Siegle, and J. Zieschang, "A DECT Transceiver Chip Set Using SiGe Technology," in *1999 IEEE International Solid-State Circuits Conference, 1999. Digest of Technical Papers (ISSCC)*, (San Francisco, CA, USA), pp. 68–69, Feb 15-17 1999. ISBN: 0-7803-5126-6.

[78] R. Götzfried, F. Beisswanger, S. Gerlach, A. Schüppen, H. Dietrich, U. Seiler, K.-H. Bach, and J. Albers, "RFIC's for Mobile Communication Systems Using SiGe Bipolar Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 661–668, May 1998. ISSN: 0018-9480.

[79] U. König and H. Dämbkes, "SiGe HBTs AND HFETs," *Solid-State Electronics*, vol. 38, no. 9, pp. 1595–1602, 1995.

[80] U. König, A. Gruhle, and A. Schüppen, "SiGe Devices and Circuits: Where are Advantages over III/V ?," in *IEEE GaAs IC Symposium*, pp. 14–17, 1995.

[81] A. Schüppen, H. Dietrich, S. Gerlach, H. Höhnemann, J. Arndt, U. Seiler, R. Götzfried, U. Erben and H. Schumacher, "SiGe technology and components for mobile communications systems," *Proc. Bipolar and BiCMOS Topical Meeting*, pp. 130–133, Oct. 1996. ISBN: 0-7803-3516-3.

[82] A. Schüppen, H. Dietrich, U.Seiler, H. von der Ropp, and U. Erben, "A SiGe RF technology for mobile communication systems," *Microwave Engineering Europe*, pp. 39–46, June 1998.

[83] A. Schüppen, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus and M. Averweg, "An 80 GHz SiGe production technology," *BCTM*, vol. 14, pp. 42–46, Aug. 2001.

[84] M. Bopp and A. Schüppen, "SiGe Transistor Technology for RF Applications," *Microwave Journal*, vol. 42, pp. 22–39, June 1999.

[85] Wolfgang Dürr, Uwe Erben, A. Schüppen, H. Dietrich and Hermann Schumacher, "Low-power low-noise active mixers for 5.7 and 11.2 GHz using commercially available SiGe HBT MMIC technology," *Electronics Letters*, vol. 34, pp. 1994–1996, Oct. 1998.

[86] Uwe Erben, Hermann Schumacher, A. Schüppen, H. Dietrich and J. Arndt, "Application of a Production Ready SiGe HBT Process to 1.9, 5.7 and 10 GHz Low Noise MMIC's," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, IEEE, Michigan*, pp. 100–104, Sept. 1998.

[87] I. Piper, "Build An E-pHEMT Low-Noise Amplifier," *Microwaves & RF*, pp. 92–102, Mar. 2004.

[88] "Atmel starts up 82 GHz SiGe foundry," *Microwave Engineering Europe*, p. 14, Dec. 2000 / Jan. 2001.

[89] N. Camilleri, J. Kirchgessner, J. Costa, D. Ngo, and D. Lovelace, "Bonding pad model for silicon VLSI-technologies and their effects on the noise figure of RF NPNs," in *Microwave and Millimeter-Wave Monolithic Circuit Symposium*, pp. 1179–1182, 1994.

[90] J. T. Colvin, S. S. Bhatia, and K. K. O, "Effect of Substrate Resistances on LNA Performance and a Bondpad Structure for Reducing the Effects in a Silicon Bipolar Technology," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1339–1344, Sept. 1999.

[91] A. Rofougaran, J. Y.-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 880–889, July 1996.

[92] H. Schumacher, U. Erben, W. Dürr and K.-B. Schad, "Low-Noise, Low-Power Wireless Frontend MMICs Using SiGe HBTs," *IEICE Transactions on Electronics*, vol. E82-C, pp. 1943–1950, Nov. 1999. Special Issue on High Frequency / High-Speed Devices for Information and Communication Systems in the 21st Century.

[93] G. Lohninger, "Diskret, aber nicht trivial, Teil 4: Monolithisch integrierte Mikrowellen-Bausteine in Si-und SiGe-Technik (in german)," *Elektronik*, no. 19, pp. 76–83, 2002. `www.elektroniknet.de`.

[94] "Walter H. Schottky," last visited Dec. 2009. `http://en.wikipedia.org/wiki/Walter_Schottky`.

[95] J.-F. Luy and P. R. (Hrsg.), *Silicon-Based Millimeter-Wave Devices*, vol. 32 of *Springer Series in Electronics and Photonics*. Heidelberg: Springer-Verlag, 1994. ISBN 3-540-58047-6.

[96] K.M. Strohm, C.N. Rheinfelder, J.-F. Luy, P. Nüchter, T. Hess, W. Heinrich, H. Kuhnert, M. Nadarassin, C. Warns and W. Menzel, "Coplanar and Microstrip Oscillators in SiGe SIMMWIC Technolopy," in *2001 IEEE MTT-S International Microwave Symposium Digest*, vol. 3, (Phoenix, AZ, USA), pp. 1563–1566, May 20-25 2001.

[97] A. Müller and E. Kasper, "SIMMWICs on Micromachined Silicon on Insulator Substrates beyond 100 GHz," in *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems SiRF*, (Orlando Florida), pp. 22–29, Jan 23-25 2008.

[98] A. Horn and A. Kruck, "Overview of the technical and geometrical parameters for electromagnetic field simulation," Tech. Rep. 4.3, Atmel Germany GmbH, Aug. 2003.

[99] D. Carver, "AT46000 Design Rule Manual, 0.35μm SiGe BiCMOS Technology," design rule manual v0.6, Atmel Corporation, Colorado Springs, CO 80906, Nov. 2003.

[100] L. Eccles, "Altered Silicon Increases Chip Speeds Up To 35%," *Electronic Design*, pp. 29–30, July 23 2001.

[101] "Raising the bar on transistor performance," *Electronic Design Europe*, p. 8, Nov. 2003.

[102] "Texas Instruments Sees Its 90nm Process Performance Exceed Earlier Generation By Over 50%," *Electronics Express*, Nov. 2003.

[103] P. MacAdam and B.-G. Goldberg, "CMOS SOS for Mixed-Signal ICs," *Applied Microwave & Wireless*, pp. 26–37, Feb. 2002.

[104] S. Richard, "A 5.8 GHz WLAN Receiver using RFCMOS Technology," Master's thesis, Ulm University, July 2003.

[105] C. C. Enz and Y. Cheng, "MOS Transistor Modelling for RF IC Design," *IEEE Transactions on Solid-State Circuits*, vol. 35, Feb. 2000.

[106] "*Micro*LeadFrame™(MLF™) Package," data sheet, Amkor Technology, Nov. 2001. `www.amkor.com`.

[107] "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages," tech. rep., Amkor Technology, Mar. 2001. Rev. B.

[108] "Thermal Considerations of QFN and Other Exposed-Paddle Packages," Application Note HFAN-08.1 (Rev. 0, 11/01), Maxim Integrated Products, 2001.

[109] Joachim N. Burghartz, "Silicon RF Technology - The Two Generic Approaches," in *ESSDERC*, pp. 143–153, 1997.

[110] E. Sönmez, P. Abele, K.-B. Schad and H. Schumacher, "MMICs in the 20 GHz Range Using A Commercially Available SiGe Foundry Process," *MIOP, Stuttgart, Germany*, May 8-10 2001.

[111] E. Sönmez, A. Trasser, K.-B. Schad, P. Abele and H. Schumacher, "High Power Ultra Compact VCO with Active Reactance Concepts at 24 GHz," in *31st European Microwave Conference, 2001*, (London, UK), pp. 1–4, Sept. 24-28 2001.

[112] E. Sönmez, A. Trasser, K.-B. Schad, P. Abele and H. Schumacher, "A single-chip 24 GHz receiver front-end using a commercially available SiGe HBT foundry process," in *2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, (Seattle, USA), pp. 159–162, June 2002.

[113] P. Abele, E. Sönmez, K.-B. Schad, and H. Schumacher, "24 GHz SiGe-MMIC Oscillator Realized with Lumped Elements in a Production Line," *30th European Microwave Conference, 2000*, pp. 1–3, Oct. 2-6 2000.

[114] F. Gruson, P. Abele, K.-B. Schad, E. Sönmez, and H. Schumacher, "24 GHz Differential SiGe-MMIC Oscillator with Integrated Mixer," in *2003 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers*, pp. 60–63, April 9-11 2003. ISBN: 0-7803-7787-7.

[115] F. Gruson, G. Bergmann, and H. Schumacher, "A frequency doubler with high conversion gain and good fundamental suppression," *2004 IEEE MTT-S International Microwave Symposium Digest*, pp. 175–178, June 6-11 2004. ISBN: 0-7803-8331-1.

[116] C. Rheinfelder, K. Strohm, L. Metzger, H. Kibbel, J.-F. Luy, and W. Heinrich, "47GHz SiGe-MMIC Oscillator," *1999 IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 5–8, June 1999.

[117] C.N. Rheinfelder, F. Beisswanger, J. Gerdes, F.J. Schmückle, K.M. Strohm, J.-F. Luy, and W. Heinrich, "A Coplanar 38-GHz SiGe MMIC Oscillator," *IEEE Microwave and Guided Wave Letters*, vol. 6, pp. 398–400, Nov. 1996.

[118] C. N. Rheinfelder, F. J. Beisswanger, and W. Heinrich, "Nonlinear Modeling of SiGe HBTs up to 50 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 2503–2508, Dec. 1997.

[119] C. N. Rheinfelder, M. Rudolph, F. J. Beisswanger, and W. Heinrich, "Nonlinear Modeling of SiGe HBTs up to 50 GHz," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 877–880, 1997.

[120] K. O, "Estimation Methods for Quality Factors of Inductors Fabricated in Silicon Integrated Circuit Process Technologies," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1249–1252, Aug. 1998.

[121] J. N. Burghartz, A. E. Ruehli, K. A. Jenkins, M. Soyuer, and D. Nguyen-Ngoc, "Novel Substrat Contact Structure for High-Q Silicon-Integrated Spiral Inductors," in *International Electron Devices Meeting (IEDM), Technical Digest.*, pp. 55 – 58, Dec. 7-10 1997.

[122] L. E. Larson, "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 387–399, Mar. 1998.

[123] W. B. Kuhn and N. K. Yanduru, "Spiral Inductor Substrate Loss Modelling in Silicon RFICs," in *RAWCON '98 Proceedings*, pp. 305–308, 1998.

[124] A. Rofougaran, J. Rael, M. Rofougaran, and A. A. Abidi, "A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," *42nd IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*, pp. 392–393, Aug. 1996. ISBN: 0-7803-3136-2.

[125] J. Craninckx and M. S. Steyaert, "A 1.8 GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 736–744, May 1997.

[126] "Spotlight on substrates at device conference," *Microwave Engineering Europe*, pp. 14–15, Feb. 2004.

[127] R. Dekker, K. Dessein, J.-H. Fock, A. Gakis, C. Jonville, O. Kuijken, T. Michielsen, P. Mijlemans, H. Pohlmann, W. Schnitt, C. Timmering, and A. Tombeur, "Substrate Transfer: Enabling Technology for RF Applications," in *IEEE International Electron Devices Meeting (IEDM '03), Technical Digest*, (Washington DC), pp. 15.4.1–15.4.4, Dec 8-10 2003. ISBN: 0-7803-7872-5.

[128] A. Chin, K. T. Chan, C. H. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M. F. Li, S. P. McAlister, and D.-L. Kwong, "RF Passive Devices on Si with Excellent Performance Close to Ideal Devices Designed by Electro-Magnetic Simulation," in *IEEE International Electron Devices Meeting (IEDM '03), Technical Digest*, (Washington DC), pp. 15.5.1–15.5.4, Dec 8-10 2003. ISBN: 0-7803-7872-5.

[129] "at59k design manual," tech. rep., Atmel, 2003.

[130] S. Jenei, G. Vanhorebreek, S. V. Huylenbroeck, S. Decoutre, and B. Nauwelaers, "High performance modules for integrated passives in silicon technologies," *Microwave Engineering Europe*, pp. 41–53, June 2001.

[131] D. Shamiryan, T. Abell, F. Iacopi, and K. Maex, "Low-k dielectric materials," *materials today (Elsevier)*, pp. 34–39, Jan. 2004.

[132] P. Garrou, "GaAs IC makers lead the way in metals and low-k dielectrics," *CompoundSemiconductor.Net*, July 2002.

[133] T. Yoshimori, "X marks the architectural spot," *Electronic Design Europe*, p. 14, Nov. 2003.

[134] "Understanding the Fundamental Principles of Vector Network Analysis," Application Note 1287-1, Agilent Technologies, 2000.

[135] J. N. Burghartz, K. A. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," *IEEE Electron Device Letters*, vol. 17, no. 9, pp. 428–430, 1996. ISSN: 0741-3106.

[136] M. Soyuer, K. A. Jenkins, J. N. Burghartz, H. A. Ainspan, F. J. Canora, S. Ponnapalli, J. F. Ewen, and W. E. Pence, "A 2.4-GHz Silicon Bipolar Oscillator with Integrated Resonator," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 268–270, Feb. 1996.

[137] J. N. Burghartz, "Progress in RF Inductors on Silicon - Understanding Substrate Losses," in *International Electron Device Meeting (IEDM), Technical Digest*, (San Francisco, CA), pp. 523–526, Dec. 6-9 1998.

[138] Y. Cao, R. A. Groves, X. Huang, N. D. Zamdmer, J.-O. Plouchart, R. A. Wachnik, T.-J. King, and C. Hu, "Frequency-Independent Equivalent-Circuit Model for On-Chip Spiral Inductors," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 419–426, Mar. 2003.

[139] S. Verma and J. M. Cruz, "On-chip Inductors and Transformers," Tech. Rep. SMLI TR-99-79, Sun Microsystems, Inc., 901 San Antonio Road, Palo Alto, CA 94303, U.S.A, Dec. 1999. `http://research.sun.com/techrep/1999/abstract-79.html`.

[140] M. Pfost, H.-M. Rein, and T. Holzwarth, "Modeling Substrate Effects in the Design of High-Speed Silicon Bipolar ICs," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1493–1501, Oct. 1996.

[141] M. Pfost and H.-M. Rein, "Modeling and Measurement of Substrate Coupling in Si-Bipolar IC s up to 40 GHz," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 582–591, Apr. 1998.

[142] U. G. P. Freyer, *Anpassung und Fehlanpassung: Grundlagen, Funktionsweise und Anwendungsbeispiele für die optimale Problemlösung (in german).* Franzis-Verlag GmbH, München, 1987. ISBN: 3-7723-8191-X.

[143] K. M. Strohm, F. J. Schmückle, B. Schauwecker, W. Heinrich, and J.-F. Luy, "Silicon Micromachined CPW Transmission Lines," in *32nd European Microwave Conference*, (Milano, Italy), pp. 1–2, Oct. 2002.

[144] S. P. O. Bruce, A. Rydberg, M. Kim, F. J. Beisswanger, J.-F. Luy, H. Schumacher, U. Erben, M. Willander, and M. Karlsteen, "Design and Realization of a Millimeter-Wave Si/SiGe HBT Frequency Multiplier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 695–700, May 1998.

[145] Ertugrul Sönmez, *24GHz Multi-Functional MMICs using SiGe HBTs.* PhD thesis, Fakultät für Ingenieurwissenschaften und Informatik der Universität Ulm, Albert-Einstein-Allee, Ulm, Germany, July 2007. Taschenbuch: 146 Seiten, Cuvillier Verlag, 1. Auflage, ISBN: 978-3867275026.

[146] J. van Hese, "Design and Simulation of Spiral Inductors on Silicon Substrates," application note, Agilent Technologies, 1999.

[147] M. Reppel, "Electromagnetic analysis of LTCC high frequency devices," *Microwave Engineering Europe*, pp. 25–30, June/July 2003.

[148] J. C. Rautio and V. Demir, "Microstrip Conductor Loss Models for Electromagnetic Analysis," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 915–921, Mar. 2003.

[149] Agilent EEsof Knowledge Center Document, ID=156382, "Comparison of MRIND model schematic results with momentum," 2003.

[150] Agilent EEsof Knowledge Center Document, ID=182.931, "How to model metal thickness in momentum," 2003.

[151] J. Rautio private communications, 2003.

[152] J. C. Rautio, "A Space Mapped Model of Thick Tightly Coupled Conductors for Planar Electromagnetic Analysis," *IEEE microwave magazine*, vol. 5, pp. 62–72, Sept. ISSN: 1527-3342.

[153] J. C. Rautio, "Free EM Simulator Analyzes Spiral Inductor on Silicon," *Microwaves & RF*, pp. 165–172, Sept. 1999.

[154] A. Kruck private communications, 2003.

[155] "About Empire," `www.empire.de/index.php`, last visited Dec. 2009.

[156] B. K. Sen and R. L. Wheeler, "Skin Effects models for Transmission Line Structures using Generic SPICE Circuit Simulators," in *IEEE 7th topical Meeting on Electrical Performance of Electronic Packaging*, pp. 128–131, Oct 26-28 1998.

[157] A. Weisshaar, H. Lan, and A. Luoh, "Accurate Closed-Form Expressions for the Frequency-Dependent Line Parameters of On-Chip Interconnects on Lossy Silicon Substrate," *IEEE Transactions on Advanced Packaging*, vol. 25, pp. 288–296, May 2002.

[158] H. Schwab, "Inductor with Scaled Parameters," Internal SCUBA Report, work package A2, DTS Design & Test Solutions, 2002–2003.

[159] J. C. Maxwell, *Electricity and Magnetism*. vols. 1 and 2, reprinted by Dover Publications, 1954.

[160] H. A. Wheeler, "Simple inductance formulas for radio coils," *Proc. IRE*, vol. 16, pp. 1398–1400, Oct. 1928.

[161] H. A. Wheeler, "Formulas for the Skin Effect," *Proc. IRE*, vol. 16, pp. 412–424, Sept. 1942.

[162] M. T. Thompson, "Inductance Calculation Techniques – Part II: Approximations and Handbook Methods," *Power Control and Intelligent Motion*, Dec. 1999. `www.thompsonrd.com/induct2.pdf`, last visited Dec. 2009.

[163] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1419–1424, Oct. 1999.

[164] S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-Based Closed-Form Inductance Expression for Compact Modeling of Integrated Spiral Inductors," *IEEE Journal of Solid-State Circuits*, vol. 37, Jan. 2002.

[165] W. Simbürger private communications, 2003.

[166] H. S. Black, "Wave Translation System," U.S. Patent 2,102,671, Dec. 21 1932. Application May 21, 1929.

[167] H. S. Black, "Inventing the negative feedback amplifier," *IEEE Spectrum*, pp. 55–60, Dec. 1977.

[168] R. Kline, "Harold Black and the negative-feedback amplifier," *IEEE Control Systems Magazine*, vol. 13, pp. 82–85, Aug. 1993.

[169] J. M. Rollett, "Stability and Power-Gain Invariants of Linear Twoports," *IRE Transactions on Circuit Theory*, pp. 29–32, Mar. 1969.

[170] R. Yogi, "Techniques for Optimizing UHF Front-End Integrated Circuits," Application Note AN2000 9397 750 04367, Philips Semiconductors, Nov. 19 1997.

[171] J. Lucek and R. Damen, "Designing an LNA for a CDMA front end," *www.rfdesign.com*, vol. 22, pp. 20–30, Feb. 1999. reprinted at `www.nxp.com/documents/application_note/LNA97.pdf`.

[172] B. K. Ko and K. Lee, "A Comparative Study on the Various Monolithic Low Noise Amplifier Circuit Topologies for RF and Microwave Applications," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1220–1225, Aug. 1996.

[173] B. K. Ko and K. Lee, "A New Simultaneous Noise and Input Power Matching Technique for Monolithic LNA's Using Cascode Feedback," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 1617–1630, Sept. 1997.

[174] B. Gilbert, *Design of Bipolar Si/SiGe LNAs, from Ground-Up.* EPFL course, Lausanne, Switzerland, July 1-5, 1996.

[175] R.J. Hawkins, "Limitations of Nielsen's and Related Noise Equations Applied to Microwave Bipolar Transistors, and a New Expression for the Frequency and Current Dependent Noise Figure," *Solid-State Electronics, Vol.20, pp.191-196*, Mar. 1977.

[176] M. Rudolph, F. Korndörfer, P. Heymann, and W. Heinrich, "Compact Large-Signal Shot-Noise Model for HBTs," *IEEE Transaction on Microwave Theory and Techniques*, vol. 56, pp. 7–14, Jan. 2008.

[177] G. Niu, J. D. Cressler, S. Zhang, W. E. Ansley, C. S. Webster, and D. L. Harame, "A Unified Approach to RF and Microwave Noise Parameter Modeling in Bipolar Transistors," *IEEE Transactions on Electron Devices*, vol. 48, pp. 2568–2574, Nov. 2001.

[178] M. Kim and B. Kim, "Analysis of High Frequency Noise of AlGaAs/GaAs HBT," *IEICE Trans. Electron.*, vol. E82, pp. 1018–1024, June 1999.

[179] D. Costa, "Impact of Al composition on RF noise figure of AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. ED-42, pp. 2043–2046, 1995.

[180] H. Schumacher, U. Erben, and W. Dürr, "SiGe heterojunction bipolar transistors - the noise perspective," *Solid-State Electronics*, vol. 41, pp. 1485–1492, Oct. 1997.

[181] W. Yanfeng and W. Dexin, "HBT´s High Frequency Noise Modeling and Analysis," *Chinese Journal of Semiconductors*, vol. 23, pp. 1140–1145, Nov. 2002. Article ID: 0253-4177(2002) 11-1140-06.

[182] D. Barker, "Darlington Gain Blocks Hurdle Reliability Problems," *Microwaves & RF*, pp. 120–122, Feb. 2004.

[183] J. Browne, "InGaP/GaAs Provides High-Linearity HBTs," *Microwaves & RF*, pp. 120–129, Feb. 2000.

[184] J. R. Long, "A Low-Voltage 5.1-5.8-GHz Image-Reject Downconverter RF IC," *IEEE Journal of Solid-State Circuits*, vol. 35, Sept. 2000.

[185] D. J. Cassan and J. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, Mar. 2003.

[186] T. Feger, "Modellierung integrierter Transformatoren auf verlustbehaftetem Silizium." Studienarbeit an der Universität Ulm, 2003.

[187] D. E. Norton, "High Dynamic Range Transistor Amplifiers using lossless feedback," *Microwave Journal*, May 1976.

[188] J. Smith, "Z10040B Broadband Norton Amplifier Assembly and Operation Manual," *Version 1.4*, Nov. 2009. `www.cliftonlaboratories.com/Documents/Z10040BManual01.pdf`, last visited Dec. 2009.

[189] M. Martin, "Neuartiger Verstärker für UKW (KW)-Empfänger (in german)," *cq-DL*, pp. 64–65, Feb. 1978.

[190] K. L. Fong and R. G. Meyer, "High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-Pair Transconductance Stages," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 548–555, Apr. 1998.

[191] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF Front-End IC," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 350–355, Mar. 1994.

[192] J. Durec, "An Integrated Silicon Bipolar Receiver Subsystem for 900-MHz ISM Band Applications," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1352–1372, Sept. 1998.

[193] J. Durec, "RF Design Techniques," in *Wireless Symposium, Spring 1999 Conference*, (San Jose, CA), Feb. 1999.

[194] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise

Amplifier Design," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1430–1438, Sept. 1997.

[195] E. Heaney, F. McGrath, P. O'Sullivan, and C. Kermarrec, "Ultra Low Power Low Noise Amplifiers for Wireless Communications," in *1993 IEEE GaAs IC Symposium*, (Santa Clara, CA), pp. 49–51, Oct. 10-13 1993.

[196] T. Chen, "Balance Trade-Offs In GaAs FET LNAs," *Microwaves & RF*, pp. 55–57, Feb. 2000.

[197] J.-S. Goo, H.-T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee, and R. W. Dutton, "A Noise Optimization Technique for Integrated Low-Noise Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 994–1001, Aug. 2002.

[198] B. Battaglia, "Design A Low-Noise Communications Amplifier," *Microwaves & RF*, pp. 59–64, Dec. 1999.

[199] M. Williams, "The Cascode Amplifier: A Useful RF Building Block," *Microwave Product Digest*, Mar. 1999.

[200] Q. Huang, F. Piazza, P. Orsati, and T. Ohguro, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1023–1036, July 1998.

[201] F. Gruson, "Voltage references and bias networks," in *High Speed Devices and Circuits for Analogue Applications beyond 3 GHz*, (`www.eurotraining.net`), June 2001.

[202] B. Gilbert, *Analogue IC design: the current mode approach*, ch. Bipolar Current Mirrors, pp. 239–296. IEE Circuits and Systems Series 2, Peter Peregrinus Ltd., 1990. ISBN: 9780863412158.

[203] R. Widlar, "New Developments in IC Voltage Regulators," in *1970 IEEE International Solid-State Conference*, (Univ. of. Pennsylvania), pp. 158–159, Feb. 1970.

[204] R. Widlar, "New Developments in IC Voltage Regulators," *IEEE Journal of Solid-State-Circuits*, vol. SC-6, pp. 2–4, Feb. 1971.

[205] R. Böhme, "Stromstabilisierung in bipolar integrierten Schaltungen," *Elektronik*, no. 5, pp. 129–133, 1988.

[206] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670–674, May 1999.

[207] P. Malcovati, F. Maliberti, C. Fiocchi, and M. Pruzzi, "Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1076–1081, July 2001.

[208] B. Gilbert, *Analogue IC design: the current mode approach*, ch. Current-mode Circuits From A Translinear Viewpoint, pp. 74–76. IEE Circuits and Systems Series 2, Peter Peregrinus Ltd., 1990. ISBN: 9780863412158.

[209] A. Dao, "Integrated LNA and Mixer Basics," Application Note 884, National Semiconductor, 1993.

[210] R. Damen private communications, Sept. 2004.

[211] "Agilent MGA-71543 Low Noise Amplifier with Mitigated Bypass Switch," Data Sheet 5988-4553EN, Avago Technologies, Nov. 2001. `www.avagotech.com`.

[212] "pHEMT Low Noise Amplifier with Bypass Switch MGA-72543," Data Sheet 5988-4279EN, Avago Technologies, `www.avagotech.com`, Oct. 2001.

[213] "Agilent MGA-725M4 Low Noise Amplifier with Bypass Switch In Miniature Leadless Package," Data Sheet 5988-4278EN, Avago Technologies, `www.avagotech.com`, Oct. 2001.

[214] G. Lohninger, "A Low Noise Amplifier at 1.9 GHz offers +14 dBm Input Intercept Point," Application Note 031, Siemens Discrete and RF Semiconductors, 1996.

[215] S. Narayanan, "Transistor Distortion Analysis Using Volterra Series Representation," *The Bell System Technical Journal*, pp. 991–1024, May-June 1967.

[216] S. Inversen, "The Effect of Feedback on Noise Figure," *Proc. IEEE*, vol. 63, pp. 540–542, Mar. 1974.

[217] L. Boglione, R. D. Pollard, and V. Postoyalko, "Analytical Behaviour of the Noise Resistance and the Noise Conductance for a Network with Parallel and Series Feedback," *IEEE Transaction on Microwave Theory and Techniques*, vol. 45, pp. 301–304, Mar. 1997.

[218] H. F. Cooke, "Microwave Transistors, Theory and Design," *Proceedings of the IRE*, vol. 59, pp. 1163–1181, Aug. 1971.

[219] H. Fukui, "Noise Measure of Microwave Transistors," *Proc. IRE*, vol. 54, pp. 1204–1205, Sept. 1966.

[220] G. Wevers, "A High IIP_3 Low Noise Amplifier fir 1900 MHz Applications using the SiGe BFP620 Transistor," *Applied Microwave & Wireless*, pp. 64–78, July 2000.

[221] S. Maas, "Why I Hate Base Resistance," *IEEE microwave magazine*, pp. 54–60, June 2004.

[222] S. A. Maas, B. L. Nelson, and D. L. Tait, "Intermodulation in Heterojunction Bipolar Transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, pp. 442–448, Mar. 1992.

[223] J. Reynolds, "Nonlinear Distortions and Their Cancellation in Transistors," *IEEE Transactions on Electron Devices*, vol. ED-12, pp. 595–599, Nov. 1965.

[224] S. Narayanan and H. Poon, "An Analysis of Distortion in Bipolar Transistors Using Integral Charge Control Model and Volterra Series," *IEEE Transactions on Circuit Theory*, vol. CT-20, pp. 341–351, July 1973.

[225] G. Niu, Q. Liang, J. D. Cressler, C. S. Webster, and D. L. Harame, "RF Linearity Characteristics of SiGe HBTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 105–108, Sept. 2001.

[226] J.-S. Ko, H.-S. Kim, B.-K. Ko, B. Kim, and B.-H. Park, "Effect of bias scheme on intermodulation distortion and its use for the design of a PCS TX driver," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, (Boston, MA), pp. 105–108, June 2000.

[227] M. P. van der Heijden, H. C. de Graaff, and L. C. N. de Vreede, "A Novel Frequency-Independent Third-Order Intermodulation Distortion Cancellation Technique for BJT Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1176–1183, Sept. 2002.

[228] K. L. Fong, "High-Frequency Analysis of Linearity Improvement Technique of Common-Emitter Transconductance Stage Using a Low-Frequency-Trap Network," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1249–1252, Aug. 2000.

[229] K. L. Fong and D. Szmyd, "Linear LNAs Boast Miniscule Noise Figures At 2 GHz," *Microwaves & RF*, pp. 162–164, Feb. 2001.

[230] M. L. Frank, "A low noise biasing technique," European Patent Application EP 1 315 287 A2, Agilent Technologies, May 28 2003.

[231] H. Patterson, "Analysis of Ground Bond Wire Arrays for RFICs," (Denver, CO), pp. 237–240, June 8-11 1997. ISBN: 0-7803-4063-9.

[232] "MMIC LNAs for Wireless Infrastructure Applications," *Microwave Journal*, vol. 46, pp. 130–138, Nov. 2003.

[233] "BGA615L7 Silicon Germanium GPS Low Noise Amplifier," Data Sheet Rev.1.3, Infineon Technologies AG, Feb. 2007.

[234] "BGA615L7 Silicon Germanium GPS LNA MMIC," product brief, ordering no. b132-h8725-x-0-7600, Infineon Technologies AG, 2006.

[235] "The BGA615L7 Silicon-Germanium Low Noise Amplifier in GPS Applications," Application Note 091, Rev. 2.0, Infineon Technologies AG, Jan. 2007.

[236] "BGA715L7 Silicon Germanium GPS Low Noise Amplifier," Data Sheet Rev 2.1, Infineon Technologies AG, Oct. 2009.

[237] "BGA715L7 SiGe Low Noise Amplifier in GPS Applications," Application Note 161, Rev 1.1, Infineon Technologies AG, July 2008.

[238] J. C. Durec and W.E. Main, "Method and circuit for current regulation," U.S. Patent 5 754 038, May 19 1998.

[239] F. Gruson, S. Hettich, A. Trasser, and H. Schumacher, "Linear Front-End ICs for TETRA / TETRAPOL Handhelds using SiGe Technology," in *2004 International Symposium on Signals, Systems, and Electronics (ISSSE'04)*, Aug. 10-13 2004.

[240] B. Gilbert, *Design considerations for active BJT mixers*, ch. 23, pp. 837–927. Low-power HF microelectronics; A Unified Approach, London: IEE, 1996.

[241] B. Gilbert, "The MICROMIXER: A Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1412–1423, Sept. 1997.

[242] "A Low Parts Count Low Noise Amplifier for GPS Applications using BGA428," Application Note 62, Rev. 2.0, Infineon Technologies AG, Jan. 2007.

[243] P. Shah, P. Gazzerro, V. Aparin, R. Sridhara, and C. Narathong, "A 2GHz Low-Distortion Low-Noise Two-Stage LNA Employing Low-Impedance Bias Terminations and Optimum Inter-Stage Match for Linearity," in *Proceedings of the 26th European Solid-State Circuits Conference (ESSCIRC)*, (Stockholm, Sweden), pp. 308 – 311, Sept. 19-21 2000.

[244] K. Alvarino, H. Bui, S. Coryell, S. Egolf, H. Jiang, C. Lazinbat, E. T. Spears, D. Spooner, and D. A. Teeter, "Next Generation CDMA2000 1X Power Amplifier Modules," *Applied Microwave & Wireless*, pp. 74–84, May 2002.

[245] L. C. de Vreede, H. C. de Graaff, K. Mouthaan, M. de Kok, J. L. Tauritz, and R. G. Baets, "Advanced Modeling of Distortion Effects in Bipolar Transistors Using the Mextram Model," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 114–121, Jan. 1996.

[246] Johannes J.E.M. Hageraats, "Broadband amplification with high linearity and low power consumption," international patent application wo 00/45505, Jan. 27 2000.

[247] Johannes J.E.M. Hageraats, "Radio Frequency Amplifier with reduced Intermodulation Distortion," U.S. Patent 6 204 728, Mar. 20 2001.

[248] "1575MHz/1900MHz Variable-IP_3 Low-Noise Amplifiers," data sheet, Maxim Integrated Products, 2002. 19-1872; Rev 1.

[249] "Silicon Germanium (SiGe) Technology Enhances Radio Front-End Performance," application note, Maxim Integrated Products, 2000. AN697.

[250] "MAX2654-MAX2656 S-Parameters and Noise Parameters," tech. rep., Maxim Integrated Products. www.maxim-ic.com.

[251] "BGA622 Silicon Germanium Wide Band Low Noise Amplifier with 2 kV ESD Protection," Data Sheet Rev. 2.2, Infineon Technologies AG, Apr. 2008.

[252] NEC Electronics, "A Low Noise Amplifier IC for 400 MHz to 2 GHz Applications," *Microwave Journal*, pp. 144–148, Apr. 2004.

[253] "NEC's SiGe Low Noise Amplifier for GPS/Mobile Communications μPC8211TK," data sheet, California Eastern Laboratories, 2005.

[254] "Agilent ATF-541M4 Low Noise Enhancement Mode Pseudomorphic HEMT in a Miniature Leadless Package," data sheet, Avago Technologies, 2001. www.avagotech.com.

[255] K. Browne, "E-PHEMT Promises High Linearity From A Single Supply," *Microwaves & RF*, p. 137, Apr. 2001.

[256] "5GHz to 6GHz Low-Noise Amplifier in 6-Pin UCSP," Data Sheet 19-2492; Rev 1, Maxim Integrated Products, 2003.

[257] "Designing with the MAX2648 5GHz LNA for High-Frequency Stability," Application Note 1756, Maxim Integrated Products, 2002.

[258] D. Linten, S. Thijs, M. I. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 90-nm RF CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1434–1441, July 2005.

[259] H. Satou, H. Yamazaki, K. Kobayashi, T. Mori, and Y. Watanabe, "5.3 GHz 1.6dB NF CMOS Low Noise Amplifier Using 0.11 μm Technology," *2004 IEEE RFIC Symposium, Fort Worth, Texas, USA*, June 6-8 2004.

[260] B. Mohammadi and C. A. T. Salama, "A 5.8 GHz CMOS LNA for WLAN Applications," *2004 IEEE RFIC Symposium, Fort Worth, Texas, USA*, June 6-8 2004.

[261] T. L. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2 ed., Dec. 2003. ISBN: 978-0521835398.

[262] "2.4GHz SiGe, High IP_3 Low-Noise Amplifier," Data Sheet 19-1786; Rev 1, Maxim Integrated Products, Mar. 2003.

[263] "RF2373 3V Low Noise Amplifier / 3V Driver Amplifier," Data Sheet Rev A8 DS081217, RF Micro Devices, Inc., 2006.

[264] A. A. Abidi, "Direct-Conversion Radio transceivers for Digital Communications," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1399–1410, Dec. 1995.

[265] H. Yoshida, T. Toyoda, T. Arai, and H. Tsurumi, "A low DC offset direct conversion receiver for W-CDMA with low current consumption," *IEICE Electronics Express*, vol. 2, pp. 434–439, August 2005.

[266] X. Ruimin and X. Shaoqiu and Y. Bo, "Devise A Millimeter-Wave PHEMT Mixer," *Microwaves & RF*, p. 56 ff., Oct. 2000.

[267] M. L. de la Fuente, J. P. Pascual, and E. Artal, "Analyze And Design A Cascode MESFET Mixer," *Microwaves & RF*, pp. 129–138, May 1998.

[268] "CMY210: Ultra-Linear Mixer with Integrated LO Buffer," Data Sheet AM50-0002, TriQuint Semiconductors, July 2003.

[269] S. Sze, *Physics of Semiconductor Devices*, ch. 1. New York: John Wiley & Sons, Inc., 2nd ed., 1981.

[270] F. Hasouneh, "Design of a Highly Linear Dual Band LNA for a PMR Front-End using SiGe HBT Technology," Master's thesis, Ulm University, Oct. 2002.

[271] Atmel Germany GmbH und EADS Telecom Deutschland GmbH, "SUPERSTAR-Leistungstechnologie und Universalplattform für Sicherheitsfunkanwendungen (MEDEA+ A108)," *Anlage zum Zwischenbericht SUPERSTAR, 01/2003 bis 06/2003, Förderkennzeichen: 01M 3120 A*, July 2003.

[272] R. Hartley, "Single-sideband modulator," U.S. Patent 1 666 206, Apr. 1928.

[273] J. Crols and M. S. J. Steyaert, "A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.

[274] S. Lee, K. Jung, W. Kim, H. Ryu, and W. Song, "A 1 GHz Image-Rejection Donw-Converter in 0.8μm CMOS Technology," *IEEE Transactions on Consumer Electronics*, vol. 44, pp. 235–239, May 1998.

[275] K. Stadius, P. Järviö, P. Paatsila, and K. Halonen, "Image-Reject Receivers with Image-Selection Functionality," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. IV, pp. 124–127, 2001.

[276] M. J. Gingell, "Singe Sideband Modulation Using Sequence Asymmetric Polyphase Networks," *Elect. Commun.*, vol. 48, pp. 21–25, 1973.

[277] A. Rofougaran, G. Chang, J. Rael, M. Rofougaran, S.Khorram, M. Ku, E. Roth, A. A. Abidi, and H. Samueli, "A 900 MHz CMOS Frequency-Hopped Spread Spectrum RF Transmitter IC," in *IEEE 1996 Custom Integrated Circuits Conference*, (San Diego, CA), pp. 209–212, May 5-8 1996.

[278] J. van der Tang and D. Kasperkovitz, "A 0.9-2.2 GHz Monolithic Quadrature Mixer Oscillator for Direct-Conversion Satellite Receivers," in *Proc. of the IEEE International Solid-State Conference*, pp. 88–89, 1997.

[279] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2 GHz," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1987–1991, Dec. 1998.

[280] J. Massen, L. Kühnke, R. Frank, and F. Gruson, "Abschlussbericht des BMBF-Projektes: KOKON, Kfz-Höchstfrequenzelektronik, Teilvorhaben Continental," tech. rep., Automotive Distance Control Systems GmbH, 2007.

[281] S. Chartier, T. Feger, T. Purtova, B. Schleicher, and H. Schumacher, "79 GHz fully integrated fully differential Si/SiGe HBT amplifier for automotive radar applications," in *Proc IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, (Nice, France), pp. 1011–1014, Dec. 10-13 2006. urn:nbn:de:bsz:289-vts-63386.

[282] S. Chartier, B. Schleicher, F. Korndörfer, S. Glisic, G. Fischer, and H. Schumacher, "A Fully Integrated Fully Differential Low-Noise Amplifier for Short Range Automotive Radar Using a SiGe:C BiCMOS Technology," in *Proc European Microwave Integrated Circuits (EuMIC) Conference*, (Munich, Germany), Oct. 8-10 2007. urn:nbn:de:bsz:289-vts-63355.

[283] B. S. S. Chartier, G. Fischer, F. Korndörfer, J. Borngräber, T. Feger, and H. Schumacher, "A Compact Low-Power SiGe:C BiCMOS Amplifier for 77-81 GHz Automotive Radar," in *Proc 2008 IEEE Topical Meeting on Silicon Monolithic ICs in RF Systems (SiRF)*, (Orlando, FL, USA), pp. 195–198, Jan. 23-25 2008. urn:nbn:de:bsz:289-vts-63003.

[284] J. Greene, "Noisemanship – The Art of Measuring Noise Figures Nearly Independent of Device Performance," *IEEE microwave magazine*, pp. 136 + 134, June 2004. reprinted from *Proceedings of the IRE, vol. 49, p.1223, 1961.*

[285] "Three Methods of Noise Figure Measurement," Application Note APP 2875, Maxim Integrated Products, Nov. 2003.

[286] G. Lohninger and L. Musiol, "Measure 3 Types of Parameter and You'll Define a Small Signal RF-Transistor: S-Parameter, Noise-Figure and Intermodulation," Application Note 008, Infineon Technologies AG, July 2000.

[287] N. Kuhn, "Accurate and Automatic noise figure measurements with standard equipment," *IEEE MTT-S International Microwave Symposium Digest*, vol. 80, pp. 425–427, May 26-30 1980.

[288] "Noise Figure Measurement Accuracy: The Y-Factor Method," application note, Agilent Technologies, 2001. 57-2.

[289] P. Robbins, "Using Noise for RF Receiver Built-in Test Applications," *Microwave Journal*, vol. 47, pp. 138–147, Feb. 2004.

[290] "Improving Noise Figure Measurement," application note, Noisecom. `www.noisecom.com`, last visited Dec. 2009.

[291] "HP 8970 Series Noise Figure Measurement Products," Product Overview 5091-6049E, Hewlett-Packard Company, June 1999.

[292] "Agilent N8972A, N8973A NFA Series Noise Figure Analyzers," Technical Specifications 5980-0164E, Agilent Technologies, Apr. 2000.

[293] "ESA-E Series Spectrum Analyzers Noise Figure Measurements Personality," Application Note 5989-0215EN, Agilent Technologies, Mar. 2004.

[294] "Agilent ATF-551M4 Low Noise Enhancement Mode Pseudomorphic HEMT in a Miniature Leadless Package," data sheet, Avago Technologies, `www.avagotech.com`, 2001.

[295] J. Smith, "6 dB Hybrid Coupler Experiments," Mar. 2008. `www.cliftonlaboratories.com/6_db_hybrid_combiner.htm`, last visited Dec. 2009.

[296] "Improve Two-tone, Third Order Testing," Sept. 1999. `www.minicircuits.com/pages/pdfs/mxr1-18.pdf`, last visited Dec. 2009.

[297] "ZESC-2-11+ ZESC-2-11 Coaxial Power Splitter/Combiner 2 Way-0° 50 Ω 10 to 2000 MHz," Sept. 2007. `www.minicircuits.com`.

[298] "Improving Network Analyzer Measurements of Frequency-translating Devices," Application Note 1287-7, Agilent Technologies, 2000.

[299] "High-frequency performance with low, stable contact resistance on aluminum pads," Data Sheet INFINITY-DS-0803, Cascade Microtech,Inc., 2003.

[300] "On-Wafer Vector Network Analyzer Calibration and Measurements," Application Note SOLT-LRRM-APP-1201, Cascade Microtech, Inc. `www.cmicro.com/file/on-wafer-vector-network-analyzer-calibration-and-measurements`, last visited Dec. 2009.

[301] A. M. E. Safwat and L. Hayden, "Sensitivity Analysis of Calibration Standards for SOLT and LRRM," application note, Cascade Microtech, Inc., 2001. `www.cmicro.com/file/sensitivity-analysis-of-calibration-standards-for-solt-and-lrrm`, last visited Dec. 2009.

[302] "A Guide to Better Vector Network Analyzer Calibrations for Probe-Tip Measurements," Technical Brief TECHBRIEF4-0694, Cascade Microtech, Inc., 1994.

[303] A. Lord, "Advanced RF Calibration Techniques," tech. rep., Cascade Microtech Europe. www.cascademicrotech.com.

[304] Süss Microtec Dresden, *SussCal User Manual*, 2003.

[305] D. F. Williams and R. B. Marks, "LRM Probe-Tip Calibrations with Imperfect Resistors and Lossy Lines," vol. 24, pp. 32–36, Dec. 1993. www.eeel.nist.gov/dylan_papers/LRMwithImperfect.pdf, last visited Dec. 2009.

[306] S. Basu and L. Hayden, "An SOLR calibrations for accurate measurement of orthogonal on-wafer DUTs," *IEEE Microwave Theory and Tech. Symp. Dig.,*, pp. 1335–1338, June 8-13 1997. www.cascademicrotech.com.

[307] D. K. Walker and D. F. Williams, "Comparison of SOLR and TRL Calibrations," *Publication of the National Institute of Standards and Technology.*

[308] "10 Hints for Making Better Network Analyzer Measurements," Application Note 1291-1B, Agilent Technologies, 2001.

[309] A. Fraser, R. Ares, and R. Gleason, "Introduction to bipolar device GHz measurement techniques – A guide for accurate on-wafer measurements on small high-speed silicon bipolar devices," application note, Cascade Microtec, Inc. www.cmicro.com/file/introduction-to-bipolar-device-ghz-measurement-techniques, last visited Dec. 2009.

[310] G. Ulbricht, *Netzwerkanalyse, Netzwerksynthese und Leitungstheorie (in german).* Teubner Verlag, Mar. 1997. ISBN: 3519001101 (out of print).

[311] "De-embedding and Embedding S-Parameter Networks Using a Vector Network Analyzer," Application Note 1364-1, Agilent Technologies, 2001.

[312] A. Gleißner, "Instruction for Calibration of Rohde & Schwarz Network Analyzers ZVR and ZVC using the TNA Calibration Method," private communications, Rohde & Schwarz.

[313] O. Ostwald, "Fragen und Antworten zum Netzwerkanalysator ZVR," Application Note 1EZ38-3D, Rohde & Schwarz, 1998.

[314] "Calibration Types," http://www.rohde-schwarz.com/webhelp/zvb/System_Overview/Calibration/Calibration_Types.htm, last visited Dec. 2009.

[315] U. Stumper, "Uncertainties of VNA S-Parameter Measurements Applying the TAN Self-Calibration Method," *IEEE Transactions on Instrumentation and Measurement*, vol. 56, pp. 597–600, Apr. 2007. ISSN: 0018-9456.

[316] Stumper, U., "A simple evaluation procedure of the TAN calibration and the influence of non-ideal calibration elements on VNA S-parameter measurements," *Advances in Radio Science*, vol. 5, pp. 5–12, 2007. `http://www.adv-radio-sci.net/5/5/2007/`, ISSN = 1684-9965.

[317] E. P. Vandamme, D. M. M.-P. Schreurs, and C. van Dinther, "Improved Three-Step De-Embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon On-Wafer RF Test-Structures," *IEEE Transactions on Electron Devices*, vol. 48, pp. 737–742, Apr. 2001.

[318] "NJG1103F1: 1.5/1.9 GHz Low Noise Amplifier GaAs MMIC," data sheet, New Japan Radio Co., Ltd.

[319] "GaAs MMIC Low Noise Amplifiers SOIC-8 Platform," Application Note M540, M/A-COM, Inc.

[320] "Low Noise Amplifier 1.5 - 1.6 GHz," data sheet, M/A-COM, Inc. MAAM12021.

[321] "Low Noise Amplifier 1.575 GHz," data sheet, M/A-COM, Inc. AM50-0002.

[322] J. Müllrich, T. Meister, M. Rest, W. Bogner, A. Schöflin, and H.-M. Rein, "40 Gbit/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fibre TDM links," *Electronics Letters*, vol. 34, no. 5, pp. 452–453, 1998.